# LogiCORE IP ChipScope Pro Integrated Controller (ICON) (v1.05a)

DS646 March 1, 2011 **Product Specification**

## Introduction

The LogiCORE™ IP ChipScope™ Pro Integrated CONtroller core (ICON) provides an interface between the JTAG Boundary Scan (BSCAN) interface of the FPGA device and the ChipScope Pro cores, including the following types of cores:

- Integrated Logic Analyzer (ILA)
- Virtual Input/Output (VIO)
- Agilent Trace Core 2 (ATC2)
- Integrated Bus Analyzer (IBA)

This interface allows the ChipScope Pro Analyzer software to communicate with these cores through the JTAG port of the device. The ICON core is designed to be easily instantiated and connected to these cores directly in a Verilog or VHDL design. The ICON core can also be added to an embedded processor system design using the Xilinx Embedded Development Kit (EDK) tools.

## Features

- Provides a communication path, using the JTAG port, between the ChipScope Pro Analyzer software and the ILA, VIO, ATC2, and IBA cores
- Connects to the JTAG chain through the USER scan chain feature of the BSCAN component
- Supports up to 15 connections to ILA, VIO, ATC2, and IBA cores
- Optionally attaches to either internally or externally instantiated BSCAN primitives, such as the one provided by the opb_mdm EDK core

For more information about the ICON core, refer to the *ChipScope Pro Software and Cores User Guide*.

| LogiCORE IP Facts Table | | | | | |
|---|---|---|---|---|---|
| **Core Specifics** | | | | | |
| Supported Device Family[1] | Kintex®-7, Virtex®-7, Virtex-6/6L, Virtex-5, Virtex-4, Spartan®-6/6L, Spartan-3E, Spartan-3, Spartan-3A/Spartan-3A DSP, XA Spartan-3/3A DSP, XA Spartan-3E, XA Spartan-6, XA Virtex-4, Spartan-6Q/6QL, Virtex-4Q, Virtex-5Q, Virtex-6Q/6QL | | | | |
| Supported User Interfaces | Not applicable. | | | | |
| **Provided with Core** | | | | | |
| | **Resources** | | | | **Frequency** |
| Configuration[2] | **LUTs** | **FFs** | **DSP Slices** | **Block RAMs** | **Max Freq** |
| Config1 | 90 | 108 | 0 | 0 | 398.867 MHz |
| Config2 | 317 | 335 | 0 | 0 | 384.919 MHz |
| Config3 | 541 | 559 | 0 | 0 | 380.055 MHz |
| Documentation | Product Specification User Guide | | | | |
| Design Files | Netlist | | | | |
| Example Design | Verilog/VHDL | | | | |
| Test Bench | Provided | | | | |
| Constraints File | Xilinx Constraints | | | | |
| Simulation Model | Not Provided | | | | |
| **Tested Design Tools** | | | | | |
| Design Entry Tools | Core Generator tool, System Generator, XPS | | | | |
| Simulation | Not provided | | | | |
| **Support** | | | | | |
| Provided by Xilinx, Inc. | | | | | |

**Notes:**

1. For a listing of supported devices, see the release notes for this core.
2. For configuration details, see Table 3, page 6.

## Applications

The ICON core is designed to be used in any application that requires verification or debugging using the ChipScope Pro software and cores.

## Functional Description

The ICON core provides an interface between the ChipScope Pro Analyzer tool and up to 15 ChipScope Pro target cores (such as ILA, IBA, VIO, and ATC2) via the JTAG Boundary Scan port of the target FPGA. The ICON core bridges the gap between the JTAG Boundary Scan TAP controller of the FPGA and the target cores using the USER scan chains provided by the BSCAN primitive component of the FPGA. The ICON core is responsible for routing various commands sent from the Analyzer tool to the intended target cores.

The ICON core can be configured to automatically include the BSCAN primitive component (see Figure 1) or to use a BSCAN elsewhere in the design (see Figure 2, page 3). The ICON core can also route unused BSCAN USER scan chains to port signals if the BSCAN is included in the ICON core and the FPGA device family supports multiple USER scan chains per BSCAN component (see Figure 3, page 3).

The ICON core connection to the target cores is implemented as a dedicated bi-directional control port. This control port includes JTAG clock, input and output data, and control signals necessary to configure and communicate with the target core.

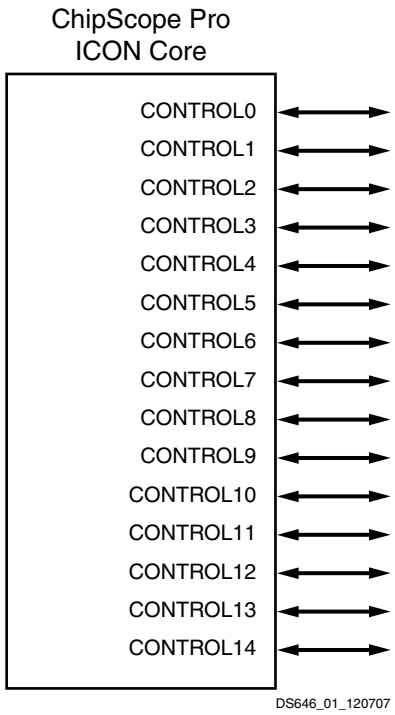


*Figure 1:* **ICON Core with Internal BSCAN Component**

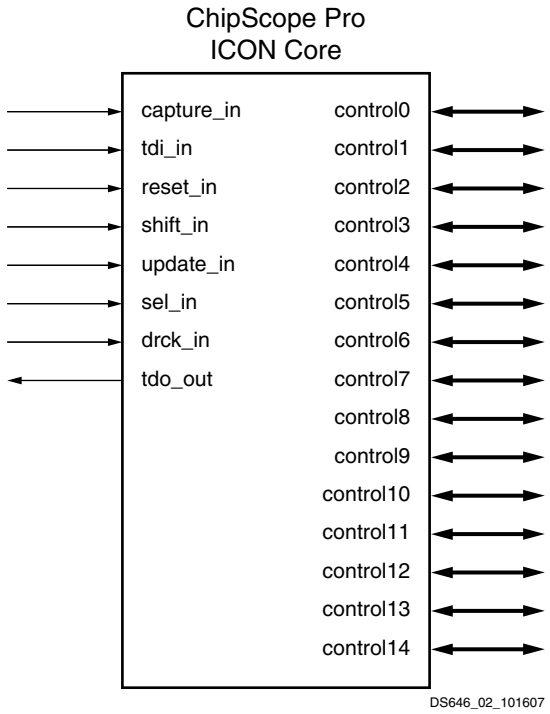


*Figure 2:* **ICON Core with External BSCAN Component**

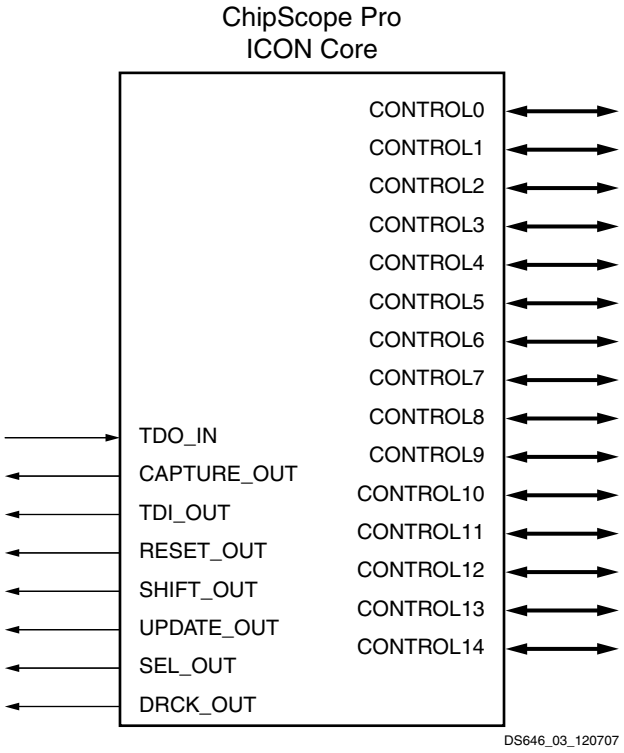


*Figure 3:* **ICON Core with Internal BSCAN Component and Exported Unused BSCAN Signals**

## ICON Interface Ports

The I/O signals of the ICON core consist of control buses necessary to connect the ICON core to the target core(s) as well as optional BSCAN-related signals.

*Table 1:* **ICON Interface Ports**

| Port Name | Direction | Description |
|---|---|---|
| CAPTURE_IN | IN | CAPTURE signal from the external BSCAN component. Optional (depends on *use_ext_bscan* parameter). |
| CAPTURE_OUT | OUT | CAPTURE signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on *use_unused_bscan* parameter). |
| CONTROL0[35:0] | INOUT(1) | Provides control and status connection to the first ChipScope Pro target core. Mandatory. |
| CONTROL1[35:0] | INOUT(1) | Provides control and status connection to the second ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL2[35:0] | INOUT(1) | Provides control and status connection to the third ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL3[35:0] | INOUT(1) | Provides control and status connection to the fourth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL4[35:0] | INOUT(1) | Provides control and status connection to the fifth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL5[35:0] | INOUT(1) | Provides control and status connection to the sixth ChipScope Pro target core. Optional (depends on *number_control_ports*parameter). |
| CONTROL6[35:0] | INOUT(1) | Provides control and status connection to the seventh ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL7[35:0] | INOUT(1) | Provides control and status connection to the eighth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL8[35:0] | INOUT(1) | Provides control and status connection to the ninth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL9[35:0] | INOUT(1) | Provides control and status connection to the tenth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL10[35:0] | INOUT(1) | Provides control and status connection to the eleventh ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL11[35:0] | INOUT(1) | Provides control and status connection to the twelfth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL12[35:0] | INOUT(1) | Provides control and status connection to the thirteenth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL13[35:0] | INOUT(1) | Provides control and status connection to the fourteenth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| CONTROL14[35:0] | INOUT(1) | Provides control and status connection to the fifteenth ChipScope Pro target core. Optional (depends on *number_control_ports* parameter). |
| DRCK_IN | IN | DRCK signal from the external BSCAN component. Optional (depends on *use_ext_bscan* parameter). |
| DRCK_OUT | OUT | DRCK signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on *use_unused_bscan* parameter). |
| RESET_IN | IN | RESET signal from the external BSCAN component. Optional (depends on *use_ext_bscan* parameter). |
| RESET_OUT | OUT | RESET signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on *use_unused_bscan* parameter). |

*Table 1:* **ICON Interface Ports *(Cont'd)***

| Port Name | Direction | Description |
|---|---|---|
| SEL_IN | IN | SEL signal from the external BSCAN component. Optional (depends on *use_ext_bscan* parameter). |
| SEL_OUT | OUT | SEL signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on *use_unused_bscan* parameter). |
| SHIFT_IN | IN | SHIFT signal from the external BSCAN component. Optional (depends on *use_ext_bscan* parameter). |
| SHIFT_OUT | OUT | SHIFT signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on *use_unused_bscan* parameter). |
| TDI_IN | IN | TDI signal from the external BSCAN component. Optional (depends on *use_ext_bscan* parameter). |
| TDI_OUT | OUT | TDI signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on *use_unused_bscan* parameter). |
| TDO_IN | IN | TDO signal to the unused USER scan chain of the internal BSCAN component. Optional (depends on *use_unused_bscan* parameter). |
| TDO_OUT | OUT | TDO signal to the external BSCAN component. Optional (depends on *use_ext_bscan* parameter). |
| UPDATE_IN | IN | UPDATE signal from the external BSCAN component. Optional (depends on *use_ext_bscan* parameter). |
| UPDATE_OUT | OUT | UPDATE signal from the unused USER scan chain of the internal BSCAN component. Optional (depends on *use_unused_bscan* parameter). |

**Notes:**

1. For projects created using Platform Studio, the direction for CONTROL ports is OUT.

## ICON XCO Parameters

The XCO parameters of the ICON core are shown in Table 2.

*Table 2:* **ICON XCO Parameters**

| Parameter Name | Allowable Values | Default Value | Description |
|---|---|---|---|
| component_name | String with A-z, 0-9, and _ (underscore) | icon | Name of instantiated component |
| number_control_ports | 1 to 15 | 1 | Number of ChipScope Pro target cores to be connected to this ICON core. |
| use_ext_bscan | False = Use internal<br>True = Use external | False | Use an external or internal instance of the BSCAN primitive component |
| use_jtag_bufg | False = Enable BUFG<br>True = Disable BUFG | False | Specifies whether or not a BUFG is added to the JTAG (or DRCK) clock signal |
| use_unused_bscan | False = Don't bond out<br>True = Bond out | 0 | Indicates whether or not unused internal BSCAN component signals are bonded out to ports. |
| user_scan_chain | USER1, USER2, USER3, USER4 | USER1 | BSCAN USER scan chain number to be used by the ICON core (1) |

**Notes:**

1. Only USER1 and USER2 are supported for Spartan-3/XA, Spartan-3E/XA, and Spartan-3A/3AN/3A DSP/XA. All other device families support USER1, USER 2, USER3 and USER4.

### Restrictions

The ChipScope Pro tools support only one ICON core per design.

## Configuration

*Table 3:* **Configuration Details**

| Configuration Name | Device | ICON Setup |
|---|---|---|
| Config1 | Xc7v450t-2ffg1761 | Control Ports (1) |
| Config2 | Xc7v450t-2ffg1761 | Control Ports (8) |
| Config3 | Xc7v450t-2ffg1761 | Control Ports (16) |

## Using ICON Core in EDK

The ICON core can be inserted into an embedded processor design using the Xilinx Embedded Development Kit (EDK). In this case, the ICON core depends on a BSCAN component instance whose interface is exported by the OPB_MDM peripheral component (see Figure 4).

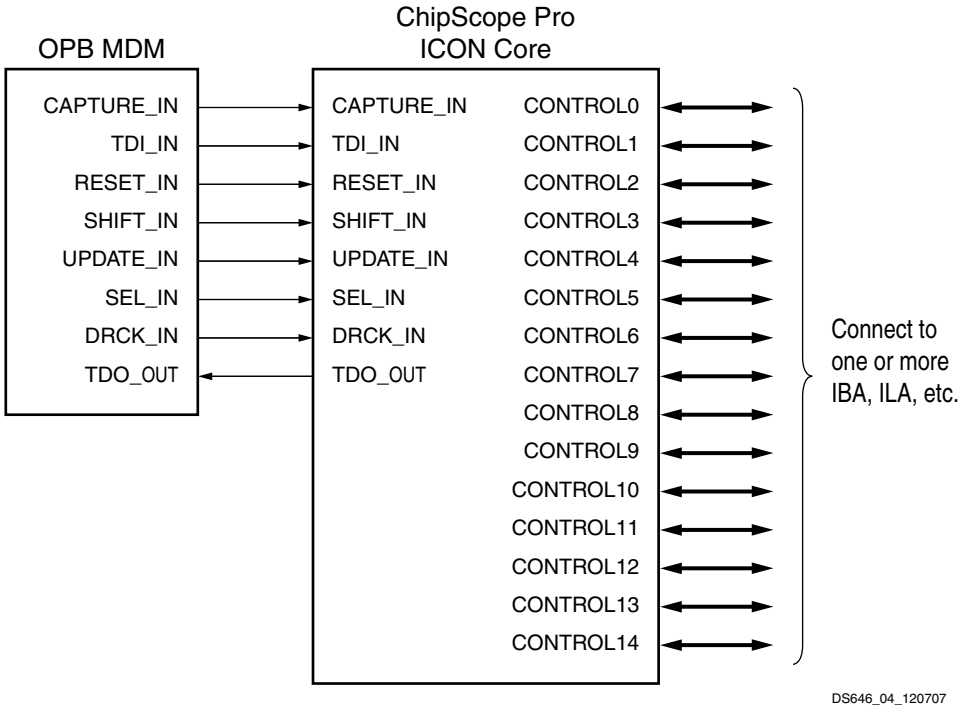


*Figure 4:* **ICON Core Component in EDK XPS Design**

In EDK, the ICON core is integrated into the tool using a Tcl script. When the EDK Hardware Platform Generator (Platgen) tool runs, the Tcl script is called and the script internally calls CORE Generator in command line mode. The Tcl script provides the CORE Generator™ software a parameters file (.xco) to generate the ICON core netlist. The Tcl script also generates an HDL wrapper to match the ICON ports based on the core parameters found in Table 4. The XST synthesis tool is used for synthesizing the wrapper HDL generated for the ICON core. The NGC netlist outputs from XST and ChipScope Pro Core Generator are subsequently incorporated into the Xilinx ISE® tool suite for actual device implementation.

*Table 4:* **ICON EDK-Specific Parameters**

| Parameter Name | Allowable Values | Default Value | Description |
|---|---|---|---|
| c_disable_jtag_bufg_insertion | Integer:<br>1 = Disable BUFG<br>0 = Enable BUFG | 0 | Specifies whether or not a BUFG is added to the JTAG (or DRCK) clock signal. |
| c_family | virtex4, virtex-5, virtex6, virtex6l, virtex7, kintex7, spartan3, spartan3a, spartan3adsp, spartan3e, spartan6, spartan6l, aspartan3, aspartan3a, aspartan3adsp, aspartan3e, aspartan6, avirtex4, qspartan6, qspartan6l, qvirtex4, qspartan6, qspartan6l, qvirtex4, qvirtex5, qvirtex6 | N/A | Target FPGA device family. |
| c_force_bscan_user_port | Integer:<br>1, 3, or 4 (port 2 is used by OPB_MDM) | 1 | BSCAN USER scan chain number to be used by the ICON core. |
| c_num_control_ports | Integer: 1-15 | 1 | Number of ChipScope Pro target cores to be connected to this ICON core. |
| c_system_contains_mdm | Integer:<br>1 = system contains MDM<br>0= system does not contain MDM | 0 (automatically calculated by tools) | Indicates whether or not the system containing the ICON core also contains the OPB_MDM peripheral. This parameter dictates whether a BSCAN component should be instantiated. |

## Verification

Xilinx has verified the ICON core in a proprietary test environment using an internally developed bus functional model.

## References

1. More information on the ChipScope Pro software and cores is available in the Software and Cores User Guide, located at http://www.xilinx.com/documentation.
2. Information about hardware debugging using ChipScope Pro in EDK is available in the Platform Studio online help, located at http://www.xilinx.com/documentation.
3. Information about hardware debugging using ChipScope Pro in System Generator for DSP is available in the Xilinx System Generator for DSP User Guide, located at http://www.xilinx.com/documentation.

## Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

## Ordering Information

This Xilinx LogiCORE IP module is provided at no additional cost with the Xilinx ISE® Design Suite Embedded Edition software under the terms of the Xilinx End User License. The core is generated using the Xilinx ISE Design Suite software. For more information, visit the Chipscope ICON page.

Information about this and other Xilinx LogiCORE IP modules is available at the Xilinx Intellectual Property page. For information on pricing and availability of other Xilinx LogiCORE modules and software, please contact your local Xilinx sales representative.

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 03/24/08 | 1.0 | Release 10.1 (Initial Xilinx release). |
| 09/19/08 | 1.1 | Release 10.1, Service Pack 3 changes. |
| 04/07/09 | 2.0 | Release 11.1. |
| 06/24/09 | 2.1 | Release 11.2. |
| 3/1/2011 | 2.2 | Updated to v1.05a for the 13.1 release. |

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