07

디지털공학개론

기본 논리 연산과 논리 Gate

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기본 논리 연산과 논리 Gate

1.논리 연산과 논리 Gate

2.Gate 회로

3.Gate용 IC Package

1. 논리 연산과 논리 Gate

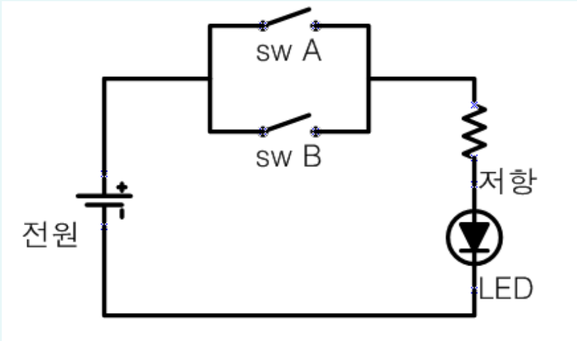
논리 연산(Logical operation, logical connective)

불 연산(Boolean operation)으로 불리며, 참, 거짓 두 가지 원소(진리값으로 불림)만 존재하는 집합(환으로 불림)에서의 연산

- 논리합(OR), 논리곱(AND), 부정(NOT),
  부정 논리-합(NOR), 부정-논리곱(NAND),
  배타적 논리합(XOR), 배타적 부정 논리-합(XNOR) 등

2. 논리합(OR), 논리곱(AND), 논리부정(NOT)

(1) 논리- 합(OR)



Input		Output
sw A	sw B	LED
off	off	off
off	on	on
on	off	on
on	on	on

[Gate Symbol]

[논리식]

$F = A + B$

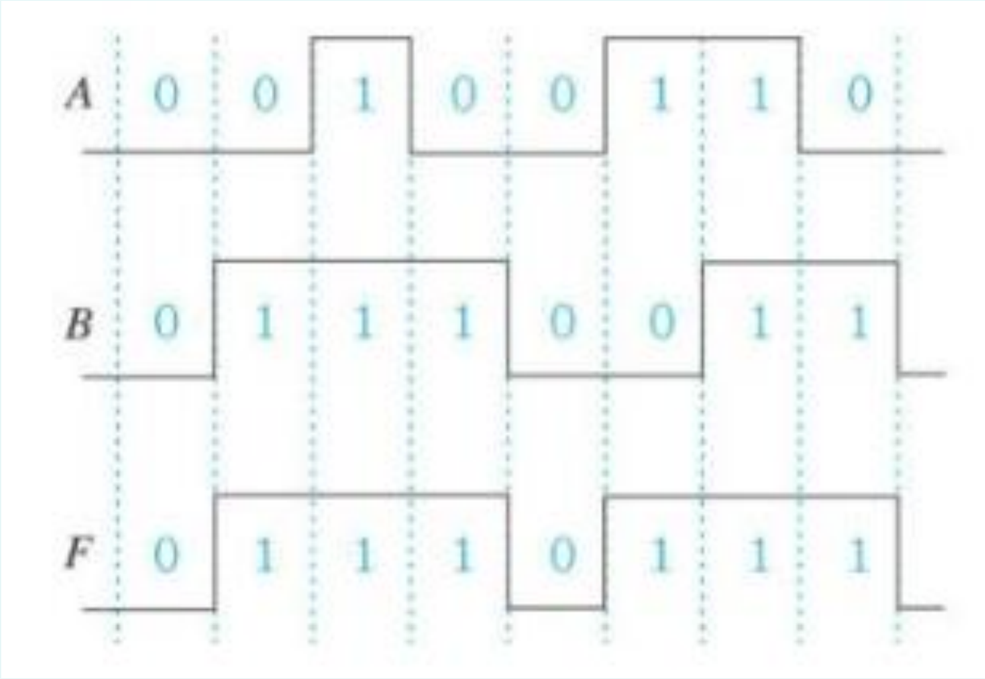
[진리치표]

Input		Output
A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

2. 논리합(OR), 논리곱(AND), 논리부정(NOT)

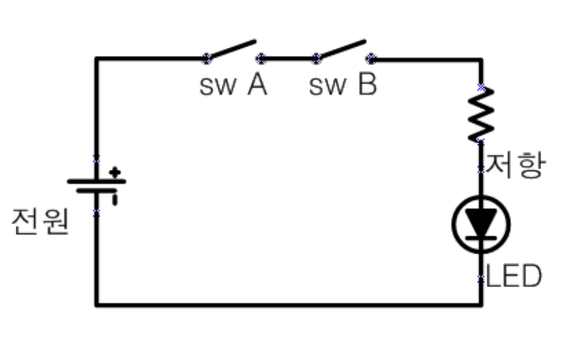
(1) 논리-합(OR)

[OR Gate 입출력 파형]



2. 논리합(OR), 논리곱(AND), 논리부정(NOT)

(2) 논리-곱(AND)



Input		Output
sw A	sw B	LED
off	off	off
off	on	off
on	off	off
on	on	on

[Gate Symbol]

[논리식]

$$F = A \cdot B = AB$$

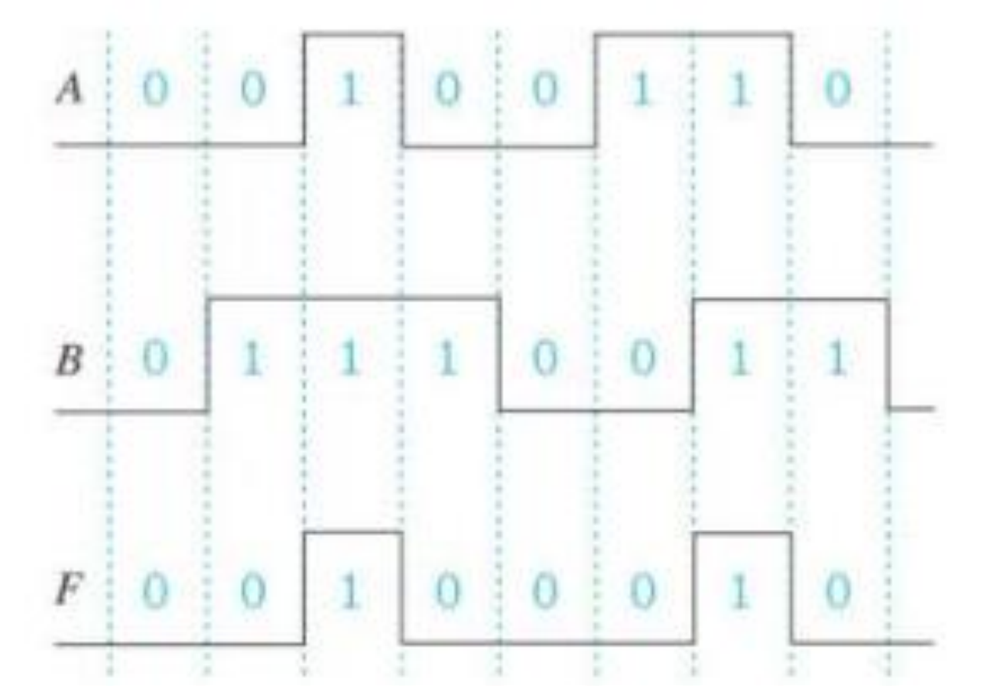
[진리치표]

Input		Output
A	B	A + B
0	0	0
0	1	0
1	0	0
1	1	1

2. 논리합(OR), 논리곱(AND), 논리부정(NOT)

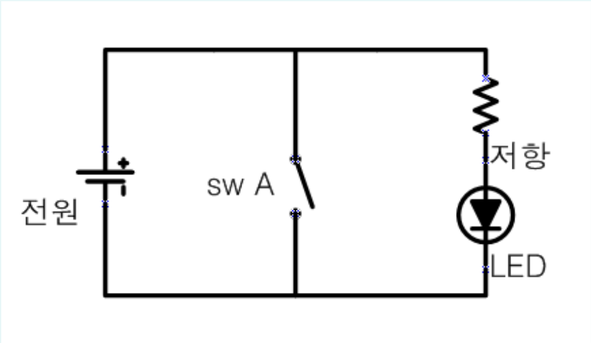
(2) 논리-곱(AND)

[AND Gate 입출력 파형]



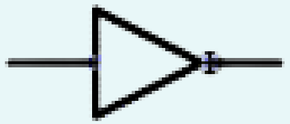
2. 논리합(OR), 논리곱(AND), 논리부정(NOT)

(3) 논리-부정(NOT)



Input	Output
sw A	LED
off	on
on	off

[Gate Symbol]



[논리식]

$$F = \overline{A} = A'$$

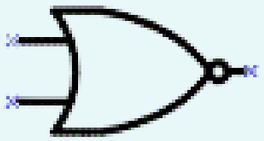
[진리치표]

Input		Output
A	B	F
0	0	1
0	1	1
1	0	0
1	1	0

3. 부정 논리합(NOR) / 부정 논리곱(NAND)

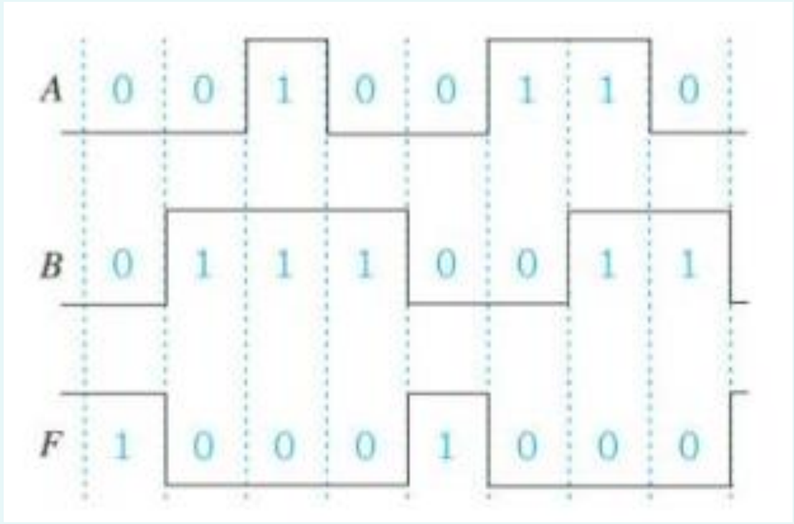
(1) 부정 논리합 (NOR)

[Gate Symbol]



[논리식]

$$F = \overline{A + B}$$



[진리치표]

Input		Output
A	B	$\overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

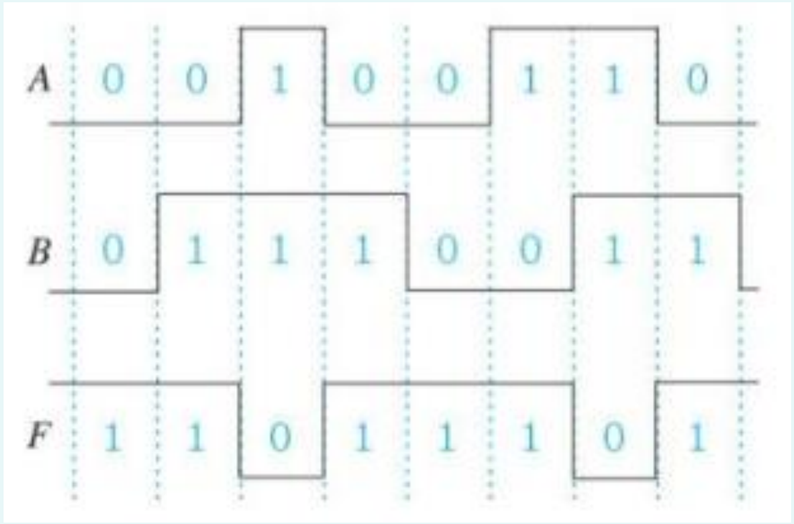
3. 부정 논리합(NOR) / 부정 논리곱(NAND)

(2) 부정 논리곱 (NAND)

[Gate Symbol]

[논리식]

$$F = \overline{A \cdot B}$$



[진리치표]

Input		Output
A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

4. 배타적 논리합(XOR) / 배타적 부정 논리합(NXOR)

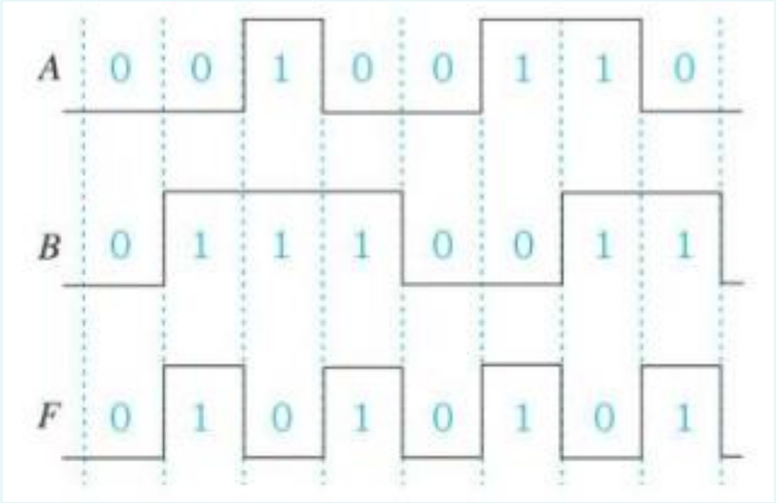
(1) 배타적 논리합(XOR)

[Gate Symbol]

[논리식]

$F = A \oplus B$

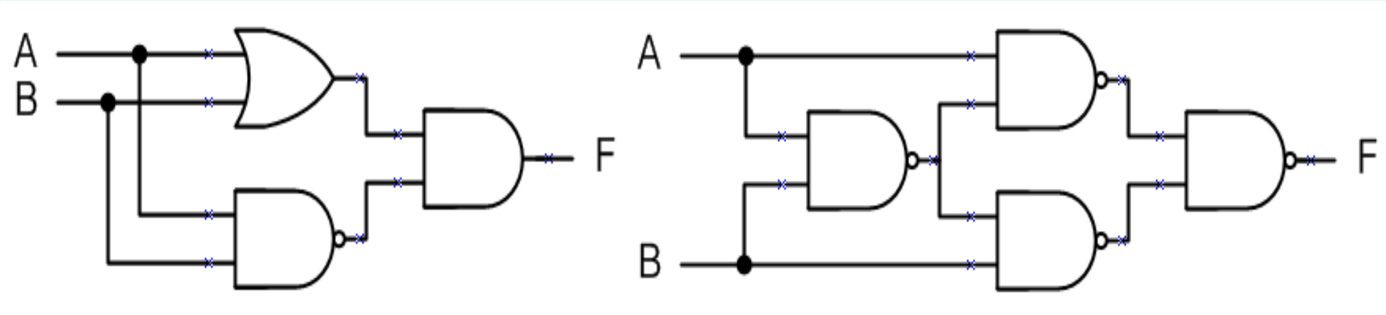
$= A'B + AB'$



[진리치표]

Input		Output
A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

※ 배타적 논리합(XOR) 등가 회로



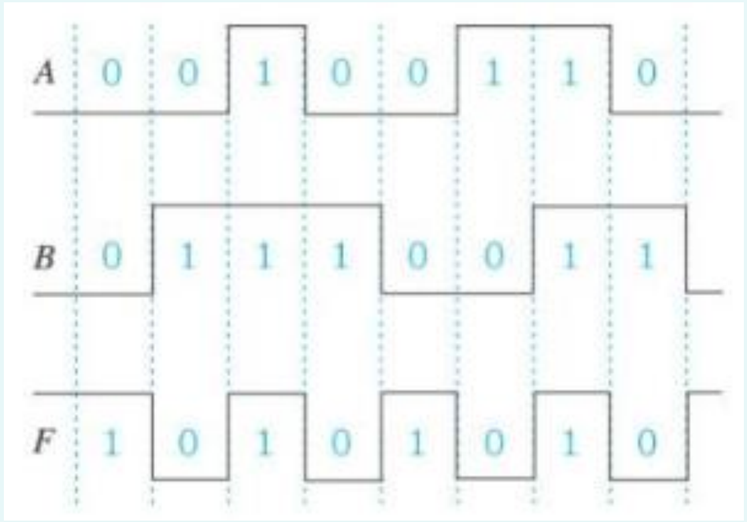
4. 배타적 논리합(XOR) / 배타적 부정 논리합(NXOR)

(2) 배타적 부정 논리합(NXOR)

[Gate Symbol]

[논리식]

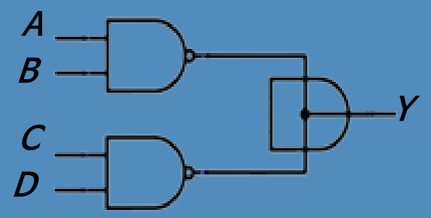
$$F = \overline{A \oplus B}$$
$$= A'B' + AB$$



[진리치표]

Input		Output
A	B	$\overline{A \oplus B}$
0	0	1
0	1	0
1	0	0
1	1	1

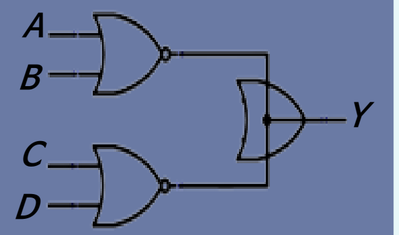
5. 결선형 AND Gate & OR Gate



결선형 AND Gate

- 개방형 콜렉터(Open-collector)형 TTL NAND Gate의 두 출력을 하나의 풀업 저항(Pull-Up Resistor)으로 공통 연결
- 두 출력을 AND 처리한 것과 같은 효과
- AND -OR-Inverter 함수
- $Y = \overline{(A \cdot B)} \cdot \overline{(C \cdot D)} = \overline{(AB + CD)}$

- ECL(Emitter Coupled Logic)의 NOR Gate의 두 출력을 직접 연결
- 두 출력을 OR 처리한 것과 같은 효과
- OR-AND-Inverter
- $Y = \overline{(A + B)} + \overline{(C + D)} = \overline{(A + B) \cdot C + D)}$



결선형 OR Gate

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기본 논리 연산과 논리 Gate

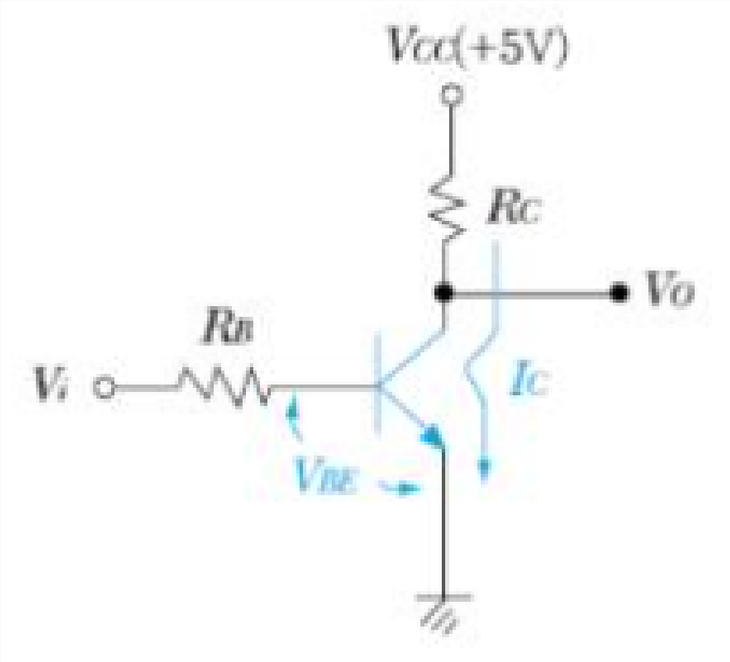
1.논리 연산과 논리 Gate

2.Gate 회로

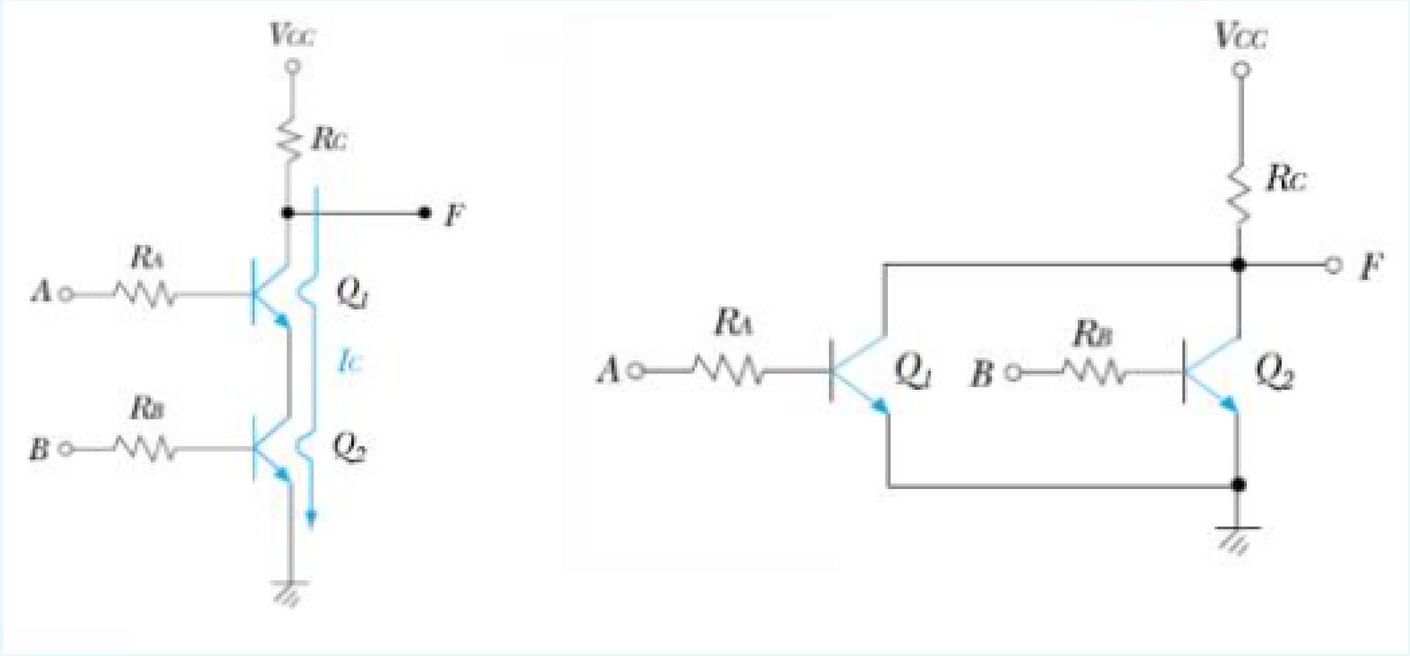
3.Gate용 IC Package

1. 인버터(NOT Gate)

- $V_i = 5V$ (전도 상태) : $V_O = 0V$
- $V_i = 0V$ (차단 상태) : $V_O = 5V$



2. RTL 형 NAND Gate, NOR Gate

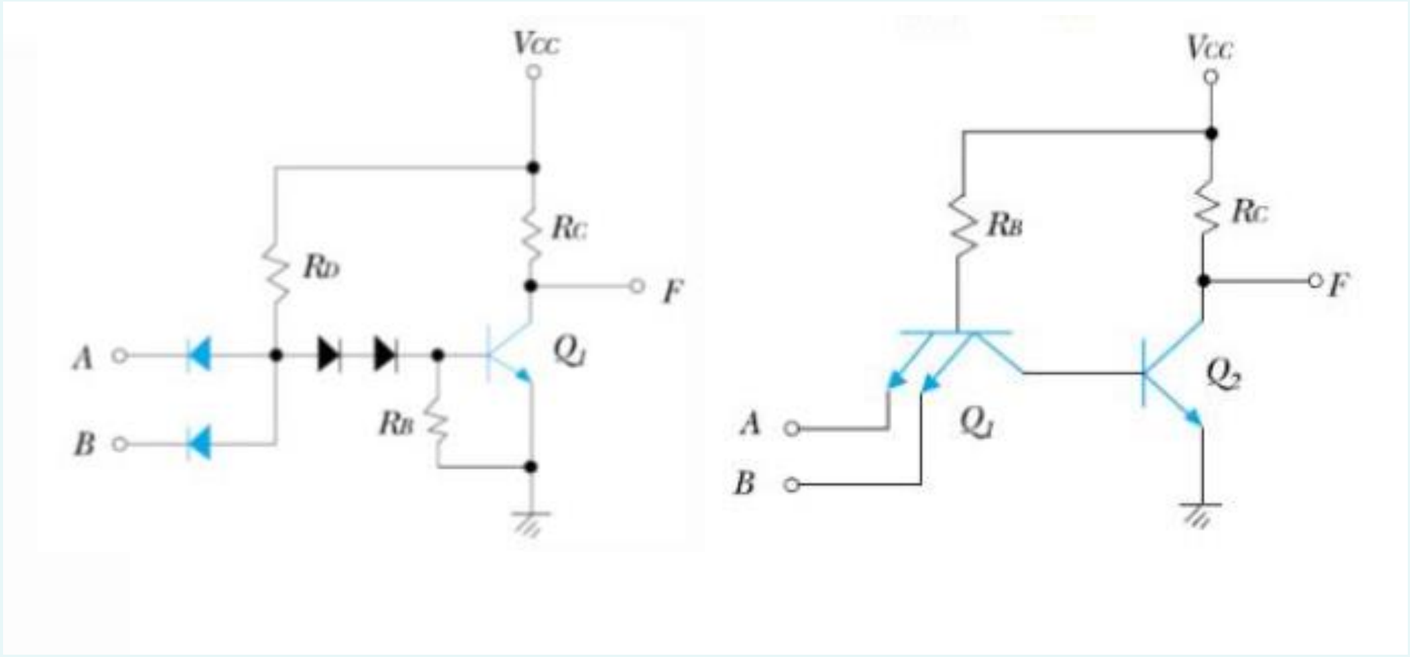


NAND Gate

NOR Gate

3. DTL/TTL형 NAND Gate

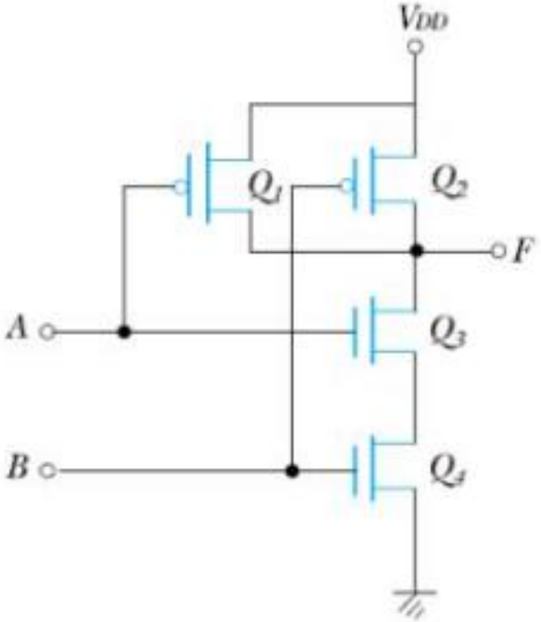
- $\mathbf{A = B = 5V}$ (Q1 전도 상태) : $V_O = 0V$
- $\mathbf{A = }\boldsymbol{and, or}\ \boldsymbol{B = 0V}$ (Q1 차단 상태) : $V_O = 5V$



DTL형 NAND Gate　　TTL형 NAND Gate

4. CMOS형 NAND Gate

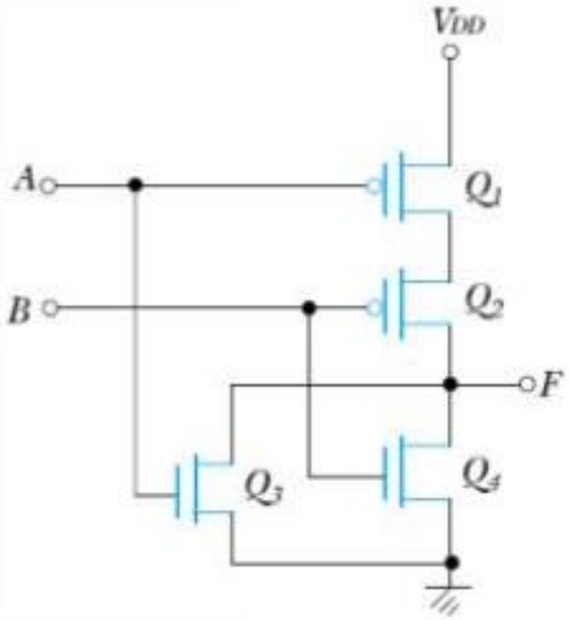
- $\mathbf{A} = \mathbf{B} = 5V$ 일 때 Q1 & Q2 차단 상태(Off), Q3 & Q4 전도 상태(On) 이므로 출력 F = 0V



A	B	Q_1	Q_2	Q_3	Q_4	F
0V	0V	*on*	*on*	*off*	*off*	5V
0V	5V	*on*	*off*	*off*	*on*	5V
5V	0V	*off*	*on*	*on*	*off*	5V
5V	5V	*off*	*off*	*on*	*on*	0V

4. CMOS형 NAND Gate

- $\mathbf{A} = \mathbf{B} = \mathbf{0}V$ 일 때 Q1 & Q2 전도 상태(On), Q3 & Q4 차단 상태(Off) 이므로 출력 F = 5V



A	B	Q_1	Q_2	Q_3	Q_4	F
0V	0V	*on*	*on*	*off*	*off*	5V
0V	5V	*on*	*off*	*off*	*on*	0V
5V	0V	*off*	*on*	*on*	*off*	0V
5V	5V	*off*	*off*	*on*	*on*	0V

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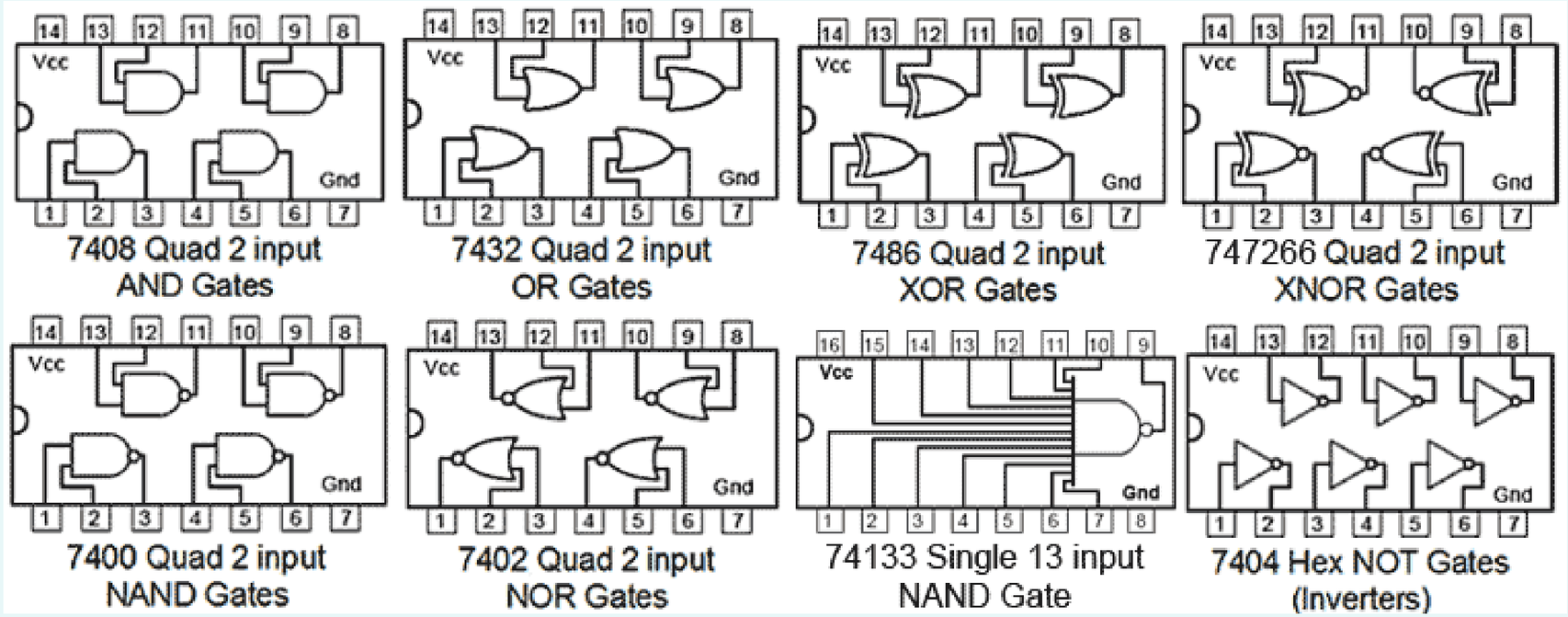
기본 논리 연산과 논리 Gate

1.논리 연산과 논리 Gate

2.Gate 회로

3.Gate용 IC Package

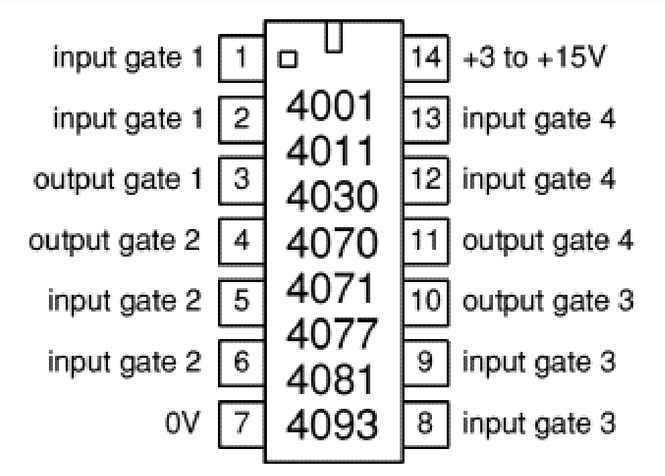
1. 74series TTL Logic ICs



2. 4000 series CMOS Logic ICs

(1) Quad 2-input gates

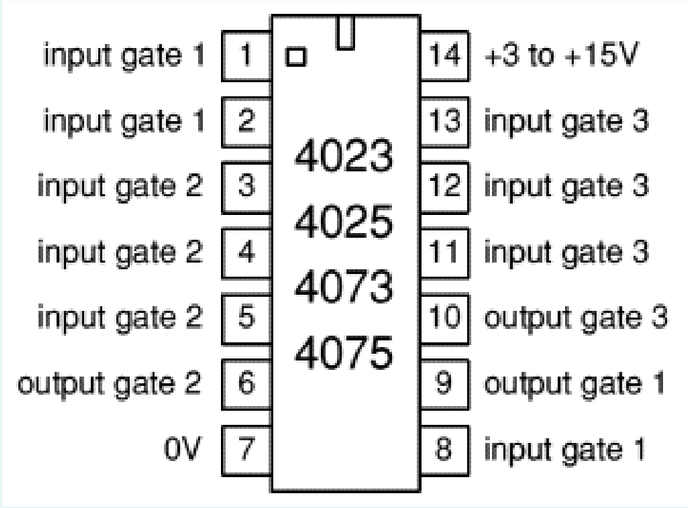
4001 quad 2-input NOR
4011 quad 2-input NAND
4030 quad 2-input EX-OR
(now obsolete)
4070 quad 2-input EX-OR
4071 quad 2-input OR
4077 quad 2-input EX-NOR
4081 quad 2-input AND
4093 quad 2-input NAND
with Schmitt trigger inputs



2. 4000 series CMOS Logic ICs

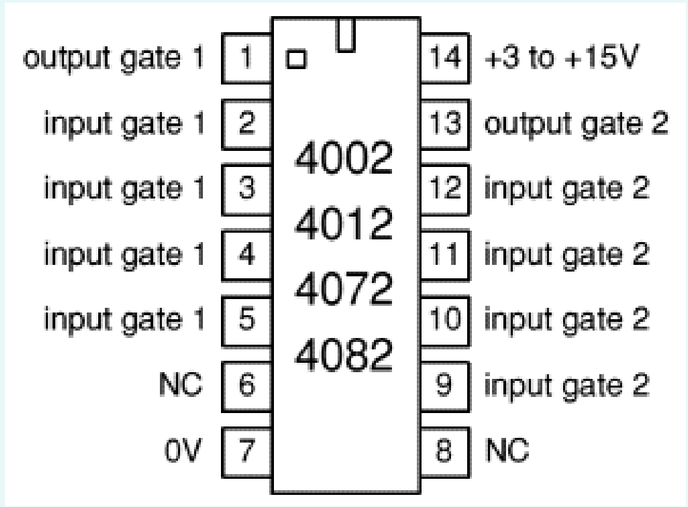
(2) Triple 3-input gates

4023 triple 3-input NAND
4025 triple 3-input NOR
4073 triple 3-input AND
4075 triple 3-input OR



(3) Dual 4-input gates

4002 dual 4-input NOR
4012 dual 4-input NAND
4072 dual 4-input OR
4082 dual 4-input AND



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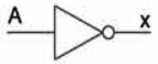
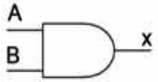
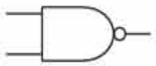
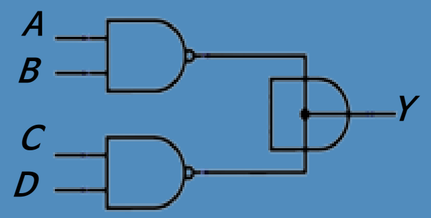
기본 논리 연산과 논리 Gate

- 학습정리

● 기본 논리 게이트

Name	NOT	AND	NAND	OR	NOR	XOR	XNOR
Alg. Expr.	$\overline{A}$	AB	$\overline{AB}$	$A+B$	$\overline{A+B}$	$A \oplus B$	$\overline{A \oplus B}$
Symbol							
Truth Table	A X 0 1 1 0	B A X 0 0 0 0 1 0 1 0 0 1 1 1	B A X 0 0 1 0 1 1 1 0 1 1 1 0	B A X 0 0 0 0 1 1 1 0 1 1 1 1	B A X 0 0 1 0 1 0 1 0 0 1 1 0	B A X 0 0 0 0 1 1 1 0 1 1 1 0	B A X 0 0 1 0 1 0 1 0 0 1 1 1

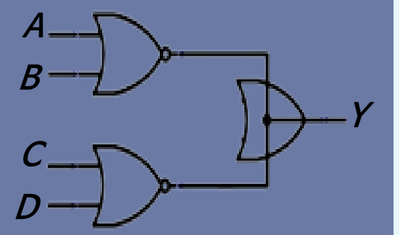
● 결선형 Gate



결선형 AND Gate

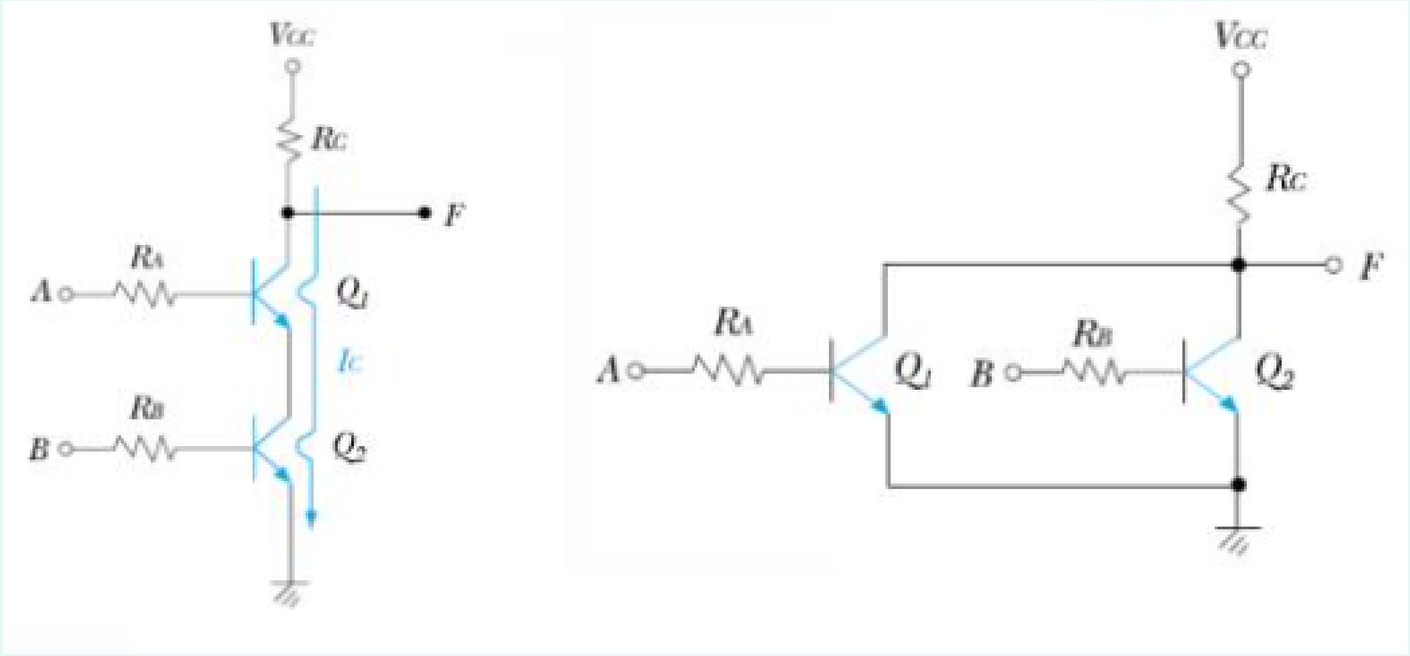
- 개방형 콜렉터(Open-collector)형 TTL NAND Gate의 두 출력을 하나의 풀업 저항(Pull-Up Resistor)으로 공통 연결
- 두 출력을 AND 처리한 것과 같은 효과
- AND -OR-Inverter 함수
- $Y = \overline{(A \cdot B)} \cdot \overline{(C \cdot D)} = \overline{(AB + CD)}$

- ECL(Emitter Coupled Logic)의 NOR Gate의 두 출력을 직접 연결
- 두 출력을 OR 처리한 것과 같은 효과
- OR-AND-Inverter
- $Y = \overline{(A + B)} + \overline{(C + D)} = \overline{(A + B) \cdot C + D)}$



결선형 OR Gate

- **RTL형 NAND Gate 및 NOR Gate**



NAND Gate

NOR Gate