Parth Nileshkumar Patel

Hatfield, PA | 267-638-7889 | parth040501@gmail.com | LinkedIn | Portfolio | US Permanent resident (Green Card)

Dynamic electrical hardware engineer with 3+ years of hands-on experience in PCB and sub-systems design for industrial imaging and camera systems from concept to commercialization. Skilled in problem solving and troubleshooting complex hardware issues.

EDUCATION

Purdue University, West Lafayette, IN |Jan. 2025 (Ongoing) – Expected Dec. 2026|
M.S. - Computer Engineering with concentration in AI/ML, ***GPA****: **3.85/4***
Core Coursework: *Random Variables & Signals, Introduction to Data Mining*

Nirma University, Ahmedabad, India |July 2018 – June 2022|
B. Tech - Electrical Engineering, ***CGPA****: **8.17/10.0 (US equivalent: 3.5/4)***
Core Coursework: *Network analysis and synthesis, Analog and digital electronics, Power electronics, Microprocessors and Microcontrollers, Electronic system design*

WORK EXPERIENCE

Datalogic Labs USA., Hatfield, PA (onsite) |Aug. 2022 – Oct. 2025|
R&D Hardware Engineer – Stationary Industrial Scanners

- Designed schematics of **high-speed, high-current PCB** involving **10G Ethernet interface** and **rigid-flex PCB** involving **HDMI, SD, SATA, USB-C interfaces** for communication with carrier card in **industrial 2D camera**.
- Designed **mixed-signal PCB** including **sensor interfaces (photodiode, IrDA)** and **ADC/DAC conditioning** to control the illuminator of a **12K linear camera**, enabling **50 KHz line rates** and high-resolution images.
- Led feasibility study and early-stage prototyping of a **high-speed focus mechanism** (PoC), assessing actuator technologies, drivers, controllers, and feedback components to enable precision control in **16K linear camera**.
- Executed SoC-centric **board bring-up** including power sequencing, interface validation (I2C, SPI, UART) functional testing, application specific python-based validation scripts, and system-level debugging to ensure a reliable beta release.
- Supported **hardware accelerator (FPGA, NNA, COMe)** validation by designing high efficiency buck converters **(5V @ 18A, 95% and 0.85 V @ 18A, 90%)** and programming low-latency, high-frequency (>100 MHz) clock generators **(LVDS, LVCMOS, LP-HCSL)** with **PLL filter design** to ensure stable timing.
- Spearheaded **electronic cost reduction** activity by redesigning circuits and testing cost-effective alternate components, resulting in annual savings of over $**200K+** for a medium volume procurement.
- Notable contributions: Coordinated with manufacturers to obtain technical data for analytical calculations, led design reviews and hardware platform evaluations, designed custom data/power cables, authored design specifications for stakeholders, troubleshot and resolved field failures, mitigated component lifecycle risks across legacy and new hardware designs, and performed statistical and physics-based data analysis for effective decision-making.

Hitachi Hi-Rel Power Electronics Pvt. Ltd., Sanand, India |Jan. – May 2022|
Project Intern

- Conducted conceptual design of a **230 VAC three phase SMPS** for a **grid-tied solar inverter,** incorporating multistage topologies: 6 Pulse rectifier (110V DC), flyback converter (24V @ 1A), and buck converter (5V @ 1A) with closed-loop control to power control and relay I/O cards.
- Proposed root cause analysis and fishbone diagram of a real-time fault in production of uninterruptible power supply.

ACADEMIC PROJECTS

Wind Energy Conversion System |July. – Dec. 2021|

- Engineered **6 KW WECS model (49% conversion efficiency)** in **MATLAB** using permanent magnet synchronous generator (PMSG) for DC grid through research of publications.
- Incorporated mathematical modelling of wind turbine and integrated it with rectifier and boost converter for direct grid interfacing. Optimization was done using **pitch angle control** and **perturb and observe (P&O) MPPT algorithm**.

Home Automation System |Aug. – Nov. 2020|

- Developed **ladder diagram logic** for controlling interrelated systems by using counters, timers, and data manipulation operations of programmable logic controller (PLC).
- Integrated the logic elements with custom GUI for an interactive environment using **TwinCAT software**.

SKILLS

Languages: C/C++, Python, Assembly (University level).
Software: Mentor graphics EDA, LTSpice, Linux OS, Saturn PCB, HyperLynx, FreeCAD, VS Code, MATLAB, PSIM, MS Office.
Hardware: Oscilloscope, Spectrum analyzer, Signal generator, Programmable load, DMM, Basic soldering & machining.
Applied Concepts: NPI/NPD, Hardware development lifecycle, Signal integrity, Power management, Time sensitive networking, MIPI & PCIe Interfaces (familiarity), Impedance control & stack-up design, Electromechanical systems (Stepper, BLDC, Voice coil actuators), Reverse engineering, Value Engineering, DFX, EMI/EMC pre-compliance.

CERTIFICATIONS

- **'Introduction to FPGA Design for Embedded Systems'** – CU Boulder (Coursera)
- **'Machine Learning'** – Stanford Online (Coursera)