Crimson's Server API

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Last Updated On: July 27th 2015

1 Introduction

A server runs on Crimson that services all UHD (USRP Hardware Driver) or custom programs from host machines. The server is invoked when the Linux OS exits boot, and the possible interfaces are:

- UHD Driver (GNU Radio or C++)
- Webserver located at 192.168.10.2 (default)
- UDP packets to 192.168.10.2:42799 (default)

The instructions for the UHD Driver and Webserver interfaces are illustrated in the Crimson User Manual, however their functions are limited, thus it is advised to use UDP packets for advanced use cases.

Any coding language that supports UDP transactions will be able to communicate with Crimson. The messages are implemented with strings. When writing your custom software to interface with Crimson, please double check the machine's network IP address and port numbers. It is important to note that some properties take extra time to update, if subsequent commands are sent in a fairly short time span, the server will drop the commands. Commands that power on channels take approximately 3 to 4s, and all other commands take approximately 0.1 to 0.7s.

2 Packet Structure

There are two different packet structures, one for transmit and one for receive. Table **??** details the packet structure for the respective transactions. The packet contents are deliminated with commas (CSV) and the data field is optional depending on the property specified.

Transmit	Sequence Number	Operation	Property	[Data]
Receive	Sequence Number	Operation	[Data]	

Table 1: Packet Structure

The description of the fields in Table **??** are described below:

Sequence No: uint32_t value to confirm corresponding acknowledge packets. Useful for UDP out-of-order messages.

Operation: "get" or "set"

Property: Full property path, refer to the API section and concatenate '/' between directories.

Data: String representation of the data, refer to Section **??** under the heading "Function"

Status: "0": no error, "1": error

3 Examples

This section will show two examples, one to set a property, and one to get a property.

Step 1: Transmit (cmd)	1,set,rx_a/rf/gain/val,65
Step 2: Receive (ack)	1,0

Table 2: Set Property

Step 1: Transmit (cmd)	78,get,rx_a/rf/gain/val
Step 2: Receive (ack)	78,0,65

Table 3: Get Property

4 API

The following pages will detail the possible properties that can be accessed with Crimson. TX and RX properties contain an additional channel field to the root path. Thus there tx_a/pwr, ta_b/pwr, tx_c/pwr, and tx_d/pwr. There are also additional notes to the properties as well, which are described here:

> [**1**]: This is a dual cycle read property. To read from it, you will need to first: write a 1 to the property first to tell the server to update the contents of the property, and then second: read the updated value from the property.

Property Path				Permissions	Notes	Function
TX	PWR			RW		Power of DSP and RF chain (1) on, (0) off, Resets all settings.
	RF	DAC	NCO	RW		DAC clock frequency (Mhz)
			TEMP	RW		Temperature of the DAC IC (Celcius)
		FREQ	VAL	RO	[1]	Tune the RF chain to desired frequency (Hz)
			BAND	RW		RF band that was chosen after tuning (1) High, (0) Low
			I_BIAS	RW		Adjust I-bias (in 100mV's)
			Q_BIAS	RW		Adjust Q-bias (in 100mV's)
		GAIN	VAL	RW		Set RF chain gain (dB)
		BOARD	STATUS	RW	[1]	Not implemented Yet
			DUMP	WO		Dump all of the registers of the device into /tmp/dump.txt
			TEST	WO		Not implemented Yet
			TEMP	RW	[1]	Temperature of the RF board (Celcius)
			LED	WO		Number of times to toggle the LED
	DSP	GAIN		RW		Not implemented Yet
		RATE		RW		Sample Rate (SPS)
		NCO_ADJ		RW		Frequency Mixing (Hz)
		RSTREQ		WO		Request a reset to the DSP chain
	ABOUT	ID		RW		ID of the TX board
		SERIAL		RO		Serial Number of the TX Board
		FW_VER		RO		Compilation Date of UHD Server
		HW_VER		RO		Compilation Date of UHD Server
		SW_VER		RO		Compilation Date of UHD Server
	LINK	VITA_EN		RW		Enable VITA headers (1) or disable (0)
		IFACE		RW		Not implemented Yet (Refer to user manual for defaults)
		PORT		RW		UDP port to receive from (host ->output packets)

Table 4: TX API Properties

Property Path				Permissions	Notes	Function
RX	PWR			RW		Power of the DSP and RF chain (1) on, (0) off, Resets all settings
	RF	FREQ	VAL	RW		Tune the RF chain to desired frequency (Hz)
			BAND	RW		RF band that was chosen after tuning (1) High, (0) Low
			LNA	RW		Bypass the LNA (1) Bypass, (0) LNA
		GAIN	VAL	RW		Set RF chain gain (dB)
		BOARD	STATUS	RW	[1]	Not implemented Yet
			DUMP	WO		Dump all of the registers of the device into /tmp/dump.txt
			TEST	WO		Not implemented Yet
			TEMP	RW	[1]	Temperature of the RF board (Celcius)
			LED	WO		Number of times to toggle the LED
	DSP	SIGNED		RW		DSP output to be signed (1) or unsigned (0)
		GAIN		RW		Not implemented Yet
		RATE		RW		Sample Rate (SPS)
		NCO_ADJ		RW		Frequency Mixing (Hz)
		RSTREQ		WO		Request a reset to the DSP chain
	ABOUT	ID		RW		ID of the TX board
		SERIAL		RO		Serial Number of the TX Board
		FW_VER		RO		Compilation Date of UHD Server
		HW_VER		RO		Compilation Date of UHD Server
		SW_VER		RO		Compilation Date of UHD Server
	LINK	VITA_EN		RW		Enable VITA headers (1) or disable (0)
		IFACE		RW		Not implemented Yet (Refer to user manual for defaults)
		PORT		RW		UDP port to transmit to (port for host to listen to)
		IP_DEST		RW		IP address to transmit to (address of host)
		MAC_DEST		RW		MAC address to transmit to (address of host)

Table 5: RX API Properties

Property Path			Permissions	Notes	Function
TIME	CLK	PPS	RW		Not implemented Yet
		CUR_TIME	RW	[1]	Current time of Crimson
	SOURCE	VCO	RW		VCO clock source (internal/external)
		SYNC	RW		Sync clock source (internal/external)
		REF	RW		Ref clock source (internal/external)
	BOARD	STATUS	RW	[1]	Not implemented Yet
		DUMP	WO		Dump all of the registers of the device into /tmp/dump.txt
		TEST	WO		Not implemented Yet
		TEMP	RW	[1]	Temperature of the RF board (Celcius)
		LED	WO		Number of times to toggle the LED
	ABOUT	ID	RW		ID of the Time board
		SERIAL	RO		Serial Number of the Time Board
		FW_VER	RO		Compilation Date of UHD Server
		HW_VER	RO		Compilation Date of UHD Server
		SW_VER	RO		Compilation Date of UHD Server

Table 6: Time API Properties

Property Path				Permissions	Notes	Function
FPGA	BOARD	STATUS		RW	[1]	Not implemented Yet
		DUMP		WO		Dump all of the registers of the device into /tmp/dump.txt
		TEST		WO		Not implemented Yet
		TEMP		RW	[1]	Temperature of the RF board (Celcius)
		LED		WO		Number of times to toggle the LED
		RSTREQ		WO		Request a reset to the FPGA
		JESD_RSTREQ		WO		Request a reset to the JESD link
		SYS_RSTREQ		WO		Request a reset to entire Crimson
	ABOUT	ID		RW		ID of the FPGA board
		SERIAL		RO		Serial Number of the FPGA Board
		FW_VER		RO		FW Version on the FPGA DSP chain
		HW_VER		RO		HW version of the FPGA Board
		SW_VER		RO		SW version of the FPGA Board
	LINK	RATE		RW		Not implemented Yet
		SFPA	IP_ADDR	RW		IP Address of SFPA port (host -¿ output packets)
			MAC_ADDR	RW		MAC Address of SFPA port (host -¿ output packets)
			VER	RW		IP protocol version (1) IPV6 (0) IPV4
			PAY_LEN	RW		Payload Len (bytes)
		SFPB	IP_ADDR	RW		IP Address of SFPA port (host -¿ output packets)
			MAC_ADDR	RW		MAC Address of SFPB port (host -¿ output packets to)
			VER	RW		IP protocol version (1) IPV6 (0) IPV4
			PAY_LEN	RW		Payload Len (bytes)
		NET	DHCP_EN	RW		Not implemented Yet
			HOSTNAME	RW		Name of Crimson
			IP_ADDR	RW		IP Address of Management Port

Table 7: FPGA API Properties