1. Description

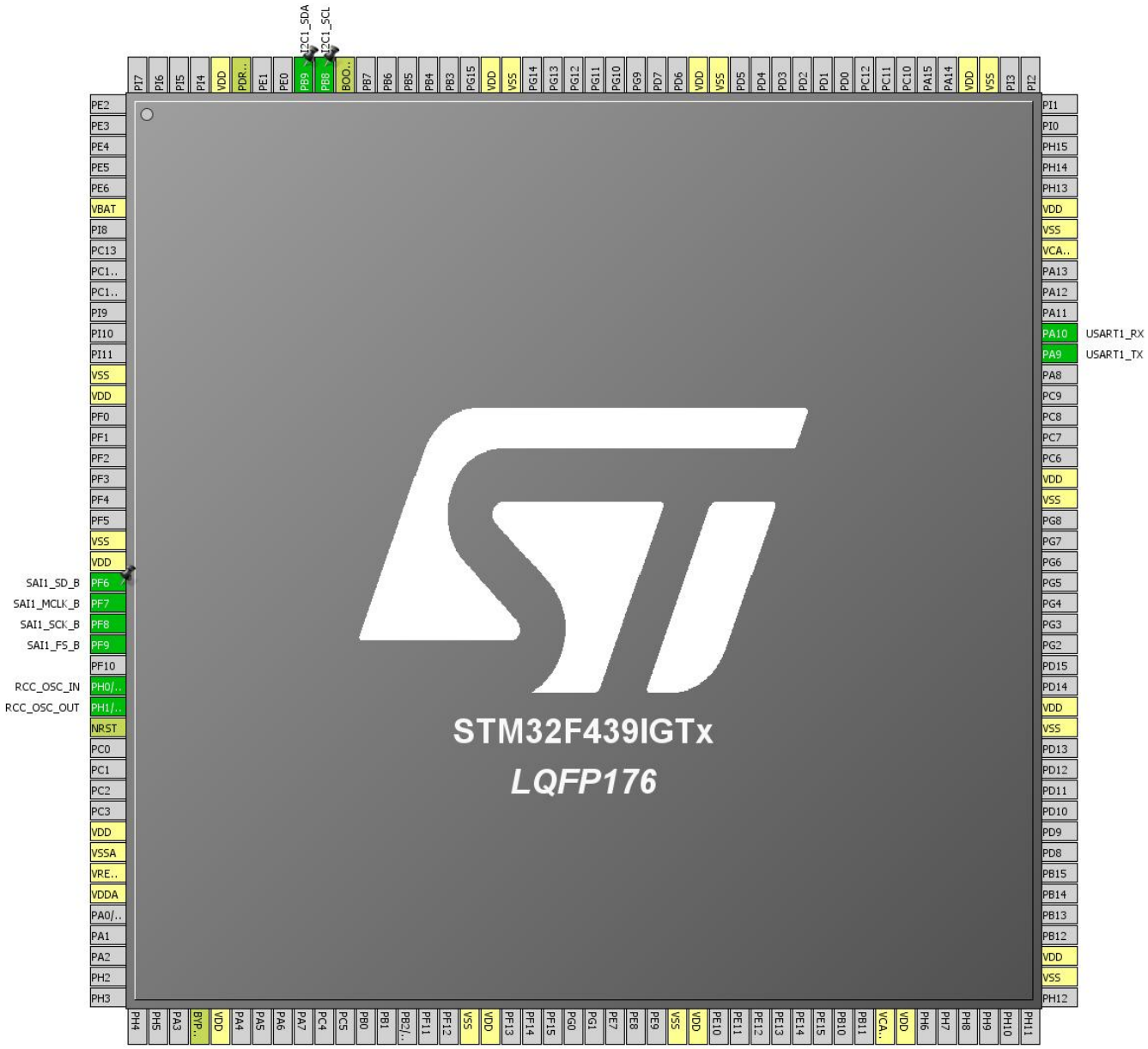
1.1. Project

Project Name	STM32F429I
Board Name	STM32F429I
Generated with:	STM32CubeMX 4.12.0
Date	12/14/2015

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F439IGTx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration

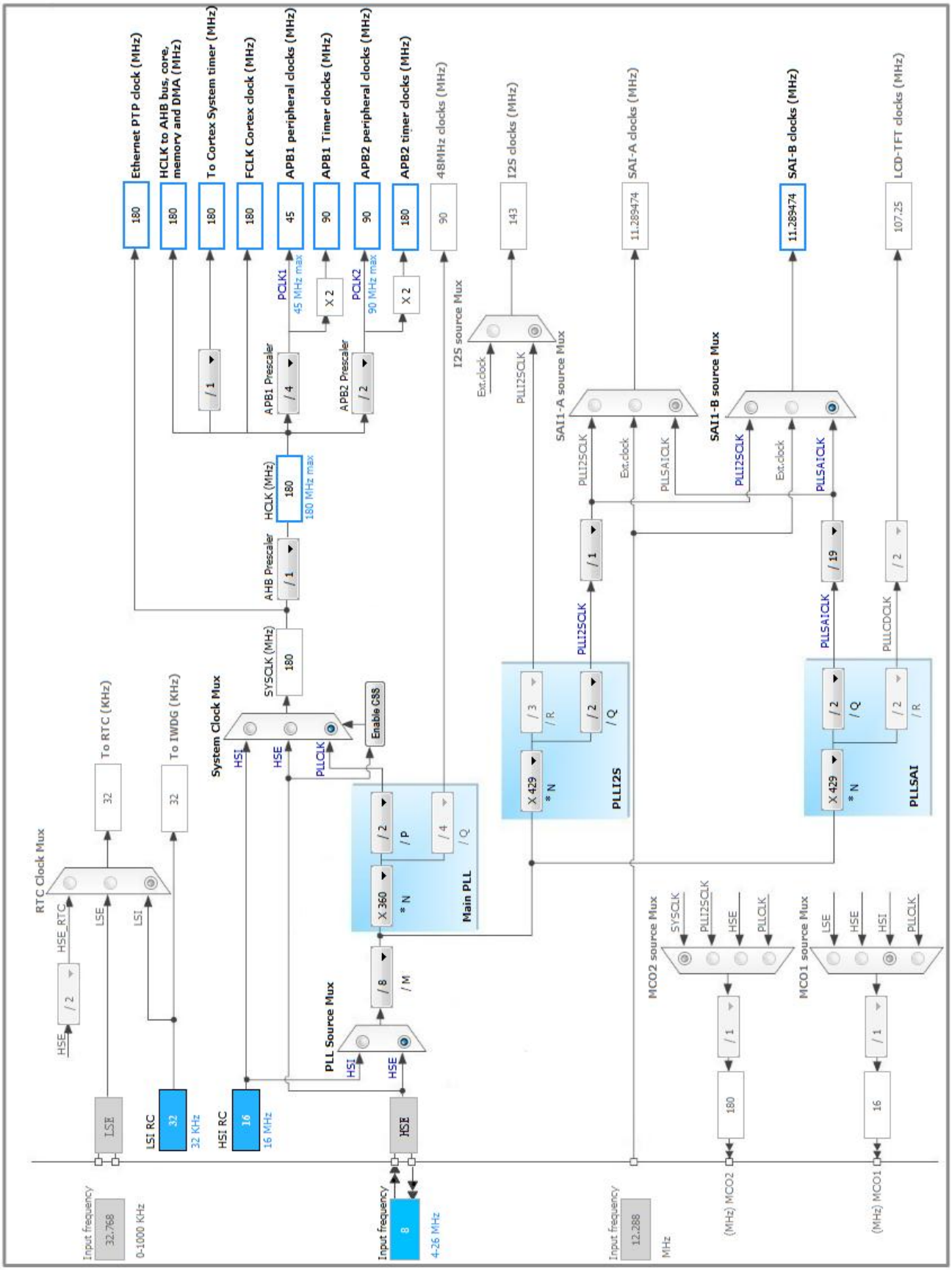


3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
14	VSS	Power		
15	VDD	Power		
22	VSS	Power		
23	VDD	Power		
24	PF6	I/O	SAI1_SD_B	
25	PF7	I/O	SAI1_MCLK_B	
26	PF8	I/O	SAI1_SCK_B	
27	PF9	I/O	SAI1_FS_B	
29	PH0/OSC_IN	I/O	RCC_OSC_IN	
30	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
48	BYPASS_REG	Reset		
49	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VSS	Power		
72	VDD	Power		
81	VCAP_1	Power		
82	VDD	Power		
90	VSS	Power		
91	VDD	Power		
102	VSS	Power		
103	VDD	Power		
113	VSS	Power		
114	VDD	Power		
120	PA9	I/O	USART1_TX	
121	PA10	I/O	USART1_RX	
125	VCAP_2	Power		
126	VSS	Power		
127	VDD	Power		
135	VSS	Power		

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
136	VDD	Power		
148	VSS	Power		
149	VDD	Power		
158	VSS	Power		
159	VDD	Power		
166	BOOT0	Boot		
167	PB8	I/O	I2C1_SCL	
168	PB9	I/O	I2C1_SDA	
171	PDR_ON	Reset		
172	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. I2C1

I2C: I2C

5.1.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

5.3. SAI1

SAI_B Mode: Master with Master Clock Out

5.3.1. Parameter Settings:

SAI B:

Basic Parameters	
Protocol	Free
Audio Mode	Master Transmit
Frame Length	**32 bits ***
Data Size	**16 Bits ***
Slot Size	**16 Bits ***
Frame Parameters	
First Bit	MSB First
Frame Synchro Active Level Length	**16 ***
Frame Synchro Definition	**Channel Identification ***
Frame Synchro Polarity	Active Low
Frame Synchro Offset	First Bit
Slot Parameters	
First Bit Offset	0
Number of Slots (only Even Values)	2
Slot Active Final Value	**0x00030000 ***
Slot Active	**User Setting ***
Slot 0 Active	**true ***
Slot 1 Active	**true ***
Clock Parameters	
Clock Source	SAI PLL Clock
Master Clock Divider	**Enabled ***
Audio Frequency	**22 KHz ***
Real Audio Frequency	**22.049 KHz ***
Error between Selected	**0.22 % ***
Clock Strobing	**Rising Edge ***
Advanced Parameters	
Fifo Threshold	**One Quarter Full ***
Output Drive	**Enabled ***

5.4. USART1

Mode: Asynchronous

5.4.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB8	I2C1_SCL	Alternate Function Open Drain	**No pull-up and no pull-down ***	**High ***	
	PB9	I2C1_SDA	Alternate Function Open Drain	**No pull-up and no pull-down ***	**High ***	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SAI1	PF6	SAI1_SD_B	Alternate Function Push Pull	**Pull-up ***	**Fast ***	
	PF7	SAI1_MCLK_B	Alternate Function Push Pull	**Pull-down ***	**Fast ***	
	PF8	SAI1_SCK_B	Alternate Function Push Pull	**Pull-up ***	**Fast ***	
	PF9	SAI1_FS_B	Alternate Function Push Pull	**Pull-up ***	**Fast ***	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**High ***	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
SAI1_B	DMA2_Stream5	Memory To Peripheral	**High ***

SAI1_B: DMA2_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	**Enable ***
FIFO Threshold:	**Half Full ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Half Word ***
Memory Data Width:	**Half Word ***
Peripheral Burst Size:	Single
Memory Burst Size:	Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
DMA2 stream5 global interrupt	true	0	0
Non maskable interrupt	unused		
Hard fault interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug monitor	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART1 global interrupt	unused		
SAI1 global interrupt	unused		

*** User modified value**

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F439IGTx
Datasheet	024244_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STM32F429I
Project Folder	C:\Users\Administrator\Desktop\stm32cube\STM32F429I\34.SAI-UDA1380
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.10.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No