

1. Description

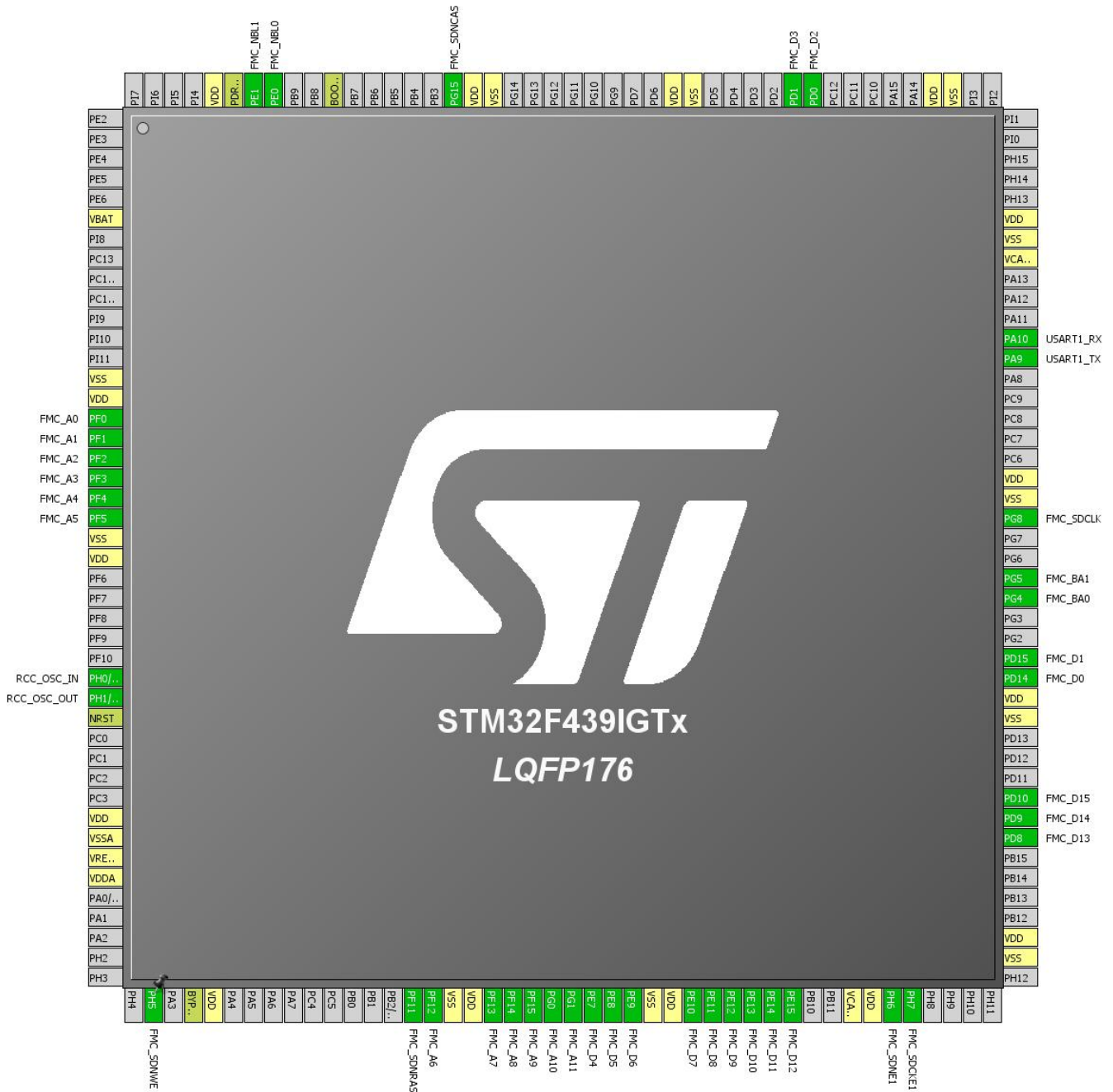
1.1. Project

Project Name	STM32F429I
Board Name	STM32F429I
Generated with:	STM32CubeMX 4.11.0
Date	10/28/2015

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F439IGTx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



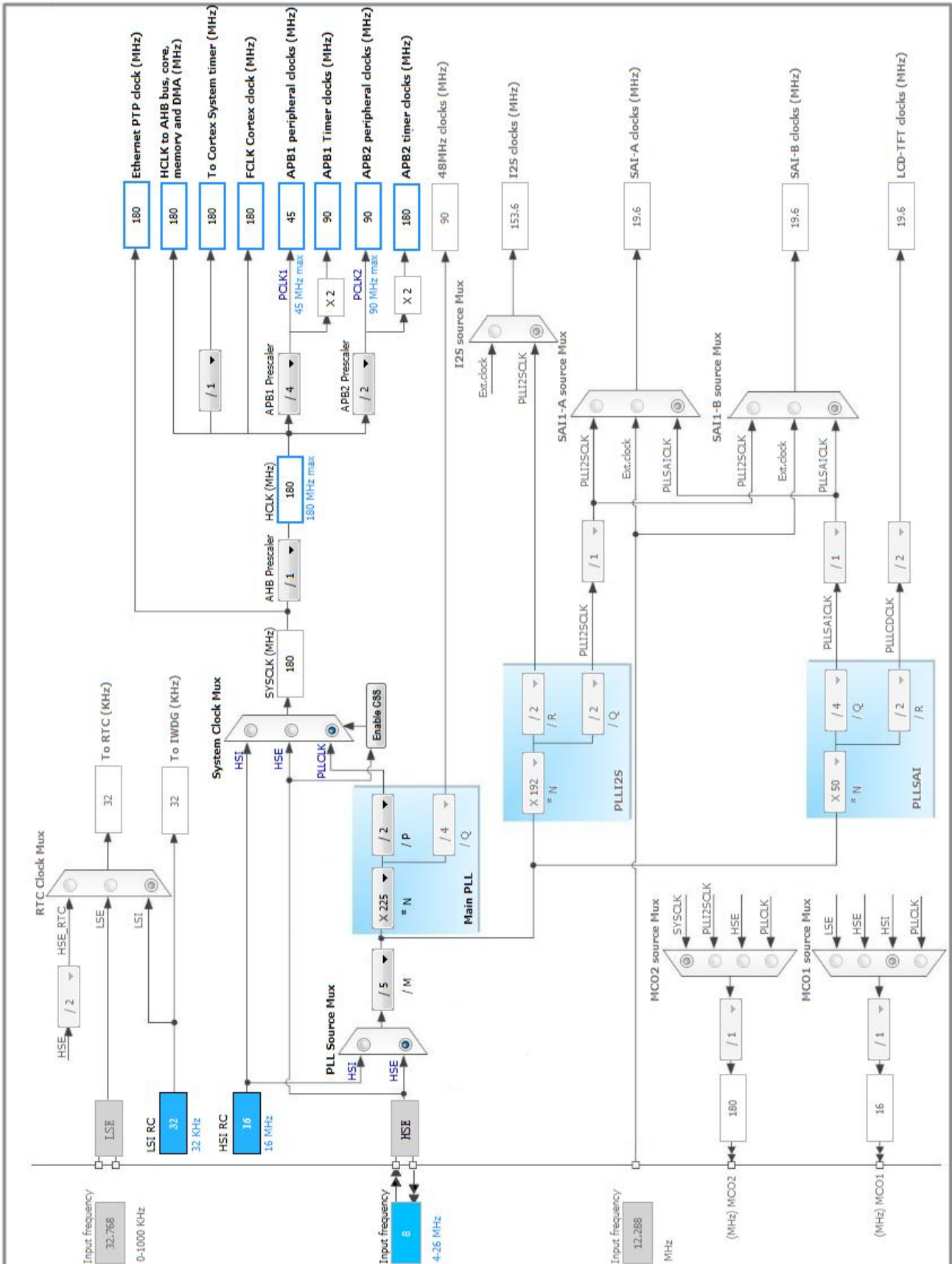
3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
6	VBAT	Power		
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	FMC_A0	
17	PF1	I/O	FMC_A1	
18	PF2	I/O	FMC_A2	
19	PF3	I/O	FMC_A3	
20	PF4	I/O	FMC_A4	
21	PF5	I/O	FMC_A5	
22	VSS	Power		
23	VDD	Power		
29	PH0/OSC_IN	I/O	RCC_OSC_IN	
30	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
46	PH5	I/O	FMC_SDNWE	
48	BYPASS_REG	Reset		
49	VDD	Power		
59	PF11	I/O	FMC_SDNRAS	
60	PF12	I/O	FMC_A6	
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	FMC_A7	
64	PF14	I/O	FMC_A8	
65	PF15	I/O	FMC_A9	
66	PG0	I/O	FMC_A10	
67	PG1	I/O	FMC_A11	
68	PE7	I/O	FMC_D4	
69	PE8	I/O	FMC_D5	
70	PE9	I/O	FMC_D6	
71	VSS	Power		
72	VDD	Power		
73	PE10	I/O	FMC_D7	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
74	PE11	I/O	FMC_D8	
75	PE12	I/O	FMC_D9	
76	PE13	I/O	FMC_D10	
77	PE14	I/O	FMC_D11	
78	PE15	I/O	FMC_D12	
81	VCAP_1	Power		
82	VDD	Power		
83	PH6	I/O	FMC_SDNE1	
84	PH7	I/O	FMC_SDCKE1	
90	VSS	Power		
91	VDD	Power		
96	PD8	I/O	FMC_D13	
97	PD9	I/O	FMC_D14	
98	PD10	I/O	FMC_D15	
102	VSS	Power		
103	VDD	Power		
104	PD14	I/O	FMC_D0	
105	PD15	I/O	FMC_D1	
108	PG4	I/O	FMC_BA0	
109	PG5	I/O	FMC_BA1	
112	PG8	I/O	FMC_SDCLK	
113	VSS	Power		
114	VDD	Power		
120	PA9	I/O	USART1_TX	
121	PA10	I/O	USART1_RX	
125	VCAP_2	Power		
126	VSS	Power		
127	VDD	Power		
135	VSS	Power		
136	VDD	Power		
142	PD0	I/O	FMC_D2	
143	PD1	I/O	FMC_D3	
148	VSS	Power		
149	VDD	Power		
158	VSS	Power		
159	VDD	Power		
160	PG15	I/O	FMC_SDNCAS	
166	BOOT0	Boot		
169	PE0	I/O	FMC_NBL0	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
170	PE1	I/O	FMC_NBL1	
171	PDR_ON	Reset		
172	VDD	Power		

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. FMC

SDRAM 1

Clock and chip enable: SDCKE1+SDNE1

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: 16-bit byte enable

5.1.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 2
Column bit number	8 bits
Row bit number	12 bits *
CAS latency	3 memory clock cycles *
Write protection	Disabled
SDRAM common clock	2 HCLK clock cycles *
SDRAM common burst read	Disabled
SDRAM common read pipe delay	0 HCLK clock cycle

SDRAM timing in memory clock cycles:

Load mode register to active delay	2 *
Exit self-refresh delay	6 *
Self refresh time	4 *
SDRAM common row cycle delay	6 *
Write recovery time	2 *
SDRAM common row precharge delay	2 *
Row to column delay	2 *

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

5.3. USART1

Mode: Asynchronous

5.3.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

* User modified value

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PH6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PH7	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	High	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	High *	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	High *	

6.2. DMA configuration

DMA request	Stream	Direction	Priority
MENTOMEM	DMA2_Stream0	Memory To Memory	Low

MENTOMEM: DMA2_Stream0 DMA request Settings:

Mode: Normal
 Use fifo: **Enable ***
 FIFO Threshold: Full
 Src Memory Increment: **Enable ***
 Dst Memory Increment: **Enable ***
 Src Memory Data Width: **Word ***
 Dst Memory Data Width: **Word ***
 Src Memory Burst Size: Single
 Dst Memory Burst Size: Single

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
FMC global interrupt	true	5	0
Non maskable interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug monitor	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USART1 global interrupt	unused		
DMA2 stream0 global interrupt	unused		

* User modified value

7. Power Plugin report

7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F439IGTx
Datasheet	024244_Rev6

7.2. Parameter Selection

Temperature	25
Vdd	null

8. Software Project

8.1. Project Settings

Name	Value
Project Name	STM32F429I
Project Folder	C:\Users\Administrator\Desktop\stm32cube\STM32F429I\26.SDRAM
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.9.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No