

## 1. Description

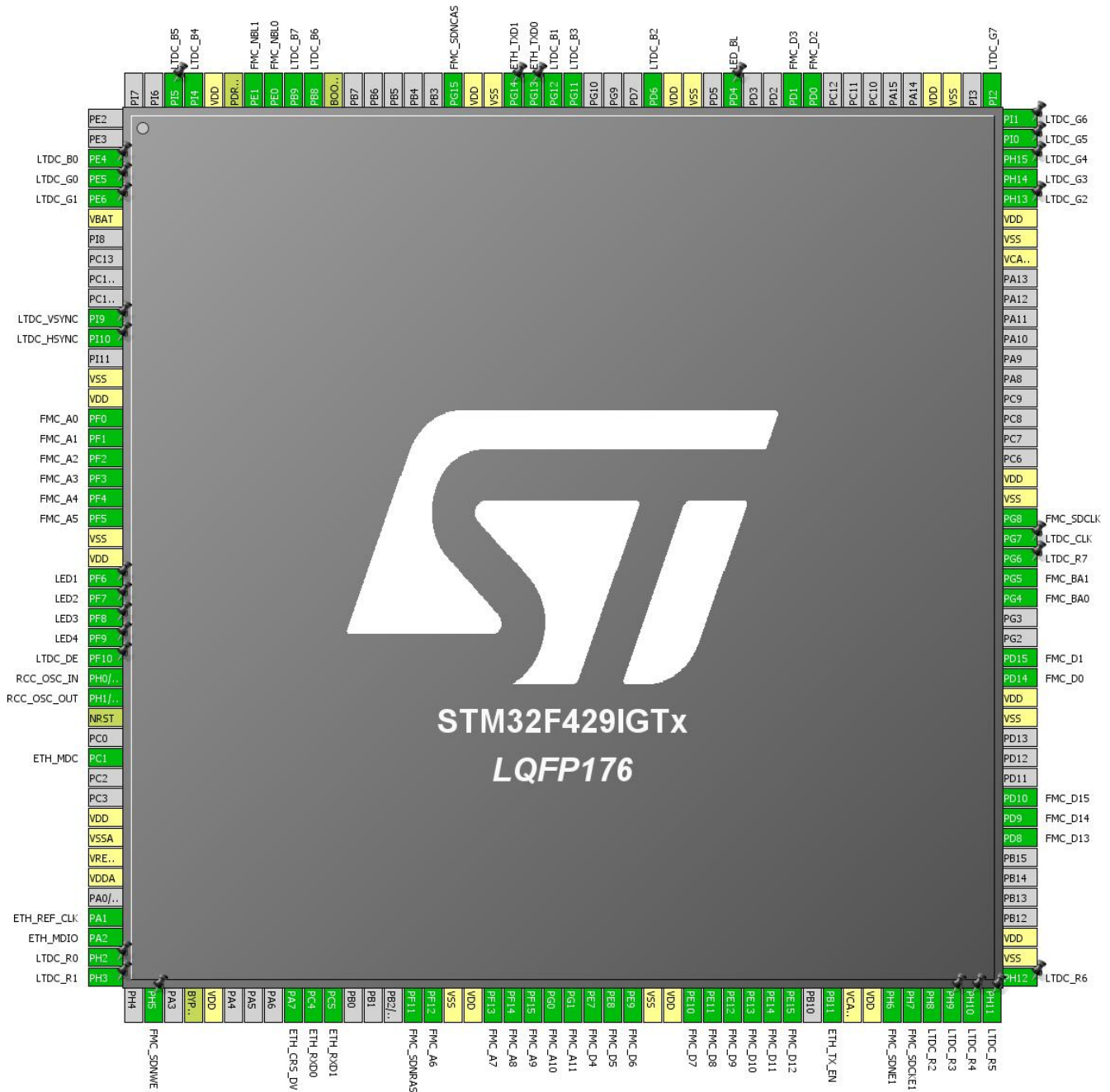
### 1.1. Project

Project Name	STM32F429I
Board Name	STM32F429I
Generated with:	STM32CubeMX 4.11.0
Date	11/24/2015

### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F429/439
MCU name	STM32F429IGTx
MCU Package	LQFP176
MCU Pin number	176

## 2. Pinout Configuration



### 3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
3	PE4	I/O	LTDC_B0	
4	PE5	I/O	LTDC_G0	
5	PE6	I/O	LTDC_G1	
6	VBAT	Power		
11	PI9	I/O	LTDC_VSYNC	
12	PI10	I/O	LTDC_HSYNC	
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	FMC_A0	
17	PF1	I/O	FMC_A1	
18	PF2	I/O	FMC_A2	
19	PF3	I/O	FMC_A3	
20	PF4	I/O	FMC_A4	
21	PF5	I/O	FMC_A5	
22	VSS	Power		
23	VDD	Power		
24	PF6 *	I/O	GPIO_Output	LED1
25	PF7 *	I/O	GPIO_Output	LED2
26	PF8 *	I/O	GPIO_Output	LED3
27	PF9 *	I/O	GPIO_Output	LED4
28	PF10	I/O	LTDC_DE	
29	PH0/OSC_IN	I/O	RCC_OSC_IN	
30	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
33	PC1	I/O	ETH_MDC	
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
41	PA1	I/O	ETH_REF_CLK	
42	PA2	I/O	ETH_MDIO	
43	PH2	I/O	LTDC_R0	
44	PH3	I/O	LTDC_R1	
46	PH5	I/O	FMC_SDNWE	
48	BYPASS_REG	Reset		
49	VDD	Power		

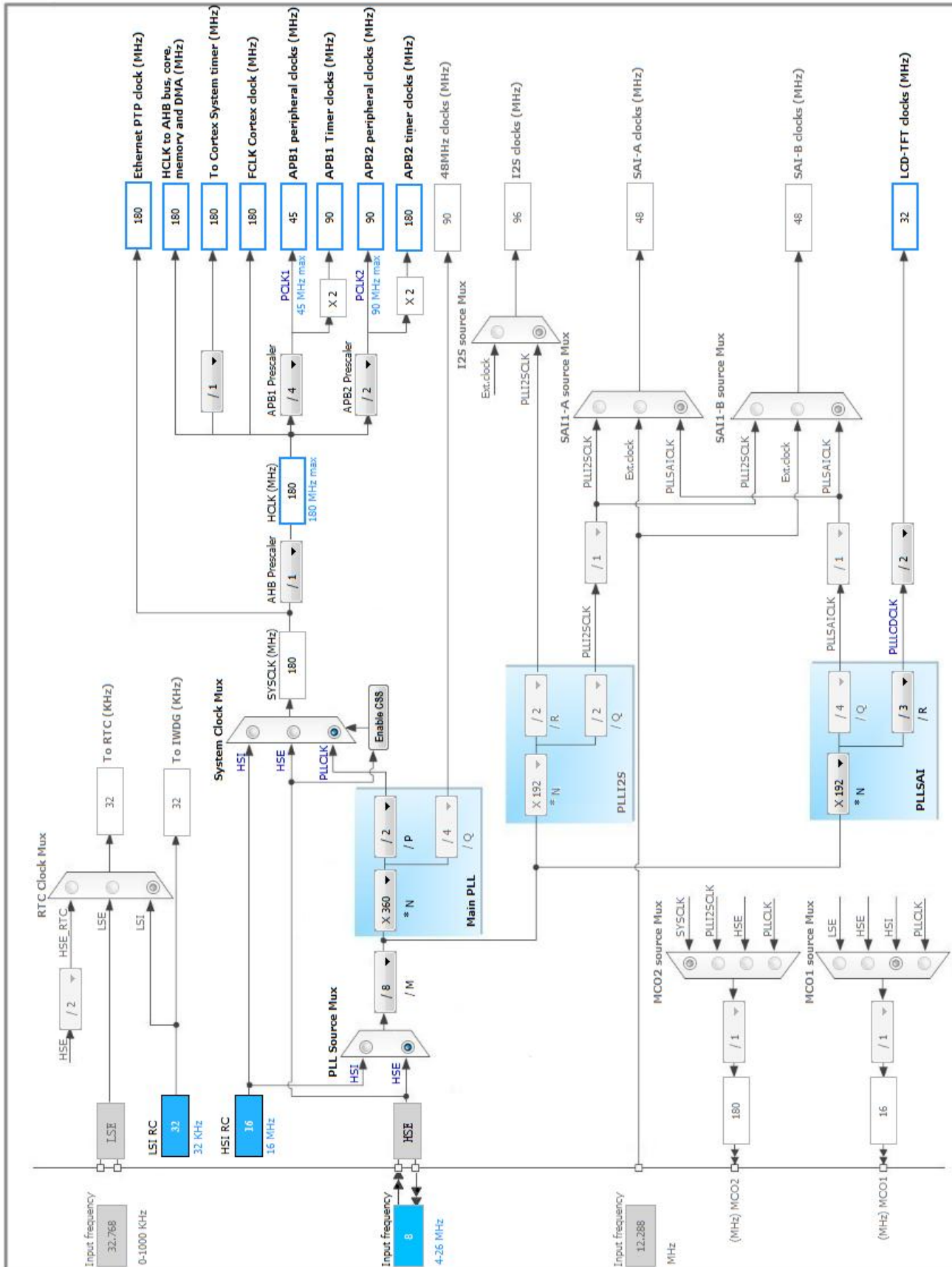
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
53	PA7	I/O	ETH_CRS_DV	
54	PC4	I/O	ETH_RXD0	
55	PC5	I/O	ETH_RXD1	
59	PF11	I/O	FMC_SDNRAS	
60	PF12	I/O	FMC_A6	
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	FMC_A7	
64	PF14	I/O	FMC_A8	
65	PF15	I/O	FMC_A9	
66	PG0	I/O	FMC_A10	
67	PG1	I/O	FMC_A11	
68	PE7	I/O	FMC_D4	
69	PE8	I/O	FMC_D5	
70	PE9	I/O	FMC_D6	
71	VSS	Power		
72	VDD	Power		
73	PE10	I/O	FMC_D7	
74	PE11	I/O	FMC_D8	
75	PE12	I/O	FMC_D9	
76	PE13	I/O	FMC_D10	
77	PE14	I/O	FMC_D11	
78	PE15	I/O	FMC_D12	
80	PB11	I/O	ETH_TX_EN	
81	VCAP_1	Power		
82	VDD	Power		
83	PH6	I/O	FMC_SDNE1	
84	PH7	I/O	FMC_SDCKE1	
85	PH8	I/O	LTDC_R2	
86	PH9	I/O	LTDC_R3	
87	PH10	I/O	LTDC_R4	
88	PH11	I/O	LTDC_R5	
89	PH12	I/O	LTDC_R6	
90	VSS	Power		
91	VDD	Power		
96	PD8	I/O	FMC_D13	
97	PD9	I/O	FMC_D14	
98	PD10	I/O	FMC_D15	
102	VSS	Power		

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
103	VDD	Power		
104	PD14	I/O	FMC_D0	
105	PD15	I/O	FMC_D1	
108	PG4	I/O	FMC_BA0	
109	PG5	I/O	FMC_BA1	
110	PG6	I/O	LTDC_R7	
111	PG7	I/O	LTDC_CLK	
112	PG8	I/O	FMC_SDCLK	
113	VSS	Power		
114	VDD	Power		
125	VCAP_2	Power		
126	VSS	Power		
127	VDD	Power		
128	PH13	I/O	LTDC_G2	
129	PH14	I/O	LTDC_G3	
130	PH15	I/O	LTDC_G4	
131	PI0	I/O	LTDC_G5	
132	PI1	I/O	LTDC_G6	
133	PI2	I/O	LTDC_G7	
135	VSS	Power		
136	VDD	Power		
142	PD0	I/O	FMC_D2	
143	PD1	I/O	FMC_D3	
146	PD4 *	I/O	GPIO_Output	LED_BL
148	VSS	Power		
149	VDD	Power		
150	PD6	I/O	LTDC_B2	
154	PG11	I/O	LTDC_B3	
155	PG12	I/O	LTDC_B1	
156	PG13	I/O	ETH_TXD0	
157	PG14	I/O	ETH_TXD1	
158	VSS	Power		
159	VDD	Power		
160	PG15	I/O	FMC_SDNCAS	
166	BOOT0	Boot		
167	PB8	I/O	LTDC_B6	
168	PB9	I/O	LTDC_B7	
169	PE0	I/O	FMC_NBL0	
170	PE1	I/O	FMC_NBL1	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
171	PDR_ON	Reset		
172	VDD	Power		
173	PI4	I/O	LTDC_B4	
174	PI5	I/O	LTDC_B5	

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. IPs and Middleware Configuration

### 5.1. ADC1

mode: Temperature Sensor Channel

#### 5.1.1. Parameter Settings:

##### ADCs\_Common\_Settings:

Mode Independent mode

##### ADC\_Settings:

Clock Prescaler PCLK2 divided by 4

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode Disabled

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection **EOC flag at the end of all conversions \***

##### ADC\_Regular\_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Edge None

Rank 1

Channel Channel Temperature Sensor

Sampling Time 3 Cycles

##### ADC\_Injected\_ConversionMode:

Number Of Conversions 0

##### WatchDog:

Enable Analog WatchDog Mode false

### 5.2. DMA2D

mode: Activated

#### 5.2.1. Parameter Settings:

##### Basic Parameters:

Transfer Mode Memory to Memory



Color Mode	<b>RGB565 *</b>
Output Offset	0
<b>Foreground layer Configuration:</b>	
DMA2D Input Color Mode	RGB565
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	<b>0xFF *</b>
Input Offset	0

## 5.3. ETH

### Mode: RMII

#### 5.3.1. Parameter Settings:

##### Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled
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##### General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

##### Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

#### 5.3.2. Advanced Parameters:

##### External PHY Configuration:

PHY Reset delay these values are based on a 1 ms Systick interrupt	<b>0x000000FF *</b>
PHY Configuration delay	<b>0x00000FFF *</b>
PHY Read TimeOut	<b>0x0000FFFF *</b>
PHY Write TimeOut	<b>0x0000FFFF *</b>

##### Common : External PHY Configuration:

Transceiver Basic Control Register	<b>0x00 *</b>
Transceiver Basic Status Register	<b>0x01 *</b>
PHY Reset	<b>0x8000 *</b>
Select loop-back mode	<b>0x4000 *</b>
Set the full-duplex mode at 100 Mb/s	<b>0x2100 *</b>
Set the half-duplex mode at 100 Mb/s	<b>0x2000 *</b>

Set the full-duplex mode at 10 Mb/s	<b>0x0100 *</b>
Set the half-duplex mode at 10 Mb/s	<b>0x0000 *</b>
Enable auto-negotiation function	<b>0x1000 *</b>
Restart auto-negotiation function	<b>0x0200 *</b>
Select the power down mode	<b>0x0800 *</b>
Isolate PHY from MII	<b>0x0400 *</b>
Auto-Negotiation process completed	<b>0x0020 *</b>
Valid link established	<b>0x0004 *</b>
Jabber condition detected	<b>0x0002 *</b>

**Extended : External PHY Configuration:**

PHY status register Offset	<b>0x10 *</b>
MI I Interrupt Control Register	<b>0x11 *</b>
MI I Interrupt Status and Misc. Control Register	<b>0x12 *</b>
PHY Link mask	<b>0x0001 *</b>
PHY Speed mask	<b>0x0002 *</b>
PHY Duplex mask	<b>0x0004 *</b>
PHY Enable interrupts	<b>0x0002 *</b>
PHY Enable output interrupt events	<b>0x0001 *</b>
Enable Interrupt on change of link status	<b>0x0020 *</b>
HY link status interrupt mask	<b>0x2000 *</b>

## 5.4. FMC

### SDRAM 1

**Clock and chip enable: SDCKE1+SDNE1**

**Internal bank number: 4 banks**

**Address: 12 bits**

**Data: 16 bits**

**Byte enable: 16-bit byte enable**

#### 5.4.1. SDRAM 1:

**SDRAM control:**

Bank	SDRAM bank 2
Column bit number	8 bits
Row bit number	<b>12 bits *</b>

CAS latency	<b>3 memory clock cycles *</b>
Write protection	Disabled
SDRAM common clock	<b>2 HCLK clock cycles *</b>
SDRAM common burst read	Disabled
SDRAM common read pipe delay	<b>1 HCLK clock cycle *</b>

**SDRAM timing in memory clock cycles:**

Load mode register to active delay	<b>2 *</b>
Exit self-refresh delay	<b>7 *</b>
Self refresh time	<b>4 *</b>
SDRAM common row cycle delay	<b>6 *</b>
Write recovery time	<b>2 *</b>
SDRAM common row precharge delay	<b>2 *</b>
Row to column delay	<b>2 *</b>

## 5.5. LTDC

**Display Type: RGB888 (24 bits)**

### 5.5.1. Parameter Settings:

**Synchronization for Width:**

Horizontal Synchronization Width	<b>30 *</b>
Horizontal Back Porch	<b>46 *</b>
Active Width	<b>800 *</b>
Horizontal Front Porch	<b>210 *</b>
HSync Width	29
Accumulated Horizontal Back Porch Width	75
Accumulated Active Width	875
Total Width	1085

**Synchronization for Height:**

Vertical Synchronization Height	<b>10 *</b>
Vertical Back Porch	<b>23 *</b>
Active Height	480
Vertical Front Porch	<b>22 *</b>
VSyn Height	9
Accumulated Vertical Back Porch Height	32
Accumulated Active Height	512

Total Height 534

**Signal Polarity:**

Horizontal Synchronization Polarity Active Low  
Vertical Synchronization Polarity Active Low  
Data Enable Polarity Active Low  
Pixel Clock Polarity Normal Input

**BackGround Color:**

Red 0  
Green 0  
Blue 0

## 5.5.2. Layer Settings:

**BackGround Color:**

Layer 0 - Blue 0  
Layer 0 - Green 0  
Layer 0 - Red 0  
Layer 1 - Blue 0  
Layer 1 - Green 0  
Layer 1 - Red 0

**Windows Position:**

Layer 0 - Window Horizontal Start 0  
Layer 0 - Window Horizontal Stop **800 \***  
Layer 0 - Window Vertical Start 0  
Layer 0 - Window Vertical Stop **480 \***  
Layer 1 - Window Horizontal Start 0  
Layer 1 - Window Horizontal Stop **800 \***  
Layer 1 - Window Vertical Start 0  
Layer 1 - Window Vertical Stop **480 \***

**Pixel Parameters:**

Layer 0 - Pixel Format **RGB565 \***  
Layer 1 - Pixel Format **RGB565 \***

**Blending:**

Layer 0 - Alpha constant for blending **255 \***  
Layer 0 - Default Alpha value 0  
Layer 0 - Blending Factor1 Alpha constant  
Layer 0 - Blending Factor2 Alpha constant  
Layer 1 - Alpha constant for blending 0  
Layer 1 - Default Alpha value 0  
Layer 1 - Blending Factor1 **Alpha constant x Pixel Alpha \***

Layer 1 - Blending Factor2	<b>Alpha constant x Pixel Alpha *</b>
<b>Frame Buffer:</b>	
Layer 0 - Color Frame Buffer Start Address	<b>0xD0000000 *</b>
Layer 0 - Color Frame Buffer Line Length (Image Width)	<b>800 *</b>
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	<b>480 *</b>
Layer 1 - Color Frame Buffer Start Address	<b>0xD0200000 *</b>
Layer 1 - Color Frame Buffer Line Length (Image Width)	<b>800 *</b>
Layer 1 - Color Frame Buffer Number of Lines (Image Height)	<b>480 *</b>

## 5.6. RCC

### High Speed Clock (HSE): Crystal/Ceramic Resonator

#### 5.6.1. Parameter Settings:

##### System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

##### RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled

##### Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

## 5.7. LWIP

### mode: Enabled

Advanced parameters are not listed except if modified by user.

#### 5.7.1. General:

#### LwIP Version:

LWIP Version (Version of LwIP supported by CubeMX) 1.4.1

#### DHCP Option:

LWIP\_DHCP (DHCP Module) Enabled

#### RTOS Settings:

WITH\_RTOS (Use FREERTOS \*\* CubeMX specific \*\*) Disabled

#### Protocols Options:

LWIP\_ICMP (ICMP Module Activation) Enabled

LWIP\_IGMP (IGMP Module) Disabled

LWIP\_DNS (DNS Module) Disabled

LWIP\_UDP (UDP Module) Enabled

MEMP\_NUM\_UDP\_PCB (Number of UDP Connections) 4

LWIP\_TCP (TCP Module) Enabled

MEMP\_NUM\_TCP\_PCB (Number of TCP Connections) 5

### 5.7.2. All LwIP Options:

#### Platform Specific Locking:

SYS\_LIGHTWEIGHT\_PROT (Memory Functions Protection) Disabled

NO\_SYS (LwIP Facilities) LwIP Facilities Disabled

NO\_SYS\_NO\_TIMERS (Drop Support For sys\_timeout) Disabled

#### Memory Options:

MEM\_SIZE (Heap Memory Size) 1600

#### Internal Memory Pool Sizes:

MEMP\_NUM\_PBUF (Number of Memory Pool struct Pbufs) 16

MEMP\_NUM\_RAW\_PCB (Number of Raw Protocol Control Blocks) 4

MEMP\_NUM\_TCP\_PCB\_LISTEN (Number of Listening TCP Connections) 8

MEMP\_NUM\_TCP\_SEG (Number of TCP Segments simultaneously queued) 16

MEMP\_NUM\_LOCALHOSTLIST (Number of Host Entries in the Local Host List) 1

#### Pbuf Options:

PBUF\_POOL\_SIZE (Number of Buffers in the Pbuf Pool) 16

PBUF\_POOL\_BUFSIZE (Size of each pbuf in the pbuf pool) 592

#### ARP Options:

LWIP\_ARP (ARP Functionality) Enabled

#### SNMP Options:

LWIP\_SNMP (SNMP Module) Disabled

#### TCP Options:

TCP\_TTL (Number of Time-To-Live Used by TCP Packets) 255

TCP\_WND (TCP Receive Window Maximum Size) 2144

TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	<b>Disabled *</b>
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9
<b>Network Interfaces Options:</b>	
LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	<b>Enabled *</b>
LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled
<b>Sequential Layer options:</b>	
LWIP_NETCONN (NETCONN API)	Disabled
<b>Socket Options:</b>	
LWIP_SOCKET (Socket API)	Disabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	Enabled
<b>Statistics Options:</b>	
LWIP_STATS (Statistics Collection)	Disabled
<b>Checksum Options:</b>	
CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled

### 5.7.3. Debug:

#### Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All
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\* User modified value

## 6. System Configuration

### 6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PG13	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PG14	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	High *	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	High	



IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PH6	FMC_SDNE1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PH7	FMC_SDCKE1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	High	
LTDC	PE4	LTDC_B0	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PE5	LTDC_G0	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PE6	LTDC_G1	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH2	LTDC_R0	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH3	LTDC_R1	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH8	LTDC_R2	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH9	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH10	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH11	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH12	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH13	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH14	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PH15	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PI1	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PI2	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	High *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD6	LTDC_B2	Alternate Function Push Pull	No pull-up and no pull-down	<b>High *</b>	
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	<b>High *</b>	
	PG12	LTDC_B1	Alternate Function Push Pull	No pull-up and no pull-down	<b>High *</b>	
	PB8	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	<b>High *</b>	
	PB9	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	<b>High *</b>	
	PI4	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	<b>High *</b>	
	PI5	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	<b>High *</b>	
RCC	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
GPIO	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED3
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED4
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_BL

## 6.2. DMA configuration

DMA request	Stream	Direction	Priority
MENTOMEM	DMA2_Stream0	Memory To Memory	Low

### MENTOMEM: DMA2\_Stream0 DMA request Settings:

Mode: Normal  
 Use fifo: **Enable \***  
 FIFO Threshold: Full  
 Src Memory Increment: **Enable \***  
 Dst Memory Increment: **Enable \***  
 Src Memory Data Width: **Word \***  
 Dst Memory Data Width: **Word \***  
 Src Memory Burst Size: Single  
 Dst Memory Burst Size: Single

### 6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
System tick timer	true	0	0
Ethernet global interrupt	true	0	0
LTDC global interrupt	true	0	0
DMA2D global interrupt	true	0	0
Non maskable interrupt	unused		
Memory management fault	unused		
Pre-fetch fault, memory access fault	unused		
Undefined instruction or illegal state	unused		
Debug monitor	unused		
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
FMC global interrupt	unused		
DMA2 stream0 global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
LTDC global error interrupt	unused		

\* User modified value

## 7. Power Plugin report

### 7.1. Microcontroller Selection

Series	STM32F4
Line	STM32F429/439
MCU	STM32F429IGTx
Datasheet	024030_Rev5

### 7.2. Parameter Selection

Temperature	25
Vdd	null

## 8. Software Project

### 8.1. Project Settings

Name	Value
Project Name	STM32F429I
Project Folder	C:\Users\Administrator\Desktop\stm32cube\STM32F429I\35.ETH\LwIP_HTTP_S
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.9.0

### 8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No