



## 1. Description

### 1.1. Project

Project Name	Evk407I_Test
Board Name	custom
Generated with:	STM32CubeMX 6.10.0
Date	05/18/2024

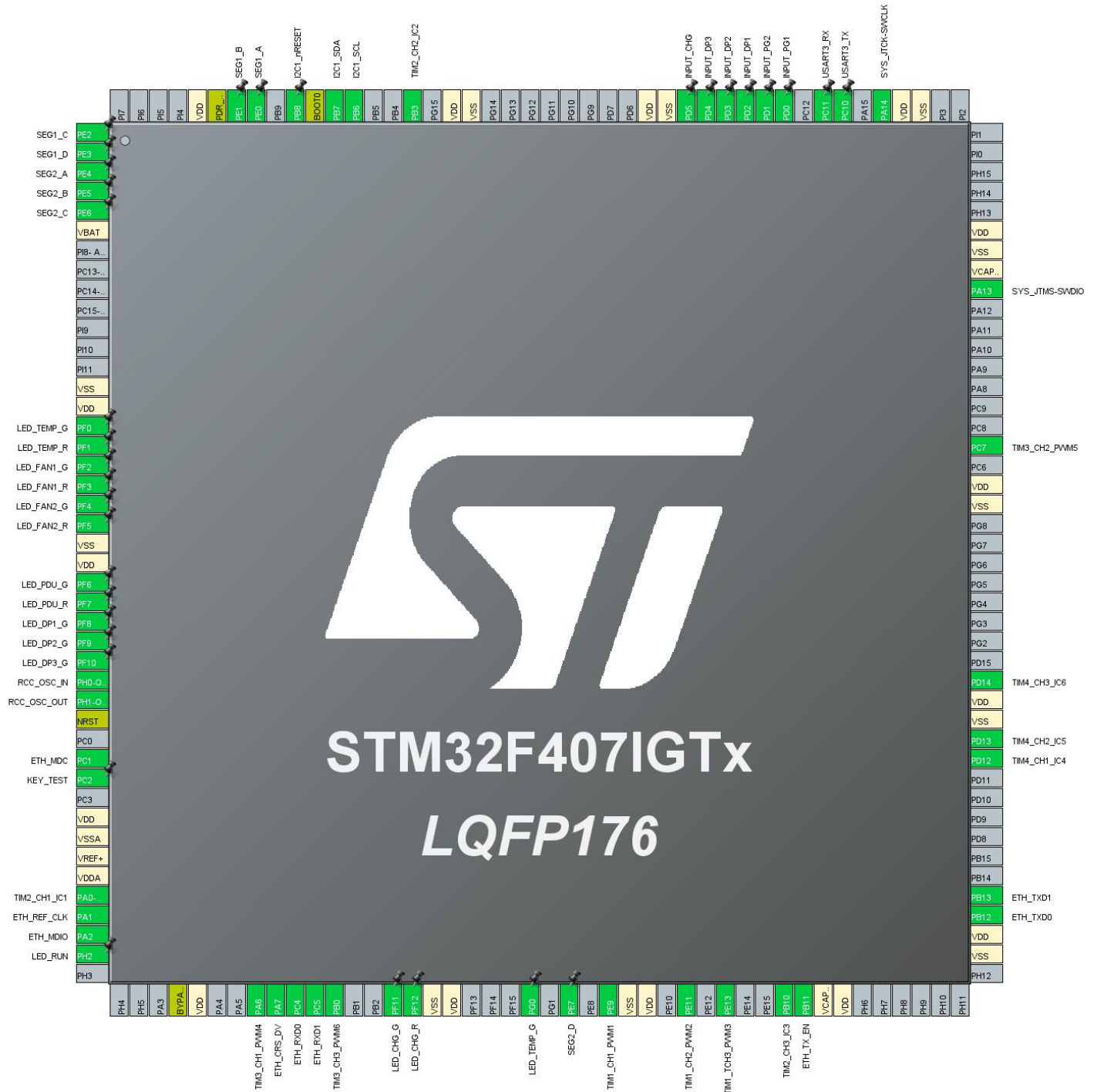
### 1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407IGTx
MCU Package	LQFP176
MCU Pin number	176

### 1.3. Core(s) information

Core(s)	Arm Cortex-M4
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## 2. Pinout Configuration



### 3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	SEG1_C
2	PE3 *	I/O	GPIO_Output	SEG1_D
3	PE4 *	I/O	GPIO_Output	SEG2_A
4	PE5 *	I/O	GPIO_Output	SEG2_B
5	PE6 *	I/O	GPIO_Output	SEG2_C
6	VBAT	Power		
14	VSS	Power		
15	VDD	Power		
16	PF0 *	I/O	GPIO_Output	LED_TEMP_G
17	PF1 *	I/O	GPIO_Output	LED_TEMP_R
18	PF2 *	I/O	GPIO_Output	LED_FAN1_G
19	PF3 *	I/O	GPIO_Output	LED_FAN1_R
20	PF4 *	I/O	GPIO_Output	LED_FAN2_G
21	PF5 *	I/O	GPIO_Output	LED_FAN2_R
22	VSS	Power		
23	VDD	Power		
24	PF6 *	I/O	GPIO_Output	LED_PDU_G
25	PF7 *	I/O	GPIO_Output	LED_PDU_R
26	PF8 *	I/O	GPIO_Output	LED_DP1_G
27	PF9 *	I/O	GPIO_Output	LED_DP2_G
28	PF10 *	I/O	GPIO_Output	LED_DP3_G
29	PH0-OSC_IN	I/O	RCC_OSC_IN	
30	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
33	PC1	I/O	ETH_MDC	
34	PC2	I/O	GPIO_EXTI2	KEY_TEST
36	VDD	Power		
37	VSSA	Power		
38	VREF+	Power		
39	VDDA	Power		
40	PA0-WKUP	I/O	TIM2_CH1	TIM2_CH1_IC1
41	PA1	I/O	ETH_REF_CLK	
42	PA2	I/O	ETH_MDIO	
43	PH2 *	I/O	GPIO_Output	LED_RUN
48	BYPASS_REG	Reset		
49	VDD	Power		

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
52	PA6	I/O	TIM3_CH1	TIM3_CH1_PWM4
53	PA7	I/O	ETH_CRSDV	
54	PC4	I/O	ETH_RXD0	
55	PC5	I/O	ETH_RXD1	
56	PB0	I/O	TIM3_CH3	TIM3_CH3_PWM6
59	PF11 *	I/O	GPIO_Output	LED_CHG_G
60	PF12 *	I/O	GPIO_Output	LED_CHG_R
61	VSS	Power		
62	VDD	Power		
66	PG0 *	I/O	GPIO_Output	LED_TEMP_G
68	PE7 *	I/O	GPIO_Output	SEG2_D
70	PE9	I/O	TIM1_CH1	TIM1_CH1_PWM1
71	VSS	Power		
72	VDD	Power		
74	PE11	I/O	TIM1_CH2	TIM1_CH2_PWM2
76	PE13	I/O	TIM1_CH3	TIM1_TCH3_PWM3
79	PB10	I/O	TIM2_CH3	TIM2_CH3_IC3
80	PB11	I/O	ETH_TX_EN	
81	VCAP_1	Power		
82	VDD	Power		
90	VSS	Power		
91	VDD	Power		
92	PB12	I/O	ETH_TXD0	
93	PB13	I/O	ETH_TXD1	
100	PD12	I/O	TIM4_CH1	TIM4_CH1_IC4
101	PD13	I/O	TIM4_CH2	TIM4_CH2_IC5
102	VSS	Power		
103	VDD	Power		
104	PD14	I/O	TIM4_CH3	TIM4_CH3_IC6
113	VSS	Power		
114	VDD	Power		
116	PC7	I/O	TIM3_CH2	TIM3_CH2_PWM5
124	PA13	I/O	SYS_JTMS-SWDIO	
125	VCAP_2	Power		
126	VSS	Power		
127	VDD	Power		
135	VSS	Power		
136	VDD	Power		
137	PA14	I/O	SYS_JTCK-SWCLK	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
139	PC10	I/O	USART3_TX	
140	PC11	I/O	USART3_RX	
142	PD0 *	I/O	GPIO_Input	INPUT_PG1
143	PD1 *	I/O	GPIO_Input	INPUT_PG2
144	PD2 *	I/O	GPIO_Input	INPUT_DP1
145	PD3 *	I/O	GPIO_Input	INPUT_DP2
146	PD4 *	I/O	GPIO_Input	INPUT_DP3
147	PD5 *	I/O	GPIO_Input	INPUT_CHG
148	VSS	Power		
149	VDD	Power		
158	VSS	Power		
159	VDD	Power		
161	PB3	I/O	TIM2_CH2	TIM2_CH2_IC2
164	PB6	I/O	I2C1_SCL	
165	PB7	I/O	I2C1_SDA	
166	BOOT0	Boot		
167	PB8 *	I/O	GPIO_Output	I2C1_nRESET
169	PE0 *	I/O	GPIO_Output	SEG1_A
170	PE1 *	I/O	GPIO_Output	SEG1_B
171	PDR_ON	Reset		
172	VDD	Power		

\* The pin is affected with an I/O function



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	Evk407I_Test
Project Folder	E:\7.Sunshine\Waveshare\Evk407I_Test\workspace\Evk407I_Test
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.28.0
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_TIM1_Init	TIM1
4	MX_TIM3_Init	TIM3
5	MX_TIM4_Init	TIM4
6	MX_I2C1_Init	I2C1
7	MX_TIM2_Init	TIM2
8	MX_LWIP_Init	LWIP
9	MX_TIM6_Init	TIM6
10	MX_USART3_UART_Init	USART3





## 1. Power Consumption Calculator report

### 1.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407IGTx
Datasheet	DS8626_Rev8

### 1.2. Parameter Selection

Temperature	25
Vdd	3.3

### 1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

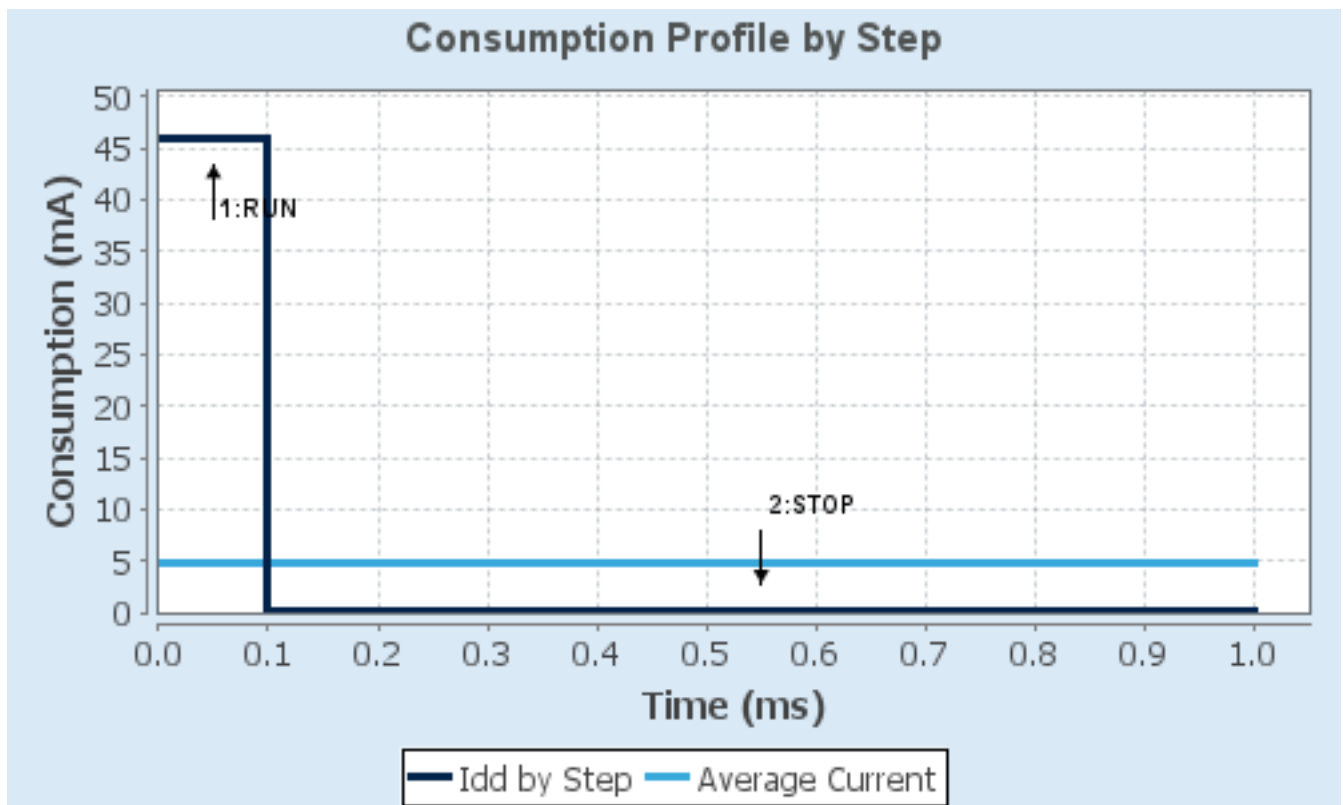
#### 1.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	Scale1-High	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	168 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP Flash-PwrDwn
<b>Clock Source Frequency</b>	4 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	46 mA	280 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	210.0	0.0
<b>Ta Max</b>	99.23	104.96
<b>Category</b>	In DS Table	In DS Table

#### 1.5. Results

Sequence Time	1 ms	Average Current	4.85 mA
Battery Life	29 days, 4 hours	Average DMIPS	210.0 DMIPS

#### 1.6. Chart



## 2. Peripherals and Middlewares Configuration

### 2.1. ETH

#### Mode: RMII

##### 2.1.1. Parameter Settings:

###### General : Ethernet Configuration:

Note	PHY Driver must be configured from the LwIP 'Platform Settings' top right tab
Ethernet MAC Address	00:80:E1:00:00:00
Rx Buffers Length	1536

###### Ethernet Basic Configuration:

Rx Mode	Polling Mode
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### 2.2. I2C1

#### I2C: I2C

##### 2.2.1. Parameter Settings:

###### Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

###### Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

### 2.3. RCC

#### High Speed Clock (HSE): Crystal/Ceramic Resonator

##### 2.3.1. Parameter Settings:

###### System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

#### RCC Parameters:

HSI Calibration Value	16
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000

#### Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
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## 2.4. SYS

### Debug: Serial Wire

Timebase Source: SysTick

## 2.5. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

### 2.5.1. Parameter Settings:

#### Counter Settings:

Prescaler (PSC - 16 bits value)	12-1 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	280-1 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

#### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

#### Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

#### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### **PWM Generation Channel 2:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

#### **PWM Generation Channel 3:**

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

## **2.6. TIM2**

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

### 2.6.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value )	4294967295
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### **Input Capture Channel 1:**

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

## 2.7. TIM3

### Channel1: PWM Generation CH1

### Channel2: PWM Generation CH2

### Channel3: PWM Generation CH3

#### 2.7.1. Parameter Settings:

##### Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	65535
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

##### Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

##### PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

##### PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

##### PWM Generation Channel 3:



Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

## 2.8. TIM4

**Channel1: Input Capture direct mode**

**Channel2: Input Capture direct mode**

**Channel3: Input Capture direct mode**

### 2.8.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>12-1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>280-1 *</b>
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

#### **Input Capture Channel 1:**

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### **Input Capture Channel 2:**

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

#### **Input Capture Channel 3:**

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

## 2.9. TIM6

**mode: Activated**

### 2.9.1. Parameter Settings:

#### **Counter Settings:**

Prescaler (PSC - 16 bits value)	<b>840-1 *</b>
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value )	<b>10000-1 *</b>
auto-reload preload	Disable

#### **Trigger Output (TRGO) Parameters:**

Trigger Event Selection	Reset (UG bit from TIMx_EGR)
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## 2.10. USART3

**Mode: Asynchronous**

### 2.10.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

#### **Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 2.11. LWIP

**mode: Enabled**

Advanced parameters are not listed except if modified by user.

### 2.11.1. General Settings:

#### **LwIP Version:**

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2
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#### **IPv4 - DHCP Options:**

LWIP_DHCP (DHCP Module)	<b>Disabled *</b>
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### IP Address Settings:

IP_ADDRESS (IP Address)	000.000.000.000
NETMASK_ADDRESS (Netmask Address)	000.000.000.000
GATEWAY_ADDRESS (Gateway Address)	000.000.000.000

### RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Disabled
RTOS_USE_NEWLIB_REENTRANT (No RTOS - 2)	Disabled

### Platform Settings:

PHY Driver	Choose/LAN8742/DP83848
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### Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

## 2.11.2. Key Options:

### Infrastructure - OS Awareness Option:

NO_SYS (OS Awareness)	OS Not Used
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### Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled
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### Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled
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### Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600
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### Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

### Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

### IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled
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### Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

#### Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

#### NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled
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#### Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Disabled
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### 2.11.3. PPP:

#### PPP Options:

PPP_SUPPORT (PPP Module)	Disabled
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### 2.11.4. IPv6:

#### IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled
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### 2.11.5. HTTPD:

#### HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled
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### 2.11.6. SNMP:

#### SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled
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### 2.11.7. SNTP/SMTP:

#### SNTP Options:

LWIP\_SNTP (LWIP SNTP Support \*\* CubeMX specific \*\*) Disabled

#### SMTP Options:

LWIP\_SMTP (LWIP SMTP Support \*\* CubeMX specific \*\*) Disabled

### 2.11.8. MDNS/TFTP:

#### MDNS Options:

LWIP\_MDNS (Multicast DNS Support \*\* CubeMX specific \*\*) Disabled

#### TFTP Options:

LWIP\_TFTP (TFTP Support \*\* CubeMX specific \*\*) Disabled

### 2.11.9. Perf/Checks:

#### Sanity Checks:

LWIP\_DISABLE\_TCP\_SANITY\_CHECKS (TCP Sanity Checks) Disabled

LWIP\_DISABLE\_MEMP\_SANITY\_CHECKS (MEMP Sanity Checks) Disabled

#### Performance Options:

LWIP\_PERF (Performace Testing for LwIP) Disabled

### 2.11.10. Statistics:

#### Debug - Statistics Options:

LWIP\_STATS (Statistics Collection) Disabled

### 2.11.11. Checksum:

#### Infrastructure - Checksum Options:

CHECKSUM\_BY\_HARDWARE (Hardware Checksum \*\* CubeMX specific \*\*) Enabled

LWIP\_CHECKSUM\_CTRL\_PER\_NETIF (Generate/Check Checksum per Netif) Disabled

CHECKSUM\_GEN\_IP (Generate Software Checksum for Outgoing IP Packets) Disabled

CHECKSUM\_GEN\_UDP (Generate Software Checksum for Outgoing UDP Packets) Disabled

CHECKSUM\_GEN\_TCP (Generate Software Checksum for Outgoing TCP Packets) Disabled

CHECKSUM\_GEN\_ICMP (Generate Software Checksum for Outgoing ICMP Packets) Disabled

CHECKSUM\_GEN\_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets) Disabled

CHECKSUM\_CHECK\_IP (Generate Software Checksum for Incoming IP Packets) Disabled

CHECKSUM\_CHECK\_UDP (Generate Software Checksum for Incoming UDP Packets) Disabled

CHECKSUM\_CHECK\_TCP (Generate Software Checksum for Incoming TCP Packets) Disabled

CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

#### 2.11.12. Debug:

##### **LwIP Main Debugging Options:**

LWIP_DBG_MIN_LEVEL (Minimum Level)	All
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#### 2.11.13. Platform Settings:

Driver_PHY	LAN8742
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**\* User modified value**

### 3. System Configuration

#### 3.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA1	ETH_REF_CLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA7	ETH_CRS_DV	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	Very High *	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1_CH1_PWM1
	PE11	TIM1_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1_CH2_PWM2
	PE13	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM1_TCH3_PWM3
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM2_CH1_IC1
	PB10	TIM2_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM2_CH3_IC3

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB3	TIM2_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM2_CH2_IC2
TIM3	PA6	TIM3_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3_CH1_PWM4
	PB0	TIM3_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3_CH3_PWM6
	PC7	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM3_CH2_PWM5
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM4_CH1_IC4
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM4_CH2_IC5
	PD14	TIM4_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	TIM4_CH3_IC6
USART3	PC10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PC11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG1_C
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG1_D
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG2_A
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG2_B
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG2_C
	PF0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_TEMP_G
	PF1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_TEMP_R
	PF2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_FAN1_G
	PF3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_FAN1_R
	PF4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_FAN2_G
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_FAN2_R
	PF6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_PDU_G
	PF7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_PDU_R
	PF8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_DP1_G
	PF9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_DP2_G
	PF10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_DP3_G
	PC2	GPIO_EXTI2	<b>External Interrupt Mode with Falling edge trigger detection</b>	<b>Pull-up *</b>	n/a	KEY_TEST
	PH2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_RUN
	PF11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_CHG_G
	PF12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_CHG_R
	PG0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_TEMP_G
	PE7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG2_D
	PD0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT_PG1
	PD1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT_PG2
	PD2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT_DP1
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT_DP2
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT_DP3



IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	INPUT_CHG
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	I2C1_nRESET
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG1_A
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SEG1_B

### 3.2. DMA configuration

nothing configured in DMA service

### 3.3. NVIC configuration

#### 3.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
EXTI line2 interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
I2C1 event interrupt	true	0	0
I2C1 error interrupt	true	0	0
USART3 global interrupt	true	0	0
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM3 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
FPU global interrupt	unused		

#### 3.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line2 interrupt	false	true	true
TIM2 global interrupt	false	true	true
TIM4 global interrupt	false	true	true
I2C1 event interrupt	false	true	true
I2C1 error interrupt	false	true	true
USART3 global interrupt	false	true	true
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	false	true	true

\* User modified value

## 4. System Views

### 4.1. Category view

#### 4.1.1. Current

Middleware						
LWIP						
System Core	Analog	Timers	Connectivity	Multimedia	Security	Computing
DMA		TIM1	ETH			
GPIO		TIM2	I2C1			
NVIC		TIM3	USART3			
RCC		TIM4				
SYS		TIM6				

## 5. Docs & Resources

Type	Link
BSDL files	<a href="https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-417_bsdl.zip">https://www.st.com/resource/en/bsdl_model/stm32f405-415_407-417_bsdl.zip</a>
IBIS models	<a href="https://www.st.com/resource/en/ibis_model/stm32f405-415_407-417_ibis.zip">https://www.st.com/resource/en/ibis_model/stm32f405-415_407-417_ibis.zip</a>
System View Description	<a href="https://www.st.com/resource/en/svd/stm32f4_svd.zip">https://www.st.com/resource/en/svd/stm32f4_svd.zip</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf">https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf</a>
Presentations	<a href="https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf">https://www.st.com/resource/en/product_presentation/stm32_eval_tools_portfolio.pdf</a>
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Presentations	<a href="https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf">https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf</a>
Brochures	<a href="https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf">https://www.st.com/resource/en/brochure/products-and-solutions-for-plcs-and-smart-i-os.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32nucleo.pdf">https://www.st.com/resource/en/flyer/flstm32nucleo.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstmcsuite.pdf">https://www.st.com/resource/en/flyer/flstmcsuite.pdf</a>
Flyers	<a href="https://www.st.com/resource/en/flyer/flstm32trust.pdf">https://www.st.com/resource/en/flyer/flstm32trust.pdf</a>
Product Certifications	<a href="https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf">https://www.st.com/resource/en/certification_document/stm32_authentication_can.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1181-electrostatic-discharge-sensitivity-measurement-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf</a>
Application Notes	<a href="https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf">https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf</a>

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