Solder Reflow Guide for Surface Mount Devices

Technical Note

FPGA-TN-02041-4.5

June 2022

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults and associated risk the responsibility entirely of the Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
BGA	Ball Grid Array
caBGA	Chip Array BGA, 0.80 mm Ball Pitch
ckfBGA	Flip Chip CSP 7 × 7 mm Body Size, 0.65 mm Ball Pitch
csBGA	Chip-Scale BGA, 0.50 mm Ball Pitch
csfBGA	Flip Chip CSP, 0.50 mm Ball Pitch
ctfBGA	Flip Chip CSP, 0.65 mm Ball Pitch
DI	Deionized
fcBGA	Flip Chip BGA, ≥ 0.80 mm Ball Pitch
fcCSP	Flip Chip CSP, ≥ 0.80mm Ball Pitch
FOWLP	Fan Out Wafer Level Package
fpBGA	Fine Pitch BGA, ≥ 1.00 mm Ball Pitch
fpSBGA	Cavity Down, Thermally Enhanced Ball Grid Array, 1.00 mm Ball Pitch
ftBGA	Fine Pitch Thin BGA, = 1.00 mm Ball Pitch
IPC	Association Connecting Electronics Industries
JEDEC	JEDEC Solid State Technology Association
JLCC	J-leaded Ceramic Chip Carrier
LCC	Leadless Chip Carrier
LQFP	Low-Profile Quad Flat Pack, 1.4 mm Thick
PCB	Printed Circuit Board
PDIP	Plastic Dual-in-Line Package
PLCC	Plastic Leaded Chip Carrier
PQFP	Plastic Quad Flat Pack
PPM	Parts per million
QFN	Quad Flat Package Punched Singulation
QFNS	Quad Flat Package Saw-Singulated
RoHS	Restriction of Use of Hazardous Substances
SBGA	Super BGA, ≥ 1.00 mm Ball Pitch
SMT	Surface-Mount Technology (Assembling and Mounting Technology)
SSOP	Shrink, Small Outline Package
TQFP	Thin Quad Flat Pack, 1.0 mm Thick
TS	Technical Specification
ucBGA	Ultra Chip-Scale BGA, 0.40 mm Ball Pitch
ucfBGA	Ultra Chip Flip Chip CSP, 0.40 mm Ball Pitch
WLCSP	Wafer Level Chip Scale Package

1. Introduction

This technical note provides general guidelines for solder reflow and rework process for Lattice Semiconductor surface mount products. The data used in this document is based on IPC/JEDEC (Association Connecting Electronics Industries/JEDEC Solid State Technology Association) standards. Each board has its own profile which depends upon the reflow equipment used and the board design. The PCB (printed circuit board) must be individually characterized to find the reliable profile. This document covers Sn/Pb (Tin/Lead), Pb-Free (Lead-Free), and Halogen-Free processes.

2. Reflow

- Use caution when profiling to ensure that the maximum temperature difference between components is less than 10 °C (7 °C within an individual component).
- Forced convection reflow with nitrogen is preferred (with maximum oxygen content of 50-75 PPM). Select an appropriate heat sink and thermal interface material for the package.

3. Inspection

- Pre-reflow – Use visual inspection to verify solder paste dispense location and quantity.
- Pick and place – Use machine vision as necessary to ensure proper component placement.
- Post reflow – Use electrical testing to verify solder joint formation (100% post-reflow visual inspection is not recommended).

4. Cleaning Recommendations

- After solder reflow, printed circuit boards should be thoroughly cleaned and dried using standard cleaning equipment.
- Final rinse should be warm deionized (DI) water (50 °C to 75 °C) with resistivity of 0.2 MΩ /cm or greater.
- After cleaning, the boards should be baked for a minimum of one hour at 125 °C to evaporate residual moisture.

5. Rework Recommendations

Removal and replacement of SMT (surface-mount technology) packages on PCBs is fairly straightforward. However, reattachment or touch-up of SMT packages that have already been soldered to the board is not practical in most cases.

A few important criteria should be considered when choosing a rework system:

- Minimize the change in temperature across the solder joint array to promote good solder joint formation, minimize intermetallic growth, improve solderability and minimize component warpage.
- Minimize die temperature to prevent die delamination and wire bond failure.
- Minimize board temperature adjacent to the rework site to reduce intermetallic growth, prevent secondary reflow, and prevent possible component delamination.
- For boards with no internal ground plane, apply localized heat to the SMT package. When the solder is molten, remove package using appropriate vacuum tool.
- While the board is still hot, remove excess solder from the site using a vacuum desoldering system or a soldering iron and solder wicking material. Use care to avoid damaging the solder pads or the surrounding solder mask.
- For PCBs with internal ground plane(s), preheat the entire board to at least 80 °C before removing the SMT packages.
- Use alcohol to remove residual flux, then wash the entire board using the standard board cleaning process before attempting to replace SMT components.

6. BGA Reballing

BGA reballing is not recommended. Reballed BGA packages void the original Lattice specifications.

7. Pb-Free/Halogen-Free (RoHS-Compliant) Products

All Lattice Pb-Free products are also fully RoHS compliant. Similarly, all Lattice Halogen-free products are also Pb-Free and RoHS compliant. Lattice offers a broad range of Pb-Free and Halogen-Free (RoHS-compliant) products in a variety of package configurations. These packages include the Thin Quad Flat Pack (TQFP), Quad Flat Pack Saw-Singulated (QFNS), Fine Pitch BGA (fpBGA), Thin BGA (ftBGA), Chip-Scale BGA (csBGA), Ultra Chip-Scale BGA (ucBGA), Chip Array BGA (caBGA) and Flip Chip BGA (fcBGA), and Wafer Level Chip Scale Package (WLCSP).

8. Peak Reflow Temperature (TP) by Package Size

Table 8.1 illustrates the peak reflow temperatures by package size. Refer to the Package Diagrams document and use maximum package dimensions to determine package thickness and volume which is computed as [D × E × (Amax-A1min)].

Table 8.1. Peak Reflow Temperature (TP)

Classification	Package Thickness	Volume < 350 mm^3*	Volume = 350–2000 mm^3*	Volume > 2000 mm^3*
SnPb Package	< 2.5 mm	235 + 0/–5 °C	220 + 0/–5 °C	
	≥ 2.5 mm	220 + 0/–5 °C		
Pb-Free and Halogen- Free Packages	< 1.6 mm	260 + 0/–5 °C		
	1.6 mm to ≤ 2.5 mm	260 + 0/–5 °C	250 + 0/–5 °C	245 + 0/–5 °C
	> 2.5 mm	250 + 0/–5 °C	245 + 0/–5 °C	

Notes:

1. Package volume excludes external terminals (balls, bumps, lands, leads) and non-integral heat sinks.
2. Based on J-STD-020E_Moisture Reflow Sensitivity Classification.

Table 8.2. shows the peak reflow temperature for Lattice devices by package type and size.

Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size

Package Type	Number of Lead/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)
caBGA / BBG	49	3	235	Package not offered	
	100	3	235	3	260
	121	Package not offered		3	260
	196	Package not offered		3	260
	256	3	235	3	260
	324	Package not offered		3	260
	332	Package not offered		3	250
	381	Package not offered		3	260
	400	Package not offered		3	260
	484	Package not offered		3	260
	554	Package not offered		3	260
	756	Package not offered		3	260
csBGA	56	3	235	3	260
	64	Package not offered		3	260
	81	Package not offered		3	260
	100	3	235	3	260
	121	Package not offered		3	260
	132	3	235	3	260
	144	Package not offered		3	260
	184	Package not offered		3	260
	196	3	235	3	260
	284	3	235	3	260
	289	Package not offered		3	260
	328	Package not offered		3	260
ckfBGA	80	Package not offered		3	260
ctfBGA	80	Package not offered		3	260
csfBGA	81	Package not offered		3	260
	121	Package not offered		3	260

Package Type	Number of Lead/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)
	256	Package not offered		3	260
	285	Package not offered		3	260
	324	Package not offered		3	260
ucBGA	36	Package not offered		3	260
	49	Package not offered		3	260
	64	Package not offered		3	260
	81	Package not offered		3	260
	121	Package not offered		3	260
	132	Package not offered		3	260
	225	Package not offered		3	260
ucfBGA	36	Package not offered		3	260
	64	Package not offered		3	260
fcCSP / CBG	256	Package not offered		3	260
fcBGA / LFG	484	Package not offered		4	250
	672	Package not offered		4	250
	676	4	220	4	245
	1020	4	220	4	245
	1152	4	220	4	245
	1704	4	220	4	245
fpBGA / BFG	100	3	235	3	260
	144	3	235	3	260
	208	3	220	3	250
	256	3	220	3	250
	272	3	220	3	250
	388	3	220	3	250
	416	3	220	Package not offered	
	484	3	220	3	250
	516	3	220	Package not offered	
	672	3	220	3	250
	676	3	220	Package not offered	
	680	3	220	3	245
	900	3	220	3	245
	1152	3	220	3	245
	1156	3	220	3	245
fpSBGA	680	3	220	Package not offered	
ftBGA	208	Package not offered		3	260
	237	Package not offered		3	260
	256[1]	3	220	3	260
	256[2]	3	220	3	250
	324	3	220	3	260

Package Type	Number of Lead/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)
LQFP	44	3	235	3	260
	48	3	235	3	260
	64	3	235	3	260
	100	3	235	3	260
	128	3	235	3	260
	144	3	220	3	260
	176	3	220	3	260
TQFP	44	3	235	3	260
	48	3	235	3	260
	100	Package not offered		3	260
	388	3	220	Package not offered	
PLCC	20	1	235	1	260
	28	1	235	1	260
	44	3	235	3	260
	68	3	235	Package not offered	
	84	3	235	4	260
PQFP	100	3	220	3	245
	120	3	220	Package not offered	
	128	3	220	3	245
	160	3	220	3	245
	208	3	220	3	245
QFNS	24	Package not offered		1	260
	32	1	235	1	260
	48	Package not offered		3	260
	64	Package not offered		3	260
	84	Package not offered		3	260
QFN	72	Package not offered		3	260
SBGA	256	3	220	Package not offered	
	320	3	220	Package not offered	
	352	3	220	Package not offered	
	432	3	220	Package not offered	
SSOP	28	1	235	Package not offered	
WLCSP	16	Package not offered		1	260
	25	Package not offered		1	260
	30	Package not offered		1	260
	36	Package not offered		1	260
	49	Package not offered		1	260
	72	Package not offered		1	260
	81	Package not offered		1	260
	84	Package not offered		1	260
FOWLP / ASG	256	Package not offered		3	260
LCC	20	1	235	Package not offered	
	28	1	235	Package not offered	
PDIP	20	1	235	1	260
	24	1	235	1	260

Package Type	Number of Lead/Balls	SnPb Package		Pb-Free / Halogen-Free Package (RoHS Compliant)	
		Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)	Moisture Sensitivity Level	Peak Reflow Temp. (+0/–5 °C)
	28	1	235	1	260
JLCC	44	3	235	Package not offered	
	68	3	235	Package not offered	
GLQFP	128	Package not offered		3	260

Notes:

1. ispMACH® 4000, MachXO2™, MachXO™, LatticeXP2™
2. LatticeECP3™

9. Reflow Profile for SMT Packages

The typical reflow process includes four phases.

1. Preheat – Brings the assembly from 25 °C to TS. During this phase the solvent evaporates from the solder paste. Preheat temperature ramp rate should be less than 2 °C/second to avoid solder ball spattering and bridging.
   - Solder Ball Spattering – The most common solder balling defect is spattering which is caused by explosive evaporation of solvents. It can be eliminated by a slower temperature rise in the preheat phase.
   - Bridging – Often seen on fine pitch components and usually caused by inaccurate or splashy screen printing. Bridging can also be a result of solder paste slumping caused by rapid temperature rise in the pre- heat phase.
2. Flux Activation – The temperature rises slowly and reaches a point at which the flux completely wets the surfaces to be soldered.
3. Reflow – In this phase, the temperature rises to a level sufficient to reflow the solder. The flux wicks surface oxides and contaminants away from the melted solder, resulting in a clean solder joint.
4. Cool Down – Ramp down rate should be as fast as possible in order to control grain size, but should not exceed 6 °C/second.

Table 9.1 and Figure 9.1 describe the reflow profile.

Table 9.1. Peak Reflow Temperature (TP)

Parameter	Description	SnPb Package	Pb-Free and Halogen-Free Packages
Ramp-Up	Average Ramp-Up Rate (T_{SMAX} to T_P)	3 °C/second max.	3 °C/second max.
T_{SMIN}	Preheat Peak Min. Temperature	100 °C	150 °C
T_{SMAX}	Preheat Peak Max. Temperature	150 °C	200 °C
t_S	Time between T_{SMIN} and T_{SMAX}	60 seconds–120 seconds	60 seconds–120 seconds
T_L	Solder Melting Point	183 °C	217 °C
t_L	Time Maintained above T_L	60 seconds–150 seconds	60 seconds–150 seconds
t_P	Time within 5 °C of Peak Temperature	10 seconds–30 seconds	30 seconds
Ramp-Down	Ramp-Down Rate	6 °C/second max.	6 °C/second max.
t 25 °C to T_P	Time from 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

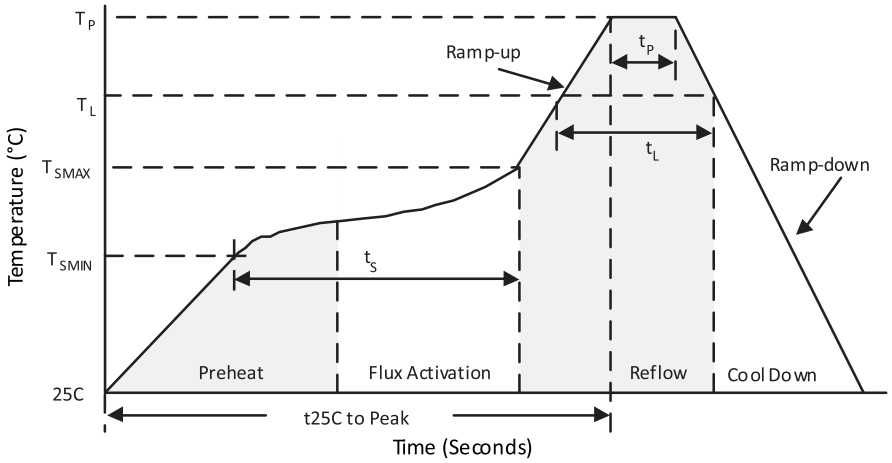

Figure 9.1. Thermal Reflow Profile

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

Revision History

Revision 4.5, June 2022

Section	Change Summary
All	Minor adjustments in formatting across the document.
Peak Reflow Temperature (TP) by Package Size	• Package Type revised from caBGA, fcCSP, fcBGA, fpBGA, and FOWLP to caBGA / BBG, fcCSP / CBG, fcBGA / LFG, fpBGA / BFG, and FOWLP / ASG respectively in Table 8.2. • Added details of the Peak Reflow Temperature of 84 Number of Lead/Balls for the WLCSP Package to Table 8.2.

Revision 4.4, April 2022

Section	Change Summary
All	Minor adjustments in formatting across the document.

Revision 4.3, June 2021

Section	Change Summary
All	Minor adjustments in formatting across the document.
Acronyms in This Document	Updated table to add definition for csfBGA, fcCSP, and FOWLP.
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 to add three packages to support CertusPro-NX: 256 FOWLP, 256 fcCSP, and 672 fcBGA.

Revision 4.2, June 2020

Section	Change Summary
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 to include 484 in fcBGA package type.

Revision 4.1, August 2020

Section	Change Summary
Acronyms in This Document	Updated content.
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 based on JEDEC reflow profile requirement. • Peak Reflow Temps were brought in line with current JEDEC standards and corresponding package volume per package diagram. • Added Reflow profile requirement of 121caBGA, 196csBGA, 284csBGA, 64ucfBGA, 676fcBGA, 237ftBGA, 44LQFP, 72QFN, 72WLCSP, LCC, PDIP, JLCC, and GLQFP to align with the packages included in the Package Diagrams document. • Added 289csBGA new package. • Changed TQFP 1.4mm to LQFP to align with Lattice standard package code • Deleted 36QFN, 20WLCSP, 256BGA, and 352BGA – not included in the Package Diagram document and no data in Agiloft. • Removed Options/Notes of the same number of leads/balls if Reflow Profile requirement is the same. • Not Available is changed to Package Offered

Revision 4.0, June 2020

Section	Change Summary
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 to add 484 and 196 for caBGA package type.

Revision 3.9, May 2020

Section	Change Summary
Disclaimers	Added this section.
Acronyms in This Document	Updated this table.
Peak Reflow Temperature (TP) by Package Size	• Updated Table 8.1.

	• Updated Table 8.2 to add package type for Snow80.
Revision History	Updated format.

Revision 3.8, November 2017

Section	Change Summary
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2. Peak Reflow Temperature (TP) by Package Type and Size. Changed Moisture Sensitivity Level value for csfBGA 285 Balls from 5 to 3.
All	• Changed document ID from TN1076 to FPGA-TN-02041. • Updated document template. • Applied minor editorial changes.
Acronyms in This Document	• Added Acronyms in This Document section.

Revision 3.7, January 2017

Section	Change Summary
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size. • Changed Moisture Sensitivity Level value for csfBGA 285 Balls from 3 to 5. • Added Moisture Sensitivity Level values for TQFP (Thickness: 1.4 mm) packages.

Revision 3.6, December 2016

Section	Change Summary
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size. Added WLCSP 30-ball package type.

Revision 3.5, June 2015

Section	Change Summary
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size. • Added caBGA package type for iCE40 Ultra. • Added QFN package type for iCE40 Ultra.
Technical Support Assistance	Updated Technical Support Assistance section.

Revision 3.4, October 2014

Section	Change Summary
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size. • Added ucFBGA packages for ECP5. • Added csfBGA package type for ECP5.

Revision 3.3, October 2014

Section	Change Summary
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size. • Added caBGA packages for MachXO3L. • Added csfBGA package type for MachXO3L. • Added WLCSP packages for MachXO3L.

Revision 3.2, June 2014

Section	Change Summary
Pb-Free/Halogen-Free (RoHS-Compliant) Products	Updated Pb-Free/Halogen-Free (RoHS-Compliant) Products section. Added packages.
Peak Reflow Temperature (TP) by Package Size	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size. Added WLCSP package types for iCE40 Ultra.

Revision 3.1, May 2014

Section	Change Summary
Pb-Free/Halogen-Free (RoHS-Compliant) Products	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size. Added QFNS package type for MachXO2 and iCE40 LP384.

Reflow Profile for SMT Packages	Updated Table 9.1 Peak Reflow Temperature (TP). Updated the t_P parameter for Pb-Free and Halogen-Free packages based on J-STD-020D.1 standard.
Technical Support Assistance	Updated Technical Support Assistance information.

Revision 3.0, August 2013

Section	Change Summary
Pb-Free/Halogen-Free (RoHS-Compliant) Products	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size.

Revision 2.9, February 2013

Section	Change Summary
Pb-Free/Halogen-Free (RoHS-Compliant) Products	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size.

Revision 2.8, August 2012

Section	Change Summary
All	Updated document to support iCE40 mobile FPGA packaging: • 36, 49, 81, 121 and 225-ball ucBGA • 81 and 121-ball csBGA • 36 and 84-ball QFNS • 100-pin TQFP (1.0 mm thickness)

Revision 2.7, April 2012

Section	Change Summary
All	Updated document to include the 328-ball csBGA package.

Revision 2.6, February 2012

Section	Change Summary
All	Updated document with new corporate logo.

Revision 2.5, June 2011

Section	Change Summary
All	Updated document to include 25 WLCSP package.

Revision 2.4, November 2010

Section	Change Summary
All	Updated for Halogen-free package support.

Revision 2.3, June 2009

Section	Change Summary
Pb-Free/Halogen-Free (RoHS-Compliant) Products	• Updated QFN information in Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size, SnPb Packages table. • Updated QFN information in Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size, Pb-Free Packages table.

Revision 2.2, April 2008

Section	Change Summary
Pb-Free/Halogen-Free (RoHS-Compliant) Products	Updated Table 8.2 Peak Reflow Temperature (TP) by Package Type and Size.

Previous Lattice releases

www.latticesemi.com