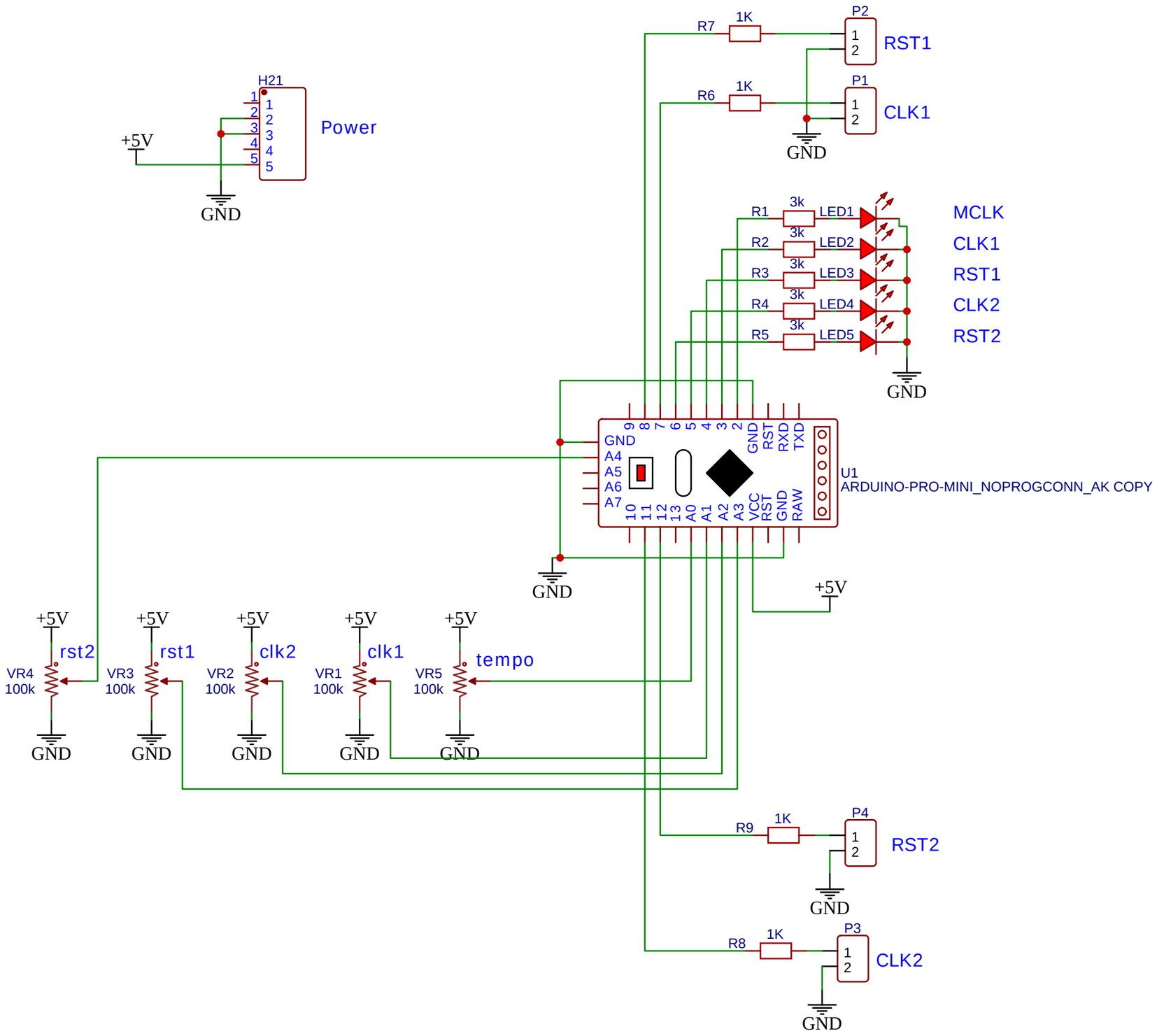

MCLK adjusts the tempo
CLK1/CLK2 sets a divider between 1 and 8 for each clock output
RST1/RST2 sets a divider for each reset between 1 and 8 (provides a reset pulse each N clock cycles)

TITLE: Sheet_1		REV: 1.0
EasyEDA	Company: Your Company	Sheet: 1/1
	Date: 2022-06-02 Drawn By: petegaggs	