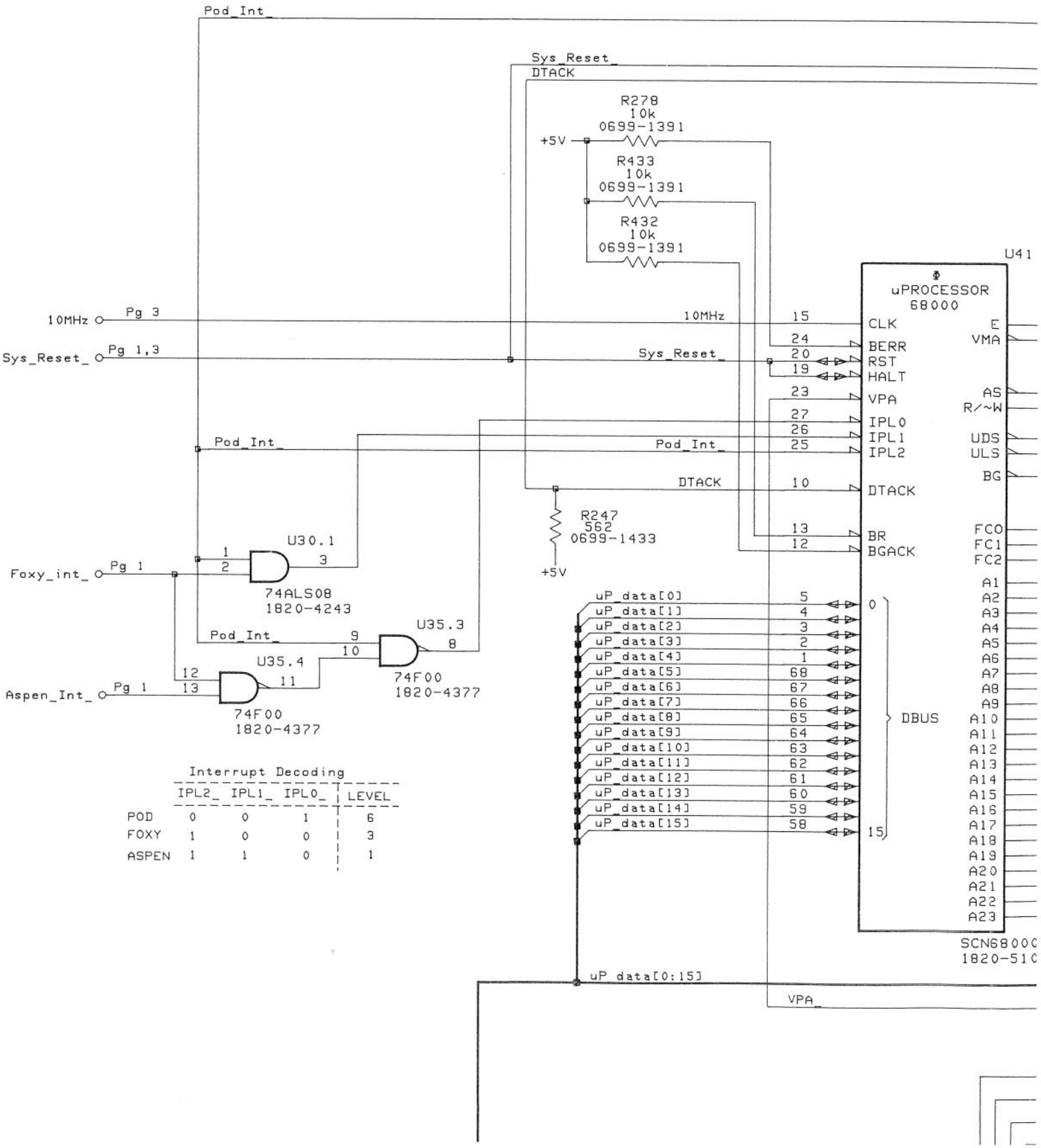
Sheet 2 of 11
Page 1 upper



Interrupt Decoding

	IPL2_	IPL1_	IPL0_	LEVEL
POD	0	0	1	6
FOXY	1	0	0	3
ASPEN	1	1	0	1

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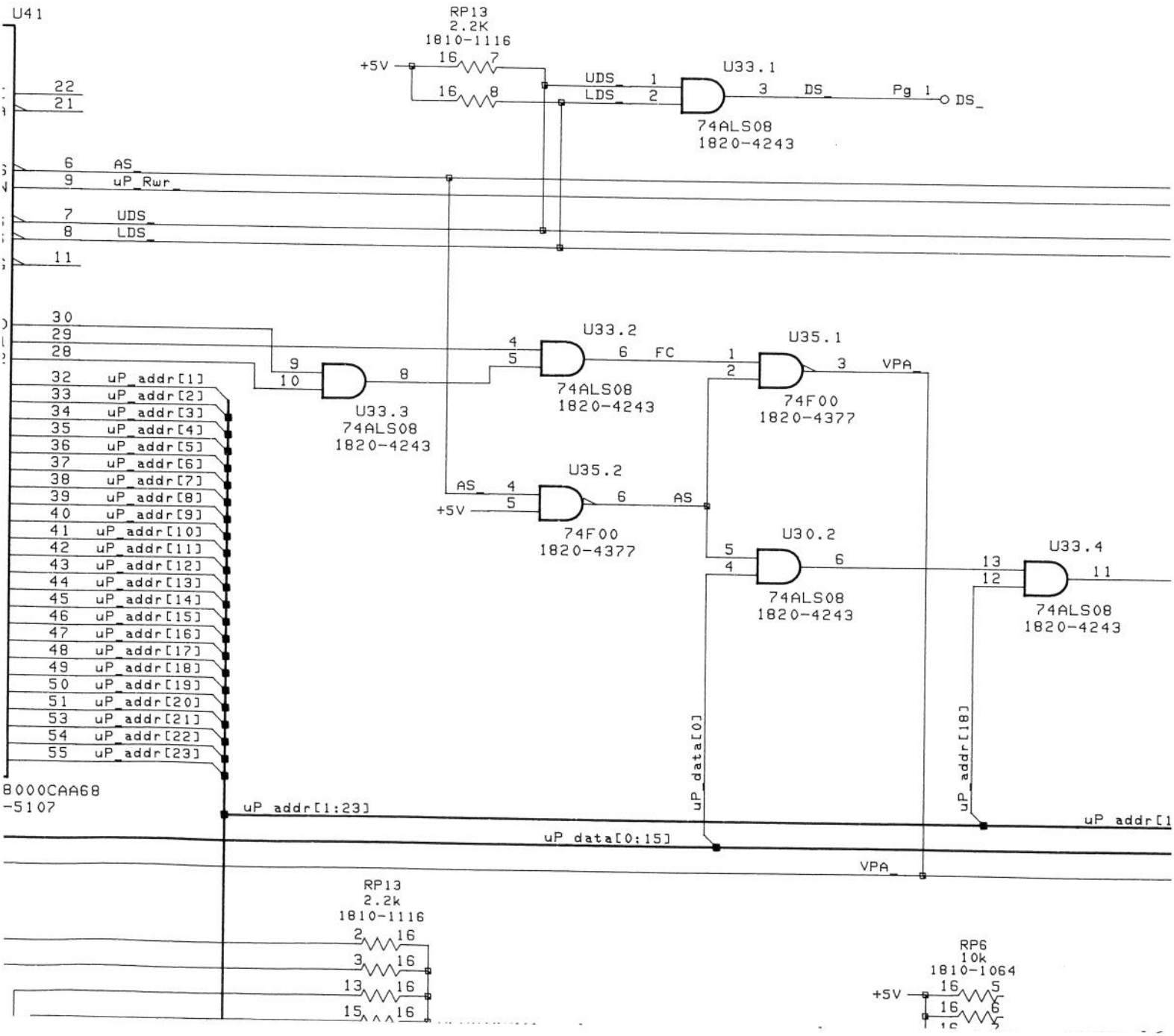
page 2 upper



16	17		19		21	22
45	48	81	83	D2		

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Pod_Int_

Sys_Reset_

DTACK

LDS_ Pg

UDS_

Pg 3

AS_

uP_Rwr_

UDS_

LDS_

+5V

U4

VPP

EPROM 128k X 16

uP_addr[1] 21
uP_addr[2] 22
uP_addr[3] 23
uP_addr[4] 24
uP_addr[5] 25
uP_addr[6] 26
uP_addr[7] 27
uP_addr[8] 28
uP_addr[9] 29
uP_addr[10] 31
uP_addr[11] 32
uP_addr[12] 33
uP_addr[13] 34
uP_addr[14] 35
uP_addr[15] 36
uP_addr[16] 37
uP_addr[17] 38

MEMDIR=
ADDR=
BITPOS=

A 0 / 131071

A(2D/▽)

DOBUF

LROM_OE_ Pg 3

2 G1
39 1C2
20 1,2EN

27C20
1818-

uP_addr[1:23]

uP_data[0:15]

U49

SRAM 8k X 8

uP_addr[1] 10
uP_addr[2] 9
uP_addr[3] 8

MEMDIR=

U48

SRAM 8k X 8

uP_addr[1] 10
uP_addr[2] 9
uP_addr[3] 8

MEMDIR=

29	30	32	33	38	43	SYM	REVISIONS	APPROVED	DATE
						A	AS ISSUED	JS	

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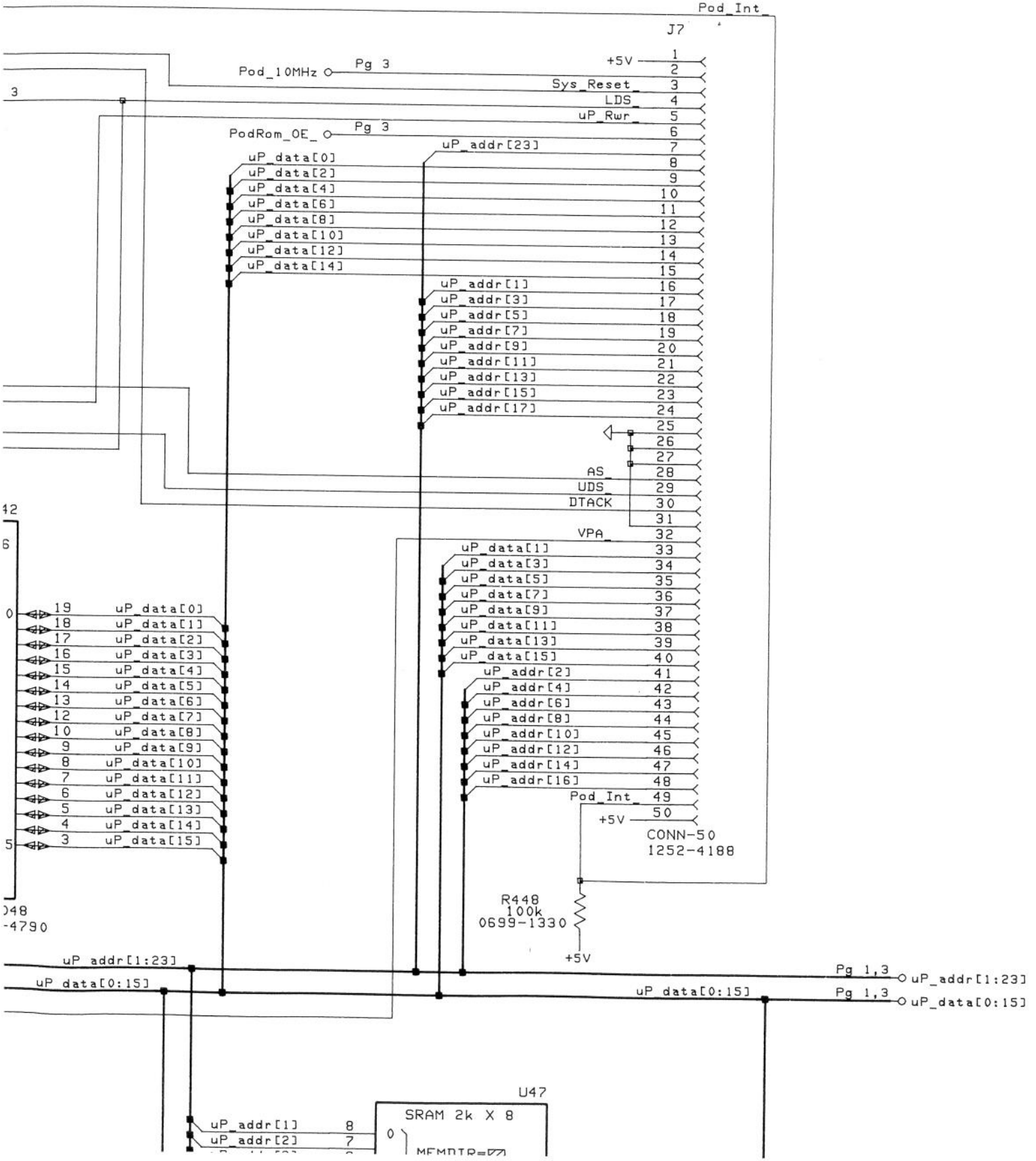

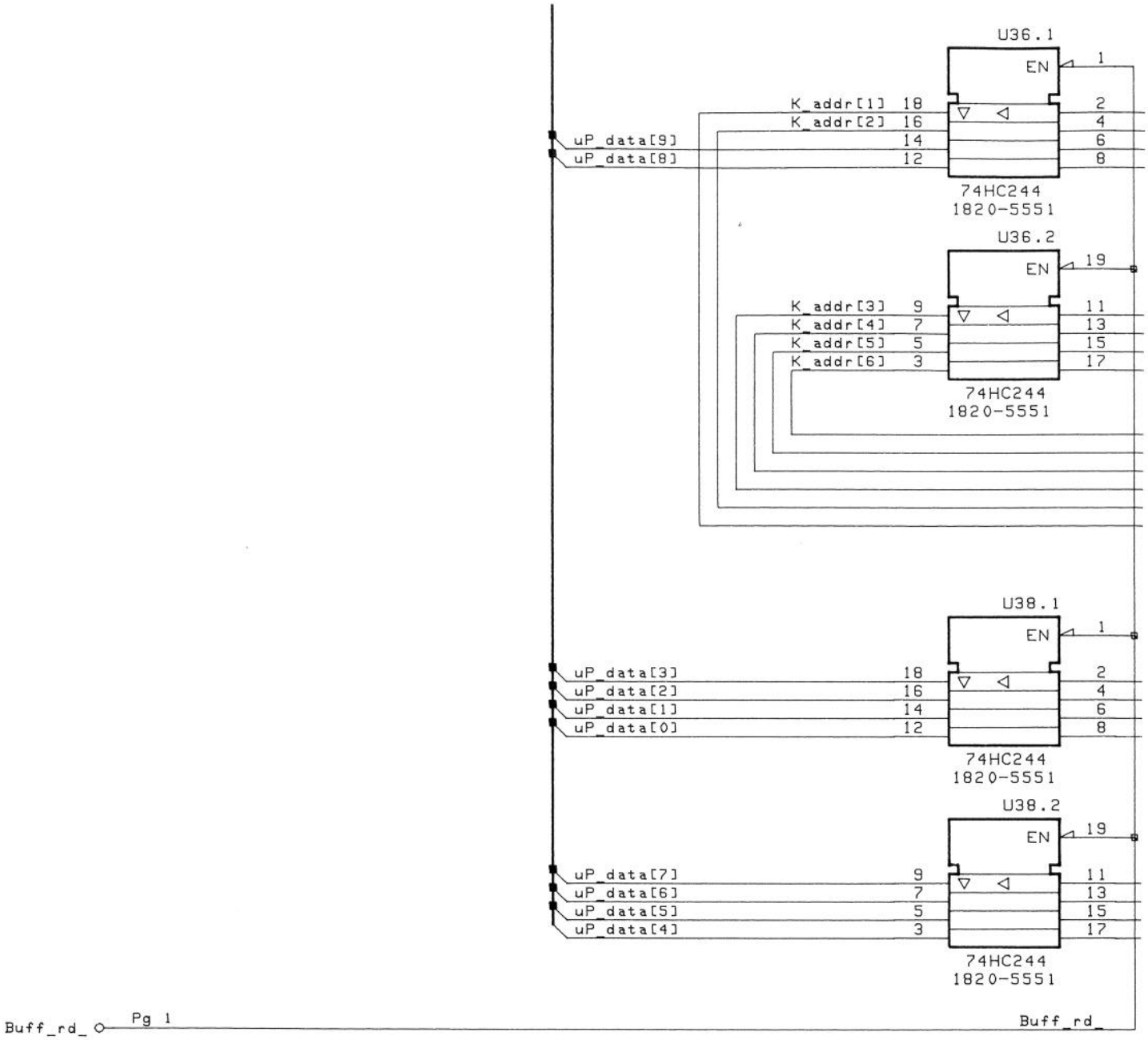

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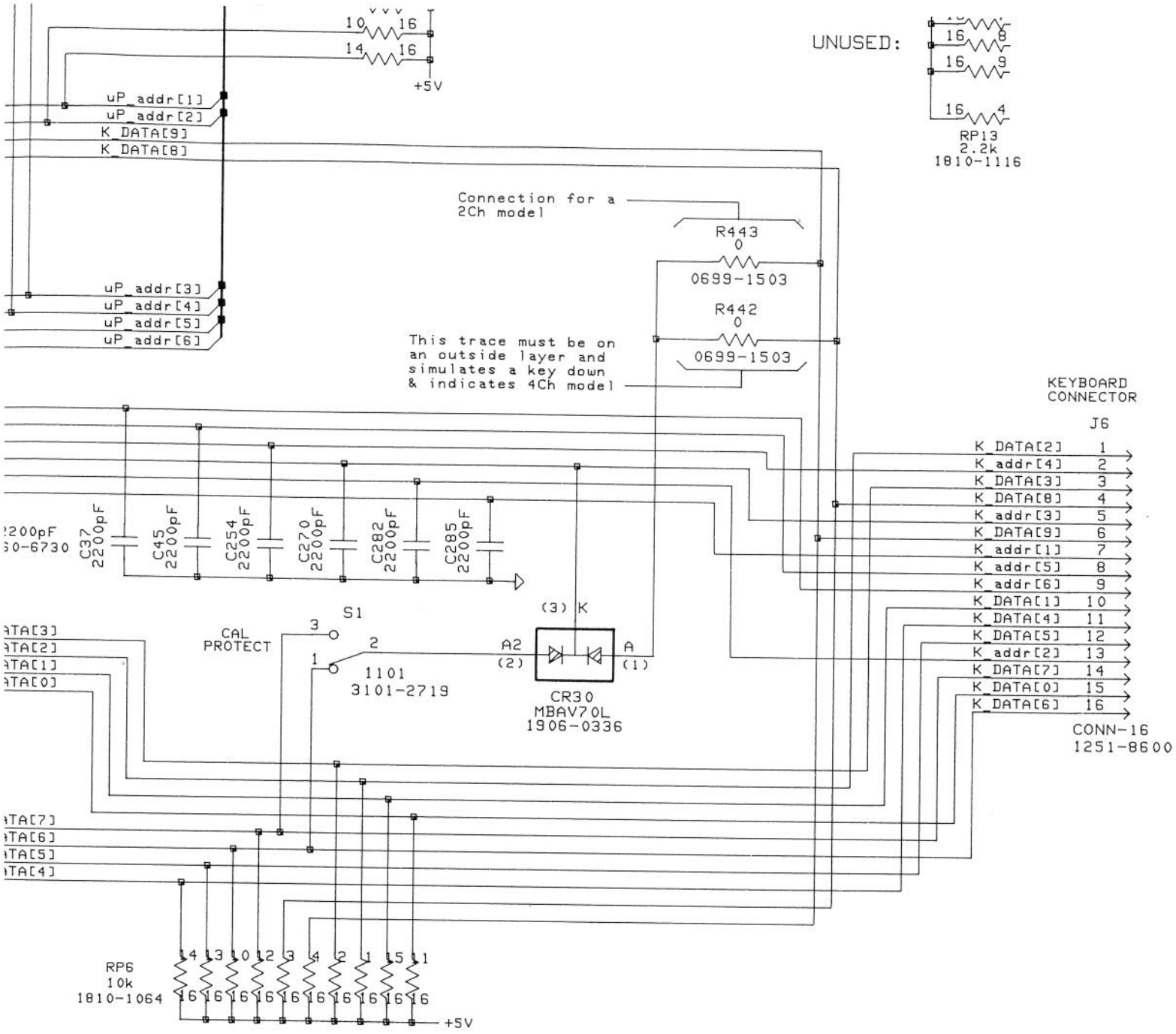
page 1 lower



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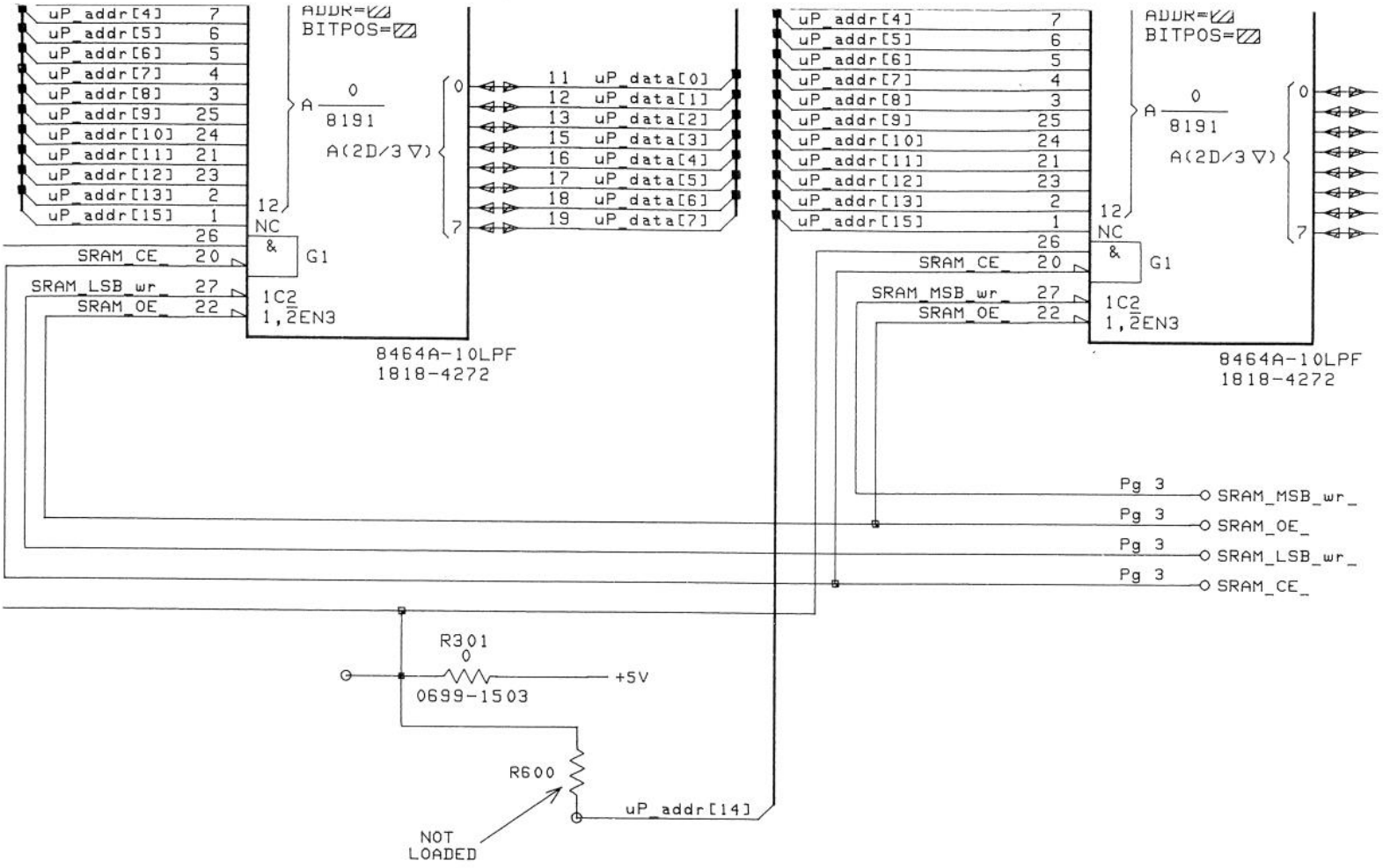
page 2 lower



Parts on this schematic:

C37, 45, 254, 270, 282, 2
CR30, 34
J6, 7
R247, 278, 301, 432, 433,
RP6.1-.16, 13.2-.4, .7-.8
U30.1-2, 33, 35, 36, 38,
S1

Power & Ground connection

	U30,33,35	U36,38	U41
+5V	14	20	14,5
GND	7	10	16,1 56,5

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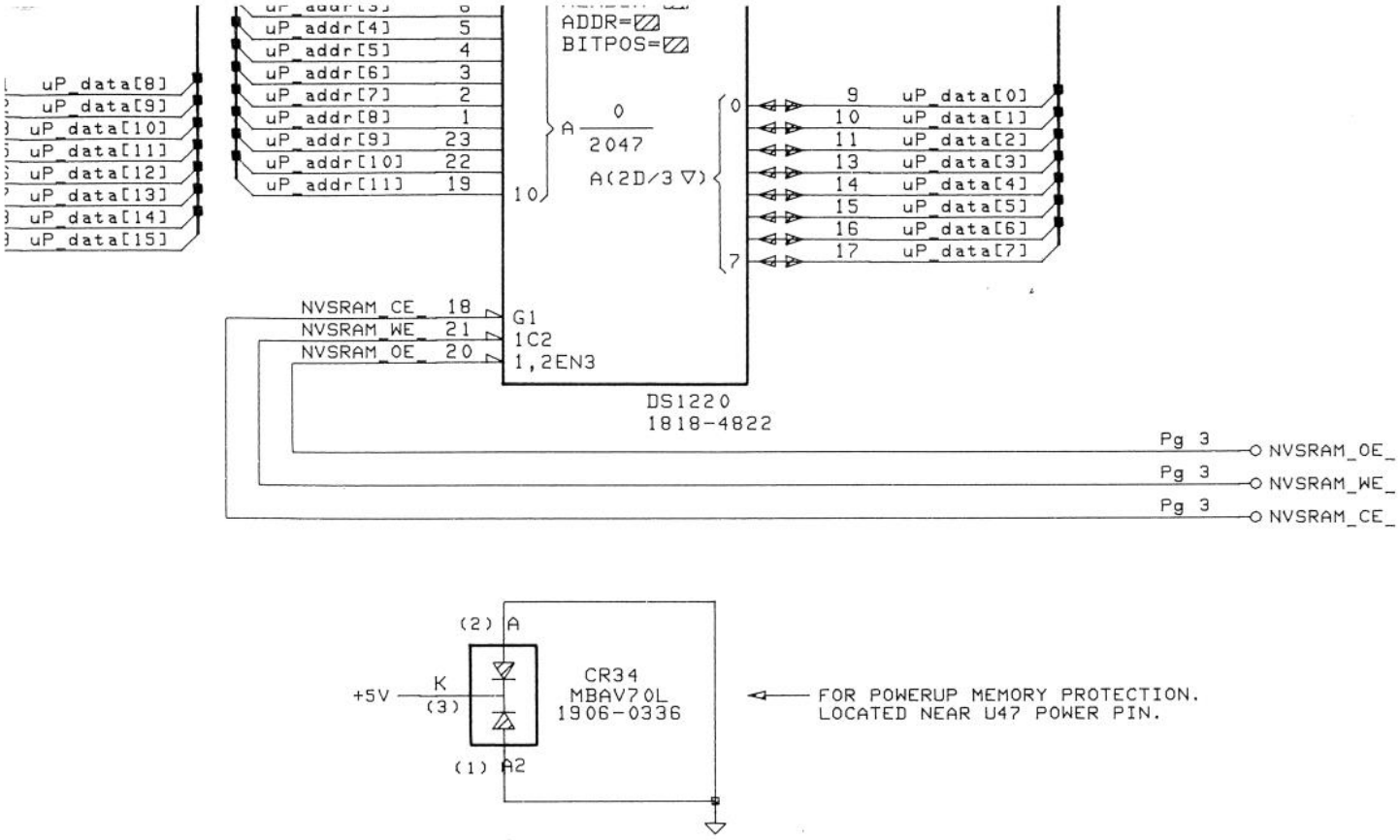
page 3 lower



← FOR POWERUP MEMORY PROTECTION.
LOCATED NEAR U47 POWER PIN.

42, 443, 448, 600
.10, .13-.15
, 42, 47-49

U42	U47	U48,49
40	24	28
30,11	12	14

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AWN BY: JIM STRINGER	DATE: 6/27/91	PROCESSOR & MEMORY	HEWLETT PACKARD	
GINEER				
LEASE TO PROD.		TITLE	PART NUMBER	
PERSEDES DWG.		SCALE	SHEET 2 OF 11	D-54600-66501-3