## FUJITSU

**DATA SHEET**

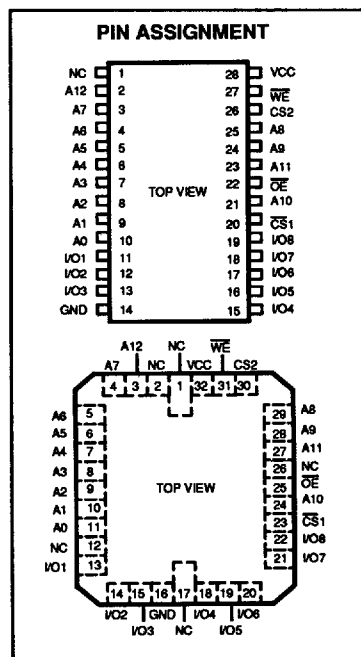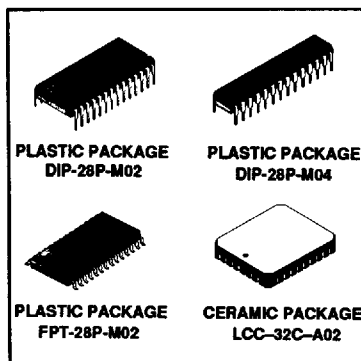# MB8464A-80/-80L/-80LL/-10/-10L/-10LL/-15/-15L/-15LL
# CMOS 64K BIT LOW POWER SRAM

## 8K Words x 8 Bits CMOS Static RAM with Low Power and Data Retention

The Fujitsu MB8464A is a 8,192 words x 8 bits static random access memory fabricated with a CMOS silicon gate process. The memory uses asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible and a single +5 V power supply is required.

The MB8464A has low power dissipation, low cost, and high performance, and it is ideally suited for use in microprocessor systems and other applications where fast access time and ease of use are required.

- Organization:    8,192 words x 8 bits
- Access time:     80 ns max.    (MB8464A-80/-80L/-80LL)
                   100 ns max.   (MB8464A-10/-10L/-10LL)
                   150 ns max.   (MB8464A-15/-15L/-15LL)
- Static operation: no clock required
- TTL compatible inputs and outputs
- Three-state outputs
- Common data inputs and outputs
- Single +5 V power supply ±10% tolerance
- Low power standby:    11 mW max.    (MB8464A-80/-10/-15)
                        0.55 mW max.  (MB8464A-80L/-10L/-15L)
                        0.55 mW max.  (MB8464A-80LL/-10LL/-15LL)
- Data retention current:    1 mA max.    (MB8464A-80/-10/-15)
                             25 µA max.   (MB8464A-80L/-10L/-15L)
                             2 µA max.    at 0°C to 40°C
                                          (MB8464A-80LL/-10LL/-15LL)
- Data retention: 2.0 V min.
- Standard 28-pin Plastic Packages:
    DIP        (600 mil)    MB8464A-xx(L/LL)P
    Skinny DIP (300 mil)    MB8464A-xx(L/LL)PSK
    SOP        (450 mil)    MB8464A-xx(L/LL)PF
- Standard 32-pad Ceramic Package:
    LCC        (metal seal)    MB8464A-xx(L/LL)CV



PLASTIC PACKAGE
DIP-28P-M02

PLASTIC PACKAGE
DIP-28P-M04

PLASTIC PACKAGE
FPT-28P-M02

CERAMIC PACKAGE
LCC-32C-A02

### PIN ASSIGNMENT



## Absolute Maximum Ratings (See Note)

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Supply Voltage | | $V_{CC}$ | −0.5 to +7.0 | V |
| Input Voltage | | $V_{IN}$ | −0.5* to $V_{CC}$ +0.5 | V |
| Output Voltage | | $V_{OUT}$ | −0.5 to $V_{CC}$ +0.5 | V |
| Temperature Under Bias | | $T_{BIAS}$ | −10 to +85 | °C |
| Storage Temperature Range | Ceramic | $T_{STG}$ | −65 to +150 | °C |
| | Plastic | | −45 to +125 | |

\* −2.0 V for pulse width less than 20 ns.

**Note:** Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – MB8464A BLOCK DIAGRAM
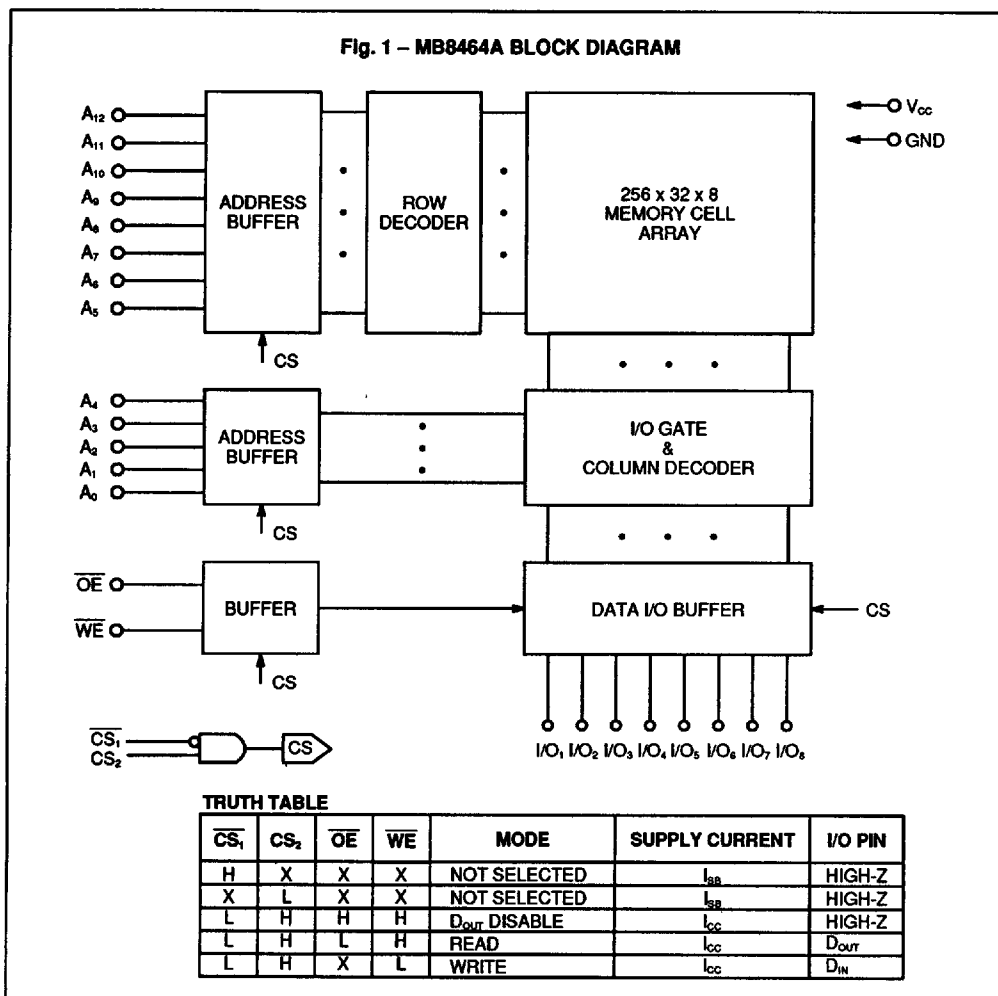
**TRUTH TABLE**

| $\overline{CS_1}$ | $CS_2$ | $\overline{OE}$ | $\overline{WE}$ | MODE | SUPPLY CURRENT | I/O PIN |
|---|---|---|---|---|---|---|
| H | X | X | X | NOT SELECTED | $I_{SB}$ | HIGH-Z |
| X | L | X | X | NOT SELECTED | $I_{SB}$ | HIGH-Z |
| L | H | H | H | $D_{OUT}$ DISABLE | $I_{CC}$ | HIGH-Z |
| L | H | L | H | READ | $I_{CC}$ | $D_{OUT}$ |
| L | H | X | L | WRITE | $I_{CC}$ | $D_{IN}$ |

# CAPACITANCE ($T_A$= 25° C, f = 1MHz)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| I/O Capacitance ($V_{I/O}$=0V) | $C_{I/O}$ | | | 8 | pF |
| Input Capacitance ($V_{IN}$=0V) | $C_{IN}$ | | | 6 | pF |

# RECOMMENDED OPERATING CONDITIONS   T-46-23-12

(Referenced to GND)

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |
| Ambient Temperature | $T_A$ | 0 | | 70 | °C |

# DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

| Parameter | Symbol | MB8464A-80/10/15 Min | MB8464A-80/10/15 Max | MB8464A-80L/80LL 10L/10LL/15L/15LL Min | MB8464A-80L/80LL 10L/10LL/15L/15LL Max | Unit | Test Condition |
|---|---|---|---|---|---|---|---|
| Standby Supply Current | $I_{SB1}$ | | 2 | | 0.1 | mA | $CS_2 \leq 0.2V$, $\overline{CS}_1 \geq V_{CC} -0.2V$ ($CS_2 \leq 0.2V$ or $CS_2 \geq V_{CC} -0.2V$) |
| | $I_{SB2}$ | | 3 | | 3 | mA | $\overline{CS}_1 = V_{IH}$ or $CS_2 = V_{IL}$ |
| Active Supply Current | $I_{CC1}$ | | 50 | | 50 | mA | $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$ $V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OUT} = 0mA$ |
| Operating Supply Current | $I_{CC2}$ | | 60 | | 60 | mA | Cycle=Min., Duty=100% $I_{OUT} = 0mA$ |
| Input Leakage Current | $I_{LI}$ | −1 | 1 | −1 | −1 | μA | $V_{IN} = 0V$ to $V_{CC}$ |
| Output Leakage Current | $I_{LIO}$ | −2 | 2 | −2 | 2 | μA | $V_{I/O} = 0V$ to $V_{CC}$ $\overline{CS}_1 = V_{IH}$ or $CS_2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ |
| Input Low Voltage | $V_{IL}$ | −2.0* | 0.8 | −2.0* | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | 2.2 | $V_{CC}+0.3$ | 2.2 | $V_{CC}+0.3$ | V | |
| Output High Voltage | $V_{OH}$ | 2.4 | | 2.4 | | V | $I_{OH} = -1.0mA$ |
| Output Low Voltage | $V_{OL}$ | | 0.4 | | 0.4 | V | $I_{OL} = 2.1mA$ |

\* −2.0V Min for pulse width less than 20ns. ($V_{IL}$ Min.=−0.3V at DC level)

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### Fig. 2 – AC TEST CONDITIONS

< Output Load >   +5V

- Input Pulse Levels:        0.6V to 2.4V
- Input Pulse Rise and Fall Times: 5ns (Transient Time between 0.8V and 2.2V)
- Timing Reference Levels:   Input : $V_{IL} = 0.8V$, $V_{IH} = 2.2V$
                             Output : $V_{OL} = 0.8V$, $V_{OH} = 2.0V$
- Output Load:

$D_{OUT}$ ○ (I/O)
$C_L$*

| | $R_1$ | $R_2$ | $C_L$ | Parameters Measured |
|---|---|---|---|---|
| Load I | 1.8kΩ | 990Ω | 100pF | except $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{WLZ}$ and $t_{WHZ}$ |
| Load II | 1.8kΩ | 990Ω | 5pF | $t_{CLZ}$, $t_{OLZ}$, $t_{CHZ}$, $t_{OHZ}$, $t_{OHZ}$, $t_{WLZ}$, and $t_{WHZ}$ |
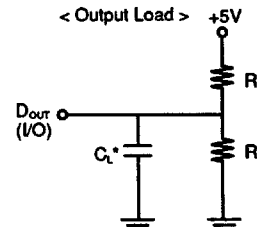
\* Including jig and stray capacitance

3

## AC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted)**

**READ CYCLE**

| Parameter | Symbol | MB8464A-80/80L/80LL | | MB8464A-10/10L/10LL | | MB8464A-15/15L/15LL | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | $t_{RC}$ | 80 | | 100 | | 150 | | ns |
| Address Access Time | $t_{AA}$ | | 80 | | 100 | | 150 | ns |
| $\overline{CS_1}$ Access Time | $t_{AC1}$ | | 80 | | 100 | | 150 | ns |
| $CS_2$ Access Time | $t_{AC2}$ | | 80 | | 100 | | 150 | ns |
| Output Enable to Output Valid | $t_{OE}$ | | 35 | | 45 | | 55 | ns |
| Output Hold from Address Change | $t_{OH}$ | 10 | | 10 | | 10 | | ns |
| Chip Select to Output Low-Z[*1] | $t_{CLZ}$ | 10 | | 10 | | 10 | | ns |
| Output Enable to Output Low-Z[*1] | $t_{OLZ}$ | 5 | | 5 | | 5 | | ns |
| Chip Select to Output High-Z[*1] | $t_{CHZ}$ | | 35 | | 35 | | 40 | ns |
| Output Enable to Output High-Z[*1] | $t_{OHZ}$ | | 30 | | 35 | | 40 | ns |

**READ CYCLE TIMING DIAGRAM [*2]**
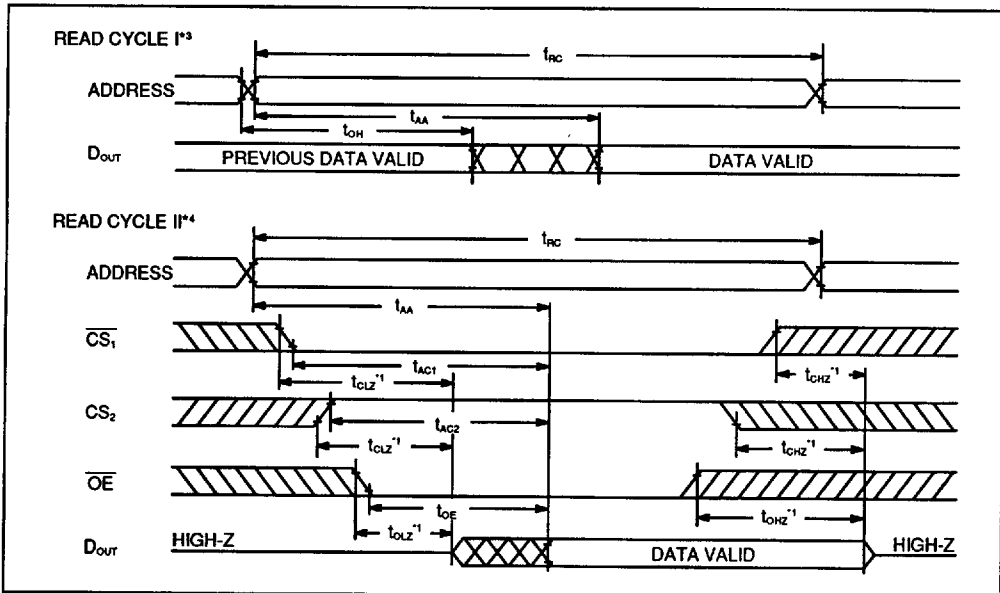


**Note:** *1 Transition is measured at the point of ±500mV from steady state voltage.
*2 $\overline{WE}$ is high for Read Cycle.
*3 Device is continuously selected, $\overline{CS_1}$=$\overline{OE}$=$V_{IL}$, $CS_2$=$V_{IH}$.
*4 Address valid prior to or coincident with $\overline{CS_1}$ transition low, $CS_2$ transition high.

MB8464A-80/80L/80LL
MB8464A-10/10L/10LL
MB8464A-15/15L/15LL

T-46-23-12

## WRITE CYCLE

| Parameter | Symbol | MB8464A-80/80L/80LL Min | Max | MB8464A-10/10L/10LL Min | Max | MB8464A-15/15L/15LL Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| Write Cycle Time | $t_{WC}$ | 80 | | 100 | | 150 | | ns |
| Address Valid to End of Write | $t_{AW}$ | 60 | | 80 | | 100 | | ns |
| Chip Select to End of Write | $t_{CW}$ | 60 | | 80 | | 100 | | ns |
| Data Valid to End of Write | $t_{DW}$ | 30 | | 35 | | 40 | | ns |
| Data Hold Time | $t_{DH}$ | 5 | | 5 | | 5 | | ns |
| Write Pulse Width | $t_{WP}$ | 60 | | 70 | | 90 | | ns |
| Address Setup Time | $t_{AS}$ | 0 | | 0 | | 0 | | ns |
| Write Recovery Time | $t_{WR}$ | 5 | | 5 | | 5 | | ns |
| Write Enable to Output Low-Z[*1] | $t_{WLZ}$ | 5 | | 5 | | 5 | | ns |
| Write Enable to Output High-Z[*1] | $t_{WHZ}$ | | 30 | | 35 | | 40 | ns |

## WRITE CYCLE TIMING DIAGRAM [*2]
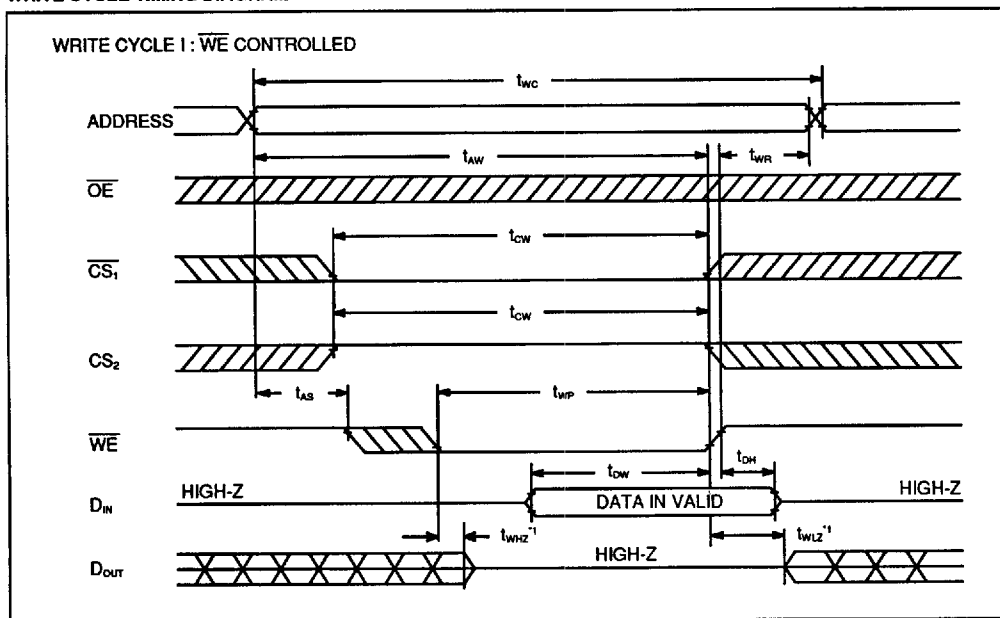


Note:  [*1] Transition is measured at the point of ±500mV from steady state voltage.
  [*2] If $\overline{OE}$, $\overline{CS_1}$ and $CS_2$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

3-9

MB8464A-80/80L/80LL
MB8464A-10/10L/10LL
MB8464A-15/15L/15LL

T-46-23-12

WRITE CYCLE II : $\overline{CS_1}$ CONTROLLED*[1]



WRITE CYCLE III : $CS_2$ CONTROLLED*[2]
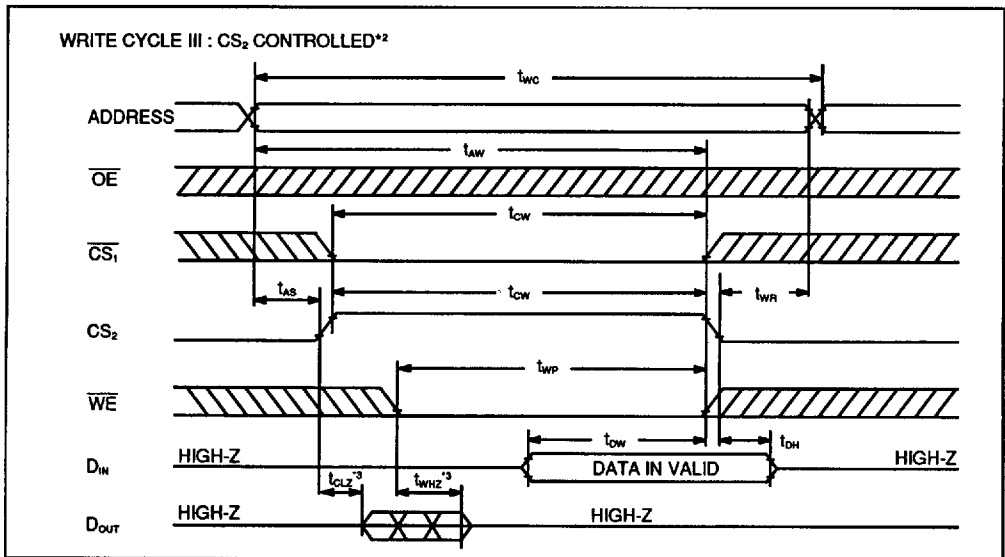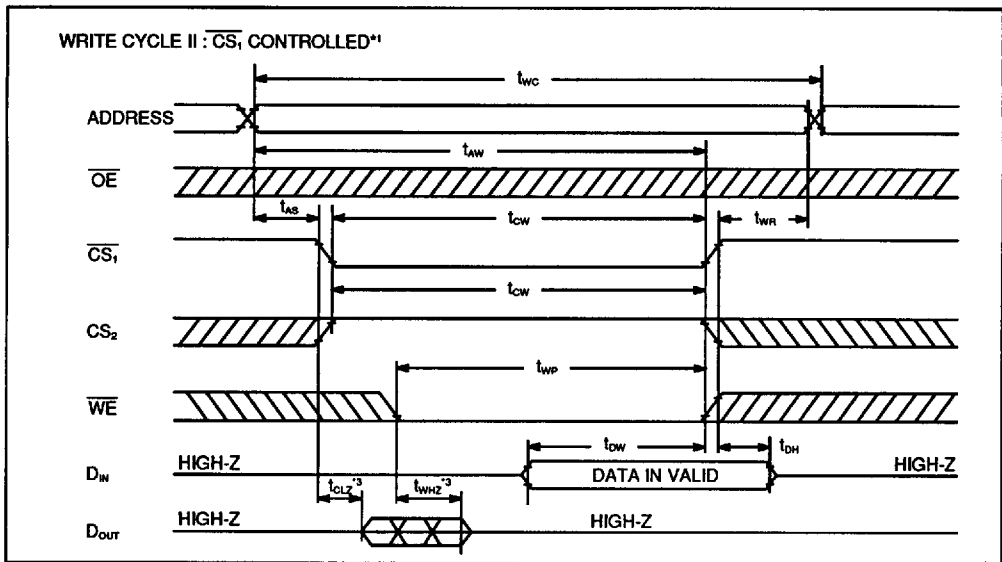


**Note:** *[1] If $\overline{OE}$, $CS_2$ and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*[2] If $\overline{OE}$, $\overline{CS_1}$ and $\overline{WE}$ are in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.

*[3] Transition is measured at the point of ±500mV from steady state voltage.

# DATA RETENTION CHARACTERISTICS    T-46-23-12

**(Recommended operating conditions unless otherwise noted)**

| Parameter | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Data Retention Supply Voltage | | $V_{DR}$ | 2.0 | | 5.5 | V |
| Data Retention Supply Current*2 | Standard | $I_{DR}$ | | | 1.0 | mA |
| | L-Version | | | 1.0 | 25 | μA |
| | LL-Version*3 | | | 1.0 | 2.0 | μA |
| Data Retention Setup Time | | $t_{DRS}$ | 0 | | | ns |
| Operation Recovery Time | | $t_R$ | $t_{RC}$ | | | ns |

**Note:** *2 $CS_2$ controlled: $V_{DR}$=3.0V, $CS_2 \leq 0.2V$
$\overline{CS_1}$ controlled: $V_{DR}$=3.0V, $\overline{CS_1} \geq V_{DR}$ −0.2V ($CS_2 \leq 0.2V$ or $CS_2 \geq V_{DR}$ −0.2V)
*3 $V_{DR}$=3.0V, $T_A$=0°C to 40°C

**3**

**DATA RETENTION TIMING**



DATA RETENTION I : $\overline{CS_1}$ CONTROLLED

DATA RETENTION II : $CS_2$ CONTROLLED
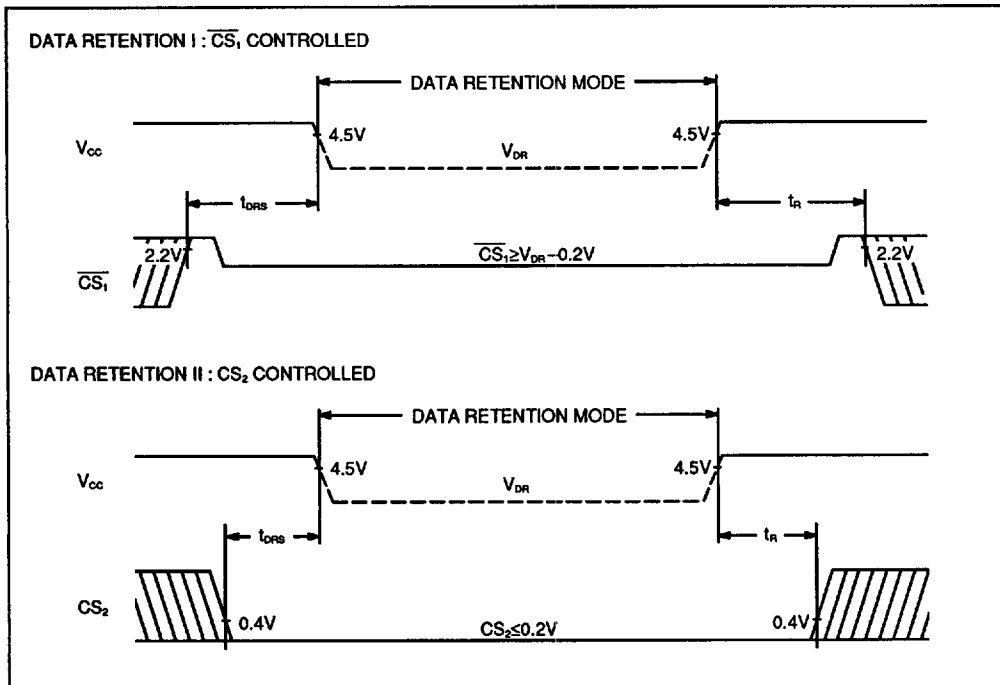
# TYPICAL CHARACTERISTICS CURVES

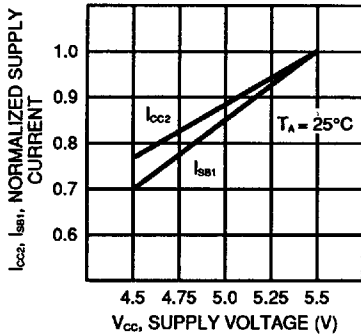### Fig. 3 – NORMALIZED POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE

### Fig. 4 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE
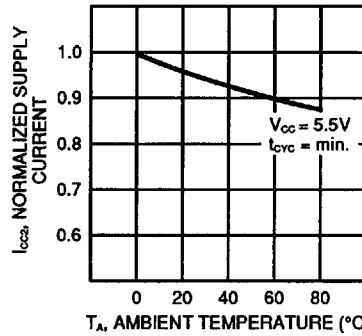
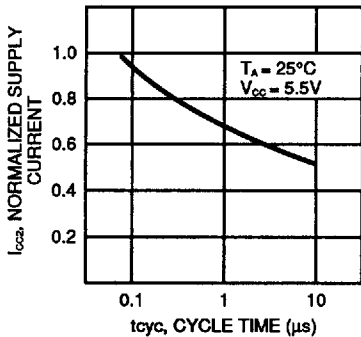### Fig. 5 – NORMALIZED POWER SUPPLY CURRENT vs. CYCLE TIME

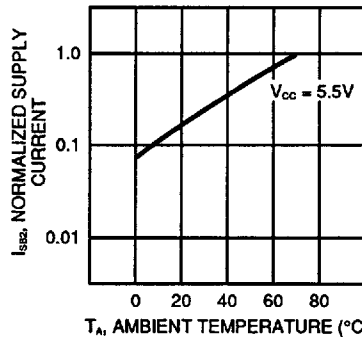### Fig. 6 – NORMALIZED POWER SUPPLY CURRENT vs. AMBIENT TEMPERATURE

### Fig. 7 – NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE
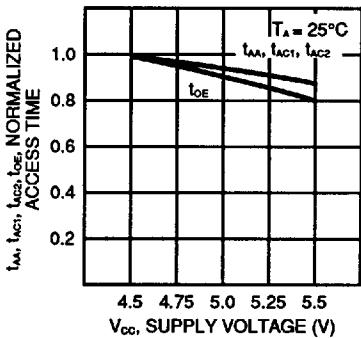
### Fig. 8 – NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE
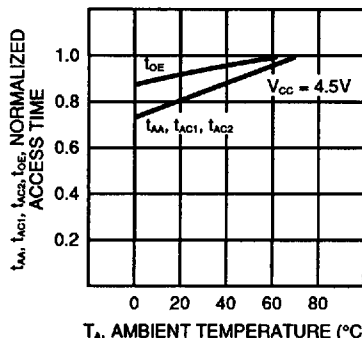
# PACKAGE DIMENSIONS
(Suffix: P)

T-46-23-12



28-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No. : DIP-28P-M02)

15°MAX

.543±.010
(13.8±0.25)

.600(15.24)TYP

INDEX

.010±.002
(0.25±0.05)

1.407$^{+.008}_{-.012}$(35.73$^{+0.20}_{-0.30}$)

.062(1.58)MAX

.039$^{+.020}_{-0}$ (0.99$^{+0.50}_{-0}$)

.195(4.96)MAX

.118(3.00)MIN

.100(2.54)
TYP

.060$^{+.020}_{-0}$
(1.52$^{+0.50}_{-0}$)

018±.003
(0.46±0.08)

.020(0.51)MIN

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Dimensions in
inches (millimeters)

3

# PACKAGE DIMENSIONS

**(Suffix: P–SK)**

## 28-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-28P-M04)

INDEX-1

INDEX-2

$1.392^{+.008}_{-.012}(35.36^{+0.20}_{-0.30})$

$260\pm.010$ $300(7.62)$
$(6.60\pm0.25)$ TYP

$034^{+.012}_{-0}$
$(0.86^{+0.30}_{-0})$

$050^{+.012}_{-0}$
$(1.27^{+0.30}_{-0})$

15° MAX

$010\pm.002$
$(0.25\pm0.05)$

207(5.25) MAX

118(3.00) MIN

050(1.27)
MAX

100(2.54)
TYP

$018\pm.003$
$(0.46\pm0.08)$

020(0.51) MIN

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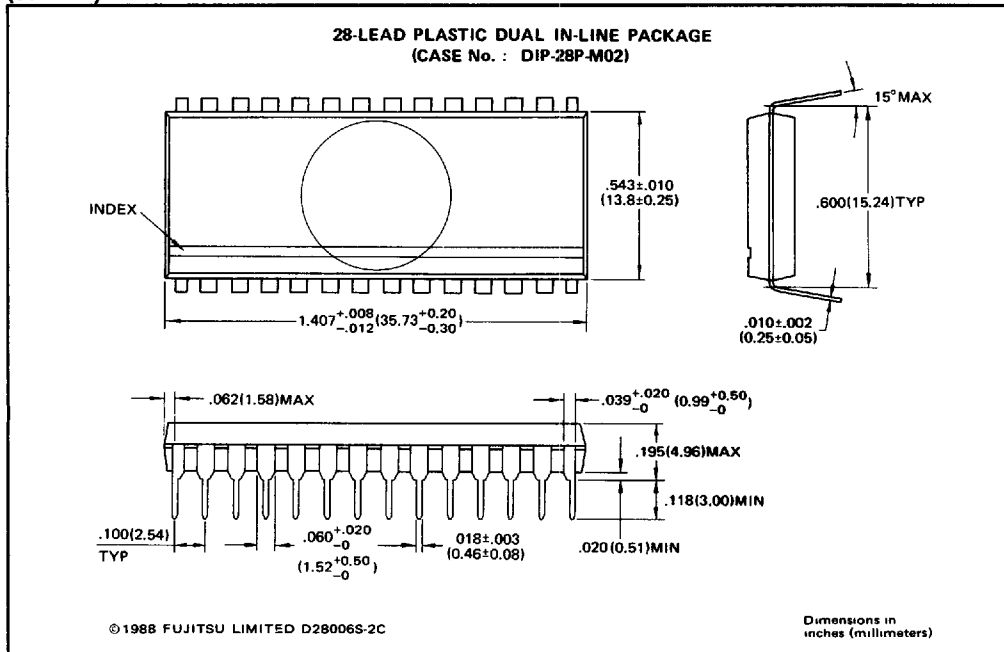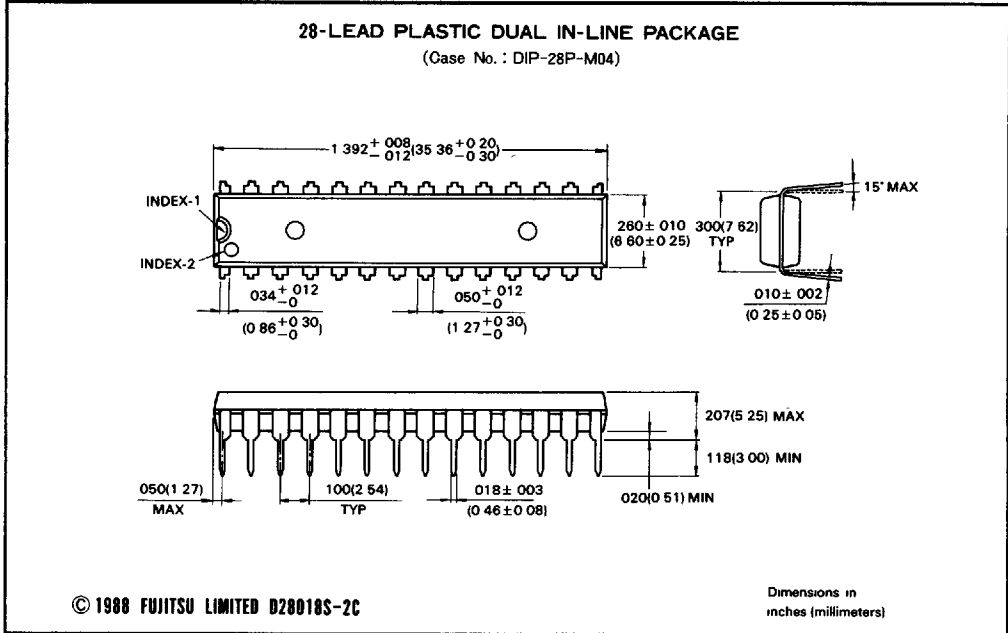
Dimensions in
inches (millimeters)

# PACKAGE DIMENSIONS (Cont'd)

T-46-23-12

(Suffix: PF)
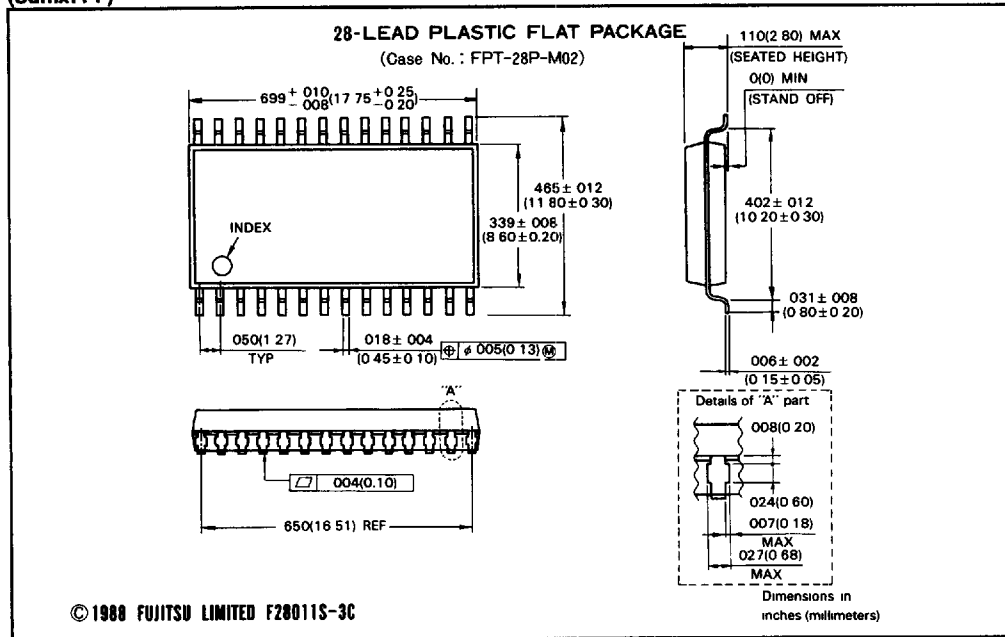
**28-LEAD PLASTIC FLAT PACKAGE**
(Case No. : FPT-28P-M02)

110(2 80) MAX
(SEATED HEIGHT)
0(0) MIN
(STAND OFF)

699 +010 −008 (17 75 +0 25 −0 20)

465 ± 012
(11 80 ± 0 30)

339 ± 006
(8 60 ± 0.20)

INDEX

402 ± 012
(10 20 ± 0 30)

031 ± 008
(0 80 ± 0 20)

050(1 27)
TYP

018 ± 004
(0 45 ± 0 10)

⊕ φ 005(0 13) Ⓜ

006 ± 002
(0 15 ± 0 05)

"A"

Details of "A" part

008(0 20)

024(0 60)

007(0 18)
MAX

027(0 68)
MAX

004(0.10)

650(16 51) REF

Dimensions in
inches (millimeters)

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# PACKAGE DIMENSIONS (Cont'd)
(Suffix: CV)

32-PAD CERAMIC (METAL SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-32C-A02)



*PIN NO.1 INDEX

C.040(1.02)TYP
(3PLCS)

.360(9 14)TYP

C.015(0.38)TYP

100(2.54)TYP

*PIN NO.1
INDEX

$.550^{+.010}_{-.005}$
$(13.97^{+0 25}_{-0.13})$

R.008(0.20)
TYP(32PLCS)

460(11 68)
TYP

.400(10.16)
TYP

.025±.005
(0.64±0.13)

$.450^{+.010}_{-.005}$
$(11.43^{+0.25}_{-0.13})$

.065(1.65)
TYP

.045(1 14)
TYP

.085(2.16)
MAX

.050±.006
(1.27±0.15)

300(7.62)TYP

.050±.006
(1.27±0.15)
.045(1 14)TYP

Dimensions in inches
(millimeters)

\* Shape of PIN NO. 1 INDEX  Subject to change without notice.

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**3**