ECE3623 Embedded System Design Laboratory

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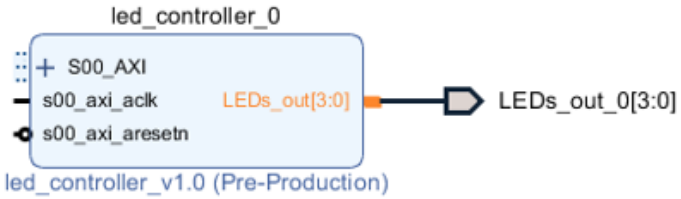
IP in Vivado HDL

In this Laboratory you will utilize the embedded development of Vivado to configure an Intellectual Property (IP) block using Verilog HDL. The reference for this Laboratory is the *Zynq Book Tutorials* pages 94-117 for IP creation as Exercise 4A.

The tasks for this Laboratory are as follows:

1. Complete and verify the performance of the template project *led_controller* with the hardware design of the IP block and the SDK software *led_controller_test_tut_4A.c*



2. Modify the simple Verilog code from the template project to perform a new logical function. Initially the Verilog code only continuously assigns the input from the AXI bus in the IP as the 32-bit slv_reg0 (or slave register 0) to the 4-bit *LEDs_out* port in the template code *led_controller_v1_S00_AXI.v*:

```
// Add user logic here
assign LEDs_out = slv_reg0;
// User logic ends
```

Here you are to perform the following logical function in the *Add user logic here* section of *led_controller_v1_S00_AXI.v* with final the assignment to *LEDs_out* port register. The 4-bit *LEDs_out* port is to display in binary the number of 1's (0 – 15) in the least significant 15 bits of the slv_reg0.

Note that the 4-bit *LEDs_out* port is not a register and a local 4-bit register for the LEDs must be used instead. Continuously assign that register to the LED port for the display.

The initial contents of the 32-bit slv_reg0 should be set to a local Verilog 32-bit register first for the analysis and other registers for the logical function.

Local registers of 1-bit, 4-bit and 32-bit can be defined in Verilog as below within the *Add user logic here* section of *led_controller_v1_S00_AXI.v.*

```
reg localreg;
reg [3:0] localreg4;
reg [31: 0] localreg32;
```

The SDK template program is to be modified to write a sequence of 10 integers up to 32767 (111 1111 1111 1111) of your choice to the new *led_controller* IP with an adequate delay between the display to verify performance. The number 32767 has 15 1's and the LEDs would all be ON (1111).

Project Summary | Package IP - led_controller | led_controller_v1_0_S00_AXI.v *

c:/Zynq_Book_Tutorial_Projects/ip_repo/led_controller_1.0/hdl/led_controller_v1_0_S00_AXI.v

```
394              begin
395                axi_rdata <= reg_data_out;     // register read data
396              end
397          end
398      end
399
400      // Add user logic here
401
402      // User logic ends
403
404      endmodule
```

This Laboratory is for the week of April 13th and due no later than Sunday April 19th 11:59 PM with an upload to Canvas of the Project Report with documentation of task completion.