ECE3623 Embedded System Design Laboratory

Dennis Silage, PhD
silage@temple.edu

TU ID FIR Digital Filter

In this Laboratory you will be introduced to the implementation of a finite impulse response (FIR) digital filter on the PS of the Zynq device on the Zybo Board with the PmodDA2 DAC external peripherals for the output. A discrete sinusoidal signal will simulate an analog-to-digital converter (ADC) input to the FIR digital filter.

The project is to implement the FIR digital filter with constant coefficients and the transfer function H(z) given by:

$$H(z) = b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3} + b_4 z^{-4} + b_5 z^{-5}$$

The coefficients are unique: b_0 is the least significant digit (LSD) of your Temple University ID *modulo* 5 *plus* 1, b_1 is the second LSD *modulo* 4 *plus* 1, b_2 is the third LSD *modulo* 3 *plus* 1, b_3 is the fourth LSD *modulo* 2 *plus* 1, b_4 is the fifth LSD *plus* 1 and b_5 is the sixth LSD *plus* 1 .

The term *plus* 1 is there so that if the *modulo* operation produces 0 the coefficient would be at least 1. For example, if the six least significant digits (left to right) are 689735 then $b_0 = 1$, $b_1 = 1$, $b_2 = 2$, $b_3 = 2$, $b_4 = 1$, $b_5 = 7$.

The project task is to implement the FIR digital filter with the PmodDA2 for output in Xilinx Vivado and SDK as a single task application (not with Free RTOS). Only the DA2Pmod IP is to be used and the *Zynq SPI Peripherals* PowerPoint (in pdf) on Canvas provides a reference for the implementation. The *Introduction to DSP* PowerPoint (in pdf) on Canvas is also a reference. The discrete sinusoidal input signal is generated as an array of 4096 samples.

The Laboratory tasks are as follows:

1. In order to test the response of the FIR digital filter in the Laboratory, you are to calculate the magnitude of the frequency response. You could use MATLAB to facilitate the process. The apparent gain G of the FIR filter is

also important so that the FIR filter output to the DAC can be properly scaled without an overload.

In this analysis you can assume that the sampling rate f_S = 50 ksamples/sec or T_S = 20 μsec. This is done because there is no sampling clock and the ADC input, or the discrete input signal, will be simulated.

If a complete 4096-point simulated discrete sinusoid is inputted to the FIR filter this would represent a period of 4096 x 20 μsec = 81.92 msec or a frequency of approximately 12.21 Hz in this simulation.

Then if every other point of the 4096-point discrete sinusoid is inputted to the FIR filter this would represent a period of 2048 x 20 μsec = 40.96 msec or a frequency of approximately 24.42 Hz.

Thus, by inputting every *n*th point, the apparent frequency increases by *n* x 12.1 Hz where 12.12 Hz is the fundamental frequency.

The filter is to be tested and compared to the theoretical response at *n* = 1, 2, 3, 4, 5, 6, 7, and 8.

2. Plot the resulting pole-zero pattern for the FIR filter. The MATLAB function *roots* can solve for the roots of a polynomial. Can you infer from the pole-zero pattern by estimating the lengths to the point P what the frequency response from f = 0 to $f_S/4$ Hz of the FIR filter might be? Compare the estimate to that calculate in Task 1.

3. Generate a discrete sinusoid of 4096 points as an array of *signed* integer numbers in the range of ± 2000 with approximately 11 bits of resolution and a sign bit. This represents the input to the FIR filter: x(m).

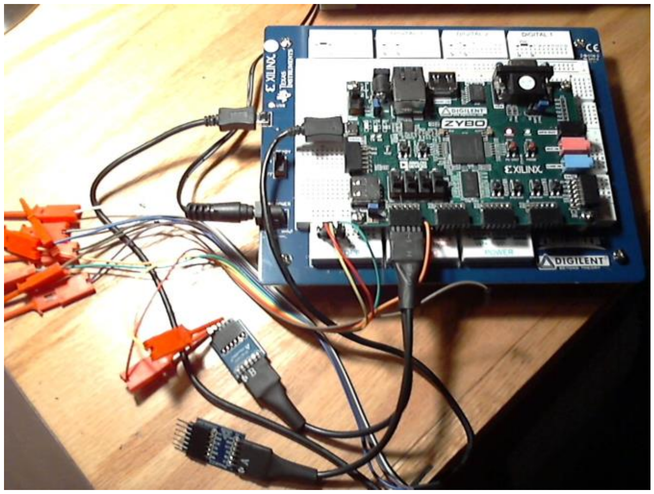
4. Generate the code necessary to process the FIR filter from the transfer function H(z) rendered as a discrete equation for the output y(m) in terms of the input x(m):

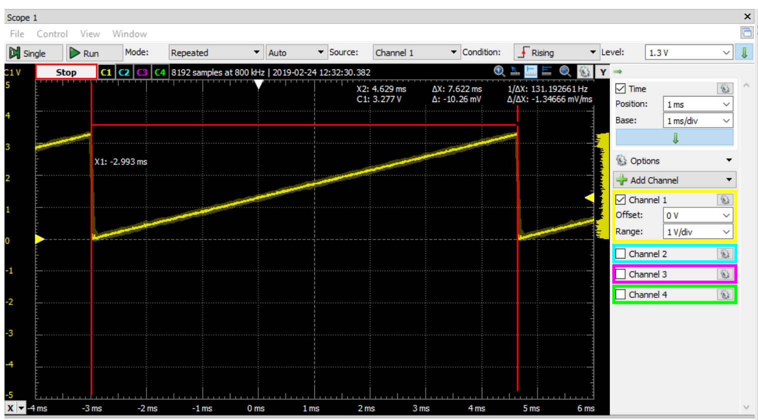
   $$y(m) = b_0\, x(m) + b_1\, x(m-1) + b_2\, x(m-2) + b_3\, x(m-3) + b_4\, x(m-4) + b_5\, x(m-5)$$

   This is accomplished by a *push-down list* where the previous input samples are maintained for the next iteration of the FIR filter.

5. The output signal to the DAC must be in the unipolar range of 0 to 4095 although the FIR filter calculated signed integers. Plot the expected range of the output of the FIR filter in MATLAB to verify the computed gain G of the filter. Describe the *offset* and *scaling* to be performed in the output processing to provide discrete data in the unipolar range of 0 to 4095 for the DAC.

6. Using the EE Board (Discovery 2) and Waveforms, show the output of the FIR filter from the DAC with the sinusoidal input at n x 12.12 Hz for n = 1, 2, 3, 4, 5, 6, 7, and 8. Measure and plot the amplitude response at a simulation of n x 12.12 Hz for n = 1, 2, 3, 4, 5, 6, 7, and 8. Compared the measurement to the calculate the amplitude magnitude of the frequency response.





DA2Pmod outputting a linear ramp

This is a two-week Lab for the weeks of March 23rd and March 30th and due no later than Sunday April 5th at 11:59 PM. Archive the project for a Quiz or Exam and you may also be required to demonstrate your project to the Laboratory Assistant.