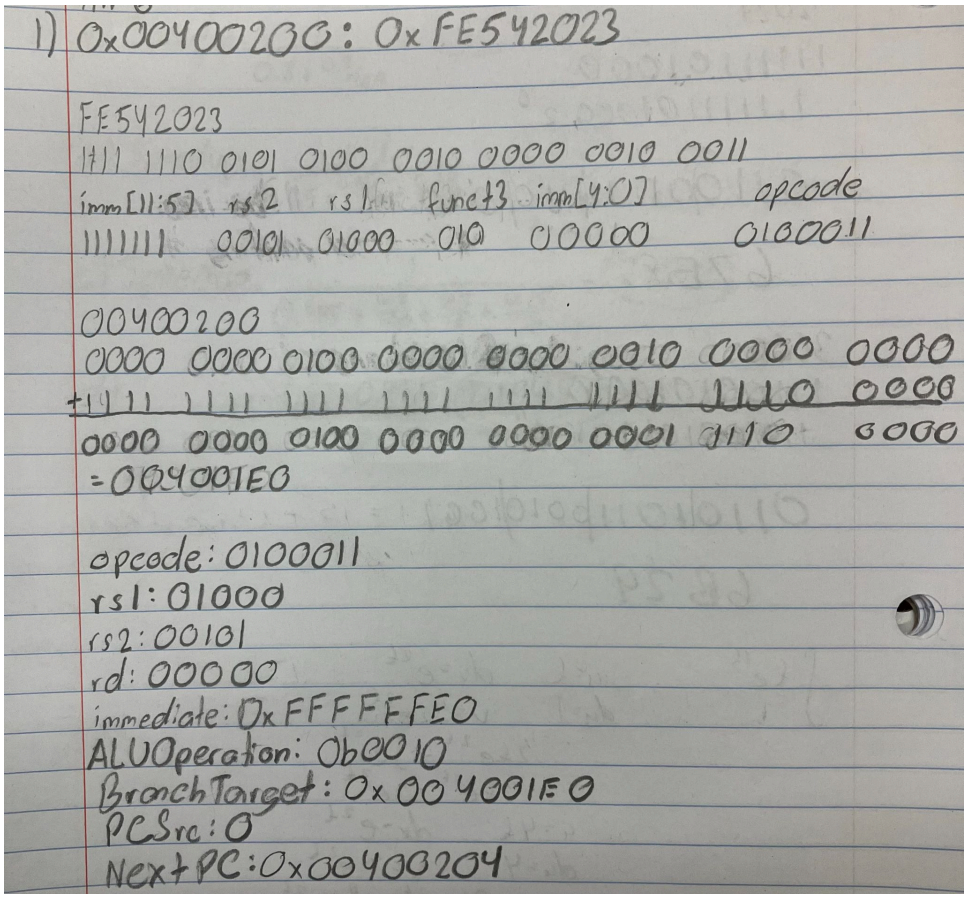
Peter Pettino
CSE 3666
30 March, 2024

Homework 6

1)



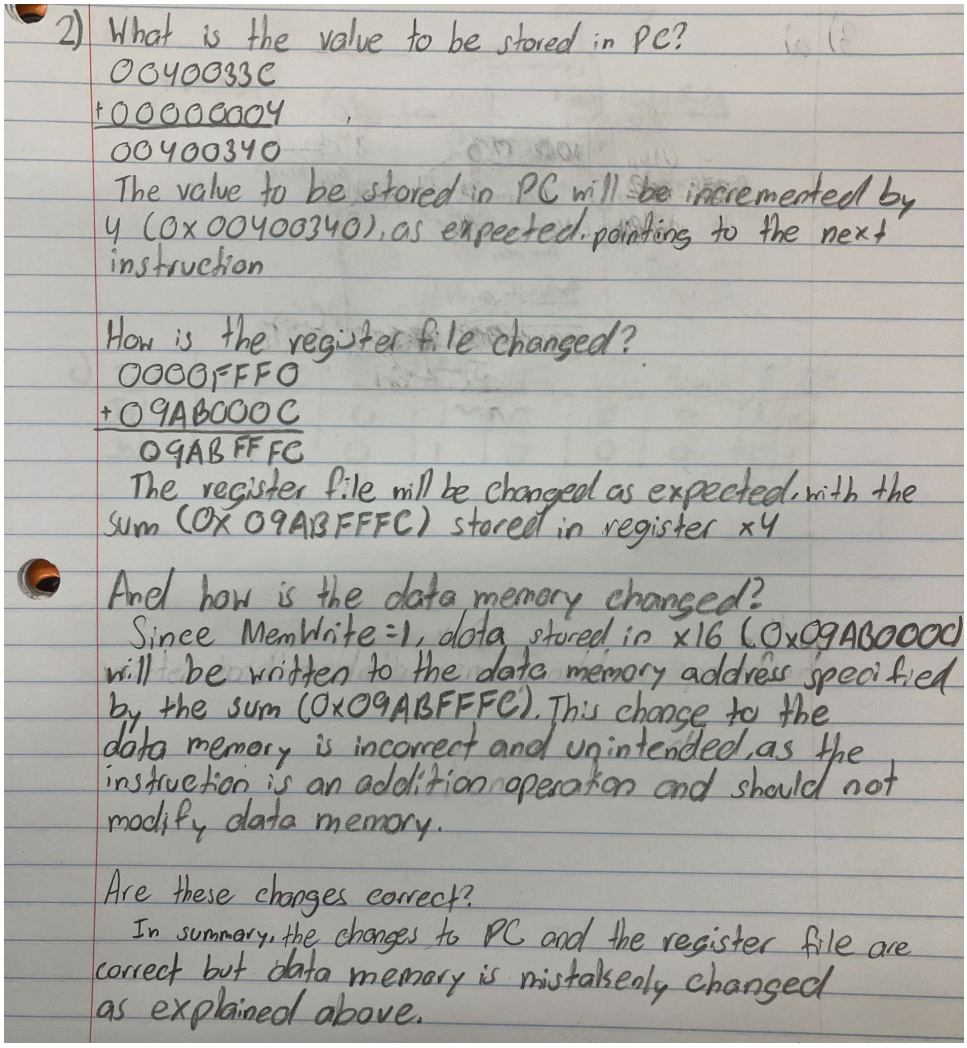
- opcode given by Instruction[6, 0]
- rs1 given by Instruction[15, 19]
- rs2 given by Instruction[20, 24]
- rd given by Instruction[7, 11], however since sw is an S-type instruction, it does not have an rd
- Immediate given by the concatenation of Instruction[31, 25] and Instruction[7, 11] in addition to the sign extension in the front

- ALUOperation given by this table:

Operation	ALUOp	funct7	funct3	ALU operation	ALU function
Load/store	00	xxx xxxx	xxx	0010	add
branch	01	xxx xxxx	xxx	0110	subtract
R-type	10	000 0000	000	0010	add
R-type	10	010 0000	000	0110	subtract
R-type	10	000 0000	111	0000	and
R-type	10	000 0000	110	0001	or

- BranchTarget calculated by addition of immediate (0xFFFFFFE0) and current address (0x00400200)
- PCSrc is 0 since instruction is not a branch operation
- NextPC is PC (0x00400200) + 4

2)



2) What is the value to be stored in PC?

00400338
+00000004
00400340

The value to be stored in PC will be incremented by 4 (0x00400340), as expected, pointing to the next instruction

How is the register file changed?

0000FFF0
+09AB000C
09ABFFFC

The register file will be changed as expected, with the sum (0x09ABFFFC) stored in register x4

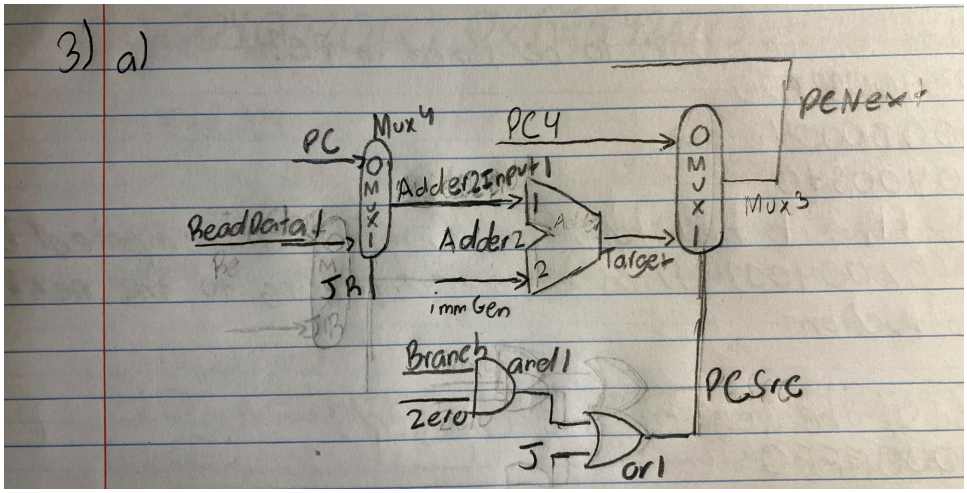
And how is the data memory changed?

Since MemWrite=1, data stored in x16 (0x09AB000C) will be written to the data memory address specified by the sum (0x09ABFFFC). This change to the data memory is incorrect and unintended, as the instruction is an addition operation and should not modify data memory.

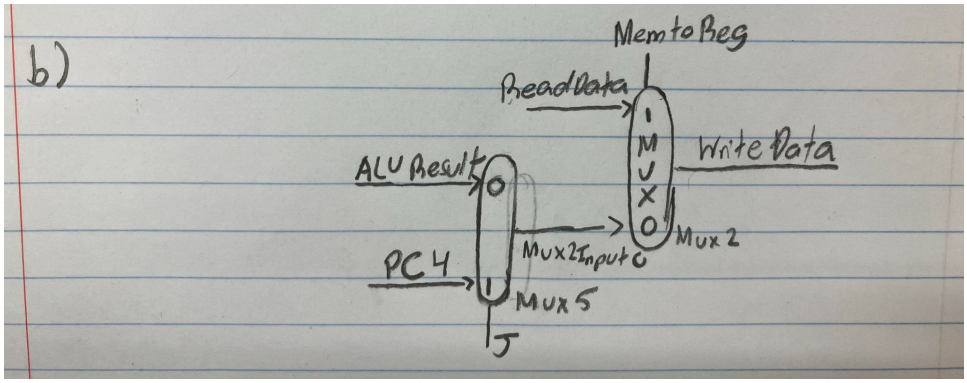
Are these changes correct?

In summary, the changes to PC and the register file are correct but data memory is mistakenly changed as explained above.

3)



The target address for JAL is computed by the addition of PC and the immediate from immGen while the target address for JALR is computed by the addition of ReadData1 and the immediate. The select signal of MUX4 is generated through the signal of JR from the control module. If JR is 1 ReadData1 will be passed through, however if JR is 0 PC will pass through.



In order to generate the select signal of the newly added MUX it must come from the J signal of the control module. If the instruction is either JAL or JALR, J will be 1 thus PC4 will be passed through as that is the data that should be written, otherwise ALUResult will be passed through.

c)

Inst.	ALUSrC	MemtoReg	RegWrite	MemRead	MemWrite	Branch	J	JR
Jal	X	0	1	0	0	0	1	0
Jalr	X	0	1	0	0	0	1	1