

SYNCRO locking platform



HRT Specification

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Device Protocol Specification

SYNCRO-BSM-66-1.1.1.148

Introduction

This document defines the specification for the protocol used for the serial communication with a Menlo Systems GmbH SYNCRO locking platform. The first part of the document describes the general concepts of message transmission over a serial bus as is common to a variety of Menlo Systems GmbH products.

The second part describes the register based remote control and readout of the SYNCRO locking platform.

Scope

This document describes the hierarchical register tree (HRT) implemented in the SYNCRO firmware.

The HRT layout described here reflects firmware version 1.1.1.148, compile-target SYNCRO-BSM-66.

For other devices or firmware versions, please contact Menlo Systems GmbH for relevant documentation.

This document extends the *Protocol Specification RBP w/ HRT version 2.1.0* provided by Menlo Systems GmbH with device specific information. Please note that throughout this document, knowledge of the RBP specification is presumed.

Note: This document uses the short-hex-notation for all register paths: A sequence of bytes is printed as a 2-digit hex representation of each byte, delimited by colons, e.g. 01:8A:7F

In many occasions, a sub-tree will occur multiple times, e.g. because of multiple units of the same kind of module installed in the system. In any case, the top-level node corresponding to a specific unit will be listed in section "*Toplevel registers*". The sub-registers however, will only be specified once for each kind of module. Their register path will start with "xx" as a wildcard for the respective top-level node. So, for top-level nodes "05", "06" and "07", the register for the motor position "xx:01" would be interpreted as "05:01", "06:01" and "07:01", respectively.

Note: RO registers can be read from at any time. If the specified register does not exist, the reply message will be NACK with the first register node index as argument.

Note: Writing to a RW register will result in changing the content of the respective register or trigger a state change of the related sub-device. Each write command is responded to by an ACK or NACK message that can be used solely for detection of protocol errors. To verify if the write command succeeded to change the register content or invoke a state change, the respective register needs to be monitored.

Document Version History

Issue	Date	Author	Annotations
01	2017-11-22	AT	First Issue

Hierarchical Register Tree – Register Description

Toplevel registers

Register	Address	Description			
LOCKBOX	01	Registers for main LOCKBOX unit			
TRACKER1	02	Registers for first TRACKER unit			
ACTUATOR1	05	Registers for first ACTUATOR unit			
ACTUATOR2	06	Registers for second ACTUATOR unit			
ACTUATOR3	07	Registers for third ACTUATOR unit			

Registers for LOCKBOX unit

Register	Address	R/W	Struct	Unit	Description
LOCKBOX	01				Registers for LOCKBOX unit
INPUT	xx:01	--	(node)		Registers for the input section
Enable modulation	xx:01:03	RW	U8	bool	Enable modulation of operating point Note: Should be 0 if no signal connected
CHANNEL 0 (F)	xx:01:04	--	(node)		Registers for input channel 1 (CH1)
Offset	xx:01:04:01	RW	S32	mV	Input offset [-1000 .. +1000]
Gain	xx:01:04:02	RW	S32		Gain (roughly 10e-3 dB) [-35000 .. +35000]
Attenuate -10 dB	xx:01:04:03	RW	U8	bool	Switch for additional attenuator
Invert	xx:01:04:04	RW	U8	bool	Switch for signal inverter
Raw Gain	xx:01:04:05	RW	S32	mV	VCA control voltage [0..2500]
CHANNEL 1 (H)	xx:01:05	--	(node)		Registers for input channel 2 (CH2)
Offset	xx:01:05:01	RW	S32	mV	Input offset [-1000 .. +1000]
Gain	xx:01:05:02	RW	S32		Gain (roughly 10e-3 dB) [-35000 .. +35000]
Attenuate -10 dB	xx:01:05:03	RW	U8	bool	Switch for additional attenuator
Invert	xx:01:05:04	RW	U8	bool	Switch for signal inverter
Raw Gain	xx:01:05:05	RW	S32	mV	VCA control voltage [0..2500]
FAULTDETECTION	xx:02	--	(node)		Registers for input signal integrity checks
AC Threshold	xx:02:01	RW	S32	mV	AC Peak detection threshold
DC Threshold	xx:02:02	RW	S32	mV	DC Window threshold
AC autodetect enable	xx:02:03	RW	U8	bool	Check AC threshold violations before engaging lock
AC autodetect threshold	xx:02:04	RW	U16		Maximum allowable violations per second
AC counter	xx:02:05	RO	U16		Actual violations per second
PID	xx:03	--	(node)		Registers for the PID controller section
On/Off	xx:03:01	RW	U8	bool	Enable loop control
Status	xx:03:02	RO	U8	enum	PID status (see below)
Last relock	xx:03:03	RO	S32	ms	Time since last relock
Lock mode	xx:03:04	RW	U8	enum	Loop controller operating mode 0: standard operating mode 1: (reserved) 2: automatic transition input channel C1 vs C2 Note: Mode 2 is only applicable for systems with two-stage-locking scheme.
Input Channel select	xx:03:05	RW	U8	enum	Select input channel for loop controller 0: input channel1 (C1) 1: input channel2 (C2)
Auto switch settle time	xx:03:06	RW	S32	ms	Time required to pass after relock at C1 before switching to C2 Note: Only applicable for operating mode 2
P	xx:03:07	--	(node)		Proportional branch
Enable	xx:03:07:01	RW	U8	bool	Enable proportional branch
Gain	xx:03:07:02	RW	S32		Gain of input channel (10-3 dB) [-35000 .. +35000]
Weight	xx:03:07:03	RW	U16		Scale [0..4095]
I	xx:03:08	--	(node)		Integrator branch
Enable	xx:03:08:01	RW	U8	bool	Enable integrator branch
Frequency	xx:03:08:02	RW	S32		Integrator cut-off frequency (Hz) [1..30000]
Weight	xx:03:08:03	RW	U16		Raw value for frequency finetuning [0..4095]
RC	xx:03:08:04	RW	U8		Selected frequency range [0..3]
D	xx:03:09	--	(node)		Differential branch

Enable	xx:03:09:01	RW	U8	bool	Enable differential branch
Frequency	xx:03:09:02	RW	S32		Differentiator cut-off frequency (Hz) [100,1'000,10'000,100'000]
Weight	xx:03:09:03	RW	U16		Raw value for frequency finetuning [0..4095]
RC	xx:03:09:04	RW	U8	enum	Selected frequency range [0..3]
OUTPUT	xx:04	--	(node)		Registers for the output section
Offset	xx:04:01	RW	S32	mV	Output offset [Limits.Low .. Limits.High]
Limits	xx:04:02	--	(node)		Output limiter
High	xx:04:02:01	RW	S32	mV	Maximum allowable output voltage Note: See user manual for valid range, invalid settings may damage external hardware!
Low	xx:04:02:02	RW	S32	mV	Minimum allowable output voltage Note: See user manual for valid range, invalid settings may damage external hardware!
Last high limit	xx:04:03	RO	S32	ms	Time since output voltage was last limited to maximum
Last low limit	xx:04:04	RO	S32	ms	Time since output voltage was last limited to minimum
Steering direct enable	xx:04:05	RW	U8	bool	Enable output steering Note: Should be 0 if no signal connected
Steering modulation enable	xx:04:06	RW	U8	bool	Enable output steering (inverted) Note: Should be 0 if no signal connected
Signal	xx:04:07	RW	S32		Signal
MONITOR	xx:05	--	(node)		Registers of the monitor section
Monitor channel	xx:05:01	RW	U8	enum	Enumerated state, connects signal to monitor jack: 0: Input channel CH1 before applying offset and gain 1: Input channel CH2 before applying offset and gain 2: PID controller input 3: Output monitor (after output limiter) Note: There may be residual offsets
ADC	xx:05:02	--	(node)		A/D conversion of signals Note: There may be residual offsets
F (post amp)	xx:05:02:01	RO	S32	µV	CH1 after applying offset and gain
H (post amp)	xx:05:02:02	RO	S32	µV	CH2 after applying offset and gain
PID input	xx:05:02:03	RO	S32	µV	PID controller input
PID output	xx:05:02:04	RO	S32	µV	PID controller output, before limiter

Registers for TRACKER units

Register	Address	R/W	Struct	Unit	Description
TRACKER#	02				Registers for TRACKER units
On/Off	xx:01	RW	U8	bool	Allow tracker operation
Min. relock time	xx:02	RW	S32	ms	Time required to pass after signal becomes valid before first correction attempt
Center value	xx:03	RW	S32	mV	Desired operating point
Max. deviation	xx:04	RW	S32	mV	Maximum allowable deviation from center without corrections
Direction invert	xx:05	RW	U8	bool	Actuator polarity 0: parallel action 1: anti-parallel action
Mode	xx:06	RW	U8		Tracker operation strategy 0: Move to center after exceeding max deviation 1: Move slightly to stay within max deviation
Step size	xx:07	RW	S32		Actuator steps per correction attempt
Step delay	xx:08	RW	S32	ms	Minimum time between correction attempts
Deviation	xx:09	RO	S32	mV	Actual deviation from operating point
ACTUATORID	xx:A0	RW	U8[4]	UID	Specifies the actuator to operate on
LOG	xx:AA	RO	TRKLOG		Four conveniently selected data channels for logging Note: May change or vanish in future versions

The tracker acts as a "very slow integrator" to the PID output; while the latter targets a relatively fast actuator with limited range of operation, the former uses a relatively slow actuator with rather large range of operation. In other words, both actuators influence the PID input signal in different orders of magnitude, and

while the PID controller is used to act fast on changes in the control loop, the tracker keeps the PID controller output in a valid range by compensating for large long-term drifts.

For more general use, the tracker can be configured to keep sensor values other than the lockbox output voltage centered to the specified value and choose an appropriate actuator to achieve this.

For details on available actuator and sensor IDs, see Appendix C.

Registers for ACTUATOR units

Register	Address	R/W	Struct	Unit	Description
ACTUATOR#	05				Registers for ACTUATOR units
Current position	xx:01	RW	S32	Steps	Absolute position of the stepper motor
Target position	xx:02	RW	S32	Steps	Absolute end position of the stepper motor
Move relative	xx:03	WO	S32	Steps	Relative amount of steps to move to new pos.
Resolution	xx:05	RW	U8	enum	Choose stepper motor micro-stepping 0: full steps 1: half steps 2: 1/4 steps 3: 1/8 steps 4: 1/16 steps 5: 1/32 steps Note: Wrong settings may damage hardware; see operating manual for details.
Speed	xx:06	RW	S32		Motor velocity [1..SPEEDLIM]

The MC3 module comprises 3 controller channels as described by the register definitions above. Note that each motor in the system must be connected to the respective output jack as specified in the system operating manual, or damage to the motor may occur.

Device registers

Register	Address	R/W	Struct	Unit	Description
DEV_addr	60	RW	U8		Device address
DEV_type	61	RO	U16		Device type
DEV	6A	--	(node)		
Addr	6A:01	RW	U8		Device address
Type	6A:02	RO	U16		Device type
Serial	6A:03	RW	SERS		Device serial number
saveset	6A:04	WO	U8		Trigger to save settings (calibration, etc.)
TStamp	6A:08	RO	TSTAMP		Current system time
ID	6A:0A	RO	Cstring		Firmware ID
Ver_HW	6A:0B	RW	VERS		Hardware version
Ver_FW	6A:0C	RO	VERS		Firmware version
Ver_DispFW	6A:0D	RO	VERS		Ver_DispFW
Uptime	6A:11	RO	TSTAMP		Time since last restart
Role	6A:30	RW	Cstring		Device role description
DEV_FILE	6B	--	(node)		File transfer
eDipShot	6B:01	RO	-		Download screenshot from the eDIP-display
eDip_FW	6B:02	WO	-		Upload firmware to the eDIP-display
REMOTE	6C	--	(node)		
Menue_eDip	6C:01	WO	U8		Menue_eDip
MODULES	6C:51	--	(node)		Installed modules
SLOT01	6C:51:01	--	(node)		Module information for slot 01
TYPE	6C:51:01:01	RW	U16		Module type ID
VERSION	6C:51:01:02	RW	VERS		Module hardware version
SERIAL	6C:51:01:03	RW	SERS		Module serial number
SLOT02	6C:51:02	--	(node)		Module information for slot 02
					Note: For sub-registers, see slot 01
SLOT03	6C:51:03	--	(node)		Module information for slot 03
					Note: For sub-registers, see slot 01
SLOT04	6C:51:04	--	(node)		Module information for slot 04
					Note: For sub-registers, see slot 01
SLOT05	6C:51:05	--	(node)		Module information for slot 05

					Note: For sub-registers, see slot 01
SLOT06	6C:51:06	--	(node)		Module information for slot 06 Note: For sub-registers, see slot 01
SLOT07	6C:51:07	--	(node)		Module information for slot 07 Note: For sub-registers, see slot 01
SLOT08	6C:51:08	--	(node)		Module information for slot 08 Note: For sub-registers, see slot 01
SLOT09	6C:51:09	--	(node)		Module information for slot 09 Note: For sub-registers, see slot 01
SLOT10	6C:51:0A	--	(node)		Module information for slot 10 Note: For sub-registers, see slot 01
SLOT11	6C:51:0B	--	(node)		Module information for slot 11 Note: For sub-registers, see slot 01
SLOT12	6C:51:0C	--	(node)		Module information for slot 12 Note: For sub-registers, see slot 01
SLOT13	6C:51:0D	--	(node)		Module information for slot 13 Note: For sub-registers, see slot 01
SLOT14	6C:51:0E	--	(node)		Module information for slot 14 Note: For sub-registers, see slot 01
Service mode	6C:FE	RW	U16		Write service code to enter service mode

HRT introspection registers

Register	Address	R/W	Struct	Unit	Description
RegFP	FC	RO	U16		Register subtree fingerprint
RegVers	FD	RO	U8[3]		HRT version
Subregs	FE	RO	U8[*]		List of sub-registers
RegDef	FF	RO	REGDEF		Register description

Appendix A: Protocol commands C-header file

```
#ifndef PROTOCOL_HEADER
#define PROTOCOL_HEADER

#define MENLO_DEVICE_TYPE_SMA1000      0x0100
#define MENLO_DEVICE_TYPE_THETA        0x0200
#define MENLO_DEVICE_TYPE_AC1550       0x0300
#define MENLO_DEVICE_TYPE_ORANGE_1     0x0400
#define MENLO_DEVICE_TYPE_ORANGE_A     0x0500
#define MENLO_DEVICE_TYPE_FIBERLINK    0x0600
#define MENLO_DEVICE_TYPE_LFC_REC      0x0700
#define MENLO_DEVICE_TYPE_SYNCRO       0x0800

#define PROTO_CMD_NACK                0x00
#define PROTO_CMD_CRCERR              0x01
#define PROTO_CMD_ACK                 0x03
#define PROTO_CMD_READ                0x04
#define PROTO_CMD_WRITE               0x05
#define PROTO_CMD_DATAGRAM            0x08
#define PROTO_CMD_ECHO                0x09
#define PROTO_CMD_REPLY               0x10

#define PROTERR_NOERROR               0x00
#define PROTERR_BUFFER_OVERFLOW        0x01
#define PROTERR_NOT_WITABLE            0x02
#define PROTERR_ARGSIZE_LOW             0x03
#define PROTERR_ARGSIZE_HIGH            0x04
#define PROTERR_INTERNAL_ERROR         0x05
#define PROTERR_AUTHORIZATION_REQUIRED 0x06

#endif
```

Appendix B: Register type definition C-header file

```
#define REGDEF_NONE          0x01
#define REGDEF_NODE           0x02
#define REGDEF_REGVERS         0x03
#define REGDEF_SUBREGS         0x04
#define REGDEF_REGDEF          0x05
#define REGDEF_ADDRESS         0x07
#define REGDEF_TYPE            0x08
#define REGDEF_SER             0x09
#define REGDEF_REMOTE_SERVICEMODE 0x0A
#define REGDEF_RTCTIME         0x0B
#define REGDEF_RTCDATE         0x0C
#define REGDEF_TSTAMP          0x0D
#define REGDEF_DEVID           0x0F
#define REGDEF_VERS             0x10
#define REGDEF_EDIP_BMP         0x20
#define REGDEF_EDIP_FW          0x21
#define REGDEF_REMOTE_EDIP      0x30
#define REGDEF_REMOTE_AMP        0x31
#define REGDEF_REMOTE_SEED      0x32
#define REGDEF_REMOTE_SPI        0x33
#define REGDEF_SAVESETTINGS     0x50
#define REGDEF_ISET             0x51
#define REGDEF_CALIB_DAC        0x52
#define REGDEF_CALIB_ADC        0x53
#define REGDEF_mV               0x54
#define REGDEF_enum              0x55
#define REGDEF_binary            0x56
#define REGDEF_ms                0x57
#define REGDEF_N                 0x58
#define REGDEF_mC                0x59
#define REGDEF_uC                0x5a
```

Appendix C: Actuator IDs

Actuator IDs are written as LOCATION.DEVICE.ASPECT.SUBDEVICE:

- LOCATION is always 0 for the local unit; in the future, any other value may refer to remote units
- DEVICE is the type of actuator device, for a list see below
- ASPECT is 0 in most cases
- SUBDEVICE denotes a specific channel within DEVICE

Actuator ID	Subdevice	Description
0.0.0.*		MC3 Motor drive
	0.0.0.0	MOTOR1 on first MC3 unit
	0.0.0.1	MOTOR2 on first MC3 unit
	0.0.0.2	MOTOR3 on first MC3 unit
	0.0.0.16	MOTOR1 on second MC3 unit
0.1.0.x		Lockbox DAC channels
	0.1.0.0	LB_CHANNEL_LOCK
	0.1.0.1	LB_CHANNEL_LLIM
	0.1.0.2	LB_CHANNEL_HLIM
	0.1.0.3	LB_CHANNEL_PEDL
	0.1.0.4	LB_CHANNEL_PIDP
	0.1.0.5	LB_CHANNEL_PIDI
	0.1.0.6	LB_CHANNEL_PIDD
	0.1.0.7	LB_CHANNEL_OFFSET_F
	0.1.0.8	LB_CHANNEL_GAIN_F
	0.1.0.9	LB_CHANNEL_GAIN_H
	0.1.0.10	LB_CHANNEL_OFFSET_H
	0.1.0.11	LB_CHANNEL_PIDWIN
	0.1.0.12	LB_CHANNEL_PEDL_RANGED: Output offset
0.2.0.x		TEC controller channels
	0.2.0.0	Target temperature of first TEC controller in 10^{-3} °C
	0.2.0.1	Target temperature of second TEC controller in 10^{-3} °C
	0.2.0.2	Target temperature of third TEC controller in 10^{-3} °C
0.3.0.x		DAC channels
	0.3.0.0	First channel on first DAC card
	0.3.0.7	Last channel on first DAC card
	0.3.0.8	First channel on second DAC card
0.4.0.x		DUO channels
	0.4.0.0	MODDUO_CHANNEL_LIMIT_LO
	0.4.0.1	MODDUO_CHANNEL_LIMIT_HI
	0.4.0.2	MODDUO_CHANNEL_INPUT_OFFSET
	0.4.0.3	MODDUO_CHANNEL_OUTPUT_OFFSET

Appendix D: Module IDs

The module type IDs reported for each slot are as follows:

ID	Module type
0x0001	System FRAM
0x0010	MC3
0x0020	Lockbox
0x0030	TEC
0x0040	DAC
0x0050	ADC
0x0060	RFC
0x0070	OFD
0x0080	DXD
0x0090	FDT1G
0x00a0	DUO