PETER YEHL

OBJECTIVE

Seeking an internship that leverages embedded software development practices and offers opportunities for professional growth.

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EDUCATION

Iowa State University
Spring 2026

Bachelor of Science
Computer Engineering

GPA 3.6 / 4.0
Major GPA 3.7 / 4.0

SKILLS

- Java
- C
- GIT Version Control
- VHDL
- MATLAB
- React JS
- HTML
- Object-Oriented Programming
- Data Structures and Algorithms
- Database Management (MySQL)
- Embedded SW Development
- Backend Development
- LTspice
- Circuit Design/Analysis
- Arduino Development
- Forklift Certified

ACTIVITIES

- CS and Software Engineering Club
- Chip Forge
- IEEE
- Mountaineering and Climbing Club
- Blessed Birthdays - Leader
- Big Brothers Big Sisters

WORK EXPERIENCE

Engineering Intern — Ames, IA
City of Ames — 2024

- Prepared CAD and GIS documentation for infrastructure projects in order to optimize the planning and execution phases
- Developed and maintained project records, “as-built” drawings, and progress payments
- Performed surveying and GPS marking using GNSS equipment
- Utilized Moasure software to measure and calculate quantities through a system of data collection and analysis

Engineering Intern — Bloomington, IL
City of Bloomington — 2023

- Maintained continuous inspection protocols for risk mitigation and quality assurance in civil engineering projects
- Ensured compliance with city standards across all project phases
- Conducted thorough inspections on various types of pavement and installation

PROJECTS

Riff Radar | Java

- Developed a mobile application connecting music fans with bands, utilizing Android Studio, IntelliJ, and Spring Boot
- Integrated Ticketmaster, Google Maps, and Spotify APIs
- Utilized Maven for build automation and MySQL for database management
- Managed code with Git and GitLab; documented with Swagger

iRobot | C

- Simulated a hospital delivery robot using manual navigation through a websocket-rooted GUI
- Utilized an ARM Cortex M4 microcontroller to conduct bit field manipulation through datasheet analysis
- Deployed UART, ADC, interrupt, memory mapping, and PWM techniques

Stereo Amplifier | LTspice

- Designed and constructed a stereo amplifier leveraging operational amplifiers and bandpass filters
- Tested and analyzed frequency components in relation to phase and magnitude characteristics using oscilloscope hardware