Graphics SIG Meeting
Oct 14, 2021
10:05am PDT

https://github.com/riscv-admin/graphics

@risc_v

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Collaborative & Welcoming Community

RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. help@riscv.org

We as members, contributors, and leaders pledge to make participation in our community a **harassment-free experience for everyone**.

https://riscv.org/risc-v-international-community-code-of-conduct/

Conventions

- Unless it is a scheduled agenda topic, we don’t solve problems or detailed topics in most meetings unless specified in the agenda because we don’t often have enough time to do so and it is more efficient to do so offline and/or in email. We identify items and send folks off to do the work and come back with solutions or proposals.
- If some policy, org, extension, etc. can be doing things in a better way, help us make it better. Do not change or not abide by the item unillaterly. Instead let's work together to make it better.
- Please conduct meetings that accommodates the virtual and broad geographical nature of our teams. This includes meeting times, repeating questions before you answer, at appropriate times polling attendees, guide people to interact in a way that has attendees taking turns speaking, …
- Where appropriate and possible, meeting minutes will be added as speaker notes within the slides for the Agenda

Agenda

- Summary from previous session (2 min)
- Charter approval vote (5 min)
- Simulator discussion (15 min)
- Compiler tech discussion (15 min)
- Docker image (10 min)

Summary from previous session
Challenges beyond the RISC-V scope

Khronos conformance test suites (CTS) not testing shading cores in isolation

Lack of microbenchmarks for shading cores

Simulator

Compile SPIR-V (GLSL flavoured) to LLVM IR

Compiler

Simulator discussion

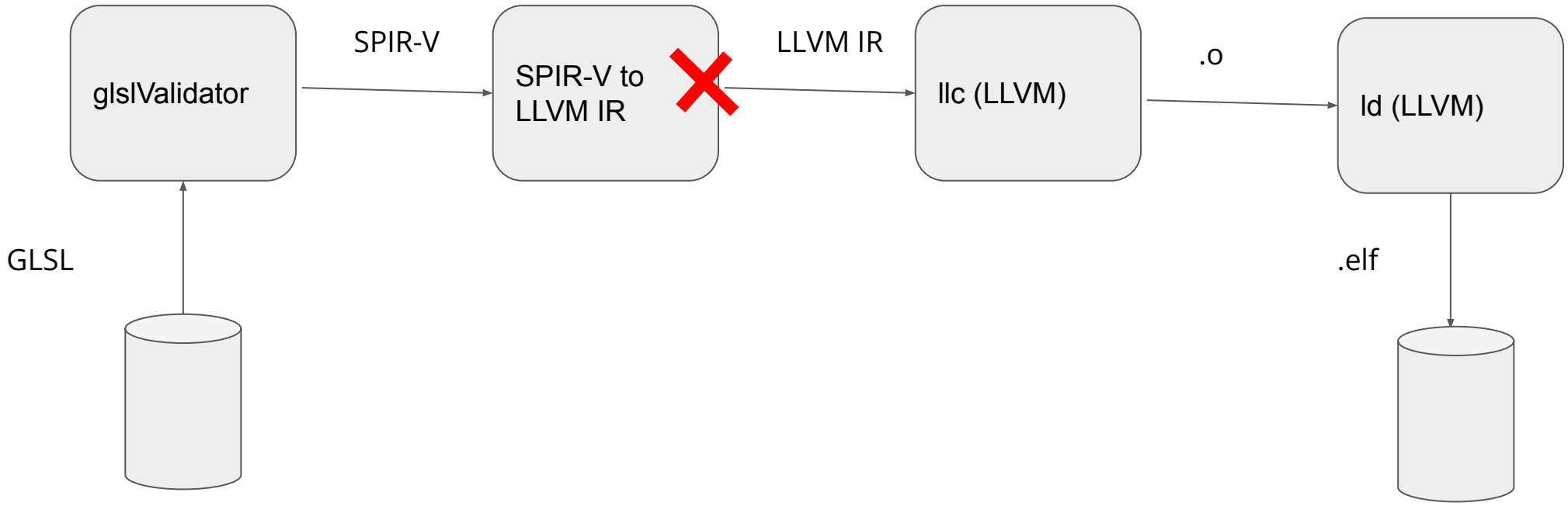
- libmesa built with offscreen rendering (rather than DRI)

(useful instructions on https://gist.github.com/mborgerson/6236caa80e0b920f5e99)

- gallium softpipe

- invoke a RISC-V simulator for issuing shader tasks

Compiler tech discussion



SPIRV to LLVM

What is available?

- https://github.com/KhronosGroup/SPIRV-LLVM-Translator
  - Industry Support
  - Tie into LLVM ecosystem
  - Vector support may require LLVM patches
- https://github.com/bradgrantham/alice5
  - Hobby project
  - Direct SPIRV to RISCV assembly
  - Less flexible, but more control
- Start from scratch?

Docker image

- Documentation of the development setup
- Reproducibility
- Time saving

Backup Slides