RISC-V®

Graphics SIG Meeting
Sept 2, 2021
10:05am PST

https://github.com/riscv-admin/graphics



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Collaborative & Welcoming Community

RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. help@riscv.org

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/risc-v-international-community-code-of-conduct/



Conventions



- Unless it is a scheduled agenda topic, we don't solve problems or detailed topics in most meetings unless specified in the agenda because we don't often have enough time to do so and it is more efficient to do so offline and/or in email. We identify items and send folks off to do the work and come back with solutions or proposals.
- If some policy, org, extension, etc. can be doing things in a better way, help us make it better. Do not change or not abide by the item unillaterly. Instead let's work together to make it better.
- Please conduct meetings that accommodates the virtual and broad geographical nature of our teams. This includes meeting times, repeating questions before you answer, at appropriate times polling attendees, guide people to interact in a way that has attendees taking turns speaking, ...
- Where appropriate and possible, meeting minutes will be added as speaker notes within the slides for the Agenda

Agenda



- Short introductions (10 min)
- Charter discussion (10 min)
- Vision (10 min)

Short introductions



- Ice breaker: chair and vice-chair start
- Next we proceed in lexicographical order

Preliminary charter



Focus on programmable shaders

Details on:

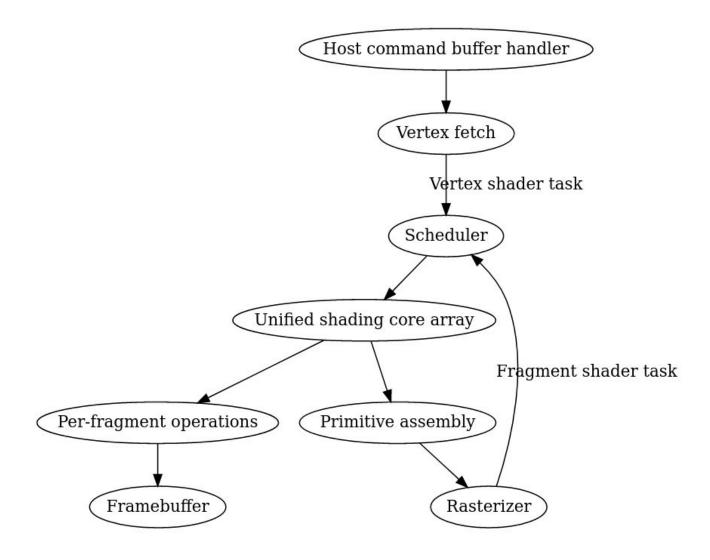
https://github.com/riscv-admin/graphics/blob/main/CHARTER.md

Survey:

- Is it general enough?
- Is it too prescriptive?
- Should explicitly mention GPGPU?
- Can we just live with it? Then say so!

Vision: RISC-V on unified shading cores





Unified shading core properties



- Input attributes and uniforms stored on a read-only registers
- Outputs stored on an write-only registers
- Temporary storage on an SRAM.
- Texture sampling support, but no other access to external memory

Backup Slides

