Assessing Performance Across Different SRAM Designs

Peter Proenca and William Hatfield

***Abstract*—The 6T SRAM is a well studied design and is commonly used for fast access memory. However, there are limitations to it due to sizing and the number of transistors used. Other designs such as 7T, 8T, 9T, and 10T exist, however they perform differently and require more physical space. We evaluate individual cell operation for all five cells and overall array operation for the 6T, 9T, and 10T cells to understand each design's benefits and drawbacks. We find that 7T, 8T, and 10T show significant improvement in the SNM-R. We also find that the 10T cell allows for a significant energy reduction relative to the 6T cell in a basic 8 by 8 array, while the 9T cell introduces additional bitline capacitance and peripheral complexity that results in increased energy consumption.**

***Index Terms*—SRAM, Array, Performance Evaluation, 6T SRAM, 7T SRAM, 8T SRAM, 9T SRAM, 10T SRAM**

I. Introduction

THE 6T SRAM cell is one of the most commonly used memory technology in fast-access memory today due to its low read and write latency as well as its simplicity and low area cost. However, the 6T cell suffers from potential issues such as read disturb and high power consumption. Other alternative SRAM cells with higher transistor counts have been introduced to potentially solve some of these issues. The higher T SRAM cells discussed in this paper include 7T, 8T, 9T and 10T designs, focused on designs intended to reduce energy consumption. Most of these designs use additional transistors to avoid read disturb issues by separating the read and write transistors, allowing for larger static noise margins as well as reduced leakage current. The larger static noise margins also allow these cells to operate at very low voltages, which reduces power consumption. We evaluate the read and hold SNM of all five designs. In addition, we use 8 by 8 arrays with each of the 6T, 9T and 10T cells to measure the maximum switching frequency and energy of the 6T, 9T, and 10T designs. All simulations were performed using Cadence Virtuoso with the 45 nm generic process design kit (GPDK).

II. Different SRAM Designs

A. 6T SRAM Cell

The 6T SRAM Cell referenced in Fig. 1 is the standard SRAM cell used in digital array designs. It takes in inputs from Word Line (WL), Bit Line (BL), and Bit Line Bar (BLB). The WL controls access to the cell and allows for a value to written to the two feedback inverters. When writing to the cell, WL is turned on and BL and BLB are driven with complementary values. When WL is disconnected, the cell will hold the value written to it. When reading, BL and BLB are precharged before WL turns on. Then, when WL turns on, BL and BLB will be driven such that the difference between BL and BLB can be differentiated at the Sense Amp.

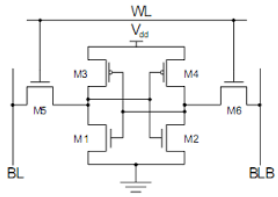

Fig. 1: 6T SRAM Cell Schematic

B. 7T SRAM Cell

The 7T SRAM Cell referenced in Fig. 2 is a modification to the 6T SRAM Cell with an additional NMOS transistor labeled as R2. Additionally, this design modifies the inputs and outputs slightly. This design takes in a Write Bit Line (WBL), Write Word Line (WWL), Read Word Line (RWL), and Read Bit Line (RBL). The WBL and WWL operate the same as Bit Line and Word Line in the 6T SRAM design for writing. However, when trying to read, only RBL must be precharged and RWL is turned high afterwards. As a result, this cell reduces power consumption as only BL needs to be pre charged. This design isolates writing and reading to separate Bit Lines and Word Lines which enables better writes and reads.

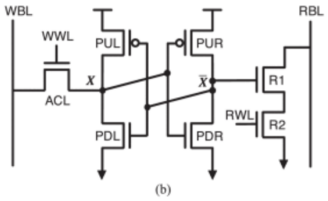

Fig. 2: 7T SRAM Cell Schematic

C. 8T SRAM Cell

The 8T SRAM Cell referenced in Fig. 3 is a modification to the 7T SRAM cell with an additional NMOS transistor which allows for a Write Bit Line Bar to exist. As a result, this design takes in an additional input of Write Bit Line Bar (WBLB) on top of the inputs that were discussed for the 7T SRAM. This allows for more robust writes to occur while also enabling

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low energy consumption by reducing precharge to only one bit line.

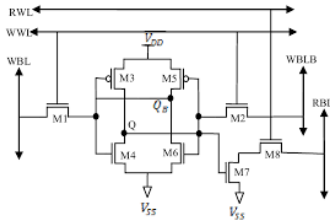

Fig. 3: 8T SRAM Cell Schematic

D. 9T SRAM Cell

The 9T SRAM Cell referenced in Fig. 4 is a modification of the original 6T SRAM Cell as it adds three NMOS transistors for reading from the cell. The added the N5, N6, and N7 transistors allow Bit Line (BL) and Bit Line Bar (BLB) to be written to when reading. However, this design uses BL and BLB for write and read which makes its overall schematic more similar to the 6T Cell. This design has Read Word Line (RWL) and Word Line (WL) as inputs and also BL and BLB.

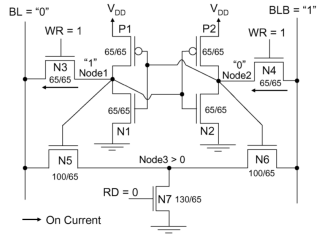

Fig. 4: 9T SRAM Cell Schematic

E. 10T SRAM Cell

The 10T SRAM Cell referenced in Fig. 5 is the most significant design compared to any of the other designs as it adds two additional PMOS transistors. This design has the same inputs as the 6T SRAM cell with a BL, BLB, and WL. However, Q is stored between PUL2 and PDL2 which is not stored and PGL does not have access to, which is significantly different compared to other designs. Additionally, the value QB turns on PDL1 which controls the value that is read when WL is high.

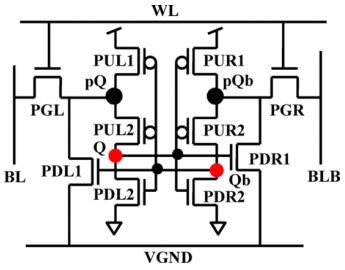

Fig. 5: 10T SRAM Cell Schematic

III. Static Noise Margin Evaluation

Static Noise Margins provide insight into the operation of SRAM cells. Specifically we will evaluate the Hold and Read Static Noise Margins to understand how these cell operate in static operation to see their response. The dc sweep from 0 to VDD allows designers to understand the potentially best VDD and sizing for a cell.

A. Static Noise Margin Test Setup

To test these various SRAM designs, we followed the designs for evaluating the Hold and Read Static Noise Margin as described in [6]. specifically for this design, all cells were kept min size and VDD was assumed to be 1.1V.

To test for Hold Static Noise Margins, WL is turned off so that the cell is isolated from BL and BLB. Then, Q or QB is driven with a vdc and the opposite QB or Q, respectively, is probed to see the output. The schematic can be seen in Fig. 24. V1 was assumed to be when Q was being Driven and V2 was assumed to be when QB was being driven. The result was then plotted with V1 on the x-axis and V2 on the y-axis. Additionally to measure the actual Hold SNM, we plotted the biggest square possible in-between the curves and measured the maximum side length of a square.

To test for Read Static Noise Margins, BL and BLB are driven at VDD while WL is high. This simulates as if BL and BLB were precharged to VDD and then Q and QB were driving BL and BLB. Similar to the Hold SNM, Q or QB were driven while QB or Q were probed. V1 was assumed to be when Q was being Driven and V2 was assumed to be when QB was being driven. The schematic can be seen in Fig. 25. The result was then plotted with V1 on the x-axis and V2 on the y-axis. Additionally to measure the actual Read SNM, we plotted the biggest square possible in-between the curves and measured the maximum side length of a square.

B. 6T Static Noise Margin

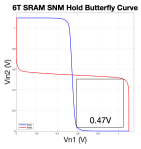

Fig. 6: 6T SRAM SNM Hold Butterfly Curve

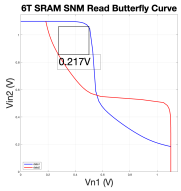

Fig. 7: 6T SRAM SNM Read Butterfly Curve

The 6T SRAM SNM reveal a lot of information about how the cell operates. In the Hold SNM, which is in Fig. 6, it shows a relatively stable SNM of 0.47V. At minimum size it demonstrates that there is relatively good hold SNM. For reading, which is in Fig. 7, the SNM was 0.217V. This leaves

a lot to be desired as it is very small and can be improved either through sizing or changing designs, as we will see in other designs.

C. 7T Static Noise Margin

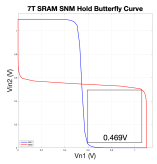

Fig. 8: 7T SRAM SNM Hold Butterfly Curve

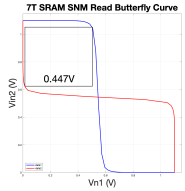

Fig. 9: 7T SRAM SNM Read Butterfly Curve

The 7T SRAM SNM maintains the same Hold SNM as the 6T cell while significantly improving Read SNM. The Hold SNM was 0.469V while the Read SNM improved from 0.217V to 0.447V. This can be attributed to the distinctive RWL and RBL that pull RBL to ground or maintain it at VDD. This design by just adding one additional NMOS provides improvements to the Read SNM. However, it adds additional array complexity because of RWL and RBL.

D. 8T Static Noise Margin

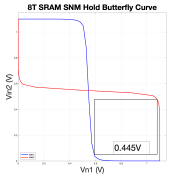

Fig. 10: 8T Read SNM

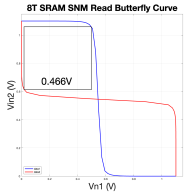

Fig. 11: 8T Hold SNM

Fig. 12: 8T SRAM SNM Read Butterfly Curve

The 8T SRAM SNM matches the 7T SRAM SNM almost identically. This can be attributed to their similarity in design for reading and holding. The 8T SRAM also has a RWL and RBL while not changing the two feedback inverters from the 6T and 7T SRAM. The Hold SNM was 0.445V as seen in Fig. 10 and the Read SNM was 0.446V as seen in Fig. 11.

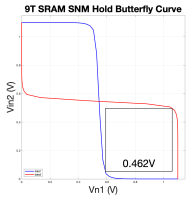

Fig. 13: 9T SRAM SNM Hold Butterfly Curve

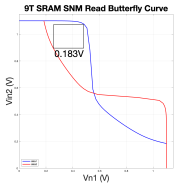

Fig. 14: 9T SRAM SNM Read Butterfly Curve

E. 9T Static Noise Margin

The 9T SRAM performs more similar to the 6T SRAM in the Read SNM. Since WL is turned high, the values driven to BL and BLB likely affected the stored Q and QB. These values were not isolated like the previous designs. The Hold SNM remained similar to other designs at 0.462V as seen in Fig. 13. The Read SNM degraded significantly to 0.183V as seen in Fig. 14

F. 10T Static Noise Margin

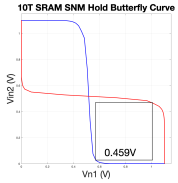

Fig. 15: 10T SRAM SNM Hold Butterfly Curve

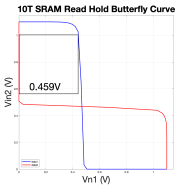

Fig. 16: 10T SRAM SNM Read Butterfly Curve

The 10T SRAM has the most stable Hold and Read SNM with both of them being 0.459V as seen in Fig. 15 and Fig. 16. This can be attributed to the isolated Q and QB as a result of the additional PMOS transistors. This design is the only design to add additional PMOS transistors and the stabilizing results at minimum size can be observed.

G. Discussion of Results

The comparison for the Static Noise margins can be seen in Table I. We observed that all of the Hold SNMs were similar to each other with a tight range from 0.445V to 0.470V. This is due to the similar design in storing Q and QB for all of the designs. The fundamental design of a SRAM cell has two

feedback inverters which ensures stable hold operations. Since none of the tested designs made changes to this, it is expected that the Hold SNM remained the same.

For the Read SNM, we found significant variance between the designs based on how the design interacted with the BLs for reading. The 9T SRAM cell had the worst Read SNM at 0.183V which is due to the lack isolation of Q and QB when reading. This is close to the 6T SRAM Read SNM at 0.217V. This is again likely due to the lack of isolation of the storage nodes and driving BL and BLB. However, the 7T and 8T designs have isolated RBLs which allow for robust reads with a Read SNM of 0.447V and 0.466V, respectively. The outlier of these designs is the 10T SRAM cell which takes in the same inputs as the 6T SRAM cell but has similar Hold and Read SNM. This is likely due to the isolated Q and QB and also the feedback loop having additional PMOS transistors. They help to ensure when reading, that Q and QB are isolated from BL and BLB and help ensure overall cell robustness.

Configuration	H-SNM (V)	R-SNM (V)
6T	0.470	0.217
7T	0.469	0.447
8T	0.445	0.466
9T	0.462	0.183
10T	0.459	0.459

TABLE I: Static Noise Margin (SNM) for Various Transistor Configurations

IV. 8x8 Array Design

We built arrays using 8 words of 8 bits to evaluate the 6T, 9T and 10T SRAM cells. The column mux ratio of the array is 1, so no additional peripherals are required to select between array columns. A 3-to-8 row decoder is used to select the row of the array, and a differential clocked sense amplifier is used to drive the signal stored on BL and BLB to the rails. These peripherals are used in all three memory arrays. The schematics for the peripherals can be found in the appendix in Figures 28 and 29. Both the 6T and 10T arrays operate the same way, using one WL and two bitlines, BL and BLB. Precharge is used for both reads and writes. The schematic for both the 6T and 10T arrays can be seen in Figure 26 in the appendix, as the schematic is the same outside of the type of SRAM cell used in the array. The clock signal controls the sense amplifier enable signal as well as the precharge enable signal. When clock is low, precharge is enabled and the PMOS pass transistors in the sense amplifier are on, while the NMOS enable transistor is off. When clock is high, precharge is turned off and sense amplifier enters the tracking phase, where the PMOS are turned off and the NMOS is turned on, so that signal driven on to the SA in the previous phase is driven to the rails. The schematic for the precharge circuit can be found in the appendix in Figure 30. Tristate buffers and inverters are used as the write drivers, with the enable signal being high if we are writing and low if we are reading. Precharge is used for both reads and writes to reduce array complexity. Although overall energy usage will increase for all three arrays, the relative energy usage should not change. The 9T array requires the use of a read WL and a write WL. A $1:2$ demultiplexer is used to select between the read and write WL based on if we are reading or writing. The schematic for the demultiplexer is shown in the appendix in Figure 31. The same enable signal used for the write drivers is used to select between the read and write WL. Due to V_T drop, buffers must be placed at the outputs of each of the pass gates, which adds further complexity to the array peripherals. Figure 27 in the appendix shows the schematic for the 9T array. Each array takes CLK, load, and the three row address bits as inputs, as well as data input for the 8 bits in the word being selected. The load signal is high for writes and low for reads.

V. 8x8 Array Simulation

A. Methods

1) V_{dd}: To measure the frequency and energy of the three SRAM arrays, we first must determine the voltage at which each array can operate. To measure the operating voltage of the array, we first write a test sequence to each column of the array and then read out the entire sequence. We perform a parametric simulation over a range of voltage values. The voltages for which the output matches the expected output are the ones at which the array can operate. The test case used were designed to ensure that the array could both hold and switch between 1s and 0s when cycling through words. The sequences used for the 6T 9T, and 10T arrays were 10100111, 00011010, and 11100101 respectively. These are the sequences of values being written to each SRAM column in the array. Since all bits in each row are written to in parallel, the word written to each row does not affect the voltage.

2) Frequency: To measure the maximum switching frequency, we need to test the case in which the output signal is most likely to deteriorate at increasing clock frequency. Writing alternating 1s and 0s to each SRAM in the each column tests the worst case, as switching between 1s and 0s requires the SRAM cells to repeatedly pull down and pull up the bitlines during reads. If the switching frequency becomes too fast, the SRAM cells will not be able to drive the signal on to the bitline during the clock phase, and the output will break down. Using a parametric simulation, we can determine the minimum clock period at which the array can operate. We first perform an initial sweep for periods from 1 to 10 ns, and then performed an additional sweep to determine the period more precisely. We then take the inverse to determine the maximum switching frequency.

3) Energy: To measure the energy usage of each SRAM array, we use a test case that we can use to compare the energy usage of each array. The case we used was writing and reading 0s to every cell in the array, then writing and reading half 1s and half 0s to the array, then writing and reading all 1s to the array. The entire test case takes 48 clock periods to complete, as it takes 16 clock periods to write and read from all cells in the array, which we do three times. We perform the test at the maximum switching frequency for each array. To calculate the energy usage during the test, we measure the current through the V_{dd} pin throughout the test, as the current from the inputs is negligible relative to the current through V_{dd}. We integrate the current for the total time of the test using the built-in

Cadence integration function to calculate the total charge, and multiply by V_{dd} to get the energy usage. Figure 17 shows the energy test case for the 6T SRAM. The test case is the same for the 9T and 10T arrays, with the only difference being that the arrays operate at their respective operating voltages and maximum switching frequencies. The test cases for the 9T and 10T arrays are shown in Figures 32 and 33 in the appendix.

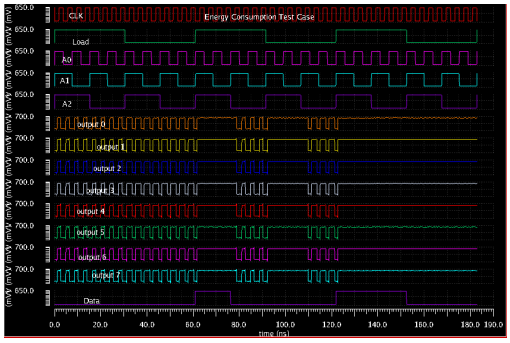

Fig. 17: Energy test case for the 6T SRAM array. The same test case was used for the 9T and 10T arrays at their respective maximum switching frequencies.

B. Results

1) 6T Array: We found that the 6T can operate at voltages of around 0.5 V or higher, although the array experiences significant delay for 0.52 V, so we used an operating voltage of 0.6 V for the array. Figure 18 shows the output of 1 of the SRAM columns after parametric analysis for voltage values between 0.4 V and 1.1 V. We can see that the sequence being written, 10100111, is read with no errors until 0.4 V, when the output no longer reflects the sequence being written. The figure also shows that the sequence is significantly delayed for an operating voltage of 0.52 V. The maximum switching frequency was found to be 262 MHz, corresponding to a period of 3.81 ns. Figure 19 shows the final parametric sweep of the array clock period, where we can see that the first period for which the array can reliably switch between 1s and 0s is 3.81 ns. The energy usage for the test case was calculated to be 2.56 pJ. The current measurement for the 6T array is included in Figure 34 in the appendix.

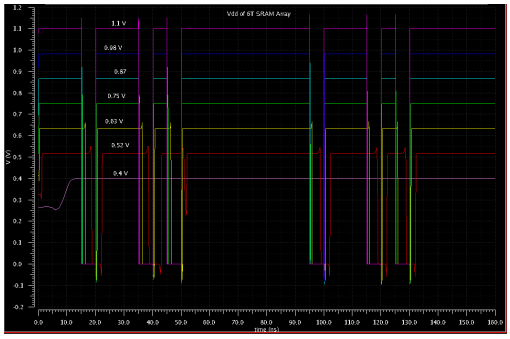

Fig. 18: Parametric V_{dd} analysis for 6T SRAM array.

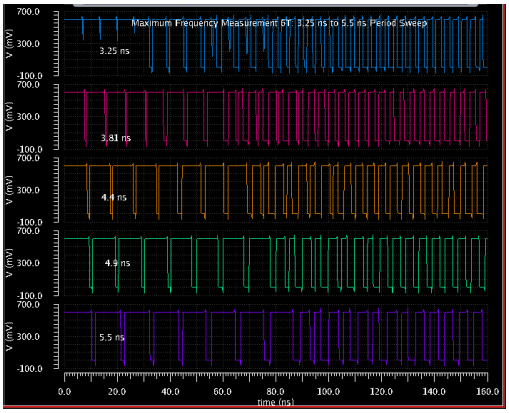

Fig. 19: Final parametric sweep of 6T array clock period from 3.25 ns to 5.5 ns. The output of a single column of the array is pictured.

2) 9T Array: The 9T SRAM array could only operate at voltages of 0.8 V or higher. As a result, we used an operating voltage of 0.8 V for the 9T array. Figure 20 shows the output of one SRAM column when the sequence 00011010 is written and read. We can see that the output deteriorates below values of 0.8 V. The maximum switching frequency was calculated to be 196 MHz, correspond to a period of 5.1 ns. Figure 21 shows the final parametric sweep of the array clock period, in which the first period for which the array operates correctly is 5.1 ns. The total energy usage during the test case was calculated at 31.9 pJ. The current measurement for the 9T array is included in Figure 35 in the appendix. The increased energy usage is likely due to the increased complexity of the 9T array in addition to the increased BL capacitance. As discussed above, the 9T array requires additional circuitry to select between the RWL and WWL, which results in increased power consumption. Another issue with the 9T SRAM cell is that the BL is connected to two transistors instead of one, which results in double the BL capacitance. As a result, double the amount of charge is needed for the BL to store a given voltage, which results in significantly higher energy consumption. A potential way to offset this problem is to decrease the number of words in the array, reducing the number of SRAM cells the BL is connected to.

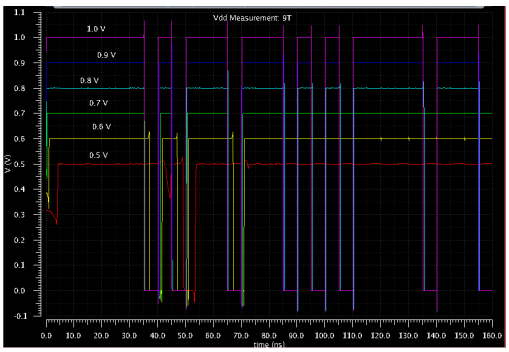

Fig. 20: Parametric V_{dd} analysis for 9T SRAM array.

3) 10T Array: We found that the 10T array could only operate at voltages of about 0.52 V. Figure 22 shows the

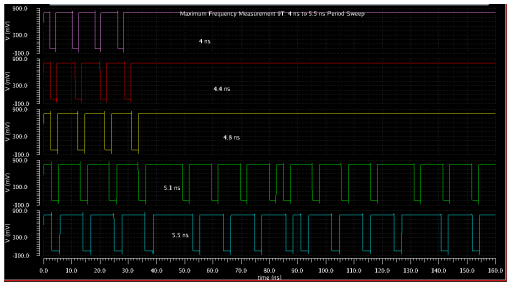

Fig. 21: Final parametric sweep of 9T array clock period from 3.25 ns to 5.5 ns. The output of a single column of the array is pictured.

ouput of one SRAM column in the array when the sequence 11100101 is written and read from the cells in the columns. We can see that the only operating voltage for which the array works properly is at 0.52 V, so the an operating voltage of 0.52 V was used. These results are in opposition to those discussed in [5], in which they find that the 10T cell can operate at voltages as low as 0.29 V. This difference is an indication that the basic 8 by 8 SRAM array is likely not enough to comprehensively test the SRAM cell. [5] uses a 16 Kb test chip with the UMC 90 nm process. In the context of a test chip that optimizes the array design to the benefits of the cell, the 10T SRAM performs significantly better. The maximum switching frequency was calculated to be 139 MHz, with a minimum period of 7.2 ns. Figure 23 shows the final parametric seep for the 10T array clock period, where we can see that the array begins to operate correctly at a period of 7.2 ns. The energy usage of the array was 1.51 pJ. The current measurement for the 10T array is included in Figure 36 in the appendix. Since the BL capacitance and peripheral circuitry is the same as for the 6T array, the 10T array uses less energy than the 6T array. The separation of read and write transistors in the cell allows for reduced energy consumption in the cell. Table II summarizes the results for all three arrays.

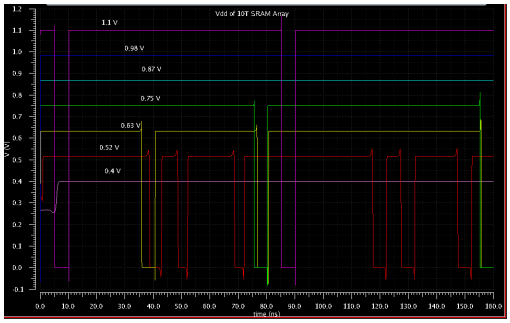

Fig. 22: Parametric V_{dd} analysis for 10T SRAM array.

VI. Conclusion

We saw a relatively similar SNM-H across all SRAM cells at minimum size, while the 7T, 8T, and 10T cells saw significantly increased SNM-R. The separate write and read WLs of the 7T and 8T transistors as well as the unique way of storing the bits in the 10T allow for significantly increased

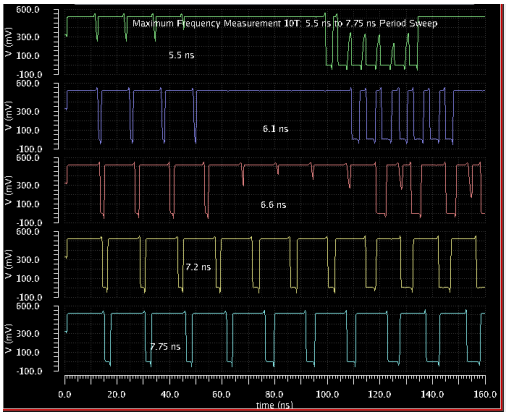

Fig. 23: Final parametric sweep of 10T array clock period from 5.5 ns to 7.75 ns. The output of a single column of the array is pictured.

read margin. We saw that the 10T SRAM array allowed for a significant reduction in energy usage from the 6T array, although the 6T could operate at a wider range of voltages and used significantly less area. The basic nature of the array used and its peripherals, as well as the process used for simulation could all be factors in the narrow range of operating voltages for the 10T design. The 9T array did not experience the same decrease in energy usage, demonstrating that further optimization is often required to see the benefits of certain designs. Potential optimizations such as less WLs and more BLs could reduce the BL capacitance and potentially reduce energy consumption. Different peripheral circuits could also help to experience the potential benefits of the 9T design.

SRAM Type	V_{dd} (V)	Frequency (MHz)	Energy (pJ)
6T Array	0.60	262	2.56
9T Array	0.80	196	31.9
10T Array	0.52	139	1.51

TABLE II: Table summary of SRAM array measurements.

APPENDIX

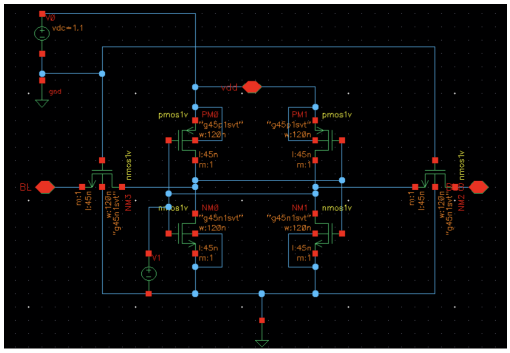

Fig. 24: Hold Static Noise Margin Schematic for the 6T SRAM

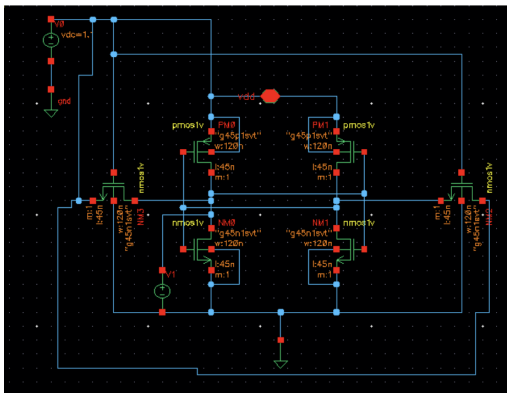

Fig. 25: Read Static Noise Margin Schematic for the 6T SRAM

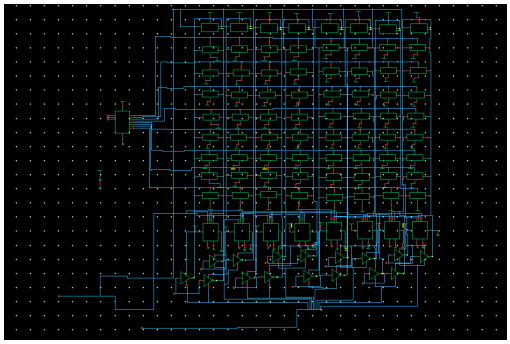

Fig. 26: Schematic for 6T SRAM array. The schematic for the 10T array is the same with the SRAM cells replaced, so it is not included.

ACKNOWLEDGMENT

Peter and William worked together on this project. Peter focused on overall SRAM design, building SRAM cells and SNM evaluation. William focused on array peripherals, building the entire array, and evaluating at various voltages and frequencies. They both assisted each other in understanding overall cell designs and understanding of operation.

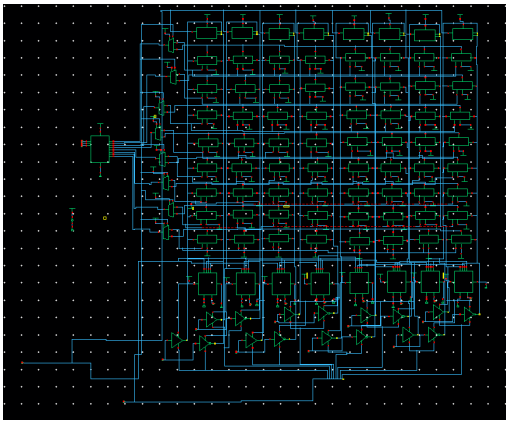

Fig. 27: Schematic for 9T SRAM array.

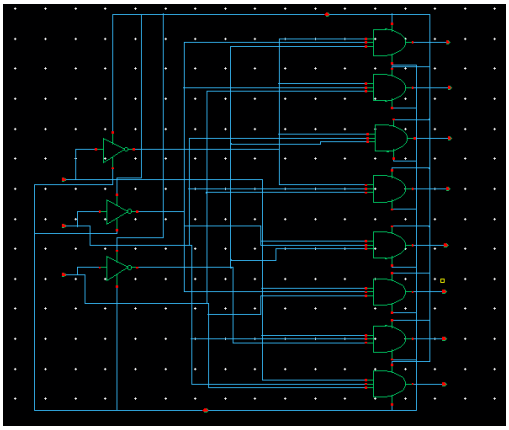

Fig. 28: 3-to-8 row decoder schematic.

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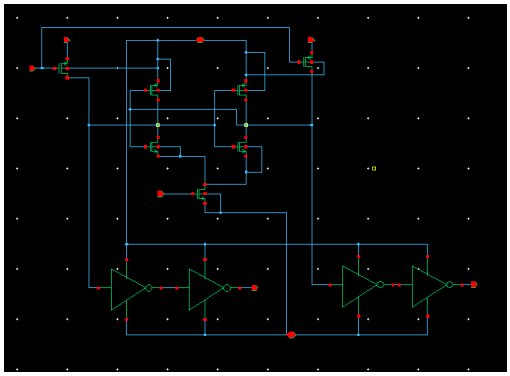

Fig. 29: Differential clocked sense amplifier schematic.

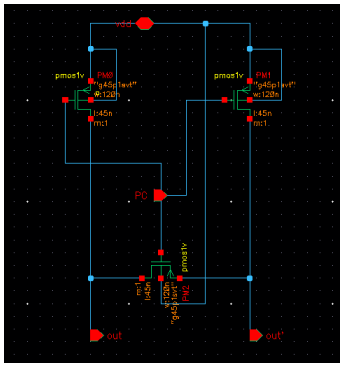

Fig. 30: Precharge schematic

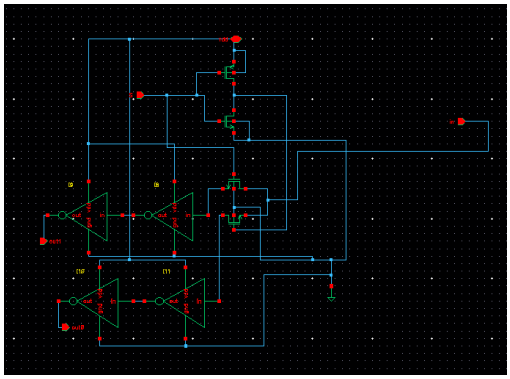

Fig. 31: Demultiplexer Schematic

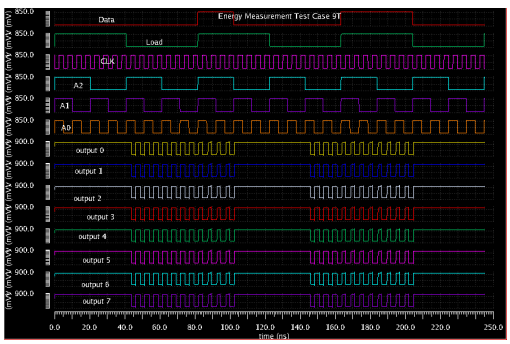

Fig. 32: Energy test case for the 9T SRAM array.

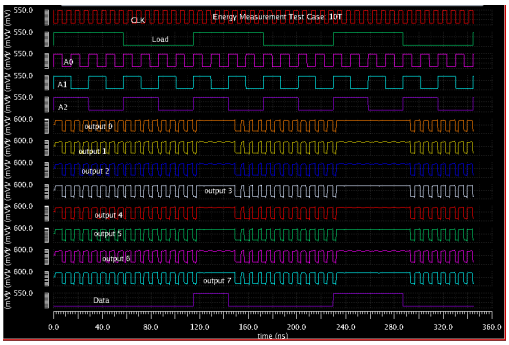

Fig. 33: Energy test case for the 10T SRAM array.

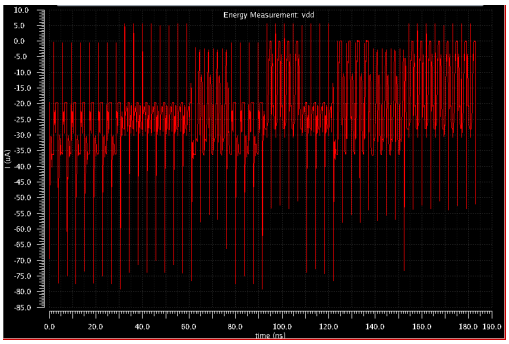

Fig. 34: Current measurement for 6T array.

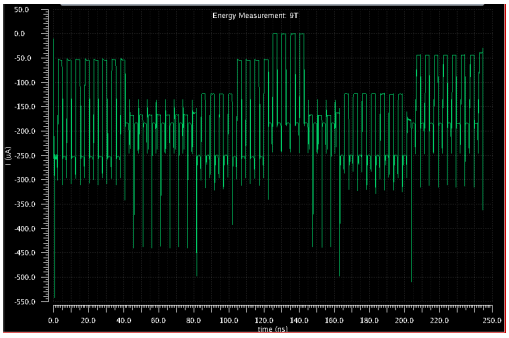

Fig. 35: Current measurement for 9T array.

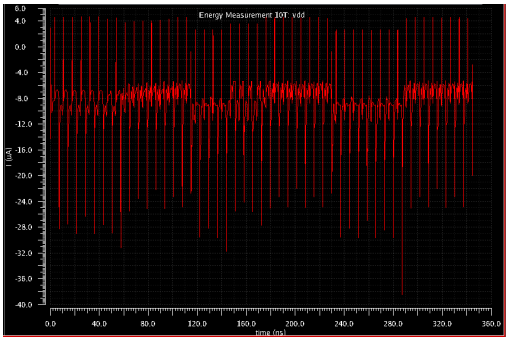

Fig. 36: Current measurement for 10T array.