



Evaluation of SRAM Designs

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All of the SRAMs

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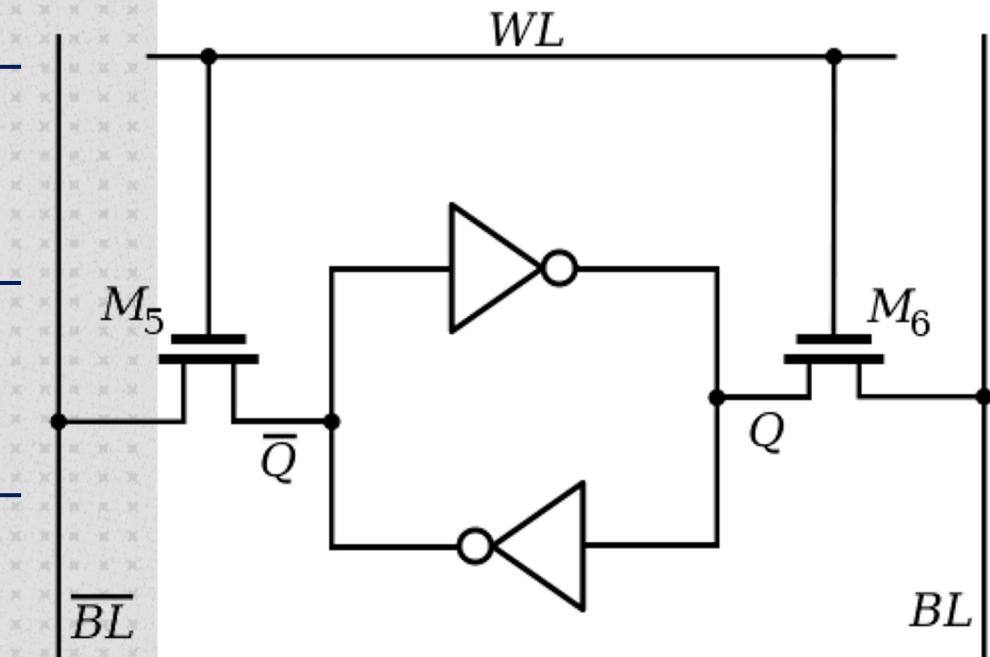
Operation Evaluation

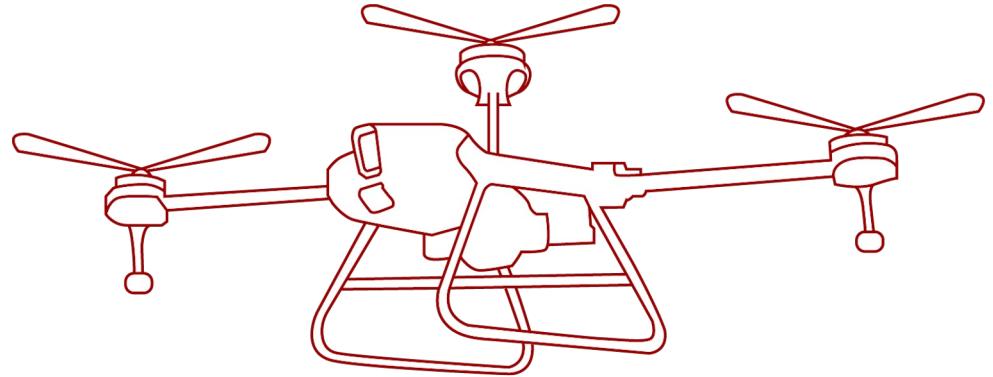
Evaluating SRAM array operation for 6T, 9T, and 10T designs

04

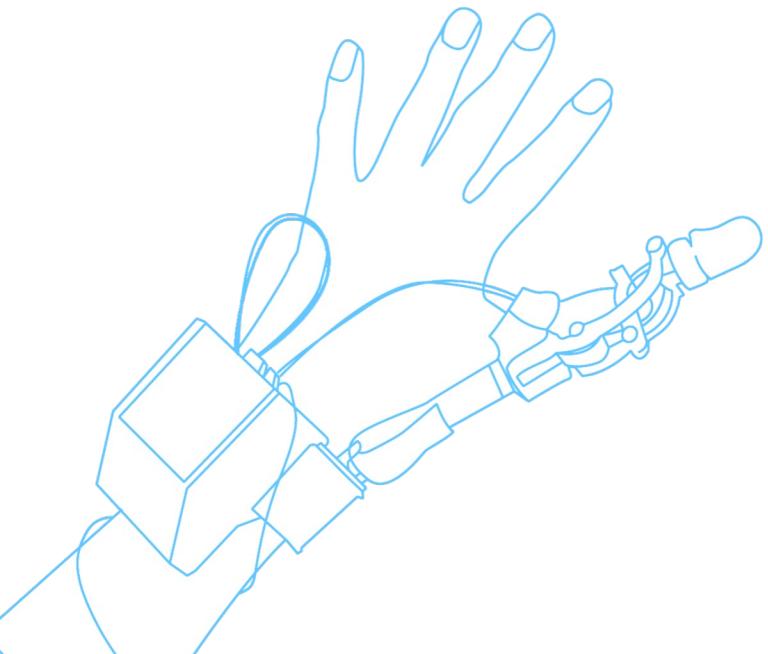
Conclusion

Takeaways from SRAM analysis



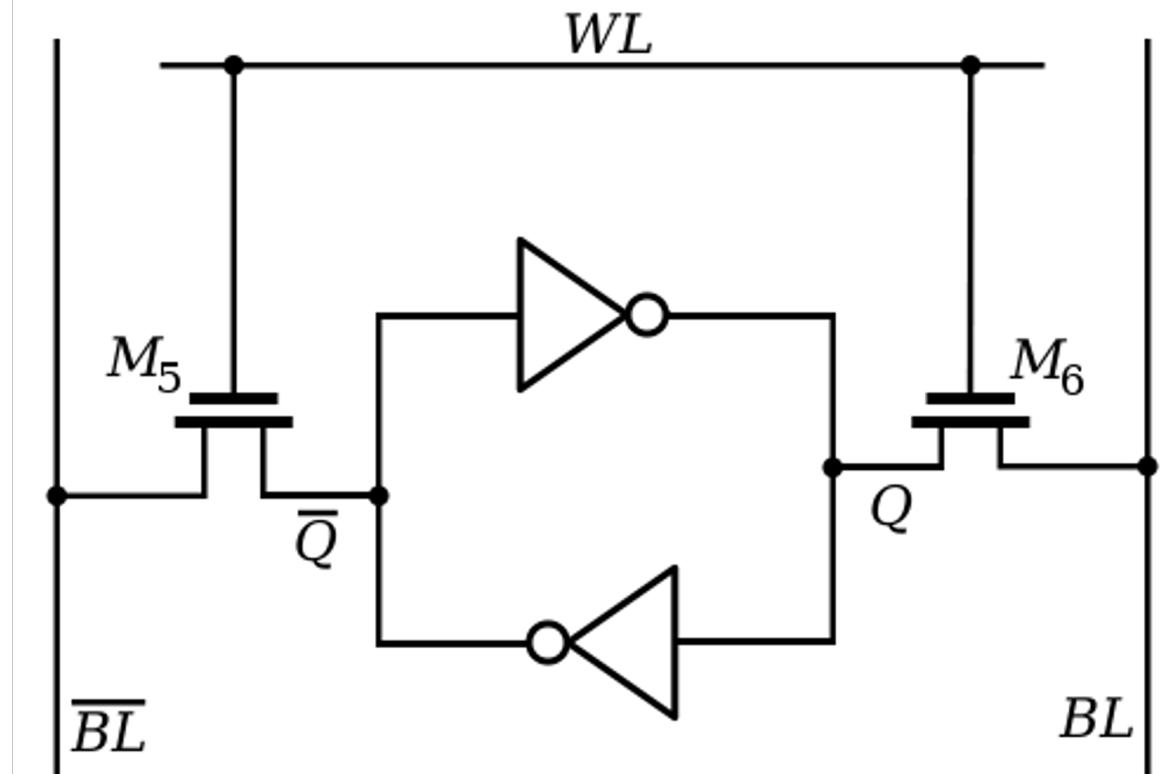


SRAM Variations

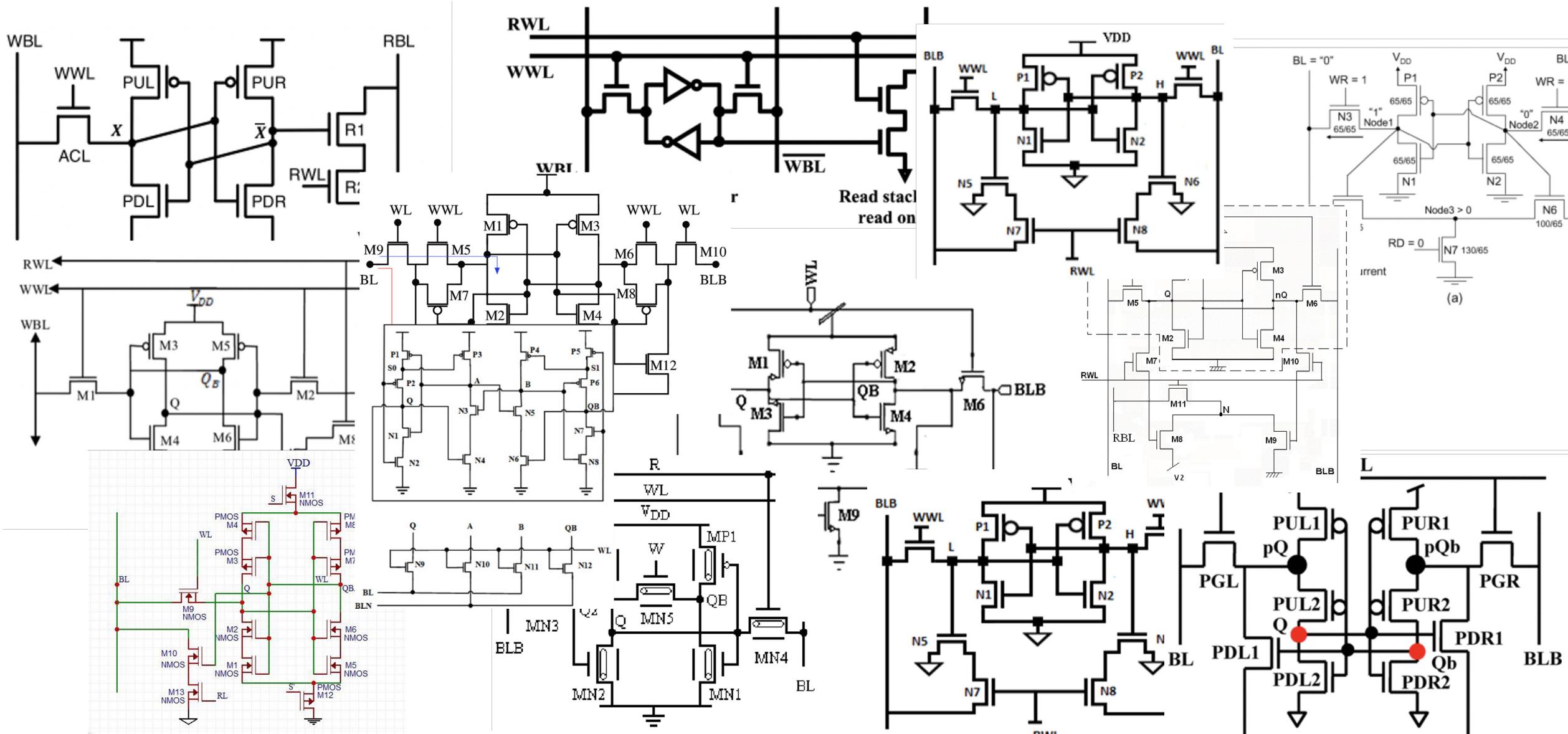


The Classic SRAM

- 6 Transistors
- Access with WL/BL

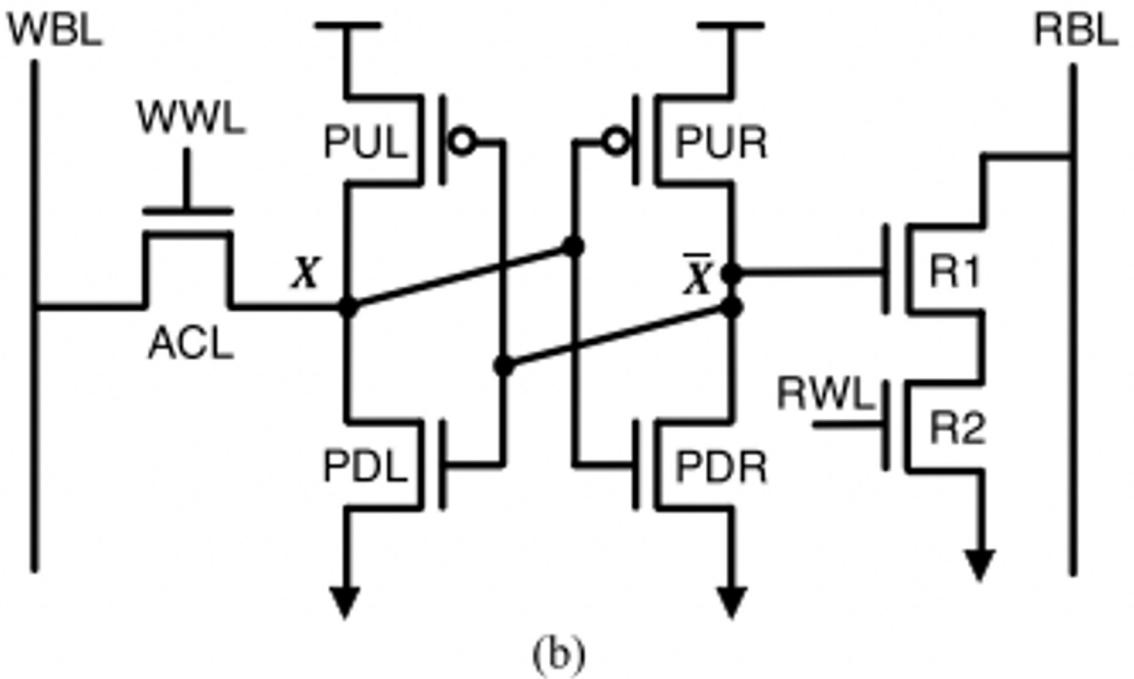


Other SRAMs



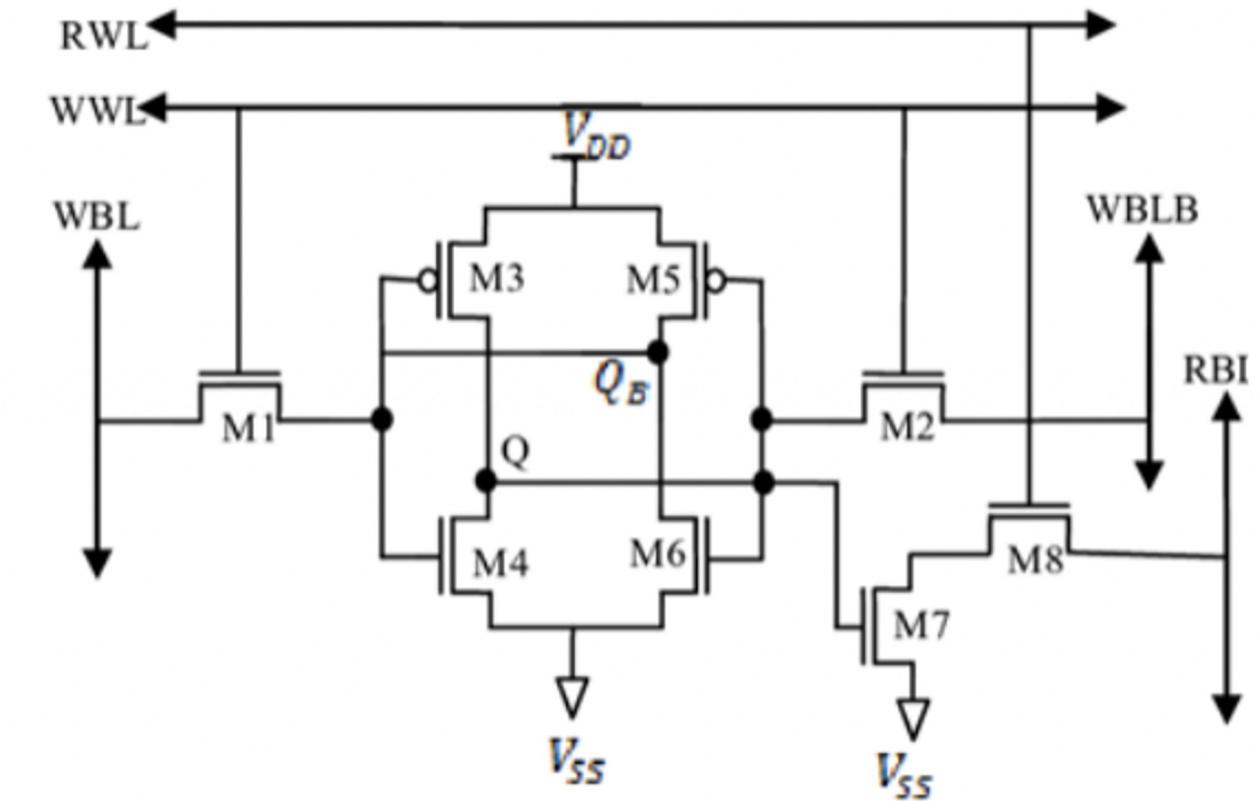
7T-SRAM

- 7 Transistors
- Write with WBL and WWL
- Read with RWL RBL



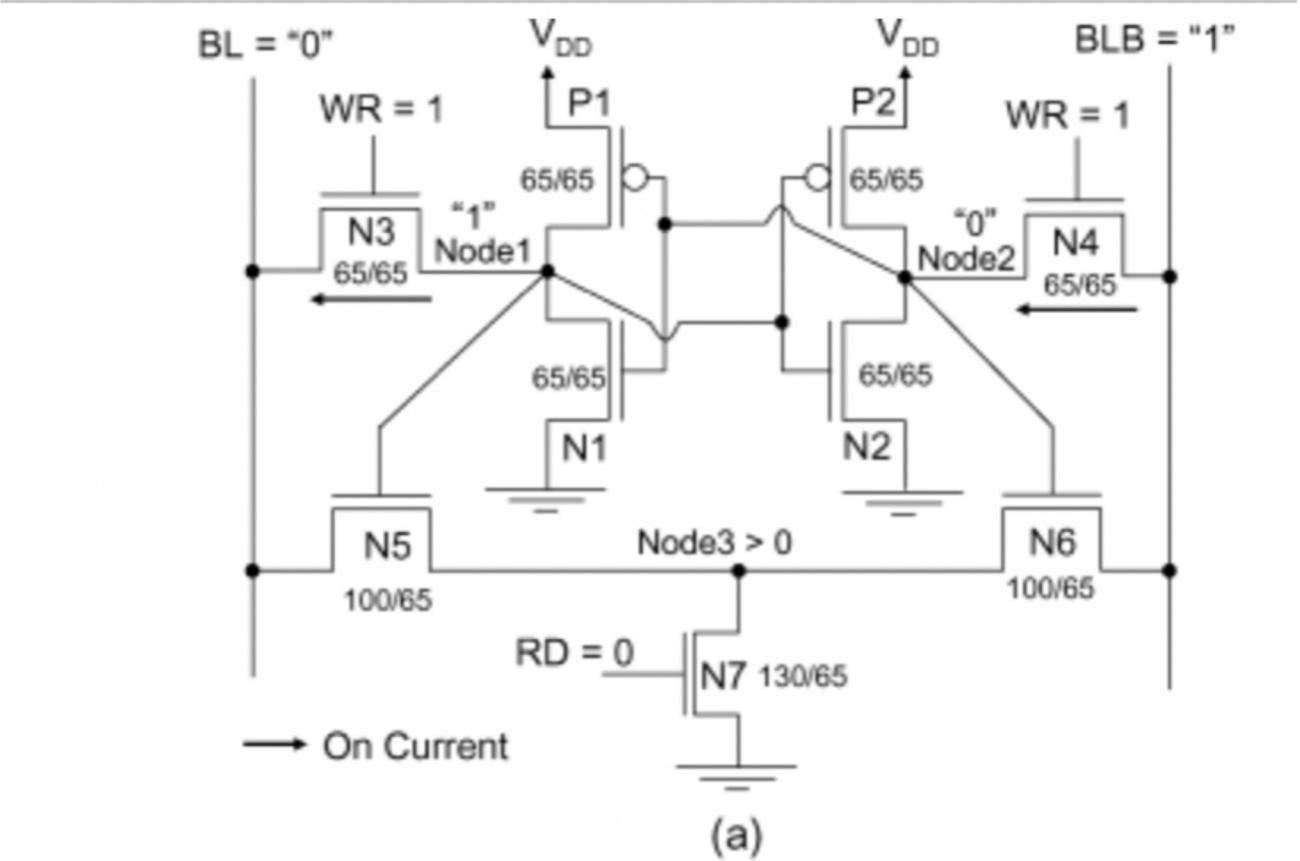
8T-SRAM

- 8 Transistors
- Write with WBL/WBLB and WWL
- Read with RWL RBI



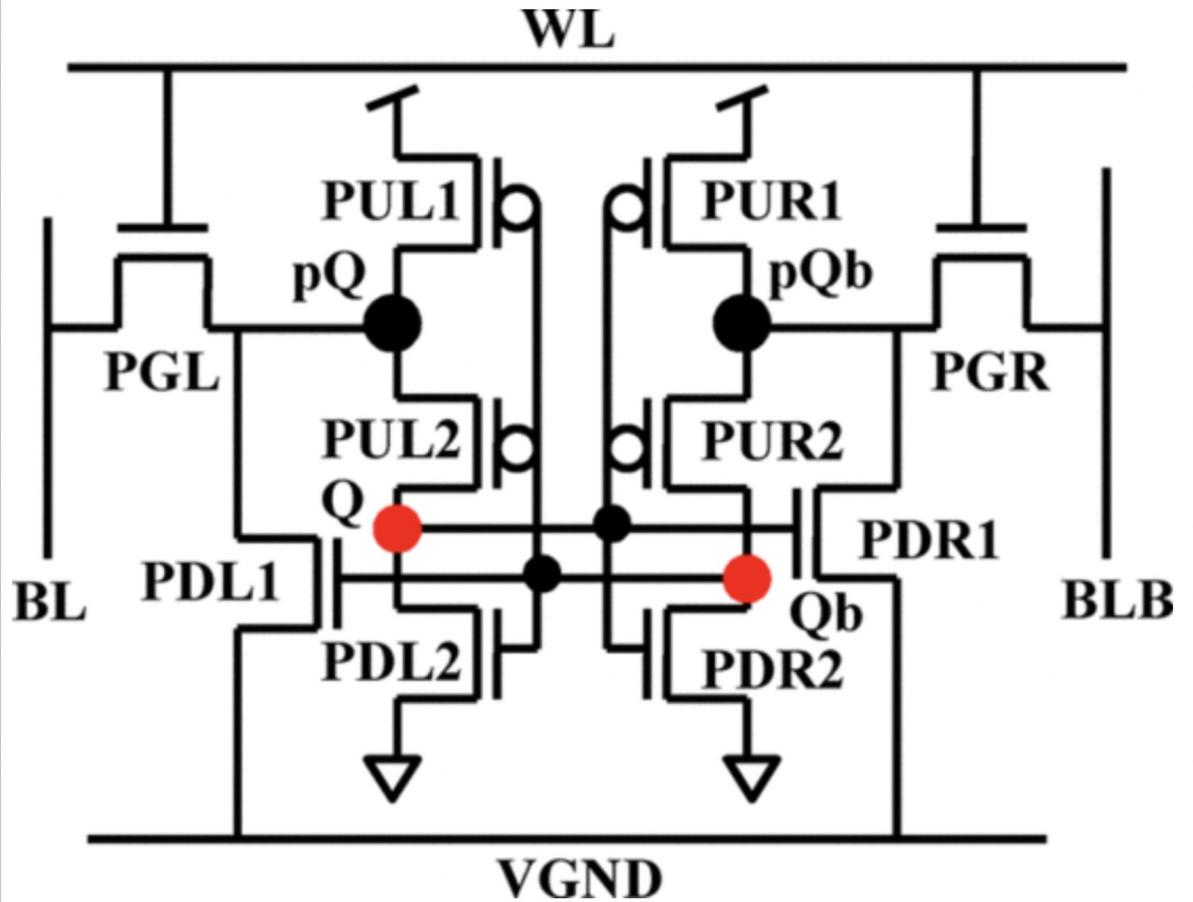
9T-SRAM

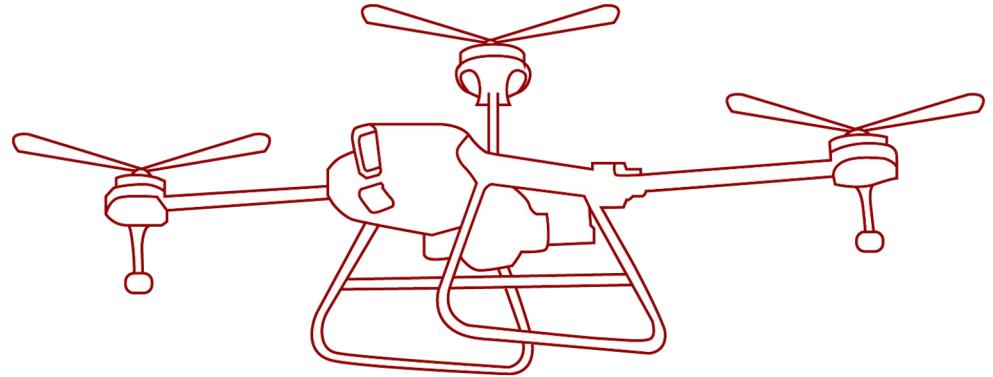
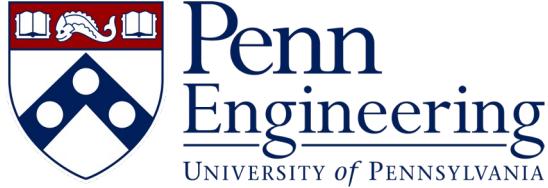
- 9 Transistors
- Access with WR/RD and BL/BLB
- Enables better read



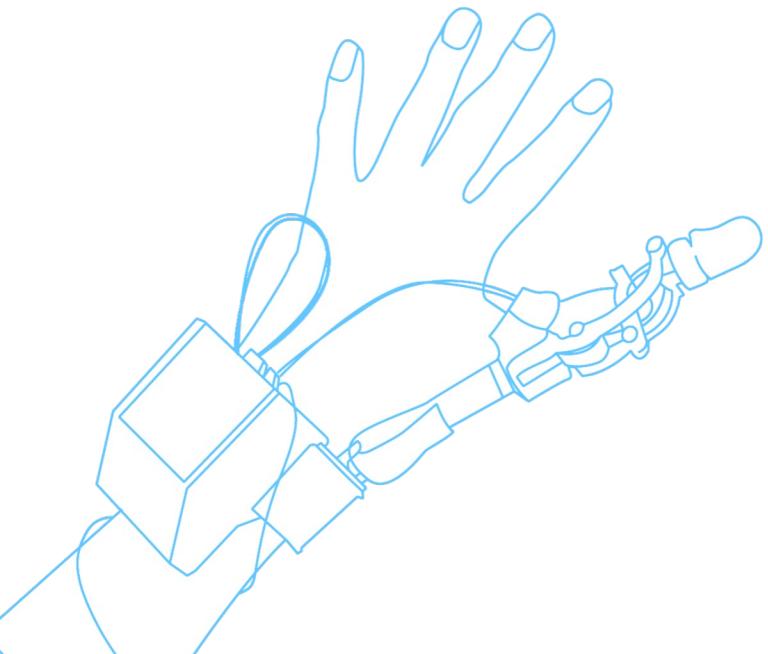
10T-SRAM

- 10 Transistors
- Access with BL/BLB and WL.
- Changes to where Q and Qb are stored

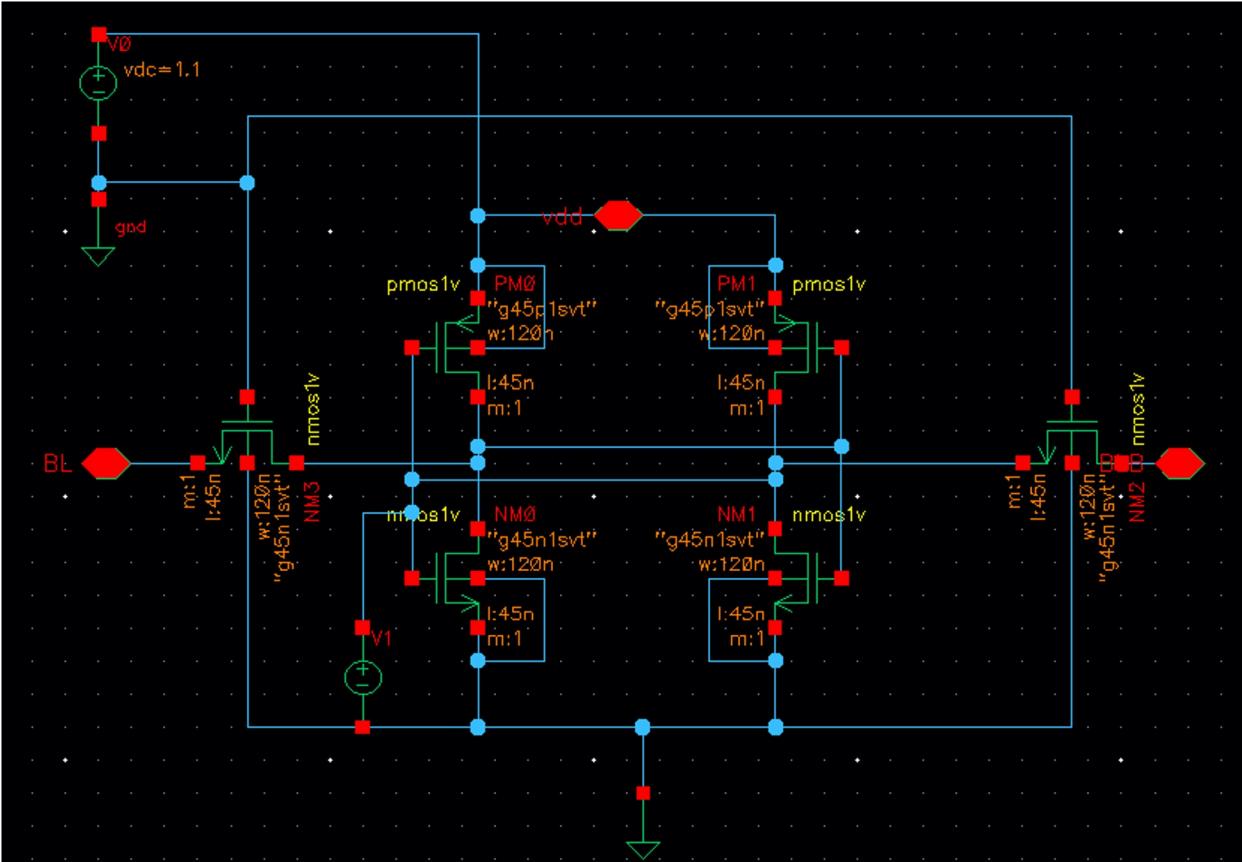




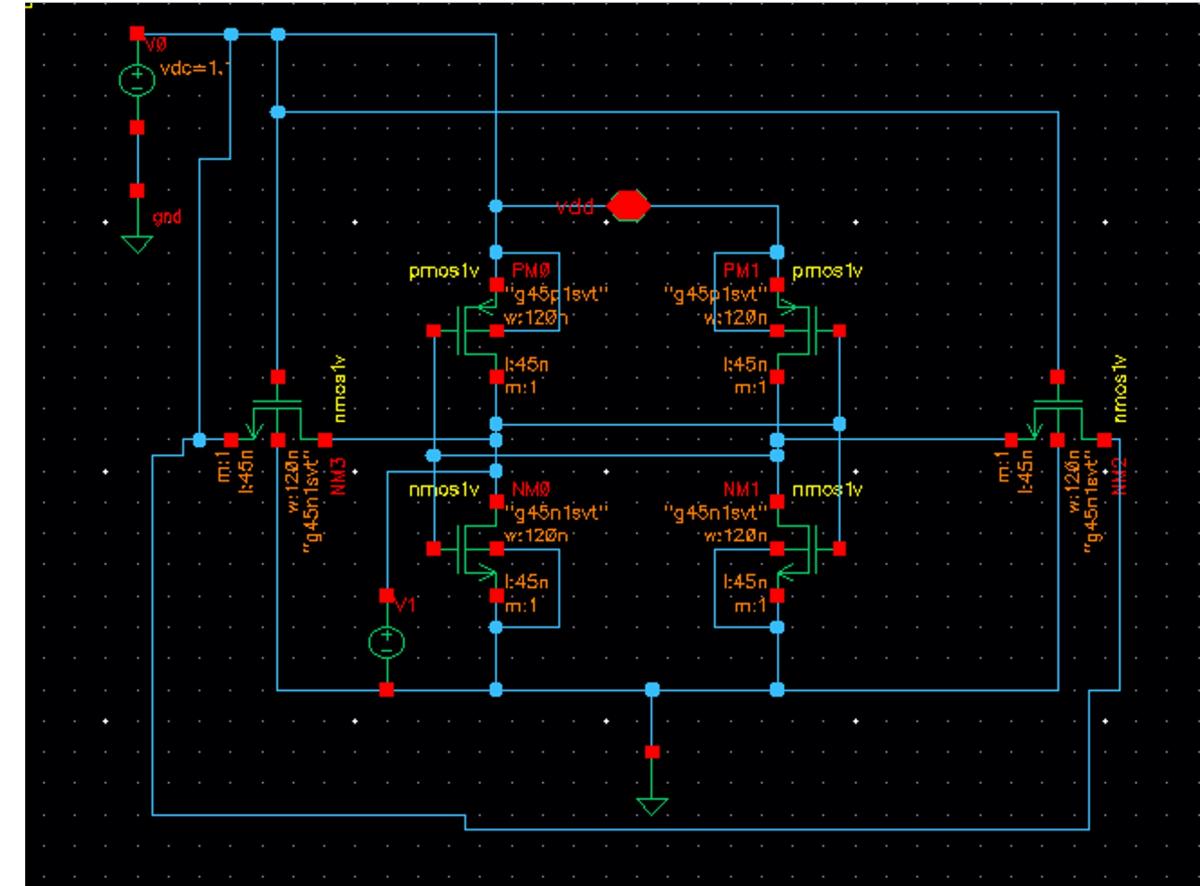
Static Noise Margins



Test Circuit - SNM

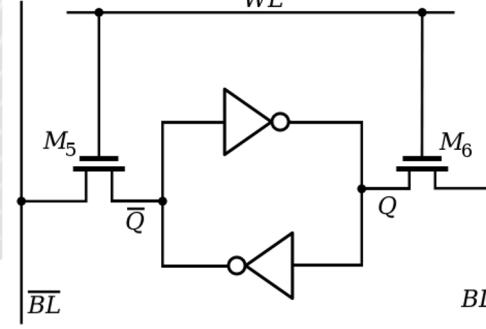


Hold SNM Test Circuit

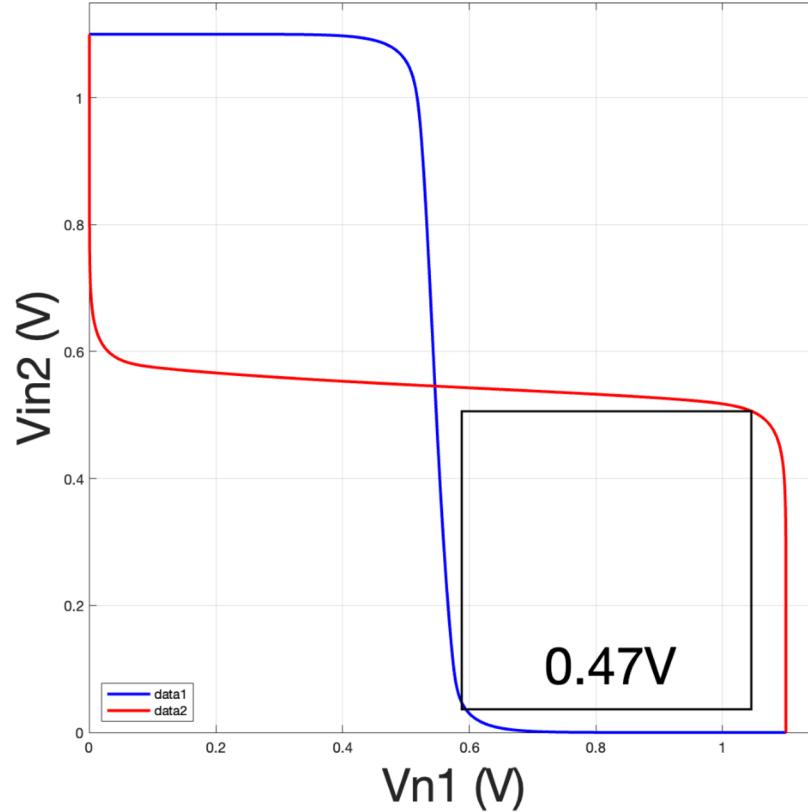


Read SNM Test Circuit

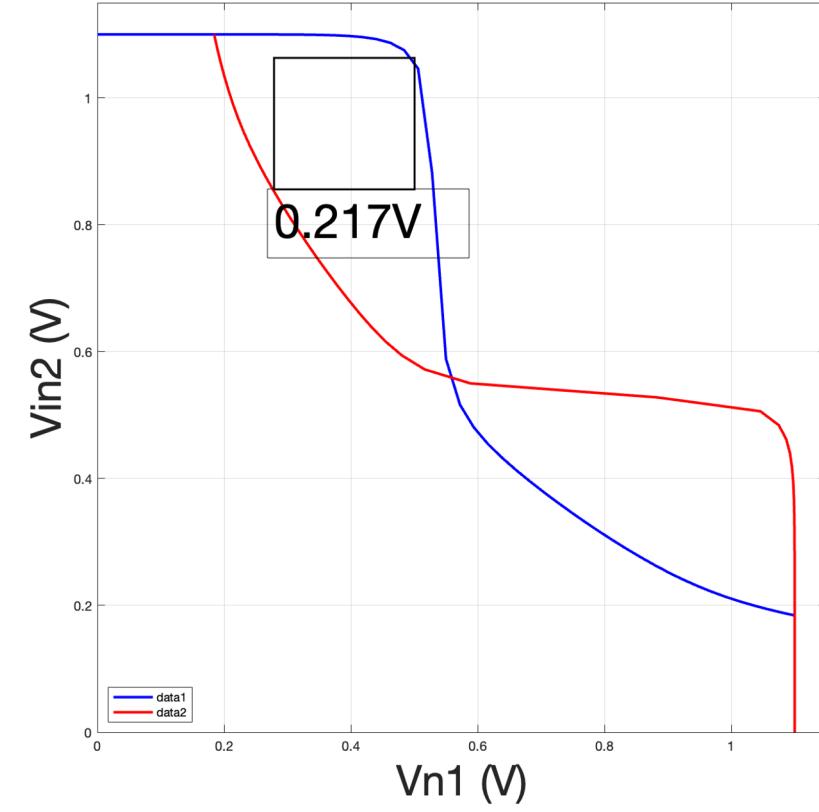
6T SNM



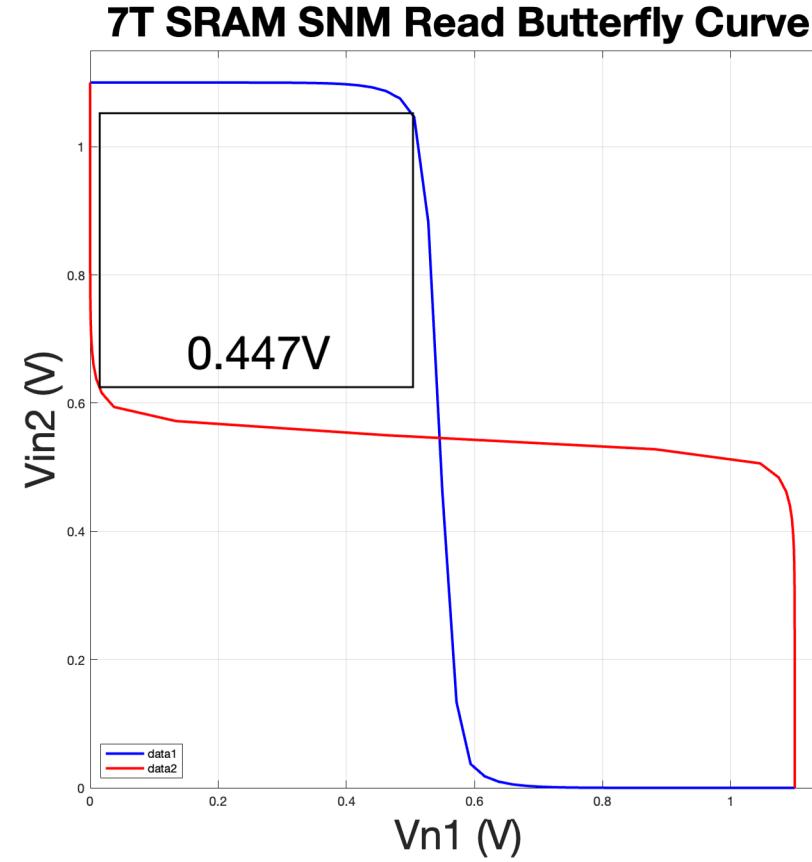
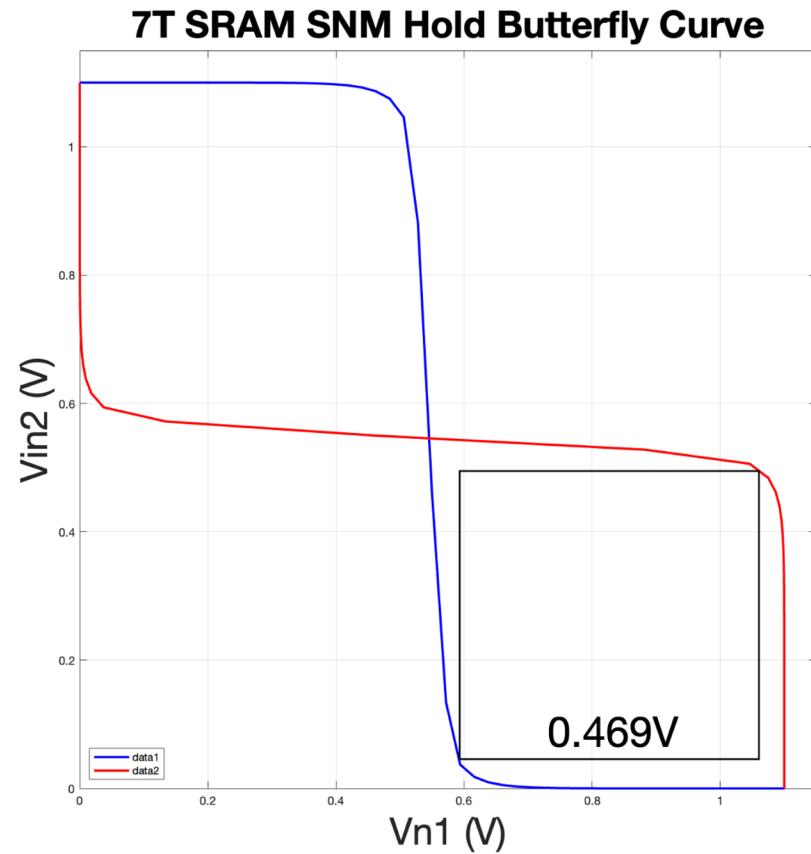
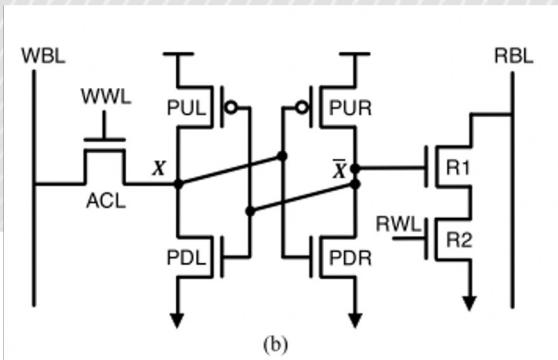
6T SRAM SNM Hold Butterfly Curve



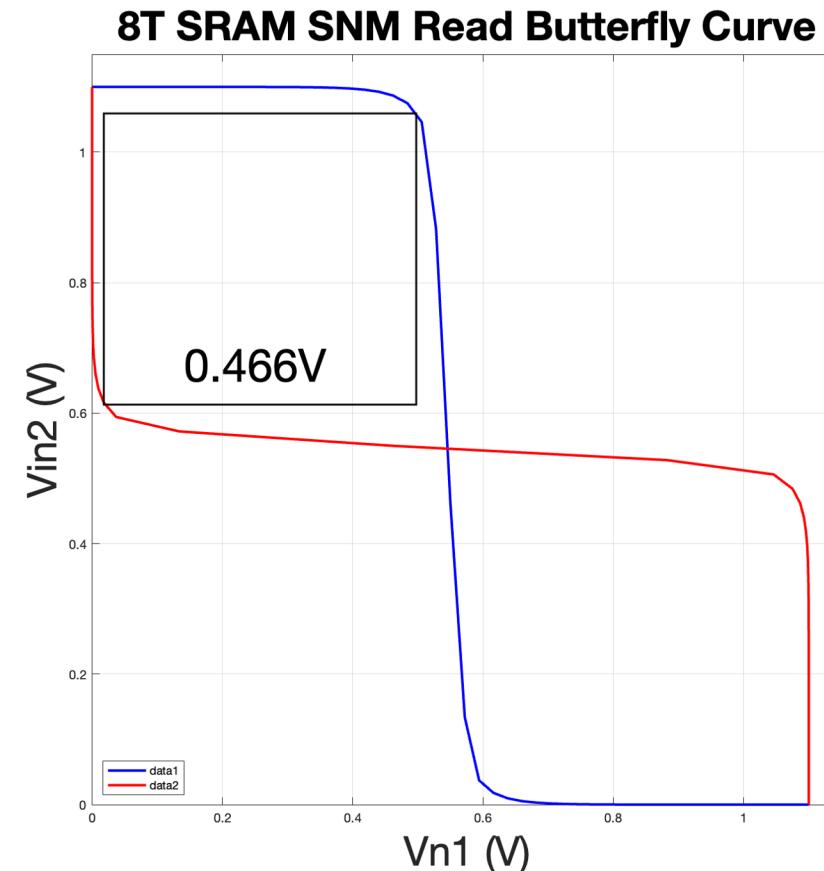
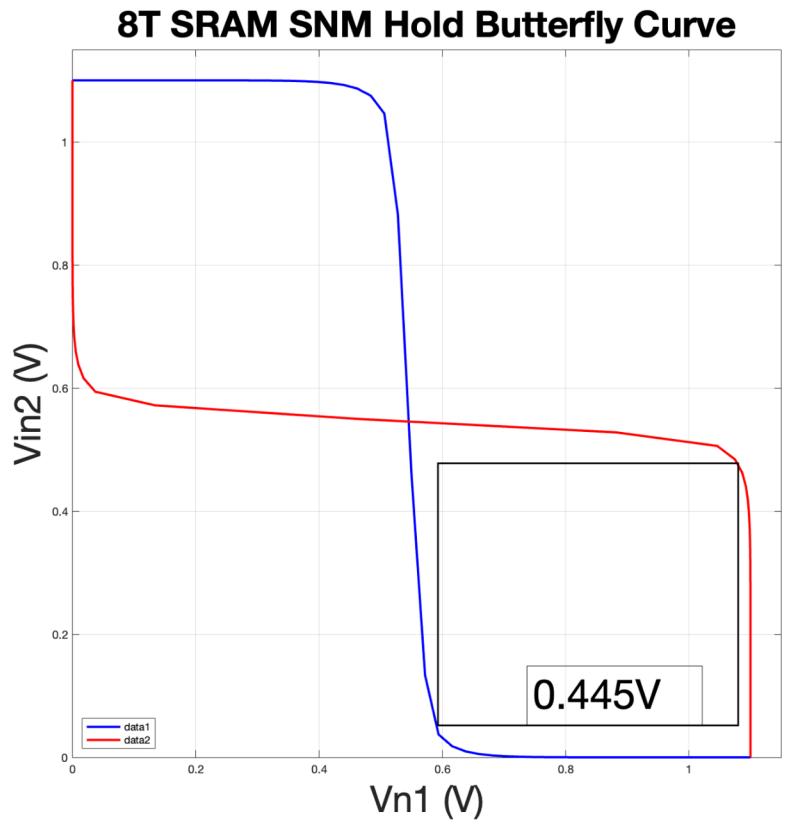
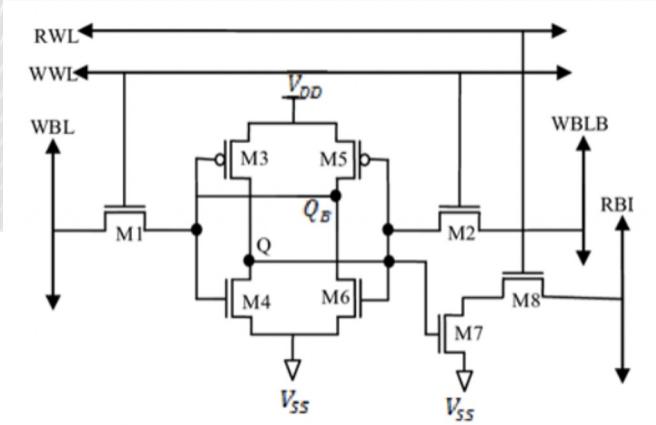
6T SRAM SNM Read Butterfly Curve



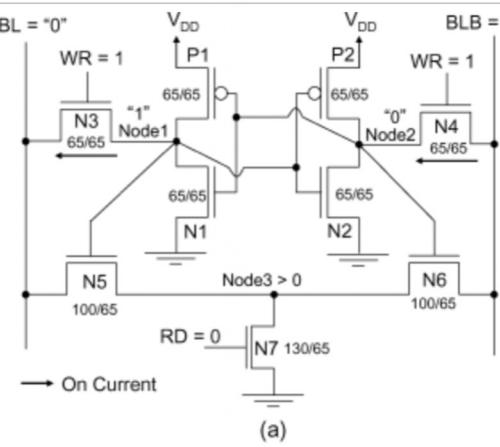
7T SNM



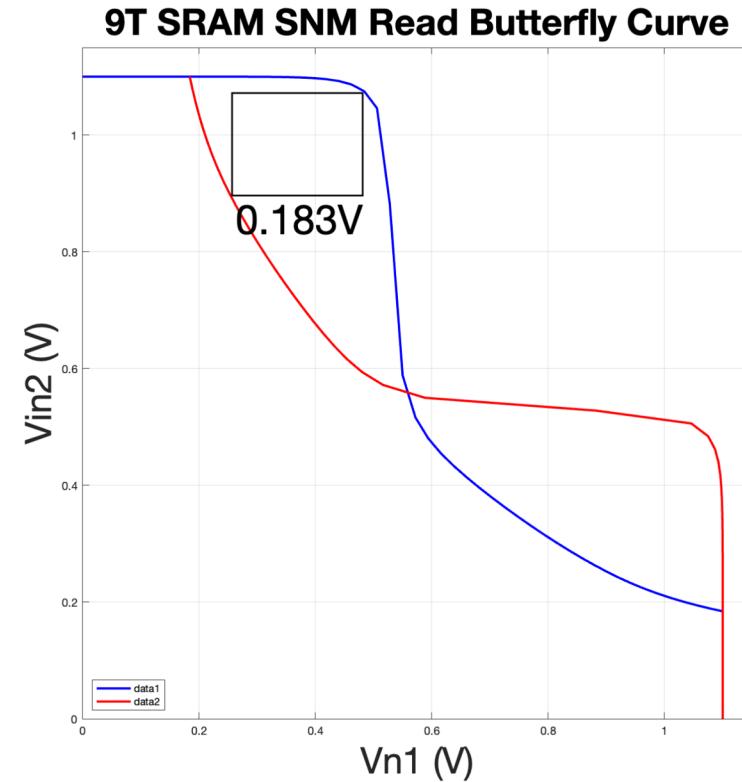
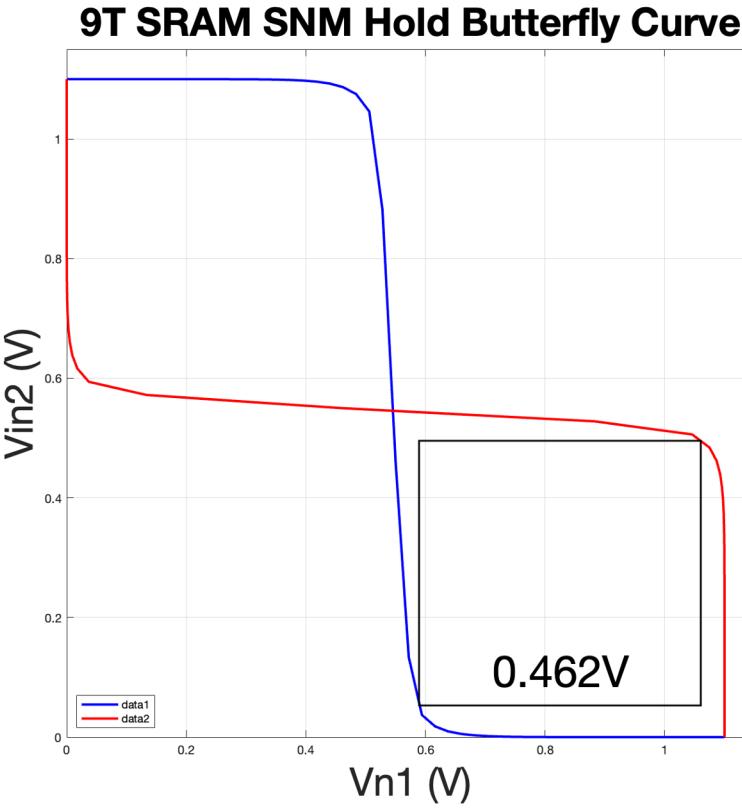
8T SNM



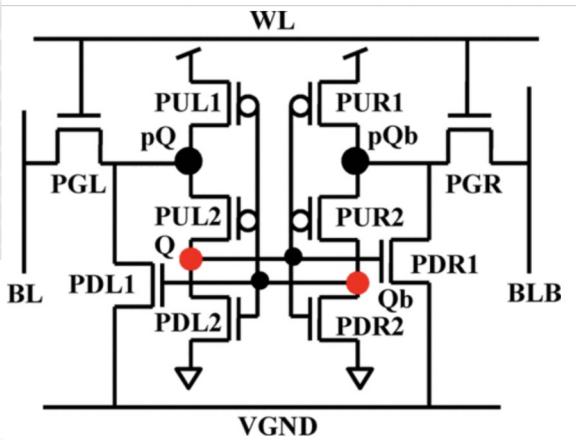
9T SNM



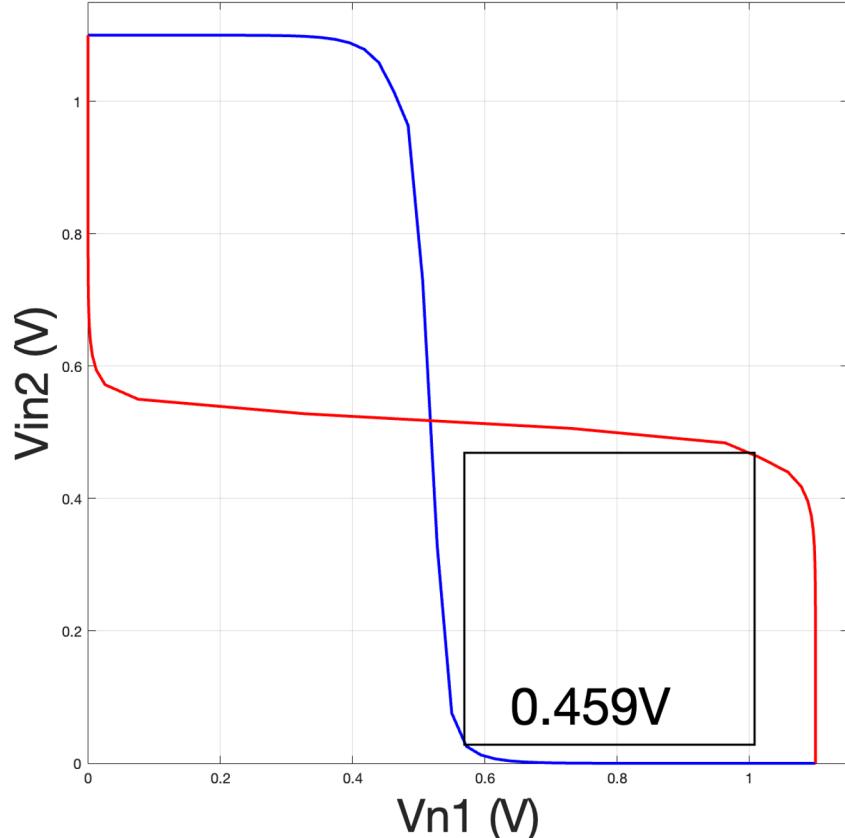
(a)



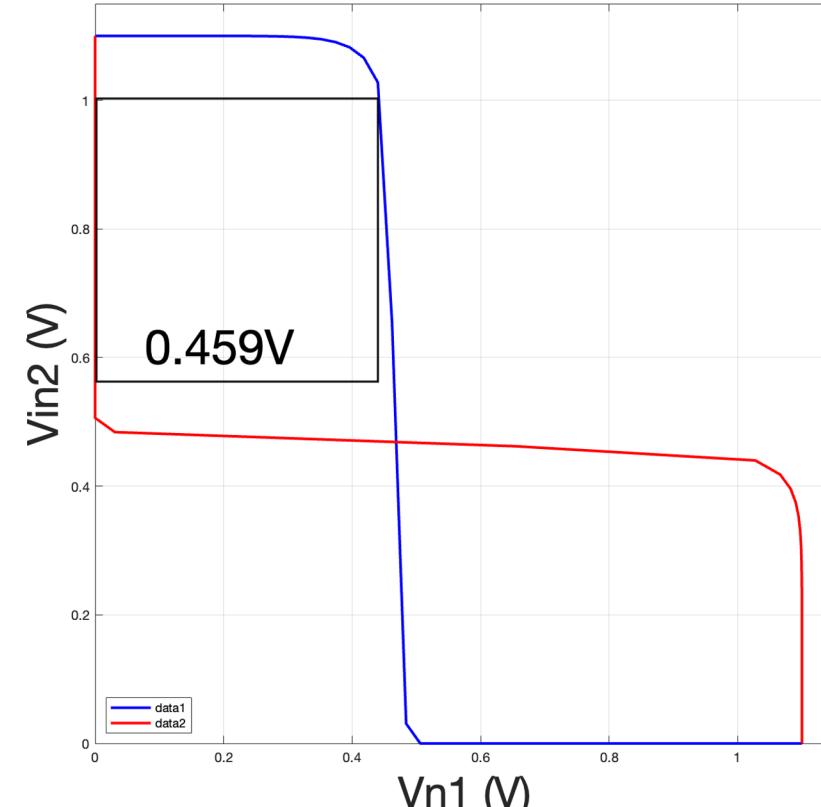
10T SNM



10T SRAM SNM Hold Butterfly Curve



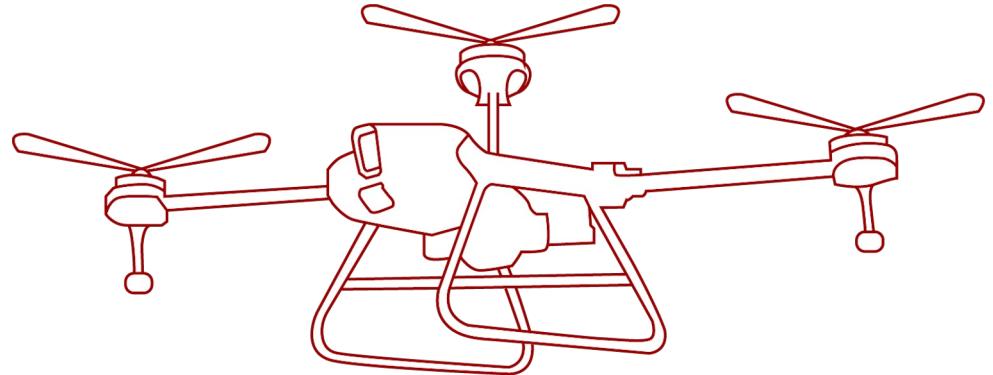
10T SRAM Read Hold Butterfly Curve



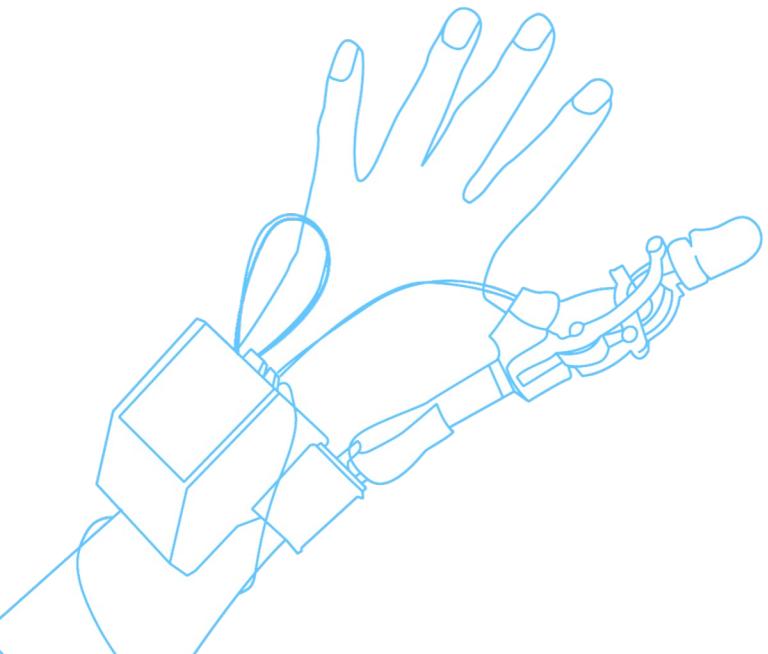
Relatively Stable SNM-H
at minimum size

SNM-R has greater variation
due to design differences

	SNM-H (V)	SNM-R (V)
6T	0.47	0.217
7T	0.469	0.447
8T	0.445	0.466
9T	0.462	0.183
10T	0.459	0.459

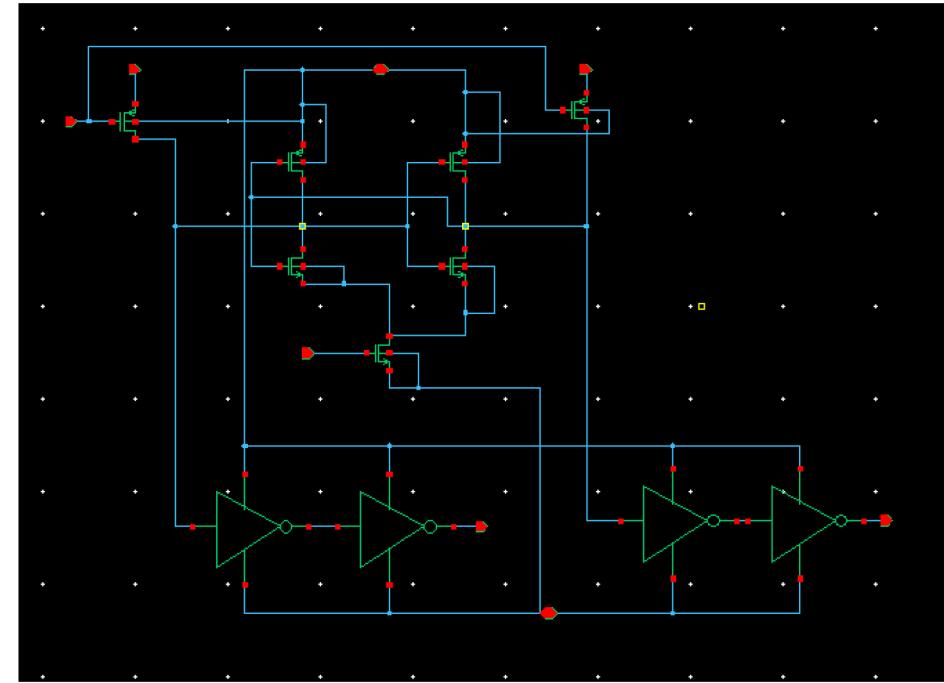
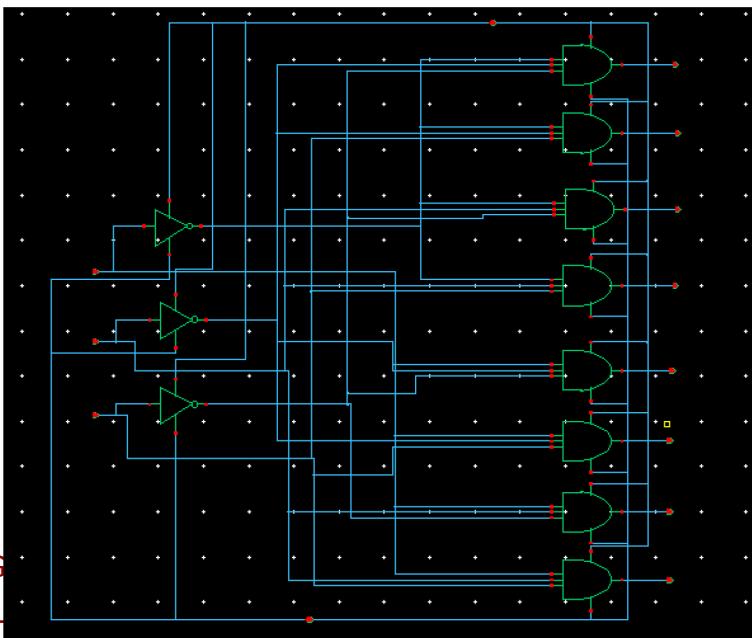
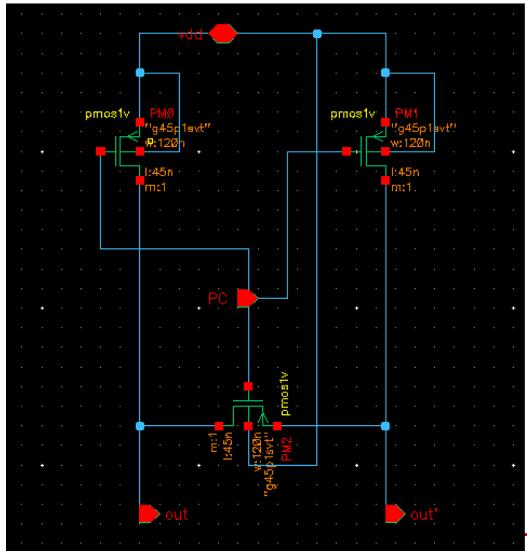


SRAM Array Evaluation



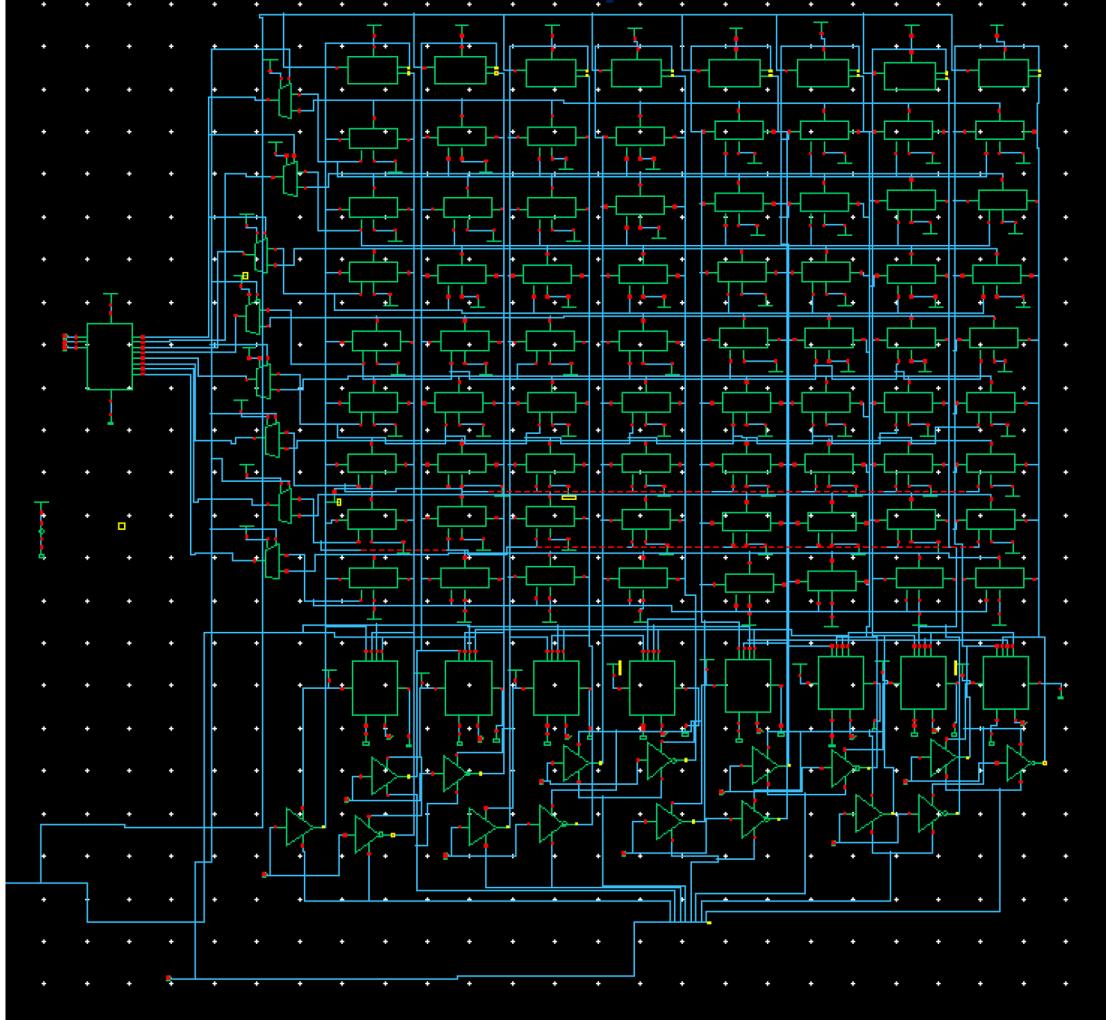
Array Details and Peripherals

- 8 words of 8 bits
- 3-to-8 row decoder
- Differential clocked sense amplifier
- Precharge

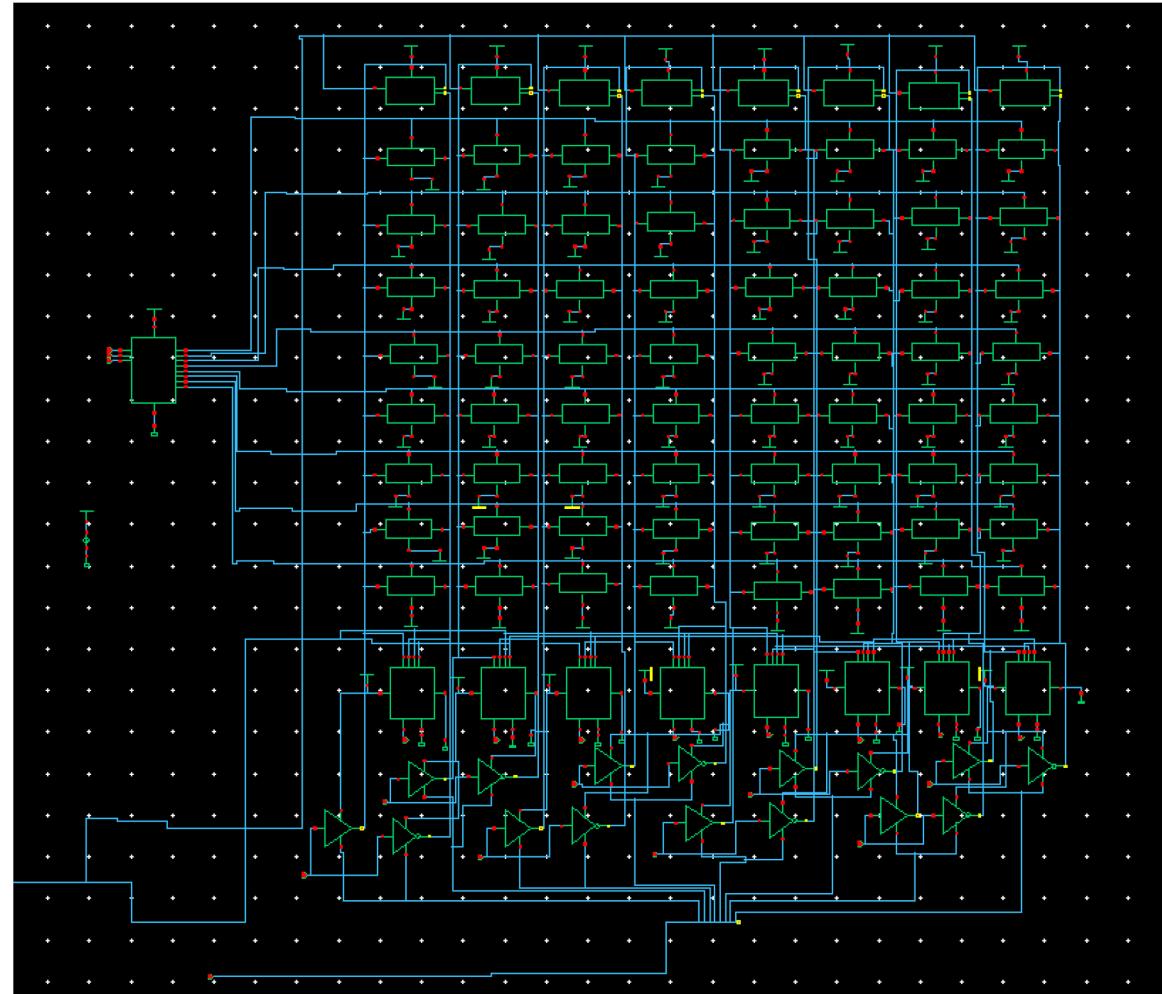


SRAM Array Designs

9T SRAM Array

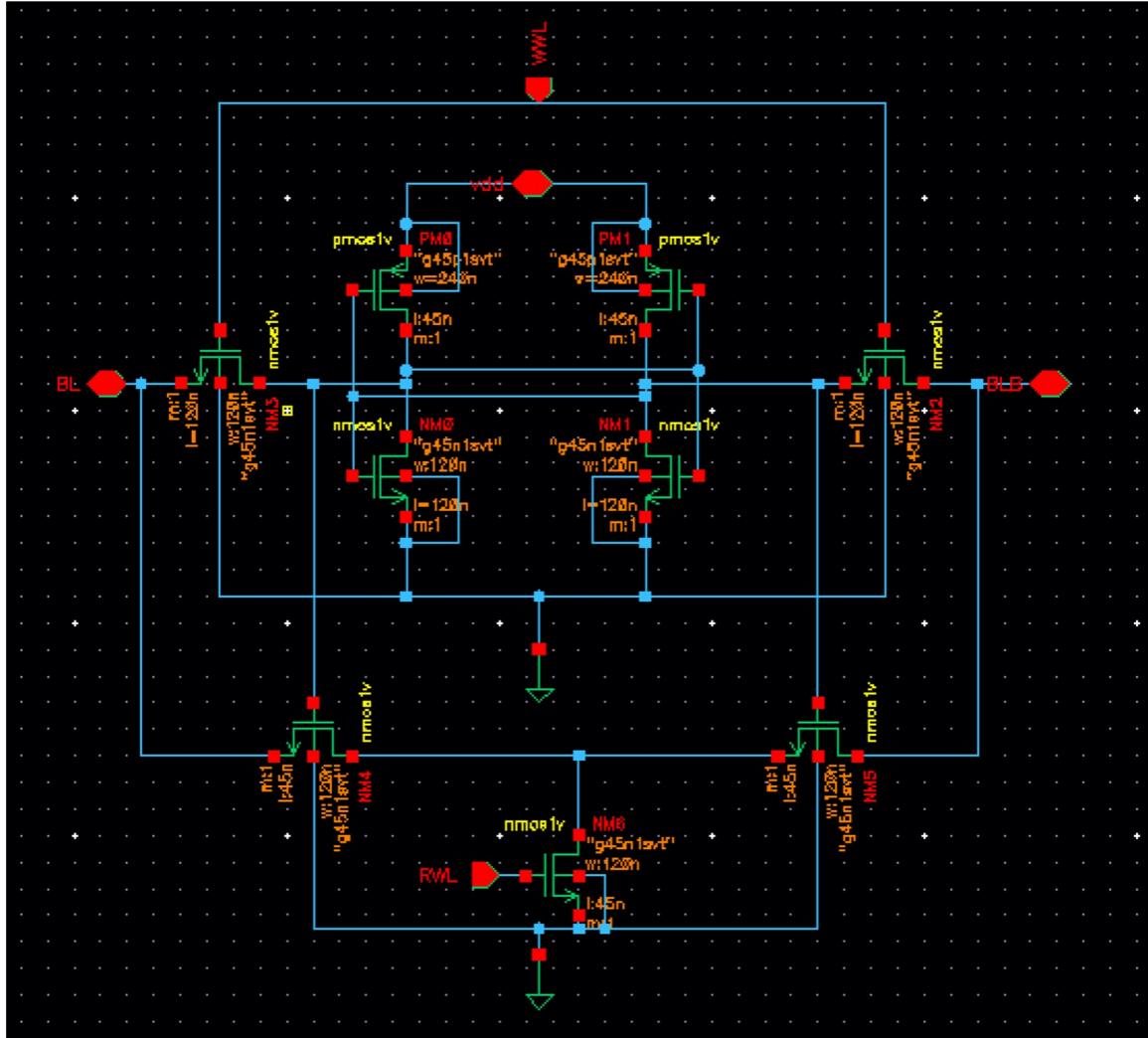


6T and 10T Array

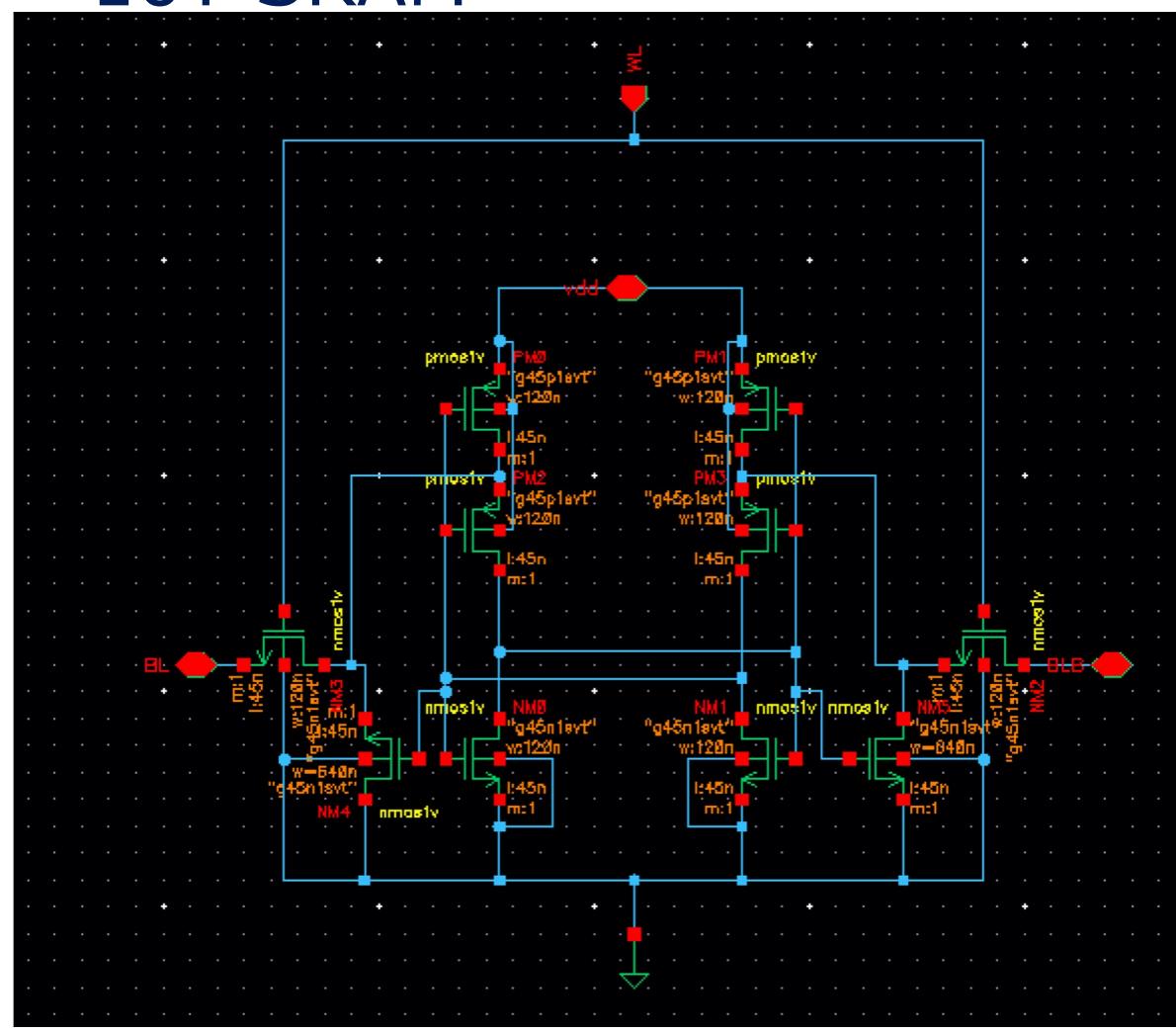


SRAM Cell Transistor Sizings

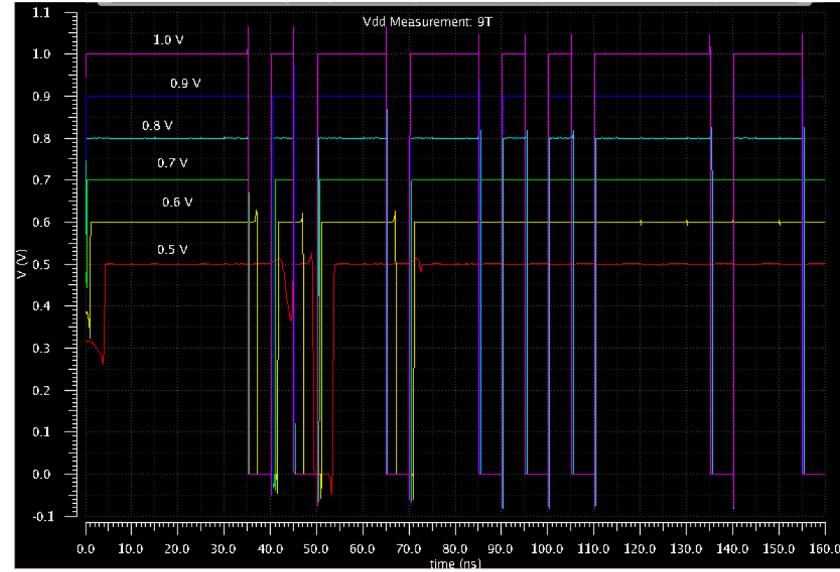
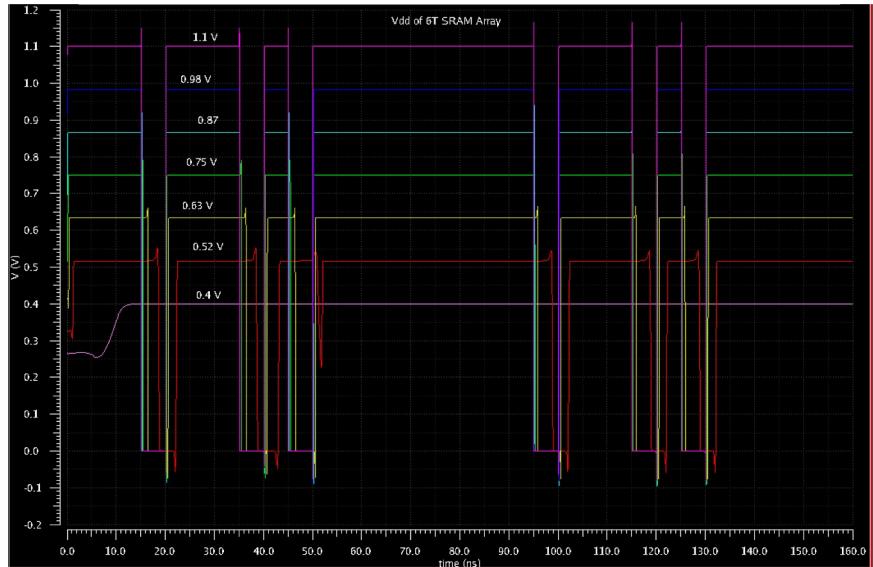
9T SRAM



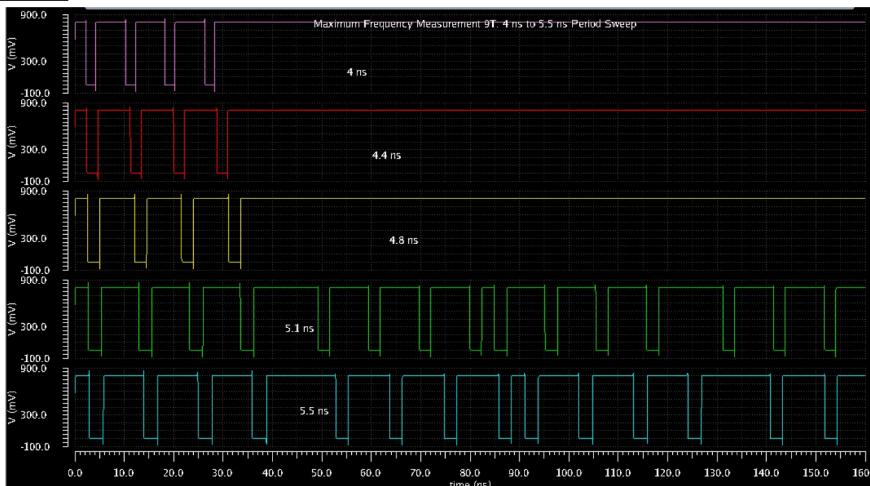
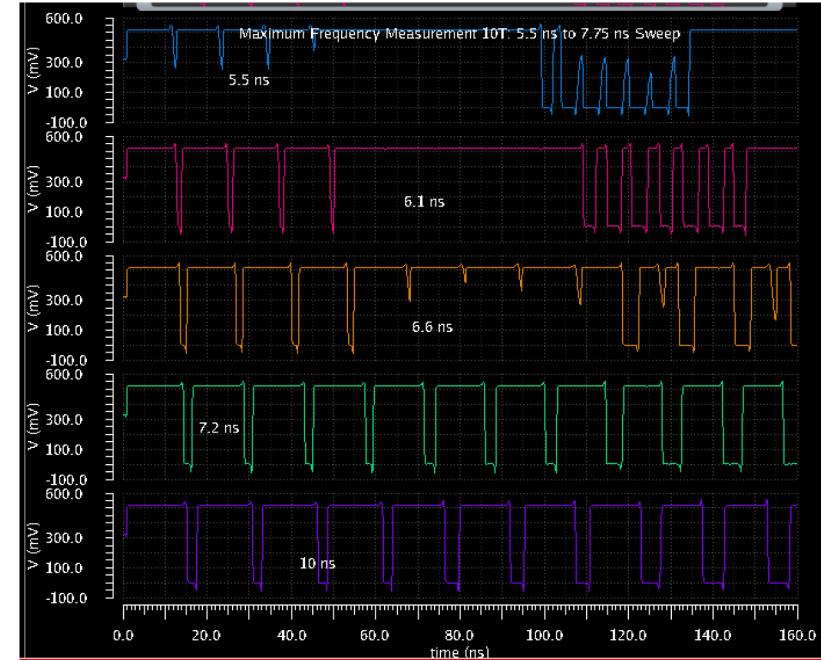
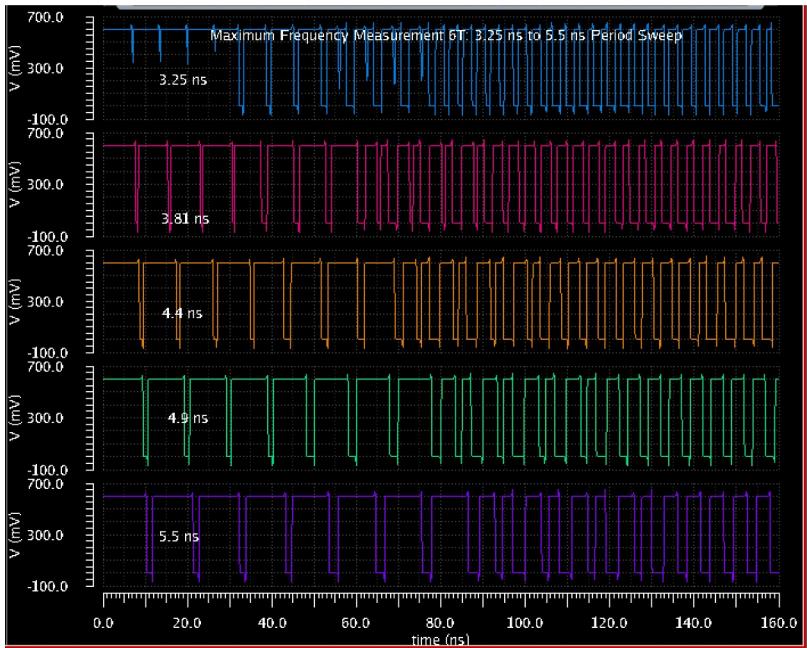
10T SRAM



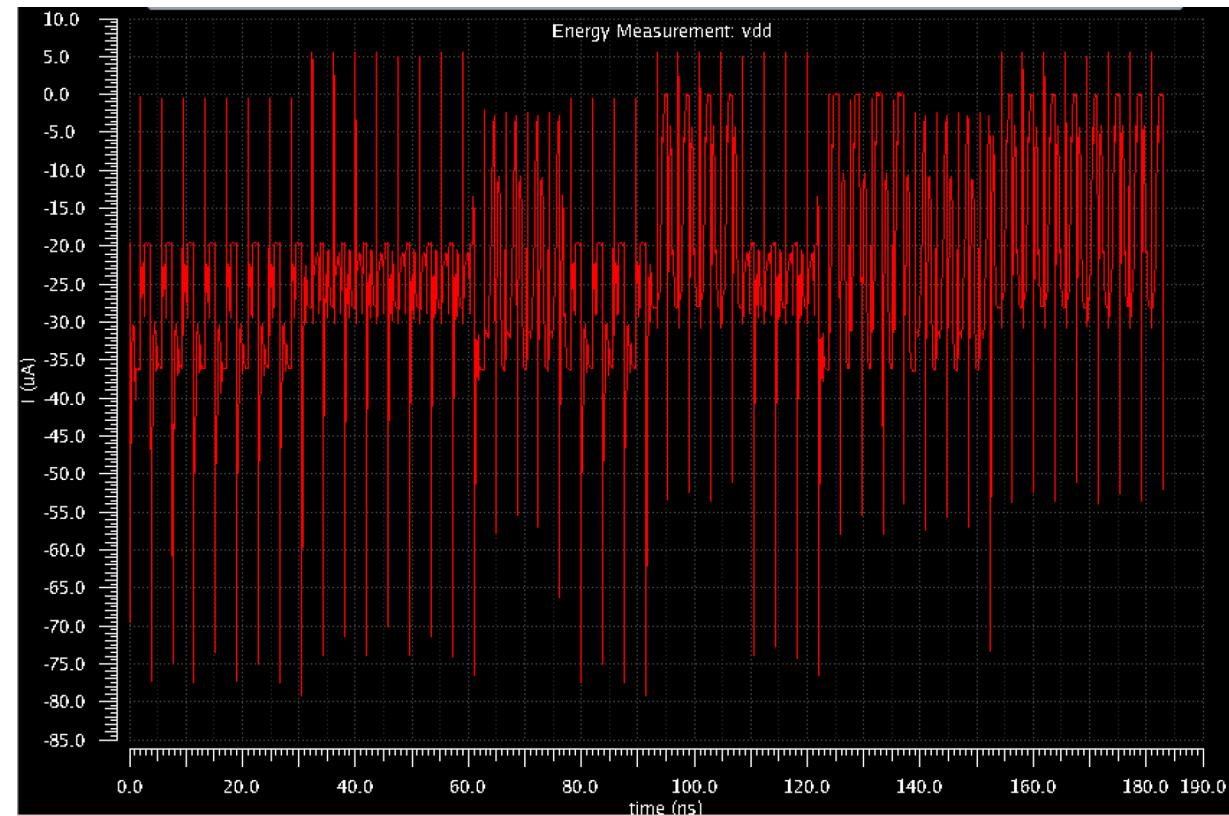
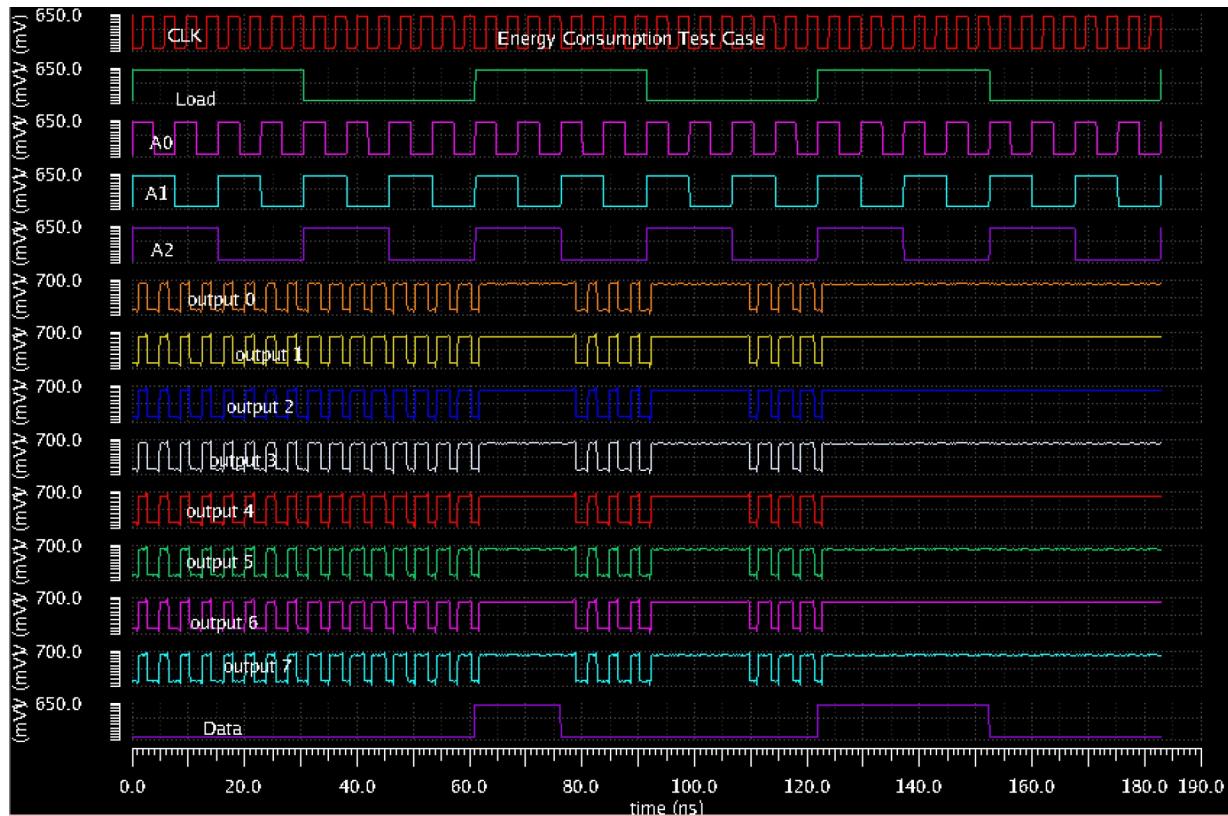
Vdd Measurement



Switching Frequency Measurement



Energy Measurement



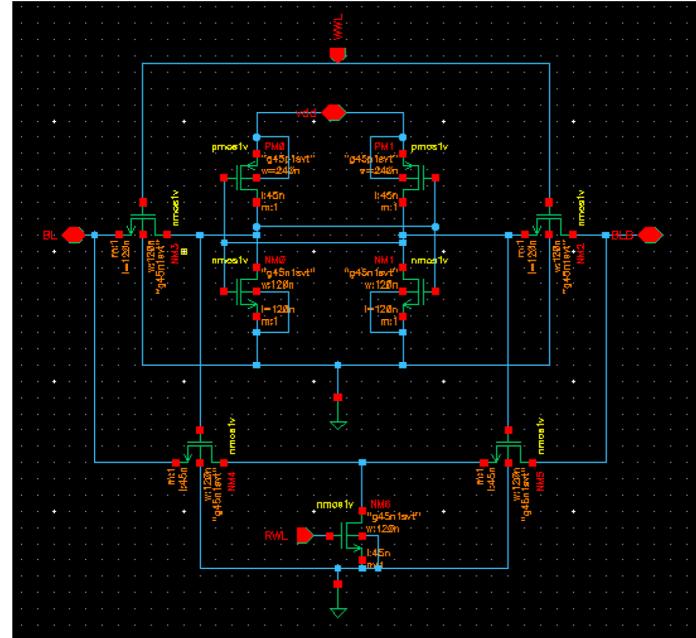
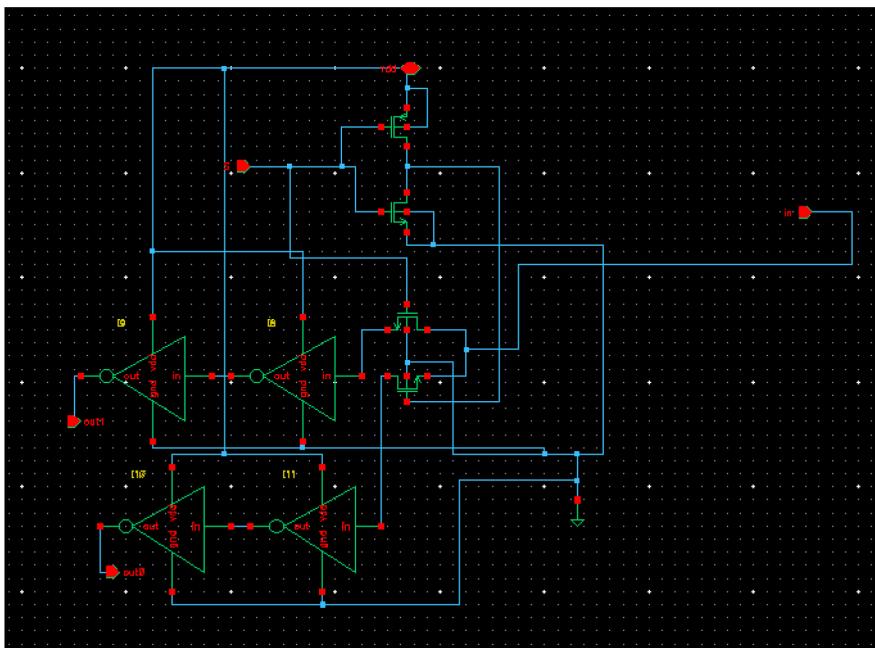
6T Array Measurements Summary



- Vdd of 0.60 V
- Maximum switching frequency of 262 MHz
- Energy usage of 2.56 pJ

9T Array Measurements Summary

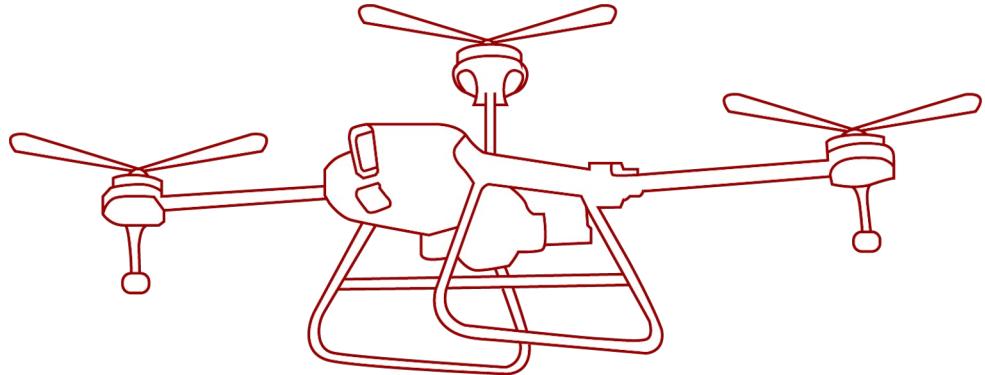
- Vdd of 0.80 V
- Maximum switching frequency of 196 MHz
- Energy usage of 31.86 pJ



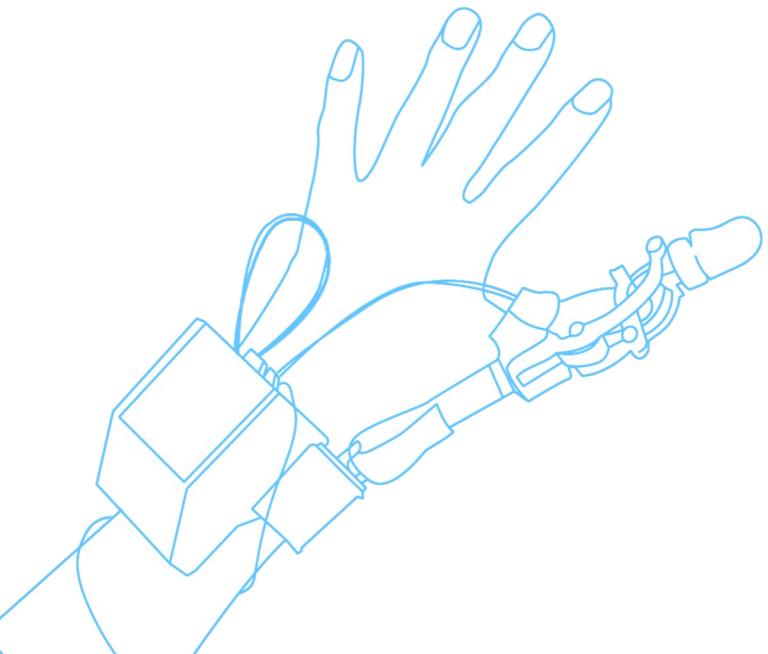
10T Array Measurements Summary



- Vdd of 0.52 V
- Maximum switching frequency of 139 MHz
- Energy usage of 1.51 pJ



Conclusion



- Various SRAM designs have design limitations and trade offs.
- As a designer, we must be aware of the pros and cons of each design and independently verify report designs before implementing them.
- Designers have a lot of choice in designing, but it has large impacts (frequency, vdd, area, etc).
- Using a specific design will likely require optimization to show its perceived benefits

Thank you!