Peter W. Deutsch

Cambridge – Massachusetts

+1 (617) 230 1114 • pwd@mit.edu • pwdeutsch

Education

Massachusetts Institute of Technology
PhD Student, Electrical Engineering and Computer Science *2020–Present*
Doctoral Supervisor: Prof. Mengjia Yan

University of British Columbia
Bachelor of Applied Science, Computer Engineering *2014–2020*
Undergraduate Supervisors: Prof. Mieszko Lis & Prof. Prashant Nair

Research Interests

Side Channels Classification: Exploration of side-channel taxonomies and comparison schemes

Hardware Defenses: Improving traffic shaping schemes, Rowhammer mitigations

Publications

Peter W. Deutsch, Yuheng Yang, Thomas Bourgeat, Jules Drean, Joel S. Emer, and Mengjia Yan. DAGguise: Mitigating Memory Timing Side Channels. In *Proceedings of the 27th ACM International Conference on Architectural Support for Programming Languages and Operating Systems*, ASPLOS 2022, page 329–343, New York, NY, USA, 2022. Association for Computing Machinery.

Oliver Willers, Christopher Huth, Jorge Guajardo, Helmut Seidel, and Peter Deutsch. On the feasibility of deriving cryptographic keys from MEMS sensors. *Journal of Cryptographic Engineering*, Apr 2019.

Work Experience

Research & Academic

Massachusetts Institute of Technology **Cambridge, MA**
Lab Assignment Developer *2022*
- Assisted in the development and testing of lab assignments for MIT's Secure Hardware Design course (6.888).
- Developed an assignment which guides students through performing and characterizing Rowhammer attacks on commodity hardware.

University of British Columbia **Vancouver, Canada**
Undergraduate Research Student *May 2019 – Aug 2020*
- Investigated methods to detect and mitigate speculative execution attacks which utilize cache and DRAM side-channels (ex. Spectre/Meltdown).
- Replicated attacks, benchmarked prior work, and explored new mitigations using SPEC CPU 2017 and gem5.

Bosch Corporate Research **Stuttgart, Germany**
Microsystems Engineering Student *Jan 2017 – Aug 2017*
- Researched the use of MEMS gyroscopes as Physical Unclonable Functions (PUFs), facilitating reliable secret key generation in IoT devices.
- Helped to devise and evaluate entropy extraction schemes to generate cryptographically secure keys from highly correlated device features.

University of British Columbia **Vancouver, Canada**
Undergraduate Teaching Assistant *2016 – 2020*
- Conveyed Verilog-focused digital design content to hundreds of second and third-year undergraduate students.
- Taught CPEN 211 (Introduction to Microcomputers), CPEN 311 (Digital Systems Design), and CPEN 391 (Computer Engineering Design Studio II).

Industry

Intel Corporation **Vancouver, Canada**
Verification Engineer Intern *May 2018 – Apr 2019*
- Verified system controller ASICs for Intel NAND devices using SystemVerilog and the Universal Verification Methodology (UVM 1.2).
- Designed end-to-end traffic tests to confirm compliance to internal architecture requirements and flash interface specifications, ensuring that comprehensive code coverage was achieved.

Microsemi (Microchip) **Vancouver, Canada**
Product Design Engineer Intern *Sep 2017 – Dec 2017*
- Designed and verified top-level RTL glue logic (SystemVerilog & VHDL) for SAS/SATA RAID controllers.
- Implemented appropriate pipelining and clock-domain-crossing synchronization strategies, ensuring that timing closure and MTBF thresholds were met.

Volunteerism

MIT Graduate Application Assistance Program **Cambridge, MA**
Graduate Student Volunteer *2021*
- Worked with underrepresented MIT PhD applicants, providing advice and detailed feedback on personal and research statements.

BC COVID-19 3D Printing Group (BCC3D) **Vancouver, Canada**
Printing / Distribution Volunteer *2020*
- Personally manufactured 300+ 3D printed face shield visors and 'ear savers' for use at hospitals and clinics.
- Inspected, sanitized, and packed 10,000+ articles of PPE produced by local volunteers.

University of British Columbia **Vancouver, Canada**
Imagine Day Orientation Leader *2015, 2016, 2019*
- Conducted informative tours for first year orientation, helping to build community relationships and increase the comfort level of new students.

Awards

Advanced Televison and Signal Processing Fellowship **2020**
Awarded on the recommendation of the Department Head of EECS

Dean's Prize for Academic Excellence in Engineering **2020**
Awarded to the head of the graduating undergraduate class in Applied Science

ECE Capstone Faculty Award **2020**
Presented to the top ECE Capstone (final year) project teams in 2020

NSERC Undergraduate Student Research Award **2019**
Awarded on the recommendation of the Faculty of Applied Science

Trek Excellence Scholarship for Continuing Students **2015, 2016, 2017, 2019**
Awarded to students in the top 5% of their program

PMC-Sierra Founders Award in Electrical and Computer Engineering **2019**
Awarded on the recommendation of the Department Head of Computer Engineering

Elizabeth and Leslie Gould Scholarship in Engineering **2019**
Awarded on the recommendation of the Faculty of Applied Science

J Fred Muir Memorial Scholarship in Engineering **2017**
Awarded on the recommendation of the Faculty of Applied Science

J K Zee Memorial Scholarship **2016**
Awarded on the recommendation of the Faculty of Applied Science