

# Peter W. Deutsch

Cambridge – Massachusetts

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## Education

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### Massachusetts Institute of Technology

*PhD Student, Electrical Engineering and Computer Science*

2022 – Present

Doctoral Supervisor: Prof. Mengjia Yan

### Massachusetts Institute of Technology

*Master of Science, Electrical Engineering and Computer Science*

2020 – 2022

Thesis: Mitigating Memory Controller Side-Channels

Masters Supervisor: Prof. Mengjia Yan

### University of British Columbia

*Bachelor of Applied Science, Computer Engineering*

2014 – 2020

Undergraduate Supervisors: Prof. Mieszko Lis & Prof. Prashant Nair

## Research Interests

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**Processor Reliability:** Improving chip design processes in light of emergent failure modes.

**Side-Channel Classification and Defense:** Exploration of side-channel taxonomies, comparison schemes, and concrete leakage evaluations.

**Memory Defenses:** Making DRAM more resilient to timing side-channels and Rowhammer effects.

## Publications

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Peter W. Deutsch\*, Vincent Quentin Ulitzsch\*, Sudhanva Gurumurthi, Vilas Sridharan, Joel Emer, and Mengjia Yan. DelayAVF: Calculating architectural vulnerability factors for delay faults. In *Proceedings of the 57th IEEE/ACM International Symposium on Microarchitecture (To Appear)*, 2024.

Peter W. Deutsch, Weon Taek Na, Thomas Bourgeat, Joel S Emer, and Mengjia Yan. Metior: A comprehensive model to evaluate obfuscating side-channel defense schemes. In *Proceedings of the 50th Annual International Symposium on Computer Architecture*, pages 1–16, 2023.

Peter W Deutsch\*, Yuheng Yang\*, Thomas Bourgeat, Jules Drean, Joel S Emer, and Mengjia Yan. DAGguise: Mitigating memory controller side-channels. In *Proceedings of the 27th ACM International Conference on Architectural Support for Programming Languages and Operating Systems*, pages 329–343, 2022.

Oliver Willers, Christopher Huth, Jorge Guajardo, Helmut Seidel, and Peter Deutsch. On the feasibility of deriving cryptographic keys from MEMS sensors. *Journal of Cryptographic Engineering*, 10(1):67–83, 2020.

## Invited Talks

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<b>DelayAVF: Calculating Architectural Vulnerability Factors for Delay Faults</b> <i>Advanced Micro Devices (AMD) - Architecting for Marginal Defects Working Group</i>	<b>May 2024</b>
<b>Increasing Architectural Resilience to Small Delay Faults</b> <i>MIT AI Hardware Program Symposium</i>	<b>May 2024</b>
<b>Strengthening Hardware Security in the Age of AI</b> <i>MIT CSAIL/UK GHCQ Delegation</i>	<b>Sept. 2023</b>
<b>Modelling Obfuscating Side-Channel Defense Schemes</b> <i>Carnegie Mellon University - Special Topics in Hardware Security (17-715)</i>	<b>Sept. 2023</b>

## Academic Service

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<b>IEEE Transactions on Computers – Special Issue on Hardware Security</b> <i>Reviewer</i>	<b>2022</b>
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## Work Experience

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### Research & Academic.....

**Advanced Micro Devices (AMD)** **Austin, TX**  
*PhD Intern* **2024**

- Applied my prior research (DelayAVF) to assess the potential reliability impacts of small delay faults in next-generation AMD products.
- Substantially expanded upon the existing open-source DelayAVF infrastructure to facilitate the reliability assessment of large out-of-order CPUs.

**Massachusetts Institute of Technology** **Cambridge, MA**  
*Teaching Assistant/Lab Assignment Developer* **2022 – 2024**

- Assisted in the development and deployment of lab assignments for MIT's Secure Hardware Design course.
- Developed an assignment which guides students through performing and characterizing Rowhammer attacks on commodity hardware.

**University of British Columbia** **Vancouver, Canada**  
*Undergraduate Research Student* **2019 – 2020**

- Investigated methods to detect and mitigate speculative execution attacks which utilize cache and DRAM side-channels (ex. Spectre/Meltdown).
- Replicated attacks, benchmarked prior work, and explored new mitigations using SPEC CPU 2017 and gem5.

**Bosch Corporate Research** **Stuttgart, Germany**  
*Microsystems Engineering Student* **2017**

- Researched the use of MEMS gyroscopes as Physical Unclonable Functions (PUFs), facilitating reliable secret key generation in IoT devices.
- Helped to devise and evaluate entropy extraction schemes to generate cryptographically secure keys from highly correlated device features.

**University of British Columbia** **Vancouver, Canada**  
*Undergraduate Teaching Assistant* **2016 – 2020**

- Conveyed Verilog-focused digital design content to hundreds of second and third-year undergraduate students.
- Taught CPEN 211 (Introduction to Microcomputers), CPEN 311 (Digital Systems Design), and CPEN 391 (Computer Engineering Design Studio II).

## Industry.....

- Intel Corporation** **Vancouver, Canada**  
*Verification Engineer Intern* *2018 – 2019*
- Verified system controller ASICs for Intel NAND devices using SystemVerilog and the Universal Verification Methodology (UVM).
  - Designed end-to-end traffic tests to confirm compliance to internal architecture requirements and flash interface specifications, ensuring that comprehensive code coverage was achieved.
- Microsemi (Microchip)** **Vancouver, Canada**  
*Product Design Engineer Intern* *2017*
- Designed and verified top-level RTL glue logic (SystemVerilog & VHDL) for SAS/SATA RAID controllers.
  - Implemented appropriate pipelining and clock-domain-crossing synchronization strategies, ensuring that timing closure and MTBF thresholds were met.

## Awards

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### Graduate.....

- Google Research Scholar Grant** **2023**  
*Topic: Leveraging Accessible Signals for the Efficient Discovery of Corrupt Execution Errors*
- Advanced Television and Signal Processing Fellowship** **2020**  
*Awarded on the recommendation of the Department Head of EECS*

### Undergraduate.....

- Dean's Prize for Academic Excellence in Engineering** **2020**  
*Awarded to the head of the graduating undergraduate class in Applied Science*
- ECE Capstone Faculty Award** **2020**  
*Presented to the top ECE Capstone (final year) project teams in 2020*
- NSERC Undergraduate Student Research Award** **2019**  
*Awarded on the recommendation of the Faculty of Applied Science*
- Trek Excellence Scholarship for Continuing Students** **2015, 2016, 2017, 2019**  
*Awarded to students in the top 5% of their program*
- PMC-Sierra Founders Award in Electrical and Computer Engineering** **2019**  
*Awarded on the recommendation of the Department Head of Computer Engineering*
- Elizabeth and Leslie Gould Scholarship in Engineering** **2019**  
*Awarded on the recommendation of the Faculty of Applied Science*
- J Fred Muir Memorial Scholarship in Engineering** **2017**  
*Awarded on the recommendation of the Faculty of Applied Science*
- J K Zee Memorial Scholarship** **2016**  
*Awarded on the recommendation of the Faculty of Applied Science*

## Volunteerism

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- MIT Graduate Application Assistance Program** **Cambridge, MA**  
*Treasurer/Graduate Student Volunteer* *2021 – Present*

- Worked with underrepresented MIT PhD applicants, providing advice and detailed feedback on personal and research statements.
- Coordinated finances for the program, raising funds to provide fee waivers for underprivileged applicants.

**BC COVID-19 3D Printing Group (BCC3D)**

**Vancouver, Canada**

*Printing / Distribution Volunteer*

*2020*

- Personally manufactured 300+ 3D printed face shield visors and 'ear savers' for use at hospitals and clinics.
- Inspected, sanitized, and packed 10,000+ articles of PPE produced by local volunteers.

**University of British Columbia**

**Vancouver, Canada**

*Imagine Day Orientation Leader*

*2015, 2016, 2019*

- Conducted informative tours for first year orientation, helping to build community relationships and increase the comfort level of new students.