

# **Experiment 4:**

## **Design and Implementation of Circuits at Gate Level Minimization with Sum-of-Product and Product-of-Sum Simplification**

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EEL3702C

Digital Logic Design

Section 04

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## Experiment 4: Design and Implement of Digital Circuits at Gate Level Minimization with Sum-of-Product and Product-of-Sum Simplification

### Objectives

After completing this experiment, you will be able

- to design and implement the digital circuits in terms of Sum-of-Product (SOP) and Product-of-Sum (POS) simplification
- to synthesize the digital circuit that implements using 74XX00 series integrated circuits.

### Experimental Equipments:

- 74LS04 1-input NOT TTL IC
- 74LS08 quad 2-input AND TTL IC
- 74LS32 quad 2-input OR TTL IC
- DC Voltmeter
- +5V Power supply
- Bread Board
- Light Emitting Diode
- Connecting Wires

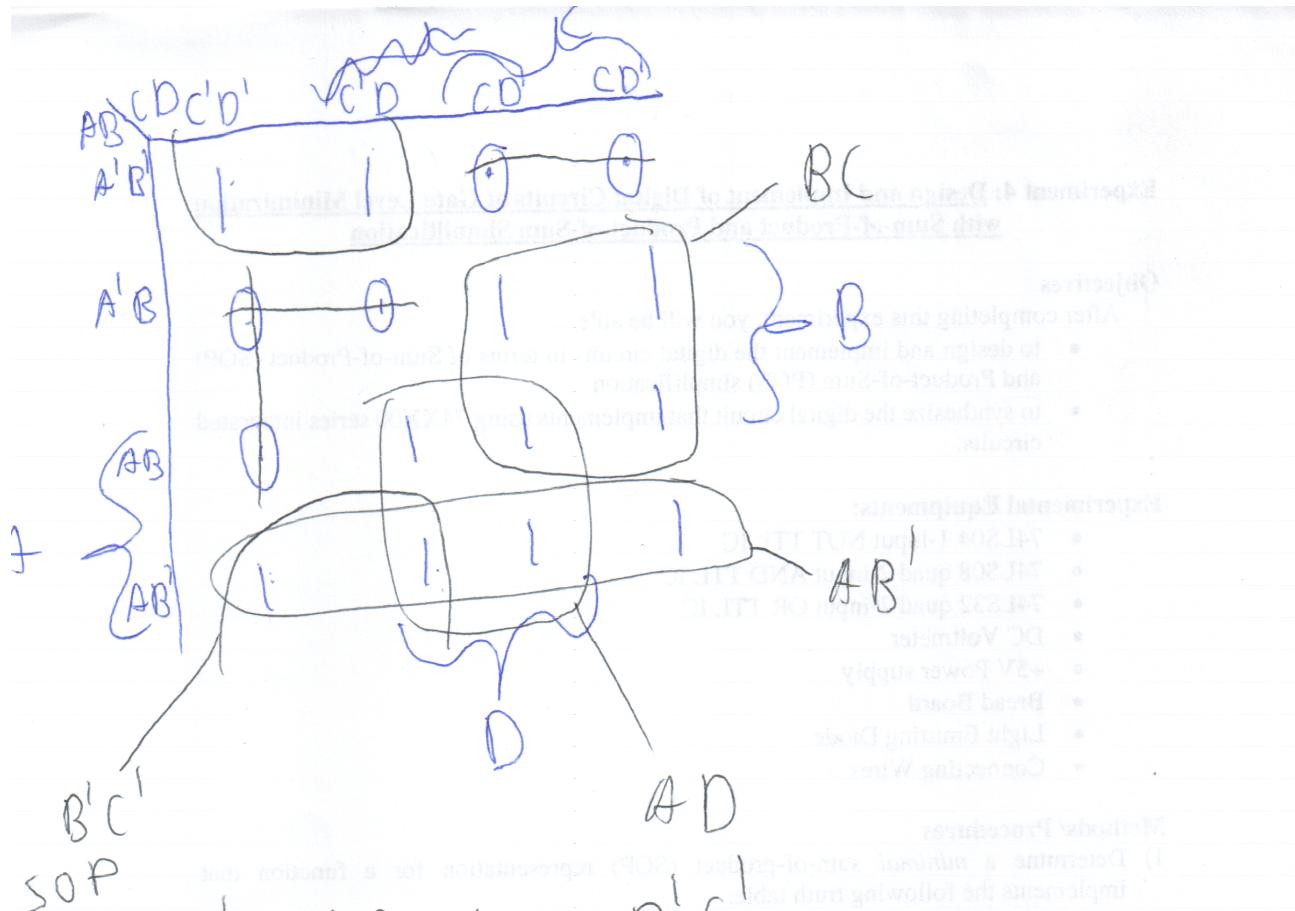
### Methods/ Procedures

- 1) Determine a *minimal* sum-of-product (SOP) representation for a function that implements the following truth table:

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

*Hint: Use a K-map to obtain the minimal representation*

- 2) Determine a *minimal* product-of-sum (POS) representation for a function that implements the previous truth table.



SOP

$$F = AB' + AD + BC + B'C'$$

$$F'' = (A'B'C + A'BC' + BC'D')$$

$$(A' + B' + C')(A + B + C)(B + C + D)$$

$$F = (A + B + C')(A + B' + C)(B' + C + D)$$

~~$$F = A'B'C' + A'BC' + BC'D'$$~~

~~$$F = (A' + B' + C)(A' + B + C')(B + C' + D')$$~~

~~$$F'' = (A'B'C + A'BC' + BC'D')$$~~

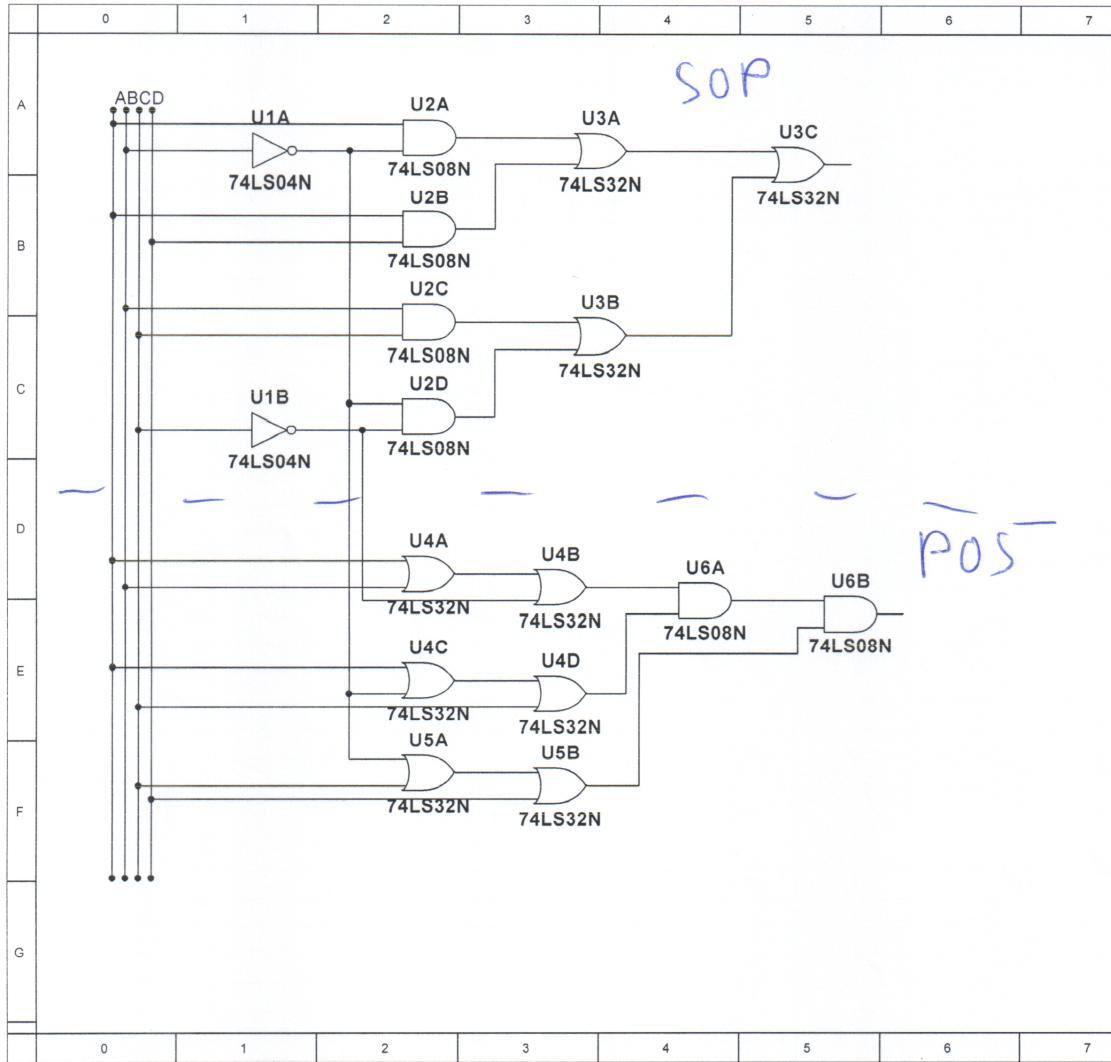
~~$$F = (A + B + C)(A + B' + C)(B' + C + D)$$~~

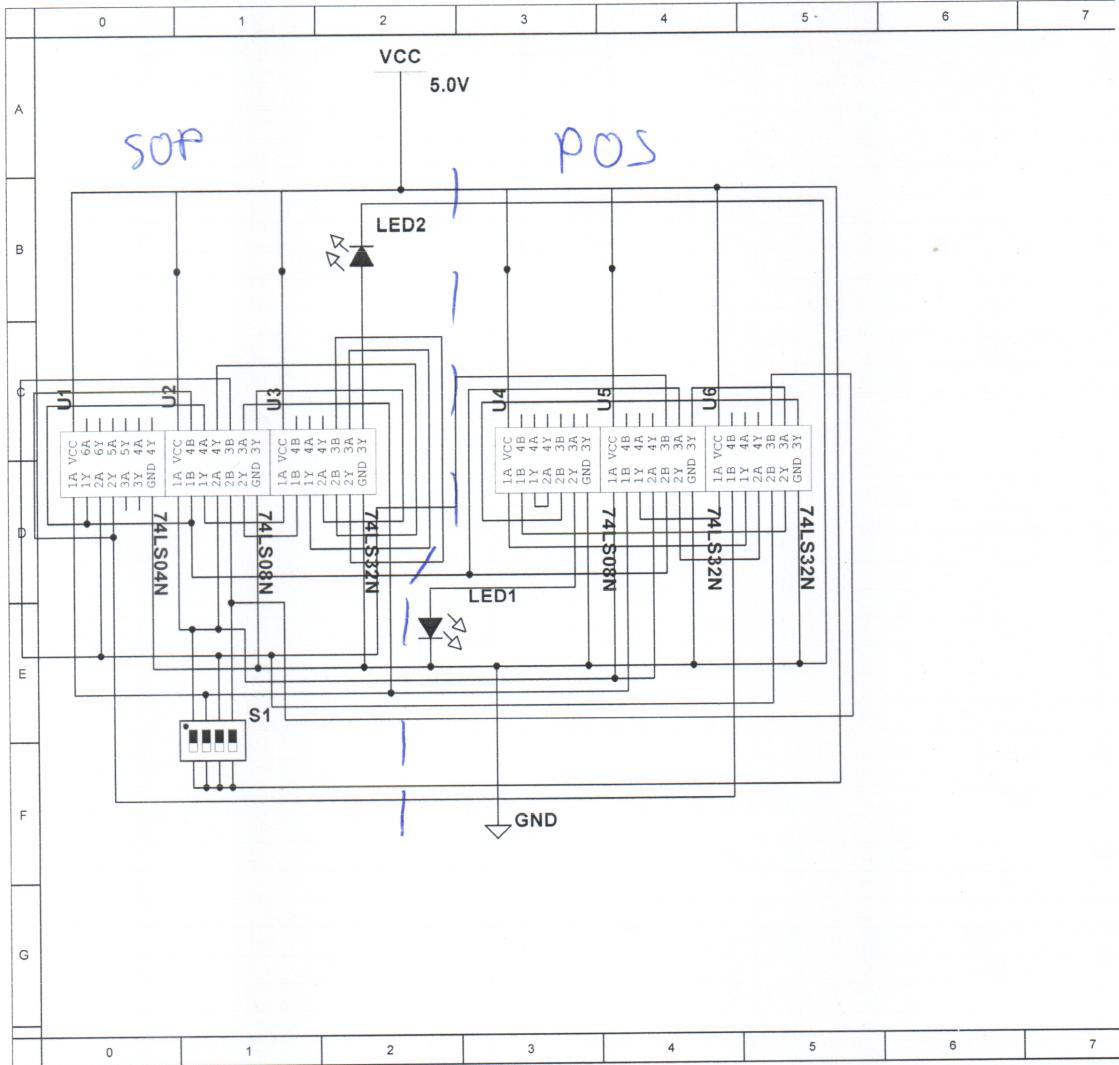
- SOP / POS
- 3) Select both of your SOP and POS representation for implementation.
  - 4) Draw a circuit diagram for your implementation using standard parts (e.g., 74XX00, 74XX02, 74XX04, 74XX32, etc.).
  - 5) Complete and label an IC diagram and label your circuit diagram with gate labels and pin numbers.
  - 6) Build, troubleshoot, and test the circuit.
  - 7) Verify your truth table that shows intermediate signals for your circuit.

**Special Instructions:** Demonstrate your circuit to your instructor when you have it working.

A	B	C	D	$F_{SOP}$	$F_{POS}$
0	0	0	0	1	1
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	0	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	1	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

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## Appendix

Integrated Circuits (ICs) pin diagram

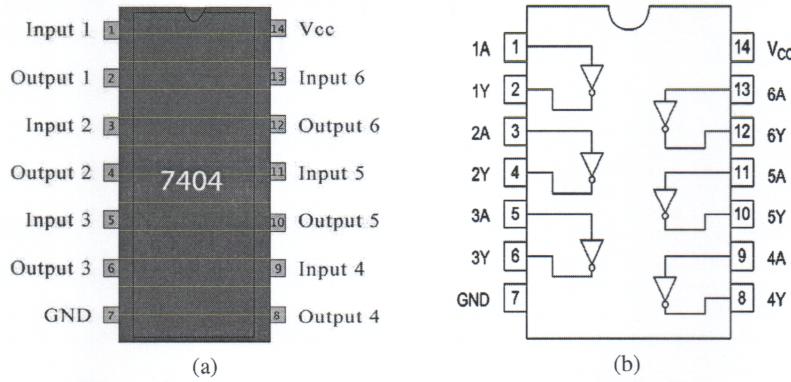


Figure 1. 74LS04 Integrated Circuits (a) Top view and (b) Pin diagram

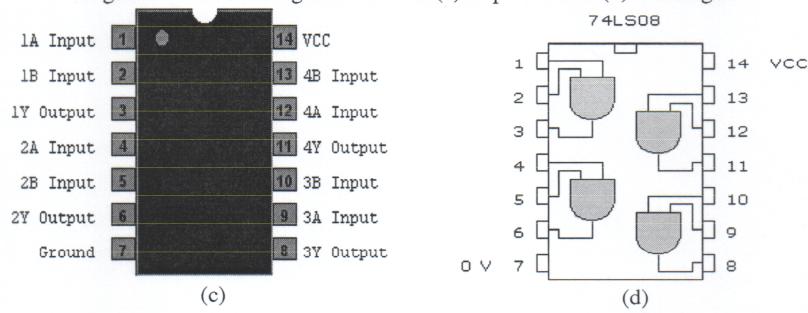


Figure 2. 74LS08 Integrated Circuits (c) Top view and (d) Pin diagram

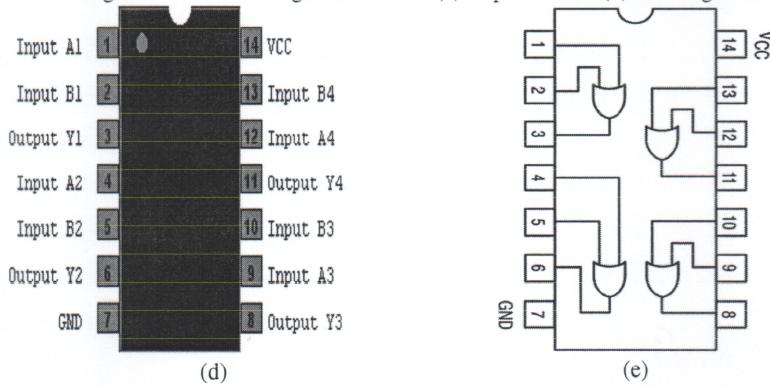


Figure 3. 74LS32 Integrated Circuits (d) Top view and (e) Pin diagram

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**Lab Check off Sheet**

Please bring a print out of this sheet before demonstrating your working circuit. Attach this check off sheet with the Lab report.

*Note: Lab check off sheet should be signed by the Instructor or TA. Lab reports without the check off sheet will not receive credit.*

Name: Peter Dranishnikov

Section: 04

Experiment: Experiment 4

Lab Demonstration Comments:

sop ab us 02/16  
pos works

Signature of Instructor/TA:

pe  
02/16

Date:

## **Results and Discussion:**

Both the Product-of-Sum and Sum-of-Product implementations matched the initial truth table I/O values in operation both in Multisim and the breadboard implementation. The implementation cost is about the same in terms of number of gates and number of IC packages required.

## **Conclusion:**

A Karhnaugh map simplifies the complexity and possible mistakes in conversion between POS and SOP forms of an expression. Additionally, simulation of a circuit in a SPICE-like simulator program (in this lab, Multisim), eases the design, testing, and troubleshooting phases of digital logic design with simulation-capable logic diagrams and IC circuit simulation.