Experiment 9: Design and Implement a Synchronous BCD Counter with J-K flip-flops

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Experiment No. 9: Design and Implement a Synchronous BCD Counter with J-K flip-flops

Objective:

After successfully completing this experiment, you will able to

1. Develop the excitation of of BCD counter
2. Design a synchronous BCD counter
3. Know how to generate clock signal using clock
4. Analyze and verify the correctness of your BCD counter

Experimental Equipment:

1. 74LS32 TTL Logic (OR gate)
2. 74LS04 TTL Logic (NOT gate)
3. 74LS08 TTL logic (AND gate)
4. 74LS76 J-K flip-flop
5. Clock generator
6. Electrical wires
7. Breadboard
8. Power Supply (+5V)
9. Light Emitting Diode (LED)

Methods/ Procedures:

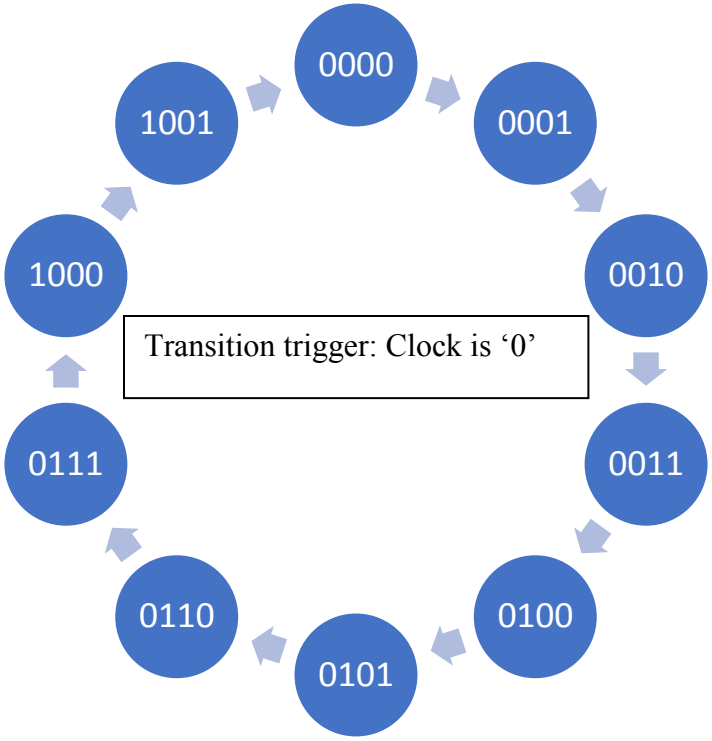
1. From the specification of the problem, develop the excitation table of BCD counter. Therefore, you need to know the excitation table of J-K flip-flop first.

2. Find out the inputs of J-K flip-flop using K-map.

3. Design BCD counter using J-K flip-flops

4. Implement the BCD counter in breadboard and verify the correctness of your design.

to obtain Q(t) to Q(t+1)		the input must be	
		J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



Q_A	Q_B	Q_C	Q_D	Q_A^+	Q_B^+	Q_C^+	Q_D^+
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0

Reset here: 1 ←

Reset: $\sum m(9) = Q_A Q_B' Q_C' Q_D$

J_D & K_D are 1 by observation

J_D				K_D			
1	X	X	1	X	1	1	X
1	X	X	1	X	1	1	X
X	X	X	X	X	X	X	X
1	X	X	X	X	1	X	X

J_A	K_A	J_B	K_B	J_C	K_C	J_D	K_D	repeat dec. trans.
0	x	0	x	0	x	1	x	0→1
0	x	0	x	1	x	x	1	1→2
0	x	0	x	x	0	1	x	2→3
0	x	1	x	x	1	x	1	3→4
0	x	x	0	0	x	1	x	4→5
0	x	x	0	1	x	x	1	5→6
0	x	x	0	x	0	1	x	6→7
1	x	x	1	x	1	x	1	7→8
x	0	0	x	0	x	1	x	8→9
x	1	0	x	0	x	x	1	9→0

$J_A = Q_B Q_C Q_D$

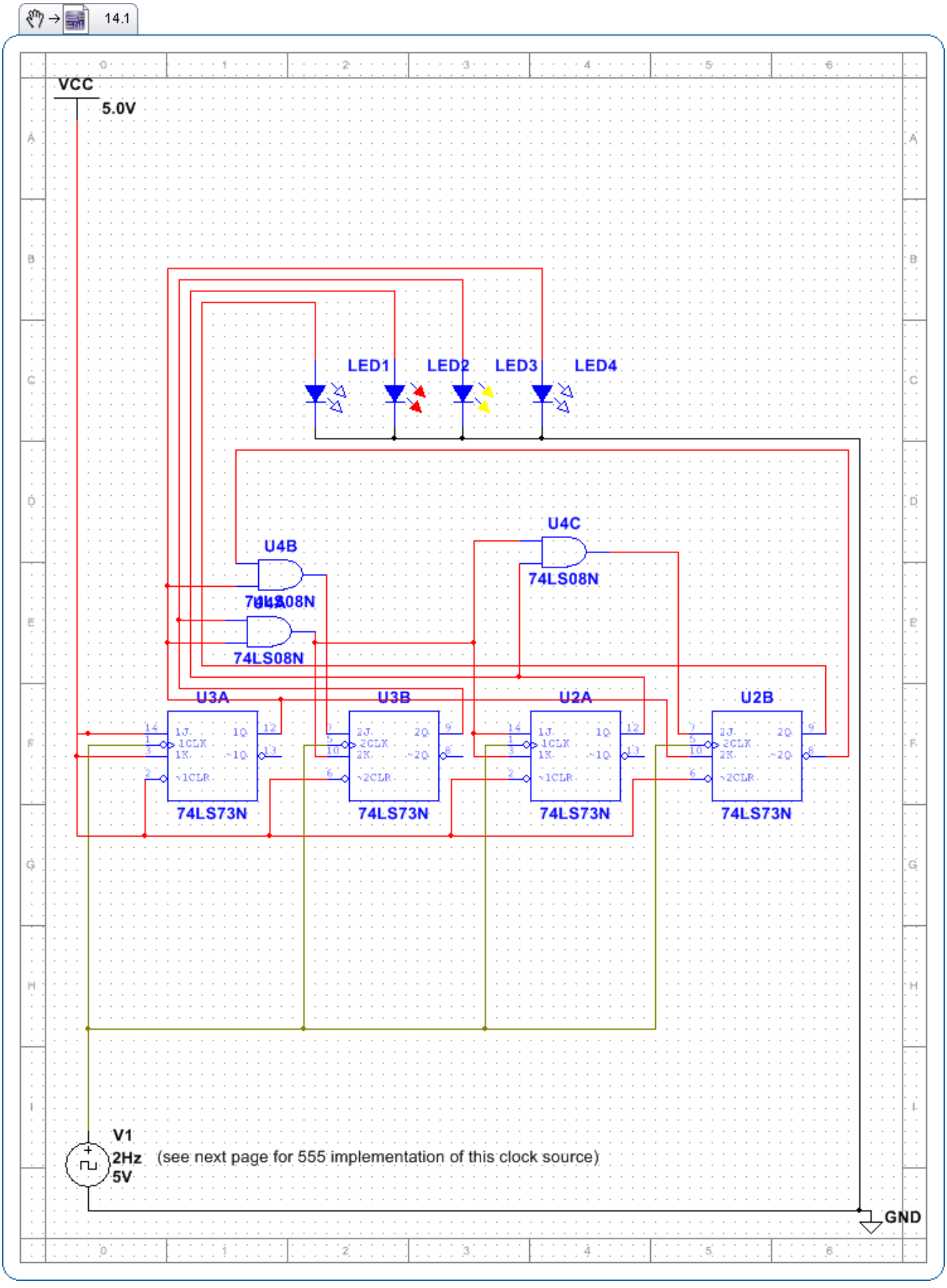
$K_A = Q_D$

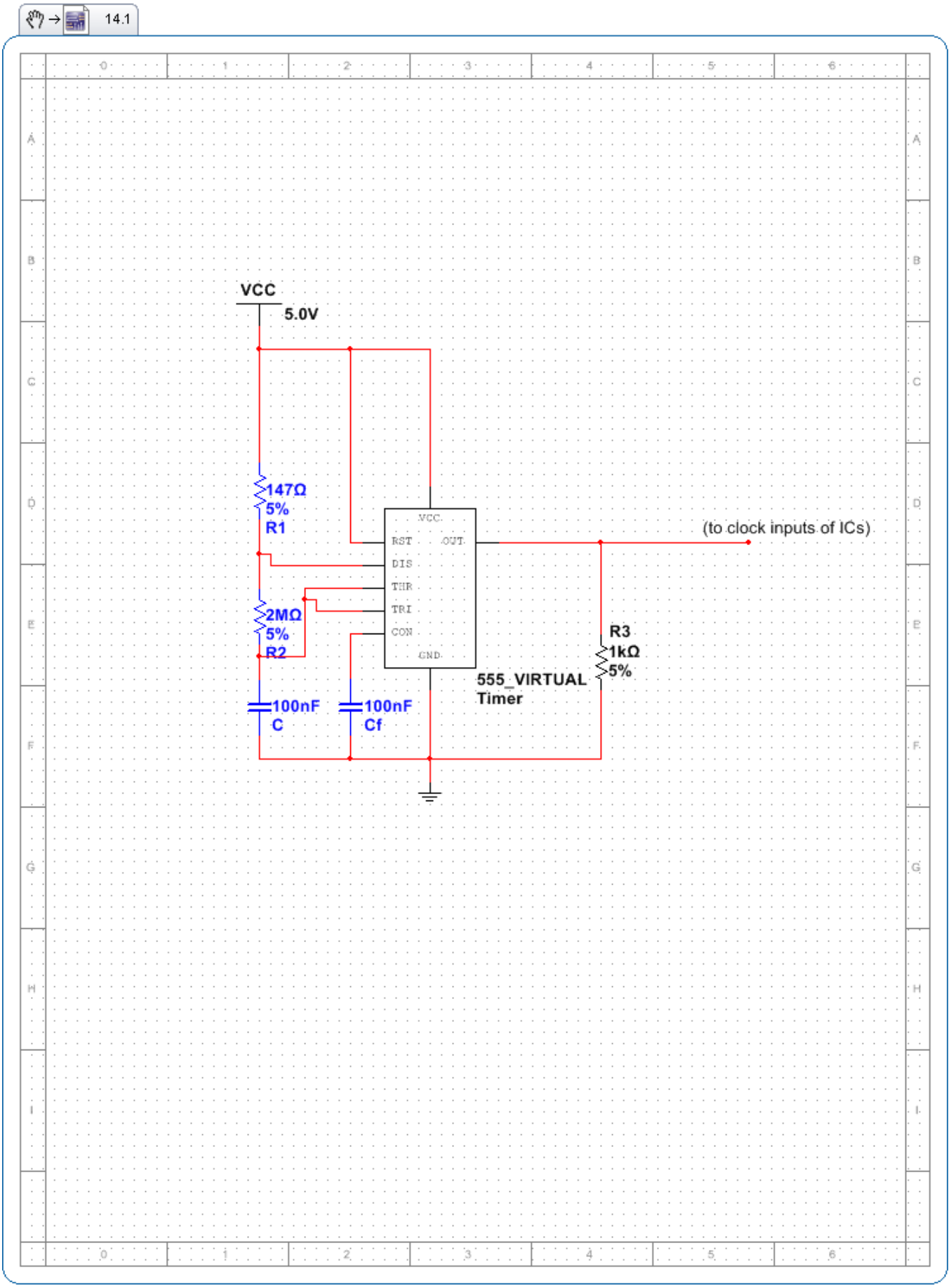
$J_B = Q_C Q_D$

$K_B = Q_C Q_D$

$J_C = Q_A Q_B$

$K_C = Q_C Q_D$


14.1
VCC
5.0V
LED1
LED2
LED3
LED4
U4B
74LS08N
U4C
74LS08N
74LS08N
U3A
U3B
U2A
U2B
74LS73N
74LS73N
74LS73N
74LS73N
V1
2Hz
5V
(see next page for 555 implementation of this clock source)
GND


14.1
VCC
5.0V
147Ω
5%
R1
2MΩ
5%
R2
100nF
C
100nF
Cf
VCC
RST
OUT
DIS
THR
TRI
CON
GND
555_VIRTUAL
Timer
R3
1kΩ
5%
(to clock inputs of ICs)

Results and Discussion:

Initially, the SN74LS76 IC was planned for use. However, supply constraints required use of the SN74LS73 IC as the J-K flip-flop. Additionally, the 555 timer used for the clock signal generator was initially tuned (schematic not shown) to 500 hz. However, it was nearly impossible to determine the correct sequence of the BCD output due to the LED switching quickly from the fast flip-flops and gate logic per clock cycle. Multiplying the capacitance by 10 and increasing the resistance between the discharge and the threshold/trigger pins to 2 MΩ.

Conclusion:

It is possible to design and construct a sequential circuit representing a finite state machine by determining the excitation table of the flip-flop(s) in use, applying that table to the full transition state table (modeled after a Moore state machine diagram) using previously-learned combinational design methods (K-maps, Boolean simplification) to determine the combinational logic and circuit between the flip-flop's I/O.

References

Texas Instruments. (1988, March). *SN74LS73.* Retrieved from http://www.ti.com/lit/ds/symlink/sn74ls73a.pdf

Texas Instruments. (2015, January). *LM555.* Retrieved from http://www.ti.com/lit/ds/symlink/lm555.pdf

EEL3702C
Lab Check off Sheet

Please bring a print out of this sheet before demonstrating your working circuit. Attach this check off sheet with the Lab report.

Note: Lab check off sheet should be signed by the Instructor or TA. Lab reports without the check off sheet will not receive credit.

Name: Peter Dranishnikov
Section: 04
Experiment: 9

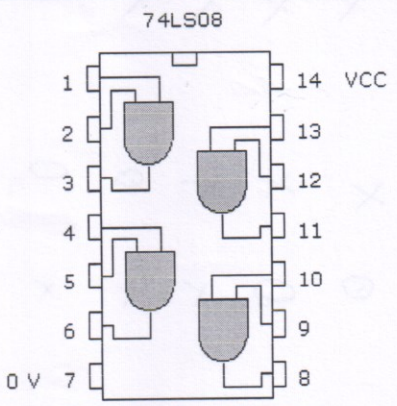
Lab Demonstration Comments:

All works.

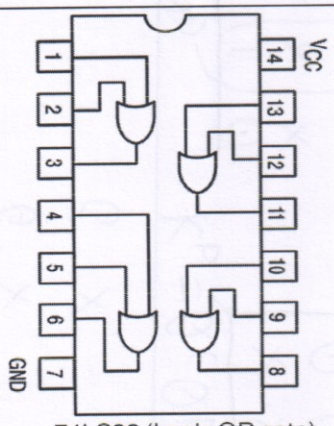
Signature of Instructor/TA:

Date:

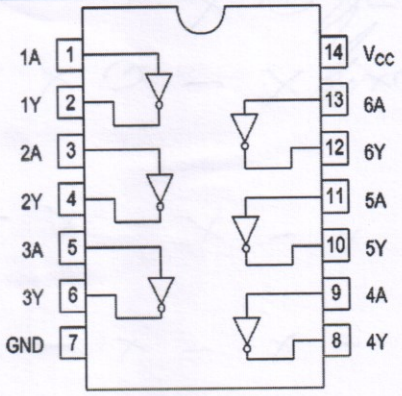
Appendix



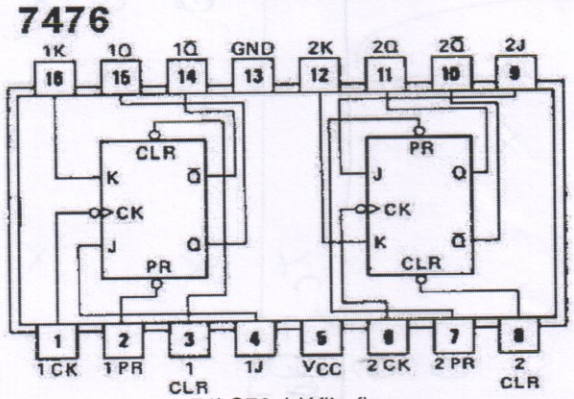
74LS08 (Logic AND gate)



74LS32 (Logic OR gate)

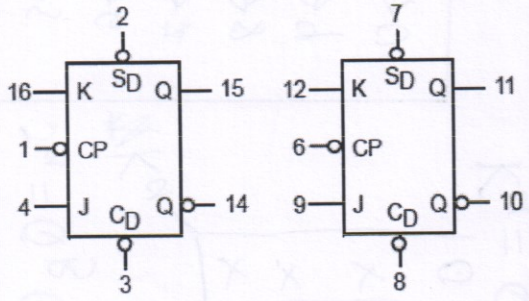


75LS04 (Logic NOT)



74LS76 J-K flip-flop

LOGIC SYMBOL



V_{CC} = PIN 5
GND = PIN 13

Logic Symbol of J-K flip-flop