

Experiment 5: Design and Implementation of Half Adder and Full Adder Circuit(s)

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EEL3702C
Digital Logic Design
Section 04

Professor: Dr. Chandrasekaran

Experiment 5: Design and Implementation of Half Adder and Full Adder Circuit

Objectives:

After completing this experiment, you will be able to

- 1) design and implement the Half Adder circuit
- 2) design and implement the Full Adder Circuit
- 3) synthesize a full and half adder circuit from truth tables

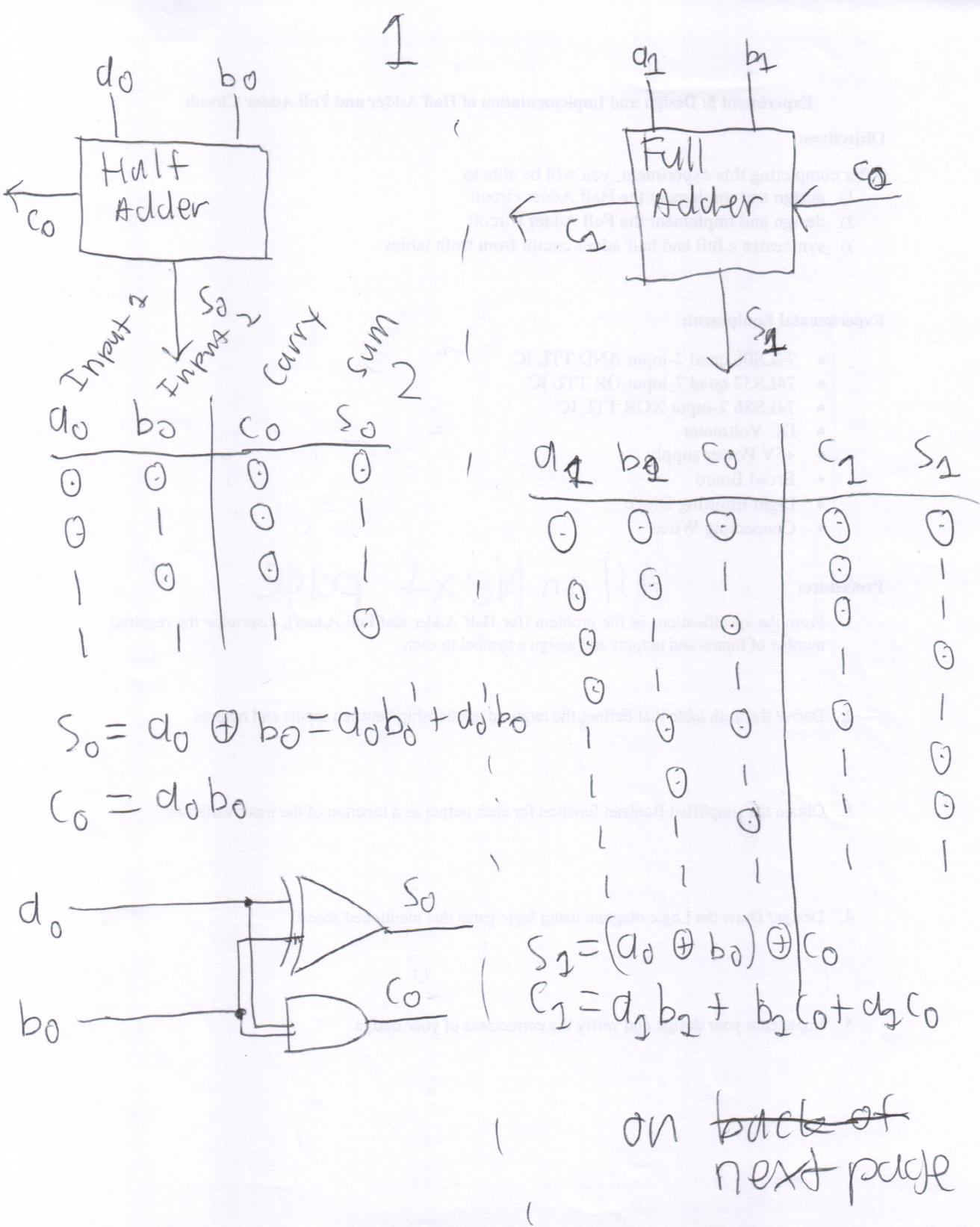
Experimental Equipment:

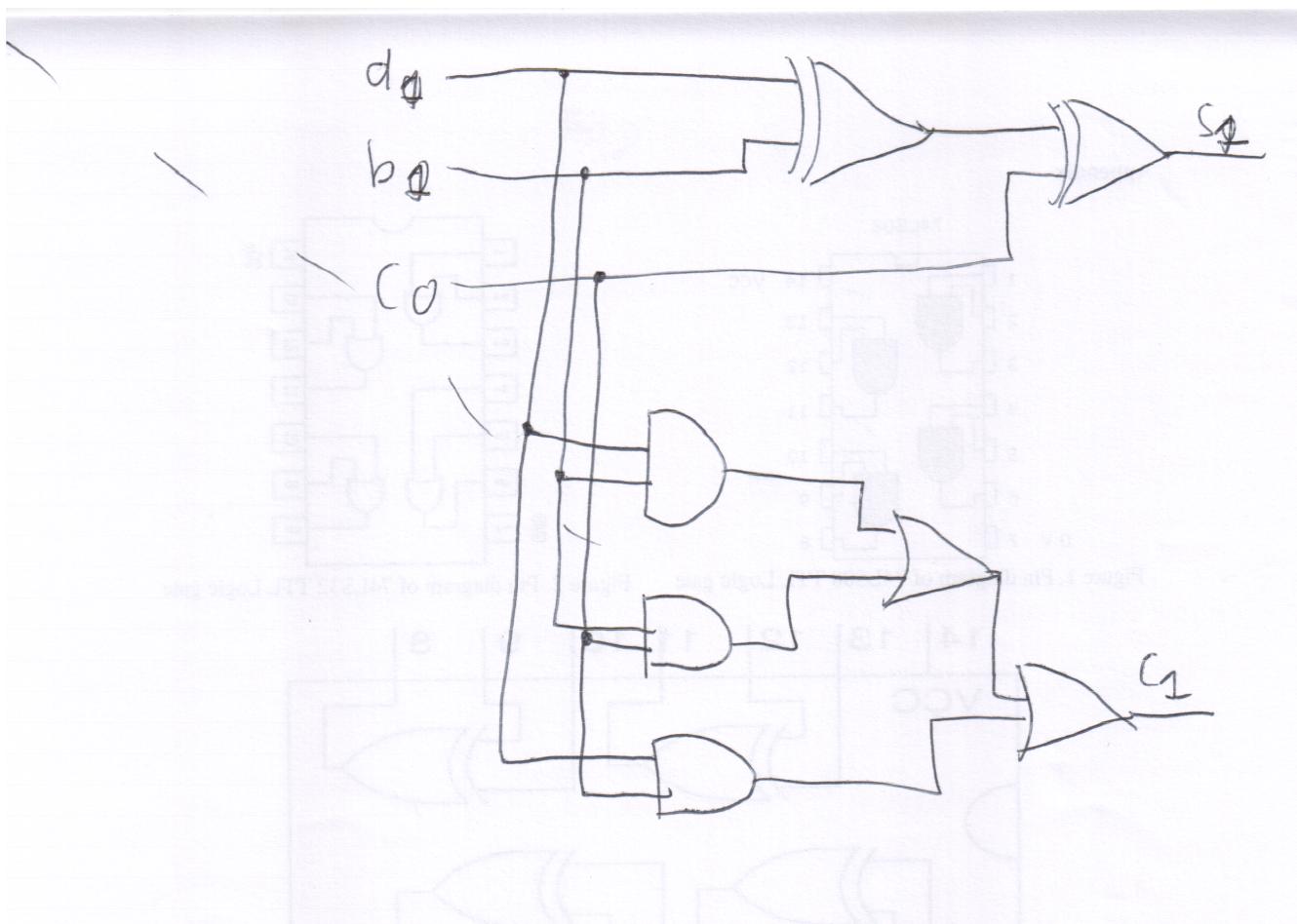
- 74LS08 quad 2-input AND TTL IC
- 74LS32 quad 2-input OR TTL IC
- 74LS86 2-input XOR TTL IC
- DC Voltmeter
- +5V Power supply
- Bread Board
- Light Emitting Diode
- Connecting Wires

Procedure:

All on Next page

1. From the specifications of the problem (for Half Adder and Full Adder), determine the required number of inputs and outputs and assign a symbol to each
2. Derive the truth table that defines the required relationship between inputs and outputs.
3. Obtain the simplified Boolean function for each output as a function of the input variables
4. Design/ Draw the Logic diagram using logic gates that mentioned above
5. Implement your design and verify the correctness of your design.





Appendix

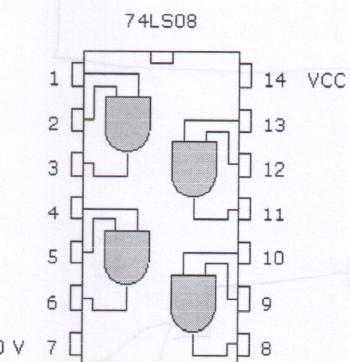


Figure 1. Pin diagram of 74LS08 TTL Logic gate

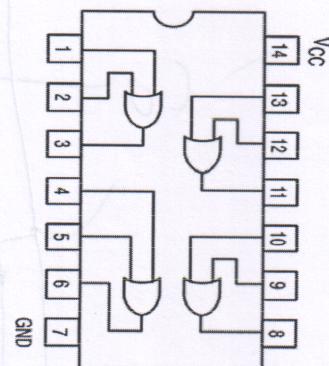


Figure 2. Pin diagram of 74LS32 TTL Logic gate

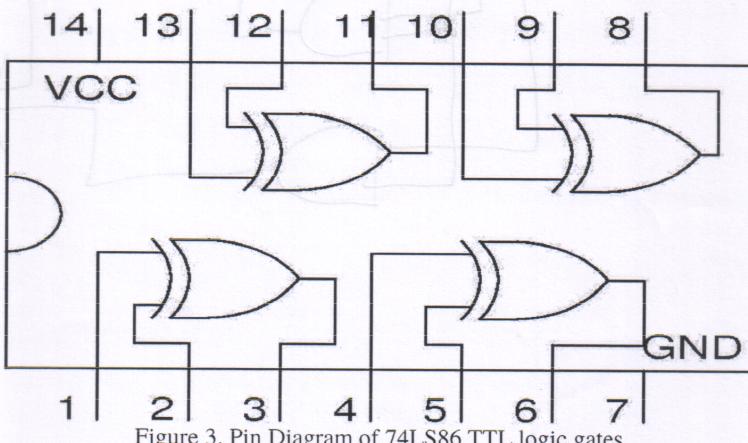


Figure 3. Pin Diagram of 74LS86 TTL logic gates

Please follow the guidelines when you submit your lab report

First Page in your lab report:

- Experiment Number, Experiment Name, Student's Information (Name, ID, etc), and Course Information (Course No, Course Title, Course Section etc.)

Second Page in your lab report

- Objectives
- Experimental Equipment
- Methods Description/Procedures (Logic diagram, Truth Table, IC pin diagram)
- Results and Discussion (Actual results and your observation results)
- Conclusion (what you learn from this experiment)
- References (if you use any other sources to write this lab report, please reference it)

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Lab Check off Sheet

Please bring a print out of this sheet before demonstrating your working circuit. Attach this check off sheet with the Lab report.

Note: Lab check off sheet should be signed by the Instructor or TA. Lab reports without the check off sheet will not receive credit.

Name: Peter Dranishnikov
Section: 04
Experiment: 5

Lab Demonstration Comments:

It works
PM

Signature of Instructor/TA:

Date:

Results and Discussion:

The design, implementation, and verification of both a half adder and full adder circuit is experimentally verified using truth tables and the boolean functions derived. The implemented design meets the specifications of the original concept process.

Conclusion:

Any functioning digital logic circuit can be designed and implemented from an original concept by using the method as described in this report.