

Experiment 3

Applications of NAND and NOR Gates

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EEL3702C
Digital Logic Design
Section 04

Experiment 3: Applications of NAND and NOR Gates

Objectives:

- (a) To verify one of the Demorgan's laws by experiment.
- (b) To show how TTL NAND and NOR gates are used to implement any logic functions and to demonstrate the value of Boolean algebra in reducing logic circuits to their minimum configuration.

Experimental Equipments:

- 74LS00 TTL IC (2-input NAND logic gate)
- 74LS02 TTL IC (2-input NOR logic gates)
- 4072 TTL IC (Dual 4-input OR logic gate)
- 74LS20 TTL IC (Dual 4-input NAND logic gate)
- DC Voltmeter
- +5V Power supply
- Connecting wires
- Light Emitting Diode (LED)

Methods/Procedure:

Part 1

1. Choose one of Demorgan's laws (i) $(A + B)' = A'B'$ or (ii) $(AB)' = A' + B'$. Design two circuits separately to perform the function of each side of the chosen Demorgan's law respectively. Students are required to do this as a **pre-lab** work.
2. Construct the circuits according to your design. Using the data switches as inputs, measure the outputs. Record your results in the truth table I and II respectively.
3. Compare the two truth tables and get the conclusion.
4. Repeat 1, 2, and 3 for other DeMorgan's Law and do the same thing.

on back

Table I (Left Hand Side of (i))

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

Table 2 (Right Hand Side of (i))

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	0

NOR

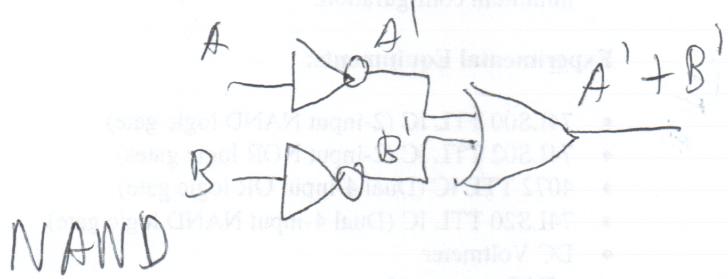
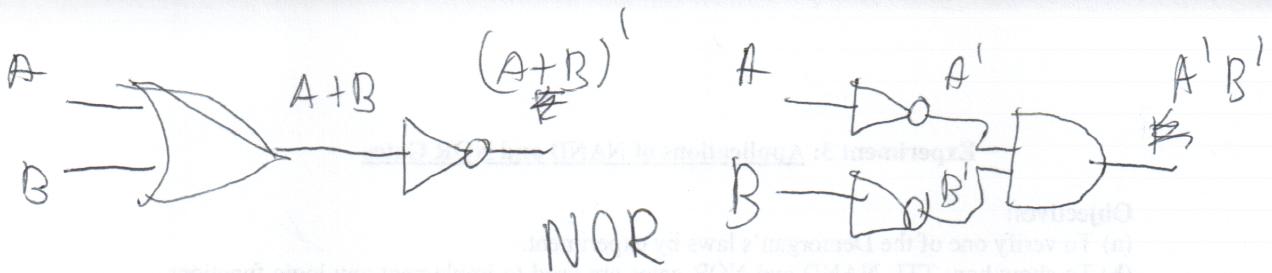


Table III (Left Hand Side of (ii))

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

Table IV (Right Hand Side of (ii))

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

NAND

Part 2

1. Write the output expression of the circuit shown in the figure 1.

$$F = \underline{AC + AD + BC + BD}$$

2. Figure 2 shows the NAND gate implementation of the circuit in Figure 1. Wire the circuit shown in figure 2. Be sure to connect pin 14 to +5 volts and pin 7 to GND on each IC.

3. Apply the inputs A, B, C and D in Table I to the circuit with data switches SW1 through SW4. Measure the output on L1 and record the state for each set of inputs on the left hand F columns in table I.

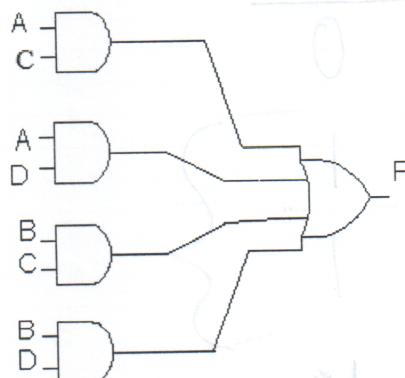


Figure 1

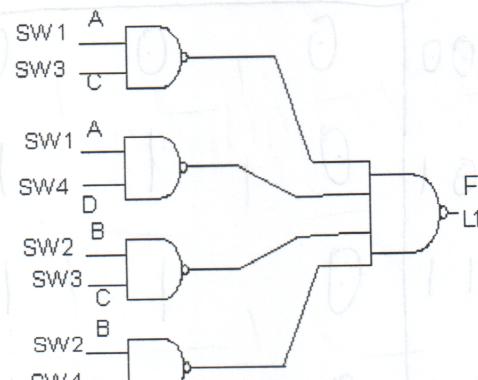


Figure 2

4. Using Boolean algebra, reduce the output equation obtained in step 1. The minimized expression is: (Product of sums form)

$$F = \underline{(A+B)(C+D)}$$

5. Write the output equation of the circuit in figure 3. Compare it to the expression you derived in step 4. $F = \underline{((A+B)'+(C+D)')}$

$$\begin{aligned} &= (A+B)(C+D) \text{ (after simplifying)} \\ &\text{on back of next page} \end{aligned}$$

$$\overline{((A+B)' + (C+D)')}'$$

$$F = AC + AB$$

$$F = AD + AC$$

$$F = AC + AD + BC + BD$$

$$= A(B + B')$$

$$= A(B + B')(C(D + D')) + A(B + B')(C + C')D$$

$$+ (A + A')BC(D + D') + (A' + A)B(C + C')D$$

	$c'b$	$c'd'$	$c'd$	cd	cd'
$A'B'$	00	0	0	0	0
$A'B$	01	0	1	1	1
AB	11	0	1	1	1
AB'	10	0	1	1	1

$$\cancel{c'd'} \quad F' = \cancel{c'b} + A'B'$$

$$F = (C+D)(A+B)$$

6. Construct the circuit shown in figure 3.

7. Apply the inputs shown in table V and record the output state in the right-hand column.

8. Compare the two F output columns in table V and get the conclusion.

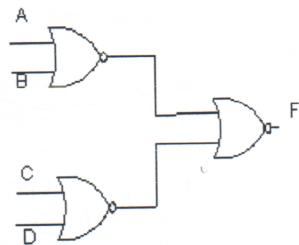


Figure 3.

Table V

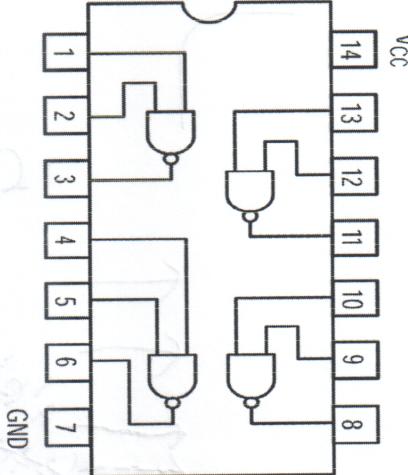
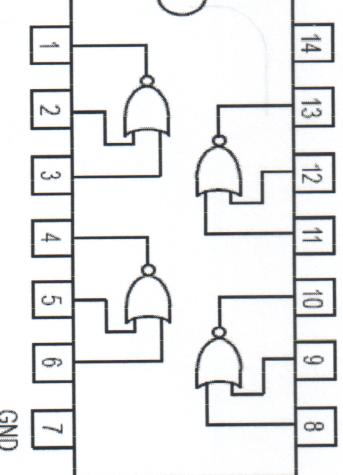
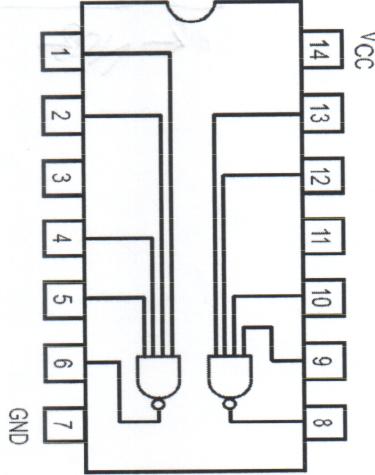
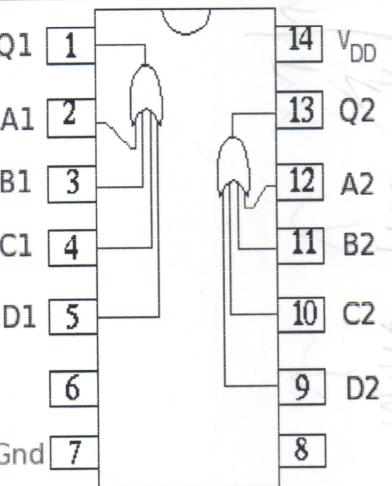
Inputs				Outputs	
A	B	C	D	F (fig2)	F (fig3)
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

$$((A+B)' + (C+D)')' \quad \text{figure 3 simp}$$

$$= ((A+B)(C+D))' = (A+B)(C+D)$$

Appendix

Integrated Circuits (ICs) pin diagram

 <p>74LS00 IC Pin diagram</p>	 <p>74LS02 IC Pin Diagram</p>
 <p>74LS20 IC Pin diagram</p>	 <p>4072 IC Pin diagram</p>

EEL3702C
Lab Check off Sheet

Please bring a print out of this sheet before demonstrating your working circuit. Attach this check off sheet with the Lab report.

Note: Lab check off sheet should be signed by the Instructor or TA. Lab reports without the check off sheet will not receive credit.

Name: Peter Pranishnikov
Section: 04
Experiment: 3

Lab Demonstration Comments:

ALL WORKS
P/02/09

Signature of Instructor/TA:

Date:

Results and Discussion:

In part 1, the first function represented the NOR gate, per the truth table, while the second function represented the NAND gate. In part 2, the function was implemented using NAND-only and NOR-only implementations. Both implementations matched the function's truth table, thus being equivalent forms of the boolean function.

Conclusion:

Using DeMorgan's law of boolean algebra, two universal gates exist. Any boolean function can be implemented exclusively using one of the universal gates. Additionally, the function exclusively implemented in one universal gate can be converted using DeMorgan's law (or bubble pushing) to the other exclusive universal gate implementation. One implementation may be smaller than the other, thus determining which is smaller can be a cost-reducing method for digital logic function design.