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# Lab 2

## Assembly Language 2

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## 1 Objective

The objective of this lab is to be able to write assembly programs that perform variable assignment, data movements, and flow control. You will also learn how to use the GDB Text User Interface (TUI).

## 2 Procedure

### 2.1 Part 1 (Practice variable assignment)

- Step 1. Type the listing in section 4.1.
- Step 2. Assemble and link the program.
- Step 3. Run the simulator and load the program in **avr-gdb**.
- Step 4. Trace the program and observe the changes on the memory and the registers. Make sure to utilize the TUI commands from Section 3.
- Step 5. What does this program do?

### 2.2 Part 2 (Loop and program control)

- Step 1. Type the listing in section 4.2.
- Step 2. Assemble and link the program.
- Step 3. Run the simulator and load the program in **avr-gdb**.
- Step 4. Trace the program and observe the changes on the memory and the registers. Make sure to utilize the TUI commands from Section 3.
- Step 5. What does this program do?

### 2.3 Part 3 (Implementing a simple algorithm)

- Step 1. Type the listing in section 4.3.
- Step 2. Assemble and link the program.
- Step 3. Run the simulator and load the program in **avr-gdb**.
- Step 4. Trace the program and observe the changes on the memory and the registers. Make sure to utilize the TUI commands from Section 3.
- Step 5. What does this program do?

### 2.4 Part 4 (Write your own code)

- Step 1. Write an AVR assembly program that will find the average of 8 unsigned characters (bytes). The values are entered in the same way as the programs provided in the class. (Hint: use division by subtraction).
- Step 2. Assemble and link the program.
- Step 3. Run the simulator and load the program in **avr-gdb**.
- Step 4. Trace the program and observe the changes on the memory and the registers. Make sure to utilize the TUI commands from Section 3.
- Step 5. Did your program perform the required task?
- Step 6. What are the limitations or drawbacks of your code?

### 3 GDB TUI commands

<code>tui enable</code>	Enable the TUI mode
<code>tui disable</code>	Disable the TUI mode
<code>layout &lt;name&gt;</code>	Display the selected layout of TUI. <b>&lt;name&gt;</b> can be one of the following: <ol style="list-style-type: none"><li>1. <b>src</b>: display the source code</li><li>2. <b>asm</b>: display the assembly of the program memory content.</li><li>3. <b>regs</b>: display the registers content</li><li>4. <b>split</b>: display the source code and the assembly of the program memory content.</li></ol>
<code>[ctrl]+[x] [1]</code>	One window
<code>[ctrl]+[x] [2]</code>	Split windows
<code>[ctrl]+[x] [o]</code>	Change window focus ( in split window mode )

## 4 Appendix

### 4.1 Code 1

```

1  .text
2  .org 0x0000
3
4  .set op1, 100020
5  .set op2, 2053
6
7  reset_vector:
8
9          jmp start      ; skip
                      interrupt vector table
10
11  .org 0x0100
12  start:
13  ; get the bytes of operand 1
14          ldi r16, lo8(op1)
15          ldi r17, hi8(op1)
16          ldi r18, hlo8(op1)
17          ldi r19, hhi8(op1)
18
19  ; store operand 1 to m
20          sts m, r16
21          sts m+1, r17
22          sts m+2, r18
23          sts m+3, r19
24
25  ; get the bytes of operand 2
26          ldi r16, lo8(op2)
27          ldi r17, hi8(op2)
28          ldi r18, hlo8(op2)
29          ldi r19, hhi8(op2)
30
31  ; store operand 2 to n
32          sts n, r16
33          sts n+1, r17
34          sts n+2, r18
35          sts n+3, r19
36
37  ; get m
38          lds r16, m
39          lds r17, m+1
40          lds r18, m+2
41          lds r19, m+3
42
43  ; get y
44          lds r20, n
45          lds r21, n+1
46          lds r22, n+2
47          lds r23, n+3

```

```
47
48 ; Add x+y
49         add r16, r20
50         adc r17, r21
51         adc r18, r22
52         adc r19, r23
53
54 ; store addition result into o
55         sts o, r16
56         sts o+1, r17
57         sts o+2, r18
58         sts o+3, r19
59
60 ; infinite loop
61 infiniteloop:
62         rjmp infiniteloop
63
64 .data
65 .org 0x00A0
66 m:
67         .skip 4, 0
68 n:
69         .skip 4, 20
70 o:
71         .skip 4, 40
```

## 4.2 Code 2

```
1  .global start
2  .text
3  .org 0x0000
4
5  .set op1, 15
6  .set op2, 16
7
8  reset_vector:
9
10                                     jmp start      ; skip
11                                     interrupt vector table
12
13  .org 0x0100
14  start:
15                                     ldi    r16, lo8(op1)
16                                     ldi    r17, lo8(op2)
17                                     ldi    r18, 0
18                                     ldi    r19, 1
19
20  do:
21                                     add    r18, r16
22                                     sub    r17, r19
23
24  while:
25                                     brne  do
26
27  ; infinite loop
28  infiniteloop:
29                                     rjmp  infiniteloop
30
31  .end
32
33  what does this code do?
```

### 4.3 Code 3

```
1  .global start
2  .text
3  .org 0x0000
4
5  .set op1, 150
6  .set op2, 12
7  .set op3, 230
8
9  reset_vector:
10         jmp start      ; skip interrupt vector table
11
12  .org 0x0100
13  start:
14         ldi r16, lo8(op1)
15         ldi r17, lo8(op2)
16         ldi r18, lo8(op3)
17         mov r20, r16      ; minimum
18         mov r21, r16      ; maximum
19         mov r19, r16
20         sub r19, r17
21         breq skip1
22         brlo less1
23         mov r20, r17
24         rjmp skip1
25  less1:
26         mov r21, r17
27  skip1:
28         mov r19, r18
29         sub r19, r21
30         brlo skip2
31         mov r21, r18
32  skip2:
33         mov r19, r18
34         sub r19, r20
35         brlo less2
36         rjmp skip3
37  less2:
38         mov r20, r18
39  skip3:
40         rjmp skip3
41
42  .end
```