EEL4768C Lab Assignment 7 (40 points)
Due 7/31/2018, 11:59 pm on Canvas

Implement the data memory shown below in VHDL/Verilog. Write a value into the memory location and read a value from the memory location. Write always happens on the rising edge of the clock and when WE (write enable) is set high. The data and address lines are 32 bits wide.