专题8-存储器控制

一、内存分类

1.1、DRAM（（Dynamic Random Access Memory），即动态随机存取存储器。）

基本原件是小电容，电容可以在两个极 板上保留电荷，但是需要定期的充电（刷新），否则数据会丢失。缺点：由于要定期刷新存储介质，存取速度较慢。

1.2、SRAM（（Static Random Access Memory），即静态随机存取存储器。）

是一种具有静止存取功能的内存，不需要 定期刷新电路就能保存它内部存储的数据。其优点： 存取速度快; 但是缺点是：功耗大，成本高。常用作 存储容量不高，但存取速度快的场合，比如stepping stone.

1.3、SDRAM

SDRAM(Synchronous Dynamic Random Access Memory):同步动态随机存储器.

同步: 内存工作需要有同步时钟，内部的命令的发送 与数据的传输都以该时钟为基准。

动态：存储阵列需要不断的刷新来保证数据不丢失。

随机：是指数据不是线性依次存储，而是自由指定地 址进行数据读写。

1.4、DDR（(Double Data Rate SDRAM)，即“双倍速率同步 动态随机存储器”。）

与早期的SDRAM相比，DDR 除了可 以在时钟脉冲的上升沿传输数据，还可以在下降沿传输信 号，这意味着在相同的工作频率下，DDR 的理论传输速率为SDRAM的两倍。

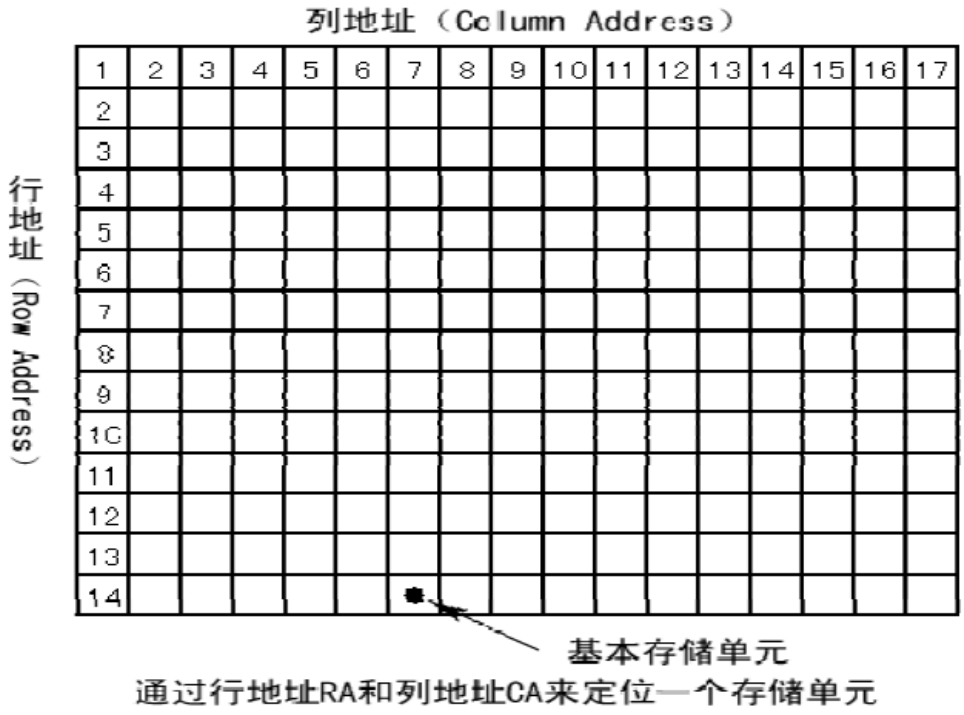
DDR2 则在DDR 的基础上再次进行了改进，使得数据传输速率在DDR 的基础上再次翻倍。

二、内存内部结构

2.1、表结构

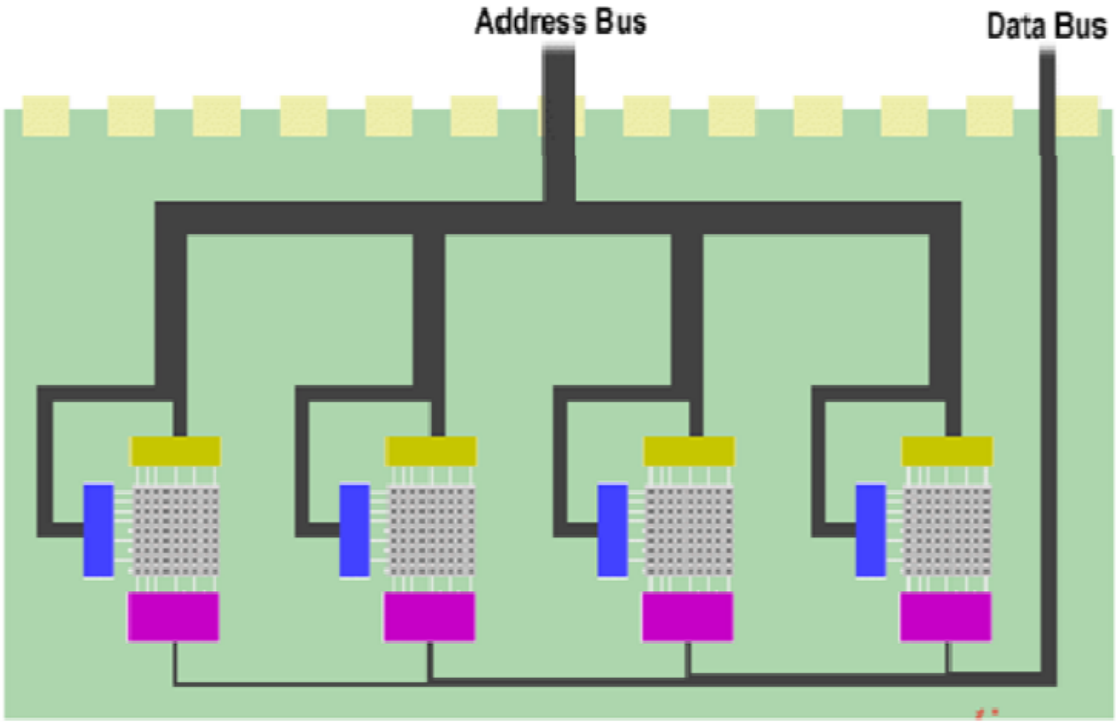
内存的内部如同表格,数据 就存放在每个单元格中。数据读写时，先指定行号(行地址)，再指定列号(列地址) ，我们就可以准确地找到所需要的单元格。而这张 表格的称为:

Logical Bank(L-Bank).



2.2、L-Bank（Logic Bank）

由于技术、成本等原因，一块内存不可能把所有的单元 格都做到一个L-Bank，现在内存内部基本都会分割成4个L-Bank。



2.3、寻址信息

2.3.1、L-BANK选择信号

2.3.2、行地址

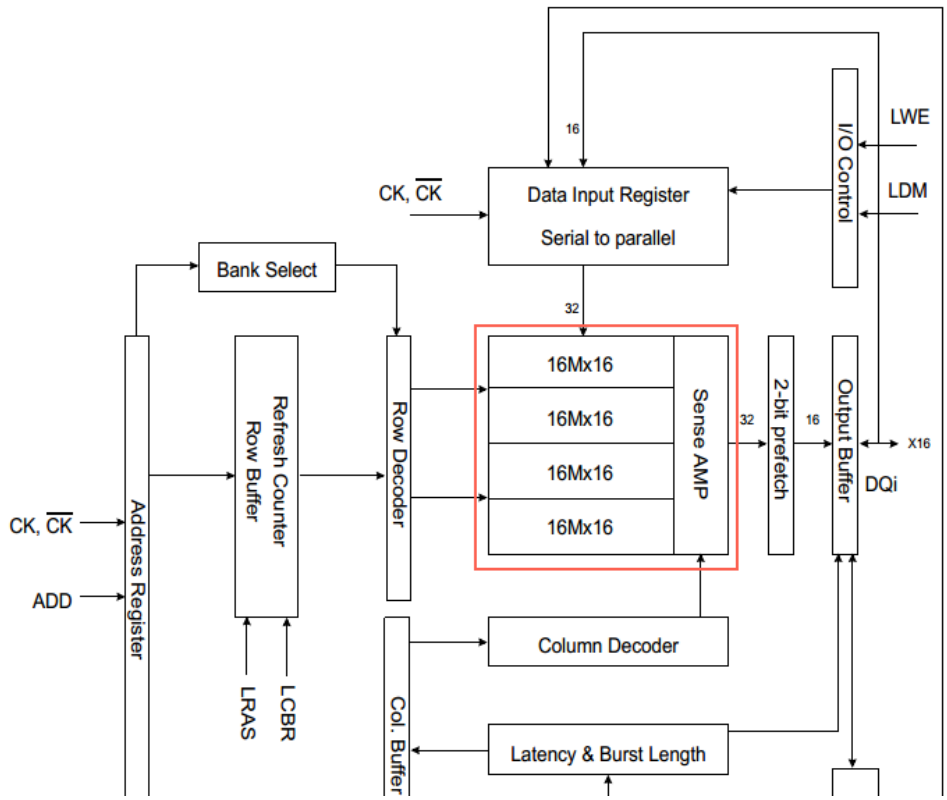
2.3.3、列地址

2.3.4、内存容量计算公式

内存容量=4*L-BANK容量

=4*（单元格数目*单元格容量）

5. FUNCTIONAL BLOCK DIAGRAM



三、6410内存初始化

3.1、6410地址空间

3.1.1、S3C6410处理器拥32位 地址总线，其寻址空间为4GB。其中高2GB为保留区，低2GB区域又可划分 为两部分：主存储区和外设区。

区域	地址分布	大小
保留区	0x80000000~0xFFFFFFFF	2GB
外设区	0x70000000~0x7FFFFFFF	256MB
主存储区	0x00000000~0x6FFFFFFF	1792MB

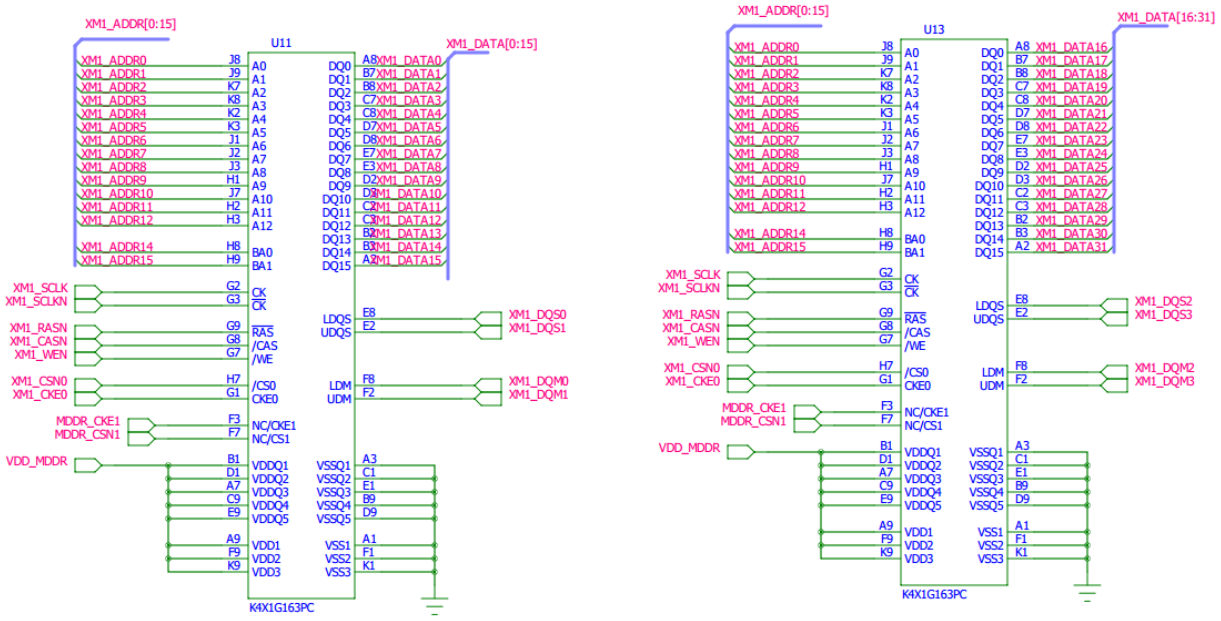
3.1.2、主存储器划分

区域	类型	地址分布	大小
动态存储区	Dynamic memory 2 * BANK	0x50000000~0x6FFFFFFF	2 *256MB
保留区	Reserved 2 * BANK	0x40000000~0x4FFFFFFF	2 *128MB
静态存储区	Static memory 6 * BANK	0x10000000~0x3FFFFFFF	6 *128MB
内部存储区	IRAM	0x0C000000~0x0FFFFFFF	64MB(8KB)
	IROM	0x08000000~0x0BFFFFFF	64MB(32KB)
Boot镜像区	Boot Image	0x00000000~0x07FFFFFF	128MB

3.2、内存芯片硬件连接

Table 5-1. Memory Port 1 Pin Description

Signal	Type	Description
Xm1SCLK	Output	Memory clock
Xm1SCLKn	Output	Memory clock (negative)
Xm1CKE[1:0]	Output	Clock enable per chip
Xm1CSN[1:0]	Output	Chip select per chip (active low)
Xm1RAS	Output	Row address strobe (active low)
Xm1CAS	Output	Column address strobe (active low)
Xm1WEN	Output	Write enable (active low)
Xm1ADDR[13:0]	Output	Address bus
Xm1ADDR[15:14]	Output	Bank select
Xm1DATA[31:0]	Inout	Data bus
Xm1DQM[3:0]	Output	Data bus mask bits
Xm1DQS[3:0]	Inout	Data strobe inout, DDR and mDDR only



3. Address configuration

Organization	Bank Address	Row Address	Column Address
64Mx16	BA0,BA1	A0 - A13	A0 - A9

3.3、芯片手册导读

5.4.1 DRAM CONTROLLER INITIALIZATION SEQUENCE

• Program memc_cmd to '3'b100', which makes DRAM Controller enter 'Config' state.
• Write memory timing parameter, chip configuration, and id configuration registers.
• Wait 200us to allow SDRAM power and clock to stabilize. However, when CPU starts working, power and clock would already be stabilized.
• Execute memory initialization sequence.
• Program memc_cmd to '3'b000', which makes DRAM Controller enter 'Ready' state.
• Check memory status field in memc_stat until memory status becomes '2'b01', which means 'Ready'.

5.4.2 SDR/MOBILE SDR SDRAM INITIALIZATION SEQUENCE

• Program mem_cmd in direct_cmd to '2'b10', which makes DRAM Controller issue 'NOP' memory command.
• Program mem_cmd in direct_cmd to '2'b00', which makes DRAM Controller issue 'Prechargeall' memory command.
• Program mem_cmd in direct_cmd to '2'b11', which makes DRAM Controller issue 'Autorefresh' memory command.
• Program mem_cmd in direct_cmd to '2'b11', which makes DRAM Controller issue 'Autorefresh' memory command.
• If memory type is mobile SDR SDRAM,
– Program mem_cmd to '2'b10' in direct_cmd, which makes DRAM Controller issue 'MRS' memory command
– Bank address for EMRS must be set.
• Program mem_cmd to '2'b10' in direct_cmd, which makes DRAM Controller issue 'MRS' memory command.
– Bank address for MRS must be set.

5.4.3 DDR/MOBILE DDR SDRAM INITIALIZATION SEQUENCE

• Program mem_cmd in direct_cmd to ‘2’b10’, which makes DRAM Controller issue ‘NOP’ memory command.
• Program mem_cmd in direct_cmd to ‘2’b00’, which makes DRAM Controller issue ‘Prechargeall’ memory command.
• Program mem_cmd in direct_cmd to ‘2’b11’, which makes DRAM Controller issue ‘Autorefresh’ memory command.
• Program mem_cmd in direct_cmd to ‘2’b11’, which makes DRAM Controller issue ‘Autorefresh’ memory command.
• Program mem_cmd to ‘2’b10’ in direct_cmd, which makes DRAM Controller issue ‘MRS’ memory command
– Bank address for EMRS must be set.
• Program mem_cmd to ‘2’b10’ in direct_cmd, which makes DRAM Controller issue ‘MRS’ memory command.
– Bank address for MRS must be set.

四、实现OK6410内存初始化

```
.text
.global men_ctrl_asm_init


#define HCLK 133 /* 133MHz */
#define DDR_tREFRESH    7800
#define DDR_tRAS        45
#define DDR_tRC         68
#define DDR_tRCD        23
#define DDR_tRFC        80
#define DDR_tRP         23
#define DDR_tRRD        15
#define DDR_tWR         15
#define DDR_tXSR        120
#define DDR_CASL        3

#define DMC_DDR_REFRESH_PRD     ((DDR_tREFRESH * HCLK / 1000) + 1)
#define DMC_DDR_CAS_LATENCY     (DDR_CASL << 1)
#define DMC_DDR_t_DQSS  1
#define DMC_DDR_t_MRD   2
#define DMC_DDR_t_RAS   ((DDR_tRAS * HCLK / 1000) + 1)
#define DMC_DDR_t_RC    ((DDR_tRC * HCLK / 1000) + 1)
#define DMC_DDR_t_RCD   ((DDR_tRCD * HCLK / 1000) + 1)
#define DMC_DDR_schedule_RCD    ((DMC_DDR_t_RCD-3)  << 3)
#define DMC_DDR_t_RFC           ((DDR_tRFC * HCLK / 1000) + 1)
#define DMC_DDR_schedule_RFC    ((DMC_DDR_t_RFC-3)  << 5)
#define DMC_DDR_t_RP            ((DDR_tRP * HCLK / 1000) + 1)
#define DMC_DDR_schedule_RP     ((DMC_DDR_t_RP-3)  << 3)
#define DMC_DDR_t_RRD           ((DDR_tRRD * HCLK / 1000) + 1)
#define DMC_DDR_t_WR            ((DDR_tWR * HCLK / 1000) + 1)
#define DMC_DDR_t_WTR   4
#define DMC_DDR_t_XP    2
#define DMC_DDR_t_XSR   ((DDR_tXSR * HCLK / 1000) + 1)
#define DMC_DDR_t_ESR   DMC_DDR_t_XSR


#define DMC_MEMC_CFG    0x10012 /* Supports one CKE control, Chip 1, Burst 4, Row 13 /Column 10 bit */
#define DMC_MEMC_CFG2   0xb45
#define DMC_CHIP0_CFG   0x150f0
#define DMC_DDR_32_CFG  0x0

#define MEM_SYS_CFG 0x7e00f120
#define DMC1_BASE 0x7e001000


#define DMC_MEMC_CMD_OFFSET     0x04
#define DIRECT_CMD_OFFSET       0x08

#define DMC_REFRESH_PRD_OFFSET  0x10
#define DMC_CAS_LATENCY_OFFSET  0x14
#define DMC_T_DQSS_OFFSET       0x18
#define DMC_T_MRD_OFFSET        0x1c
#define DMC_T_RAS_OFFSET        0x20
#define DMC_T_RC_OFFSET         0x24
#define DMC_T_RCD_OFFSET        0x28
```

```
56 #define DMC_T_RFC_OFFSET        0x2c
57 #define DMC_T_RP_OFFSET         0x30
58 #define DMC_T_RRD_OFFSET        0x34
59 #define DMC_T_WR_OFFSET         0x38
60 #define DMC_T_WTR_OFFSET        0x3c
61 #define DMC_T_XP_OFFSET         0x40
62 #define DMC_T_XSR_OFFSET        0x44
63 #define DMC_T_ESR_OFFSET        0x48
64
65 #define DMC_MEMC_CFG_OFFSET     0x0c
66 #define DMC_MEMC_CFG2_OFFSET    0x4c
67 #define DMC_CHIP_0_CFG_OFFSET   0x200
68 #define DMC_USER_CONFIG_OFFSET  0x304
69
70 #define DMC_MEMC_STATUS_OFFSET  0x00
71
72 men_ctrl_asm_init:
73         @Set data pin
74         ldr r0, =MEM_SYS_CFG
75         mov r1, #0xd
76         str r1, [r0]
77
78         @Make DMC into config state
79         ldr r0, =DMC1_BASE
80         ldr r1, =0x04
81         str r1, [r0, #DMC_MEMC_CMD_OFFSET]
82
83         @Config registers
84
85         ldr r1, =DMC_DDR_REFRESH_PRD
86         str r1, [r0, #DMC_REFRESH_PRD_OFFSET]
87
88         ldr r1, =DMC_DDR_CAS_LATENCY
89         str r1, [r0, #DMC_CAS_LATENCY_OFFSET]
90
91         ldr r1, =DMC_DDR_t_DQSS
92         str r1, [r0, #DMC_T_DQSS_OFFSET]
93
94         ldr r1, =DMC_DDR_t_MRD
95         str r1, [r0, #DMC_T_MRD_OFFSET]
96
97
98         ldr r1, =DMC_DDR_t_RAS
99         str r1, [r0, #DMC_T_RAS_OFFSET]
100
101         ldr r1, =DMC_DDR_t_RC
102         str r1, [r0, #DMC_T_RC_OFFSET]
103
104         ldr r1, =DMC_DDR_t_RCD
105         ldr r2, =DMC_DDR_schedule_RCD
106         orr r1, r1, r2
107         str r1, [r0, #DMC_T_RCD_OFFSET]
108
109         ldr r1, =DMC_DDR_t_RFC
110         ldr r2, =DMC_DDR_schedule_RFC
111         orr r1, r1, r2
112         str r1, [r0, #DMC_T_RFC_OFFSET]
113
114         ldr r1, =DMC_DDR_t_RP
115         ldr r2, =DMC_DDR_schedule_RP
116         orr r1, r1, r2
117         str r1, [r0, #DMC_T_RP_OFFSET]
118
119         ldr r1, =DMC_DDR_t_RRD
120         str r1, [r0, #DMC_T_RRD_OFFSET]
121
122         ldr r1, =DMC_DDR_t_WR
123         str r1, [r0, #DMC_T_WR_OFFSET]
```

```
124
125         ldr r1, =DMC_DDR_t_WTR
126         str r1, [r0, #DMC_T_WTR_OFFSET]
127
128         ldr r1, =DMC_DDR_t_XP
129         str r1, [r0, #DMC_T_XP_OFFSET]
130
131         ldr r1, =DMC_DDR_t_XSR
132         str r1, [r0, #DMC_T_XSR_OFFSET]
133
134         ldr r1, =DMC_DDR_t_ESR
135         str r1, [r0, #DMC_T_ESR_OFFSET]
136
137         ldr r1, =DMC_MEMC_CFG
138         str r1, [r0, #DMC_MEMC_CFG_OFFSET]
139
140         ldr r1, =DMC_MEMC_CFG2
141         str r1, [r0, #DMC_MEMC_CFG2_OFFSET]
142
143         ldr r1, =DMC_CHIP0_CFG
144         str r1, [r0, #DMC_CHIP_0_CFG_OFFSET]
145
146         ldr r1, =DMC_DDR_32_CFG
147         str r1, [r0, #DMC_USER_CONFIG_OFFSET]
148
149         @DMC0 DDR Chip 0 configuration direct command reg
150
151         @NOP
152         ldr r1, =0xc0000
153         str r1, [r0, #DIRECT_CMD_OFFSET]
154
155         @Precharg all
156         ldr r1, =0x0
157         str r1, [r0, #DIRECT_CMD_OFFSET]
158
159         @Autore fresh 2 time
160         ldr r1, =0x40000
161         str r1, [r0, #DIRECT_CMD_OFFSET]
162         str r1, [r0, #DIRECT_CMD_OFFSET]
163
164         @MRS
165         ldr r1, =0xa0000
166         str r1, [r0, #DIRECT_CMD_OFFSET]
167
168         @Mode reg
169         ldr r1, =0x080032
170         str r1, [r0, #DIRECT_CMD_OFFSET]
171
172         ldr r1, =0x0
173         str r1, [r0, #DMC_MEMC_CMD_OFFSET]
174
175 check_dmc1_ready:
176         ldr r1, [r0, #DMC_MEMC_STATUS_OFFSET]
177         mov r2, #0x3
178         and r1, r1, r2
179         cmp r1, #0x1
180         bne check_dmc1_ready
181         nop
182
183         mov pc, lr
```

首先，需要配置内存子系统配置寄存器。

3.4.2.10 Memory controller status register

Memory controller status registers must be initialized by software except MEM_CFG_STAT.

REGISTER	ADDRESS	R/W	DESCRIPTION	RESET VALUE
MEM_SYS_CFG	0x7E00_F120	R/W	Memory Subsystem configuration register	0x0000_0080
RESERVED	0x7E00_F124	R/W	RESERVED	0x0000_0000
QOS_OVERRIDE1	0x7E00_F128	R/W	DMC1 QOS Override register	0x0000_0000
MEM_CFG_STAT	0x7E00_F12C	R	Memory Subsystem setup status register	0x0000_0000

<table>
<tr><td>EBI_PRI</td><td>[11]</td><td>Set EBI priority scheme.
0 = Fixed priority scheme.
1 = Circular priority scheme.</td><td>0</td></tr>
<tr><td>EBI_FIX_PRI</td><td>[10:8]</td><td>Set EBI fixed priority setting.
<table>
<tr><td></td><td>Highest <-> Lowest</td></tr>
<tr><td>0,6,7</td><td>SROMC - OneNANDC CS0 - OneNANDC CS1 – NFCON – CFCON</td></tr>
<tr><td>1</td><td>OneNANDC CS0 – OneNANDC CS1 – SROMC – NFCON – CFCON</td></tr>
<tr><td>2</td><td>OneNANDC CS1 – NFCON – SROMC - OneNANDC CS0 – CFCON</td></tr>
<tr><td>3</td><td>NFCON – SROMC - OneNANDC CS0 - OneNANDC CS1 – CFCON</td></tr>
<tr><td>4</td><td>CFCON – SROMC - OneNANDC CS0 - OneNANDC CS1 – NFCON</td></tr>
<tr><td>5</td><td>SROMC - OneNANDC CS0 - OneNANDC CS1 – NFCON – CFCON</td></tr>
</table></td><td>000</td></tr>
<tr><td>ADDR_EXPAND (CFG_SROM_ADDR_EXPAND_To</td><td>[7]</td><td>Set usage of Xm1DATA[31:16] pins.
0 = Xm1DATA[26:16] pins are used for DMC1 upper halfword</td><td>1</td></tr>
<tr><td>MP0_CS_CFG</td><td>[5:0]</td><td>Set static memory chip selection multiplexing of memory port 0.
Setting for MP0_CS_CFG[0] and MP0_CS_CFG[2] are ignored. Distinguishing OneNANDC and NFCON is done by XSELNAND pin value instead of MP0_CS_CFG[0] and MP0_CS_CFG[2]. When XSELNAND is 0, OneNANDC is selected. When XSELNAND is 1, NFCON is selected.
When OneNAND booting (OM[4:1] = 0110) is selected, the setting values of MP0_CS_CFG[1] and MP0_CS_CFG[3] are ignored and Xm0CSn[2] and Xm0CSn[3] are used as OneNANDC CS0 and OneNANDC CS1. In this case, XSELNAND should be set to 0.
<table>
<tr><td></td><td colspan="6">MP0_CS_CFG</td><td></td></tr>
<tr><td></td><td>[5]</td><td>[4]</td><td>[3]</td><td>[2]</td><td>[1]</td><td>[0]</td><td></td></tr>
<tr><td>Xm0CSn[0]</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>SROMC CS0</td></tr>
<tr><td>Xm0CSn[1]</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>SROMC CS1</td></tr>
<tr><td rowspan="3">Xm0CSn[2]</td><td>-</td><td>-</td><td>-</td><td>-</td><td>1</td><td>-</td><td>SROMC CS2</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>-</td><td>OneNANDC CS0</td></tr>
<tr><td>-</td><td>-</td><td>-</td><td>-</td><td>0</td><td>-</td><td>NFCON CS0</td></tr>
<tr><td rowspan="3">Xm0CSn[3]</td><td>-</td><td>-</td><td>1</td><td>-</td><td>-</td><td>-</td><td>SROMC CS3</td></tr>
<tr><td>-</td><td>-</td><td>0</td><td>-</td><td>-</td><td>-</td><td>OneNANDC CS1</td></tr>
<tr><td>-</td><td>-</td><td>0</td><td>-</td><td>-</td><td>-</td><td>NFCON CS1</td></tr>
<tr><td rowspan="2">Xm0CSn[4]</td><td>-</td><td>0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>SROMC CS4</td></tr>
<tr><td>-</td><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>CFCON CS0</td></tr>
<tr><td rowspan="2">Xm0CSn[5]</td><td>0</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>SROMC CS5</td></tr>
<tr><td>1</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>CFCON CS1</td></tr>
</table></td><td>0x00</td></tr>
</table>

Note) 6410X PoP A type doesn't support NAND Flash. Don't care the description regarding NAND Flash.
6410X PoP D type doesn't support OneNAND Flash. Don't care the description regarding OneNAND Flash.

其中，最重要的一位是MEM_SYS_CFG [7] ，设置数据位高16位的作用，使用两个DDR应该将其设置为上半字。

Set usage of Xm1DATA[31:16] pins.
0 = Xm1DATA[26:16] pins are used for DMC1 upper halfword

4.1、写 '3' b100' 到memc_cmd ，使DRAM控制器进入配置状态。

5.5.2 DRAM CONTROLLER COMMAND REGISTER

Register	Address	R/W	Description	Reset Value
P1MEMCCMD	0x7E001004	W	32-bit DRAM controller command register	

PnMEMCCMD	Bit	Description	Initial State
	[31:3]	Undefined. Write as Zero	
Memc_cmd	[2:0]	Changes the state of the DRAM controller 000 = Go 001 = Sleep 010 = Wakeup 011 = Pause 100 = Configure101~111 = Reserved	

4.2、写内存时序参数寄存器，芯片配置寄存器，ID配置寄存器。

4.2.1、首先需要根据使用的DDR型号的手册，找到一些重要信息，如下：

1. FEATURES

- VDD/VDDQ = 1.8V/1.8V
- Double-data-rate architecture; two data transfers per clock cycle
- Bidirectional data strobe(DQS)
- Four banks operation
- Differential clock inputs(CK and $\overline{CK}$)
- MRS cycle with address key programs
  - CAS Latency (3)
  - Burst Length (2, 4, 8, 16)
  - Burst Type (Sequential & Interleave)
- EMRS cycle with address key programs
  - Partial Array Self Refresh (Full, 1/2, 1/4 Array)
  - Output Driver Strength Control (Full, 1/2, 1/4, 1/8)
- Internal Temperature Compensated Self Refresh
- All inputs except data & DM are sampled at the positive going edge of the system clock(CK).
- Data I/O transactions on both edges of data strobe, DM for masking.
- Edge aligned data output, center aligned data input.
- No DLL; CK to DQS is not synchronized.
- LMD, UMD for write masking only.
- Auto refresh duty cycle
  - 7.8us for -25 to 85 °C

7800ns

K4X1G163PC - L(F)E/G **Mobile DDR SDRAM**

14. AC Timming Parameters & Specifications

Parameter		Symbol	DDR333		DDR266		Unit	Note
			Min	Max	Min	Max		
Clock cycle time	CL=2	tCK	12.0		12.0		ns	
	CL=3		6		7.5			
Row cycle time		tRC	60		67.5		ns	
Row active time		tRAS	42	70,000	45	70,000	ns	
RAS to CAS delay		tRCD	18		22.5		ns	
Row precharge time		tRP	18		22.5		ns	
Row active to Row active delay		tRRD	12		15		ns	
Write recovery time		tWR	12		15		ns	
Last data in to Active delay		tDAL	2tCK+tRP		2tCK+tRP		-	2
Last data in to Read command		tCDLR	1		1		tCK	
Col. address to Col. address delay		tCCD	1		1		tCK	
Clock high level width		tCH	0.45	0.55	0.45	0.55	tCK	
Clock low level width		tCL	0.45	0.55	0.45	0.55	tCK	
DQ Output data access time from CK/$\overline{CK}$	CL=2	tAC	2	8	2	8	ns	3
	CL=3		2	5.5	2	6		
DQS Output data access time from CK/$\overline{CK}$	CL=2	tDQSCK	2	8	2	8	ns	
	CL=3		2	5.5	2	6		
Data strobe edge to ouput data edge		tDQSQ		0.5		0.6	ns	
Read Preamble	CL=2	tRPRE	0.5	1.1	0.5	1.1	tCK	
	CL=3		0.9	1.1	0.9	1.1		
Read Postamble		tRPST	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.75	1.25	0.75	1.25	tCK	
DQS in setup time		tWPRES	0		0		ns	4

DQS-in setup time	tWPRES	0		0		ns	4
DQS-in hold time	tWPREH	0.25		0.25		tCK	
DQS-in high level width	tDQSH	0.4	0.6	0.4	0.6	tCK	
DQS-in low level width	tDQSL	0.4	0.6	0.4	0.6	tCK	
DQS falling edge to CK setup time	tDSS	0.2		0.2		tCK	
DQS falling edge hold time from CK	tDSH	0.2		0.2		tCK	
DQS-in cycle time	tDSC	0.9	1.1	0.9	1.1	tCK	
Address and Control Input setup time	tIS	1.1		1.3		ns	1
Address and Control Input hold time	tIH	1.1		1.3		ns	1
Address & Control input pulse width	tIPW	2.2		2.6			1
DQ & DM setup time to DQS	tDS	0.6		0.8		ns	5,6
DQ & DM hold time to DQS	tDH	0.6		0.8		ns	5,6
DQ & DM input pulse width	tDIPW	1.2		1.8		ns	
DQ & DQS low-impedence time from CK/$\overline{CK}$	tLZ	1.0		1.0		ns	
DQ & DQS high-impedence time from CK/$\overline{CK}$	tHZ		5.5		6.0	ns	
DQS write postamble time	tWPST	0.4	0.6	0.4	0.6	tCK	
DQS write preamble time	tWPRE	0.25		0.25		tCK	
Refresh interval time	tREF		64		64	ms	
Mode register set cycle time	tMRD	2		2		tCK	
Power down exit time	tPDEX	1		1		tCK	
CKE min. pulse width(high and low pulse width)	tCKE	2		2		tCK	

Parameter	Symbol	DDR333		DDR266		Unit	Note
		Min	Max	Min	Max		
Auto refresh cycle time	tRFC	72		80		ns	7
Exit self refresh to active command	tXSR	120		120		ns	
Data hold from DQS to earliest DQ edge	tQH	tHPmin - tQHS		tHPmin - tQHS		ns	
Data hold skew factor	tQHS		0.65		0.75	ns	
Clock half period	tHP	tCLmin or tCHmin		tCLmin or tCHmin		ns	

NOTE :

1) Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
1.0	0	0
0.8	+50	+50
0.6	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 1.0V/ns.

2) Minimum 3CLK of tDAL(= tWR + tRP) is required because it need minimum 2CLK for tWR and minimum 1CLK for tRP.

3) tAC(min) value is measured at the high Vdd(1.95V) and cold temperature(-25°C).
tAC(max) value is measured at the low Vdd(1.7V) and hot temperature(85°C).
tAC is measured in the device with half driver strength and under the AC output load condition (Fig.7 in next Page).

4) The specific requirement is that DQS be valid(High or Low) on or before this CK edge. The case shown(DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on tDQSS.

5) I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	ΔtIS	ΔtIH
(V/ns)	(ps)	(ps)
1.0	0	0
0.8	+75	+75

0.6	+150	+150

This derating table is used to increase t_{DS}/t_{DH} in the case where the I/O slew rate is below 1.0V/ns.

6) I/O Delta Rise/Fall Rate(1/slew-rate) Derating

Data Rise/Fall Rate	ΔtIS	ΔtIH
(ns/V)	(ps)	(ps)
0	0	0
±0.25	+50	+50
±0.5	+100	+100

This derating table is used to increase tDS/tDH in the case where the DQ and DQS slew rates differ. The Delta Rise/Fall Rate is calculated as 1/SlewRate1-1/SlewRate2. For example, if slew rate 1 = 1.0V/ns and slew rate 2 =0.8V/ns, then the Delta Rise/Fall Rate =-0.25ns/V.

7) Maximum burst refresh cycle : 8

在这个表中可以得到我们需要设置的所有参数。
在设置时，有一个原则，那就是所有的都以内存时钟为参考。寄存器中的值都是内存时钟的比值（周期比或者时间值比）。
内存挂载于AHB总线上，使用的时钟为HCLK，前期的时钟配置里配置HCLK为133MHz。可计算得：
每个内存时钟周期 T(mem) = 1000 / 133 (ns) = 7.518 (ns)
各参数与周期时间的比值 K = t * 133 / 1000 + 1 （+1是为了确保大于最小值）

4.2.2、配置寄存器

4.2.2.1、设置内存刷新周期

5.5.5 REFRESH PERIOD REGISTER

Register	Address	R/W	Description	Reset Value
P1REFRESH	0x7E001010	R/W	32-bit DRAM controller refresh period register	0xA60

PnREFRESH	Bit	Description	Initial State
	[31:15]	Read undefined. Write as Zero	
Refresh period	[14:0]	Memory refresh period in memory clock cycles.	0xA60

内存刷新周期要求为7.8us =7800 ns value = 1038.4

4.2.2.2、设置列地址选通脉冲时间延迟

5.5.6 CAS LATENCY REGISTER

Register	Address	R/W	Description	Reset Value
P1CASLAT	0x7E001014	R/W	32-bit DRAM controller CAS latency register	0x6

PnCASLAT	Bit	Description	Initial State
	[31:4]	Read undefined. Write as Zero	
CAS Latency	[3:1]	CAS latency in memory clock cycles.	011
CAS Half cycle	[0]	Encodes whether the CAS latency is half a memory clock cycle more than the value given in bits[3:1] 0 = Zero cycle offset to value in [3:1]. [0] is forced to 0 in MDDR and SDR mode. 1 = Half cycle offset to the value in [3:1].	0

什么是CAS，CL（CAS Latency）？ CAS意为列地址选通脉冲(Column Address Strobe 或者Column Address Select),CAS控制着从收到命令到执行命令的间隔时间，通常为2，2.5，3这个几个时钟周期。在整个内存矩阵中，因为CAS按列地址管理物理地址，因此在稳定的基础上，这个非常重要的参数值越低越好。过程是这样的，在内存阵列中分为行和列，当命令请求到达内存后，首先被触发的是tRAS (Active to Precharge Delay)，数据被请求后需预先充电，一旦tRAS被激活后，RAS才开始在一半的物理地址中寻址，行被选定后，tRCD初始化，最后才通过CAS找到精确的地址。整个过程也就是先行寻址再列寻址。从CAS开始到CAS结束就是现在讲解的CAS延迟了。因为CAS是寻址的最后一个步骤，所以在内存参数中它是最重要的。
CL（CAS Latency）：为CAS的延迟时间，这是纵向地址脉冲的反应时间，也是在一定频率下衡量支持不同规范的内存的重要标志之一。

4.2.2.3、设置DQSS

5.5.7 T_DQSS REGISTER

Register	Address	R/W	Description	Reset Value
P1T_DQSS	0x7E001018	R/W	32-bit DRAM controller t_DQSS register	0x1

PnT_DQSS	Bit	Description	Initial State
	[31:2]	Read undefined. Write as Zero	
t_DQSS	[1:0]	Write to DQS in memory clock cycles.	1

数据选取脉冲（DQS）

总结DQS：它是双向信号；读内存时，由内存产生，DQS的沿和数据的沿对齐；写入内存时，由外部产生，DQS的中间对应数据的沿，即此时DQS的沿对应数据最稳定的中间时刻。 DQS是DDR SDRAM中的重要功能，它的功能主要用来在一个时钟周期内准确的区分出每个传输周期，并便于接收方准确接收数据。每一颗芯片都有一个DQS信号线，它是双向的，在写入时它用来传送由北桥发来的DQS信号，读取时，则由芯片生成DQS向北桥发送。完全可以说，它就是数据的同步信号。

写入延迟（tDQSS）

在上面的DQS写入时序图中，可以发现写入延迟已经不是0了，在发出写入命令后，DQS与写入数据要等一段时间才会送达。这个周期被称为DQS相对于写入命令的延迟时间（tDQSS， WRITE Command to the first corresponding rising edge of DQS），对于这个时间大家应该很好理解了。

为什么要有这样的延迟设计呢？原因也在于同步，毕竟一个时钟周期两次传送，需要很高的控制精度，它必须要等接收方做好充分的准备才行。tDQSS是DDR内存写入操作的一个重要参数，太短的话恐怕接受有误，太长则会造成总线空闲。tDQSS最短不能小于0.75个时钟周期，最长不能超过1.25个时钟周期。有人可能会说，如果这样，DQS不就与芯片内的时钟不同步了吗？对，正常情况下，tDQSS是一个时钟周期，但写入时接受方的时钟只用来控制命令信号的同步，而数据的接受则完全依靠DQS进行同步，所以 DQS与时钟不同步也无所谓。不过，tDQSS产生了一个不利影响——读后写操作延迟的增加，如果CL=2.5，还要在tDQSS基础上加入半个时钟周期，因为命令都要在CK的上升沿发出。

4.2.2.4、设置tMRD

5.5.8 T_MRD REGISTER

Register	Address	R/W	Description	Reset Value
P1T_MRD	0x7E00101C	R/W	32-bit DRAM controller t_MRD register	0x02

PnT_MRD	Bit	Description	Initial State
	[31:7]	Read undefined. Write as Zero	
t_MRD	[6:0]	Set mode register command time in memory clock cycles.	0x02

4.2.2.5、设置tRAS

5.5.9 T_RAS REGISTER

Register	Address	R/W	Description	Reset Value
P1T_RAS	0x7E001020	R/W	32-bit DRAM controller t_RAS register	0x7

PnT_RAS	Bit	Description	Initial State
	[31:4]	Read undefined. Write as Zero	
t_RAS	[3:0]	Set RAS to precharge delay in memory clock cycles.	0x7

4.2.2.6、设置tRC

5.5.10 T_RC REGISTER

Register	Address	R/W	Description	Reset Value
P1T_RC	0x7E001024	R/W	32-bit DRAM controller t_RC register	0xB

PnT_RC	Bit	Description	Initial State
	[31:4]	Read undefined. Write as Zero	
t_RC	[3:0]	Set Active bank x to Active bank x delay in memory clock cycles.	0xB

4.2.2.7、设置tRCD个scheduled_RCD

5.5.11 T_RCD REGISTER

Register	Address	R/W	Description	Reset Value
P1T_RCD	0x7E001028	R/W	32-bit DRAM controller t_RCD register	0x1D

PnT_RCD	Bit	Description	Initial State
	[31:6]	Read undefined. Write as Zero	
scheduled_RCD	[5:3]	Set t_RCD-3	011
t_RCD	[2:0]	Set the RAS to CAS minimum delay in memory clock cycles	101

4.2.2.8、设置tRFC个scheduled_RFC

5.5.12 T_RFC REGISTER

Register	Address	R/W	Description	Reset Value
P1T_RFC	0x7E00102C	R/W	32-bit DRAM controller t_RFC register	0x212

PnT_RFC	Bit	Description	Initial State
	[31:10]	Read undefined. Write as Zero	
scheduled_RFC	[9:5]	Set t_RFC -3.	0x10
t_RFC	[4:0]	Set the autorefresh command time in memory clock cycles	0x12

4.2.2.8、设置tRP个scheduled_RP

5.5.13 T_RP REGISTER

Register	Address	R/W	Description	Reset Value
P1T_RP	0x7E001030	R/W	32-bit DRAM controller t_RP register	0x1D

PnT_RP	Bit	Description	Initial State
	[31:6]	Read undefined. Write as Zero	
scheduled_RP	[5:3]	Set t_RP -3.	011
t_RP	[2:0]	Set the precharge to RAS delay in memory clock cycles	101

4.2.2.9、设置tRRD

5.5.14 T_RRD REGISTER

Register	Address	R/W	Description	Reset Value
P1T_RRD	0x7E001034	R/W	32-bit DRAM controller t_RRD register	0x2

PnT_RRD	Bit	Description	Initial State
	[31:4]	Read undefined. Write as Zero	
t_RRD	[3:0]	Set Active bank x to Active bank y delay in memory clock cycles.	0x2

4.2.2.10、设置tWR

5.5.15 T_WR REGISTER

Register	Address	R/W	Description	Reset Value
P1T_WR	0x7E001038	R/W	32-bit DRAM controller t_WR register	0x3

PnT_WR	Bit	Description	Initial State
	[31:3]	Read undefined. Write as Zero	
t_WR	[2:0]	Set the write to precharge delay in memory clock cycles.	011

4.2.2.11、设置tWTR

5.5.16 T_WTR REGISTER

Register	Address	R/W	Description	Reset Value
P1T_WTR	0x7E00103C	R/W	32-bit DRAM controller t_WTR register	0x2

PnT_WTR	Bit	Description	Initial State
	[31:3]	Read undefined. Write as Zero	
t_WTR	[2:0]	Set the write to read delay in memory clock cycles.	010

4.2.2.12、设置tXP

5.5.17 T_XP REGISTER

Register	Address	R/W	Description	Reset Value
P1T_XP	0x7E001040	R/W	32-bit DRAM controller t_XP register	0x01

PnT_XP	Bit	Description	Initial State
	[31:8]	Read undefined. Write as Zero	
t_XP	[7:0]	Set the exit power down command time in memory clock cycles.	0x01

4.2.2.13、设置tXSR

5.5.18 T_XSR REGISTER

Register	Address	R/W	Description	Reset Value
P1T_XSR	0x7E001044	R/W	32-bit DRAM controller t_XSR register	0x0A

PnT_XSR	Bit	Description	Initial State
	[31:8]	Read undefined. Write as Zero	
t_XSR	[7:0]	Set the exit self refresh command time in memory clock cycles.	0x0A

4.2.2.14、设置tESR

5.5.19 T_ESR REGISTER

Register	Address	R/W	Description	Reset Value
P1T_ESR	0x7E001048	R/W	32-bit DRAM controller t_ESR register	0x14

PnT_ESR	Bit	Description	Initial State
	[31:8]	Read undefined. Write as Zero	
t_ESR	[7:0]	Set the self refresh command time in memory clock cycles.	0x14

4.2.2.15、设置内存配置寄存器

5.5.4 MEMORY CONFIGURATION REGISTER

Register	Address	R/W	Description	Reset Value
P1MEMCFG	0x7E00100C	R/W	32-bit DRAM controller memory config register	0x01_0020

PnMEMCFG	Bit	Description	Initial State
Reserved	[31]	Reserved. It should be write as Zero.	0
Reserved	[30:23]	Read undefined. Write as zero.	
Active chips	[22:21]	Enables the refresh command generation for the number of memory chips. It is only possible to generate commands up to and including the number of chips in the configuration defined in the DRAM controller status register: 00 = 1 chip 01 = 2 chips 10 = Reserved 11 = Reserved	00
		Encodes the four bits of the 8-bit AXI ARID that are used to	

QoS master bits	[20:18]	select one of the 16 QoS values: 000 = ARID[3:0] 001 = ARID[4:1] 010 = ARID[5:2] 011 = ARID[6:3] 100 = ARID[7:4] 101~111 = Reserved	000
Memory burst	[17:15]	Encodes the number of data accesses that are performed to the SDRAM for each Read and Write command: 000 = Burst 1 001 = Burst 2 010 = Burst 4 011 = Burst 8 100 = Burst 16 101~111 = Reserved This value must also be programmed into SDRAM mode register using the DIRECTCMD register and must match it.	010
Stop_mem_clock	[14]	When enabled the memory clock is dynamically stopped when not performing an access to the SDRAM.	0
Auto power down	[13]	When Auto power down is set, the memory interface automatically places the SDRAM into power-down state by de-asserting CKE when the command FIFO has been empty for Power_down_prd memory clock cycles.	0
Power_down_prd	[12:7]	Number of memory clock cycles for auto power-down of SDRAM.	000000
AP bit	[6]	Encodes the position of the auto-precharge bit in the memory address: 0 = address bit 10. 1 = address bit 8.	0
Row bits	[5:3]	Encodes the number of bits of the AXI address that comprise the	100

		row address: 000 = 11 bits 001 = 12 bits 010 = 13 bits 011 = 14 bits 100 = 15 bits 101 = 16 bits	
Column bits	[2:0]	Encodes the number of bits of the AXI address that comprise the column address: 000 = 8 bits 001 = 9 bits 010 = 10 bits 011 = 11 bits 100 = 12 bits	000

选择 Active chips 1，Burst 4，Supports one CKE control，Row bits 14，Column bits。

4.2.2.16、设置内存配置寄存器2

5.5.20 MEMORY CONFIGURATION 2 REGISTER

Register	Address	R/W	Description	Reset Value
P1MEMCFG2	0x7E00104C	R/W	32-bit DRAM controller configuration register	0x0B45

PnMEMCFG2	Bit	Description	Initial State
Reserved	[31:13]	Read undefined. Write as Zero.	
Read delay	[12:11]	Encodes the delay used when reading from the pad interface to allow for de-skew of incoming read data 00 = Read delay 0 cycle (usually for SDR SDRAM. The SDR configuration requires read_dealy set to zero.) 01 = Read delay 1 cycle (usually for DDR SDRAM and mobile DDR SDRAM) 10, 11 = Read delay 2 cycle	01
Memory type	[10:8]	The type of SDRAM that is attached to DRAM controller: 000 = SDR SDRAM 001 = DDR SDRAM 011 = Mobile DDR SDRAM Note It is only legal to program the memory type between SDR and (LP)DDR for a memory controller configuration that supports it	011
Memory width	[7:6]	The width of the external memory 00 = 16-bit 01 = 32-bit 10 = Reserved 11 = Reserved Note Only a memory width that is legal for the memory controller can be programmed.	00 / 01
Reserved	[5:4]	Read undefined. Write as Zero.[1]	00
cke_init	[3]	Sets the level for the cke outputs after reset.	1/0
DQM init	[2]	Sets the level for the dqm outputs after reset.	1
a_gt_m_sync	[1]	Requires to be set HIGH when running the aclk and mclk synchronously but with aclk running faster than mclk.	0
sync	[0]	Set high when aclk and mclk are synchronous.	1

4.2.2.17、设置CHIP_N_CFG寄存器

5.5.23 CHIP_N_CFG REGISTER

Register	Address	R/W	Description	Reset Value
P1_chip_0_cfg P1_chip_1_cfg	0x7E001200 0x7E001204	R/W	32-bit DRAM controller chip_<n>_cfg register	0x0FF00

Pn_chip_<n>_cfg	Bit	Description	Initial State
	[31:17]	Read undefined. Write as Zero	
BRC_RBC	[16]	Selects the memory organization as decoded from the AXI address: 0 = Row-Bank-Column organization. 1 = Bank-Row-Column organization.	0
Address match	[15:8]	Comparison value for AXI address bits [31:24] to determine which chip is selected.	0xFF
Address mask	[7:0]	The mask for AXI address bits [31:24] to determine which chip is selected: 1 = corresponding address bit is to be used for comparison	0x00

内存对应的AXI地址为B-R-C（bank，行，列）；因为DDR内存从0x50开始，两个DDR总大小为256MB（0x1000 0000），所以Address match为0x50，掩码Address mask为F0（1111 0000），如果内存大小为128MB（0x8000 0000），那样掩码Address mask为F8（1111 1000）。

4.2.2.18、设置用户配置寄存器

5.5.25 USER_CONFIG REGISTER

Register	Address	R/W	Description	Reset Value
P1_user_cfg	0x7E001304	W	32-bit DRAM controller user_cfg register	0x00

P1_user_cfg	Bit	Description	Initial State
Reserved	[31:16]	Read undefined. Write as Zero	0
Reserved	[15]		0
DQS3 input chain delay selection	[14:12]	Sets DQS[3] input chain delay value. When it is set to 3'b000, minimum delay chain is used.	0
Reserved	[11]		0
DQS2 input chain delay selection	[10:8]	Sets DQS[2] input chain delay value. When it is set to 3'b000, minimum delay chain is used.	0
Reserved	[7]		0
DQS1 input chain delay selection	[6:4]	Sets DQS[1] input chain delay value. When it is set to 3'b000, minimum delay chain is used.	0
Reserved	[3]		0
DQS0 input chain delay selection	[2:0]	Sets DQS[0] input chain delay value. When it is set to 3'b000, minimum delay chain is used.	0

4.3、等待200uS以允许SDRAM电源和时钟稳定（可忽略）。

4.4、执行内存初始化程序。

5.5.3 DIRECT COMMAND REGISTER

Register	Address	R/W	Description	Reset Value
P1 DIRECTCMD	0x7E001008	W	32-bit DRAM controller direct command register	

PnDIRECTCMD	Bit	Description	Initial State
Reserved	[31:23]	Undefined. Write as Zero	
Extended Memory command	[22]	Extended memory command, see note after the table	
Chip number	[21:20]	Bits mapped to external memory chip address bits.	
Memory command	[19:18]	Determines the command required, see note after the table.	
Bank address	[17:16]	Bits mapped to external memory bank address bits when command is MRS or EMRS access.	
	[15:14]	Undefined. Write as Zero	
Address_13_to_0	[13:0]	Bits mapped to external memory address bits [13:0] when command is MRS or EMRS access.	

Note: Memory command encoding. This encoding uses the "Extended Memory command" bits concatenated to "Memory command", therefore providing 3 bits.

3'b000 = Prechargeall

3'b001 = Autorefresh

3'b010 = Modereg or Extended modereg access

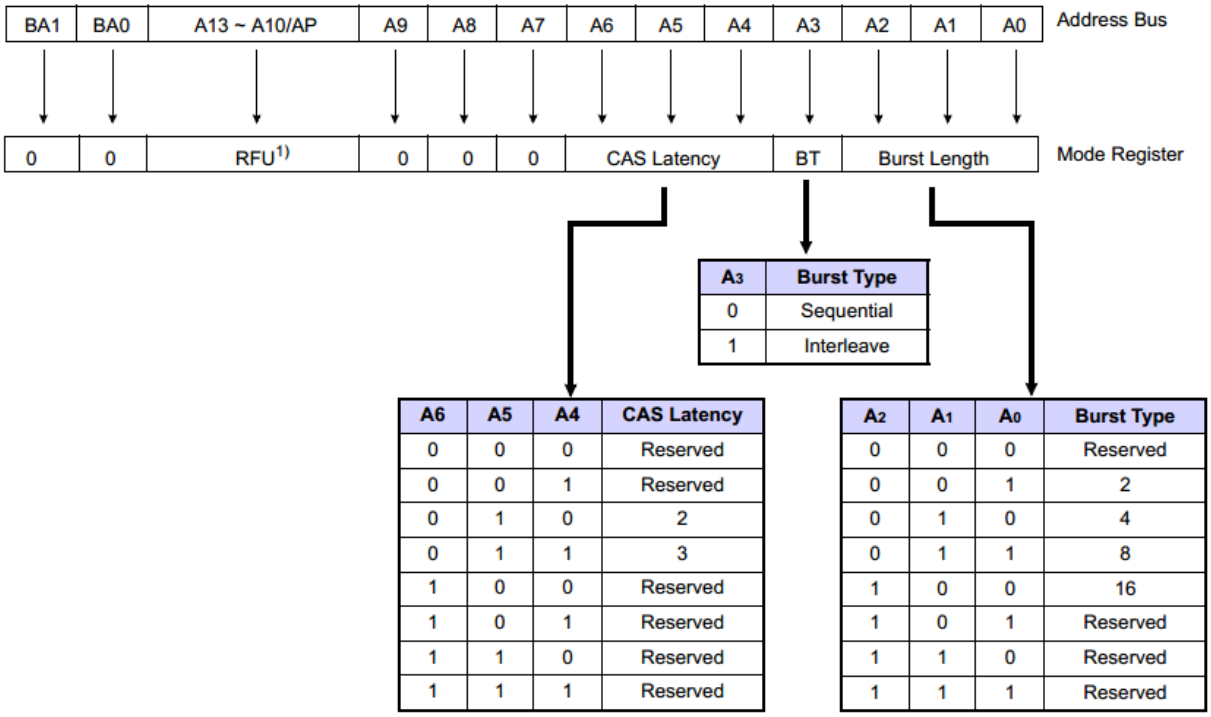
3'b011 = NOP

3'b100 = DPD (Deep Power Down)

All other combinations are illegal and might cause undefined behavior. A NOP command asserts all chip selects that are set as active_chips when the chip_nmbr is set to 0.

Mode Register Set(MRS)

Figure 2. Mode Register Set



A_3	Burst Type
0	Sequential
1	Interleave

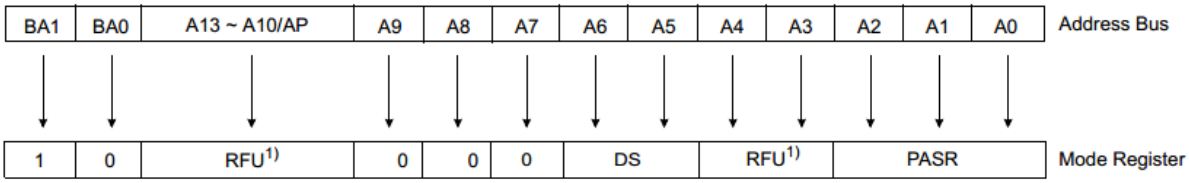
A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A_2	A_1	A_0	Burst Type
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE :
1) RFU(Reserved for future use) should stay "0" during MRS cycle

Extended Mode Register Set(EMRS)

Figure 3. Extended Mode Register Set



DS		
A_6	A_5	Driver Strength
0	0	Full
0	1	1/2
1	0	1/4
1	1	1/8

PASR			
A_2	A_1	A_0	Refreshed Area
0	0	0	Full Array
0	0	1	1/2 Array
0	1	0	1/4 Array
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE :
1) RFU(Reserved for future use) should stay "0" during EMRS cycle

4.5、写‘3’b000’到memc_cmd ，使DRAM控制器进入就绪状态。

4.6、检查memc_stat中的内存状态域，直到内存状态变为“2'b01” ，表明内存进入“就绪”。

5.5.1 DRAM CONTROLLER STATUS REGISTER

Register	Address	R/W	Description	Reset Value
P1MEMSTAT	0x7E001000	R	32-bit DRAM controller status register	0x8C4

PnMEMSTAT	Bit	Description	Initial State
Reserved	[31:14]	Read undefined.	
Reserved	[13:12]	Read always 0	00
Reserved	[11:10]	Read always “10”	10
Reserved	[9]	Read always zero.	0
Memory chips	[8:7]	The maximum number of different chip selects that DRAM controller can supports: 01 = 2 chips 6410X only supports 2 chips, and “Memory chips” reads only as 01.	01
Memory type	[6:4]	The type of SDRAM that DRAM controller supports: 100 = Any of the followings: MSDR, SDR, MDDR, or DDR	100
Memory width	[3:2]	The width of the external memory 00 = 16-bit 01 = 32-bit 10 = reserved 11 = reserved	01
Controller status	[1:0]	The status of the DRAM controller 00 = Config. 01 = Ready 10 = Paused 11 = Low-Power	00