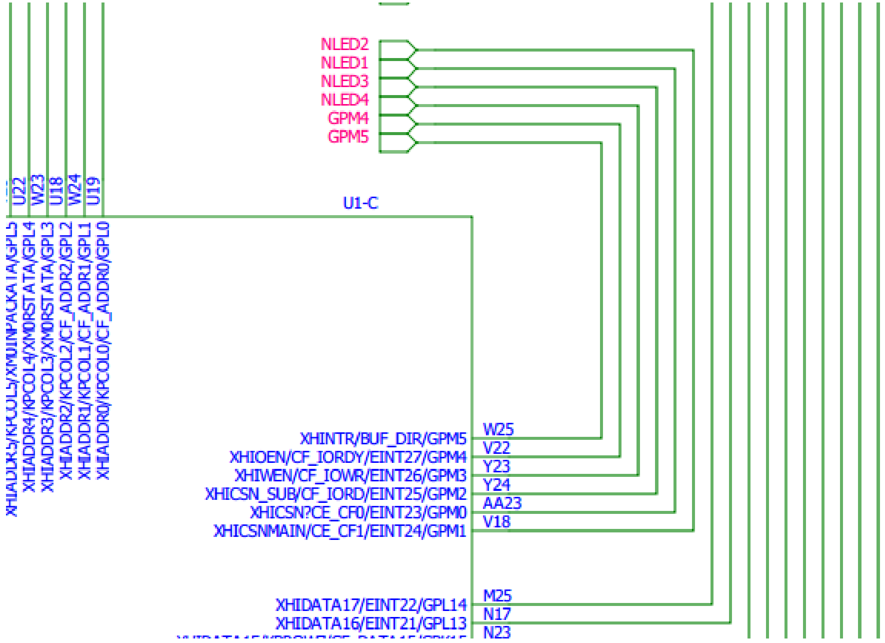
专题6-点亮LED

一、根据原理图确认LED所用IGPIO

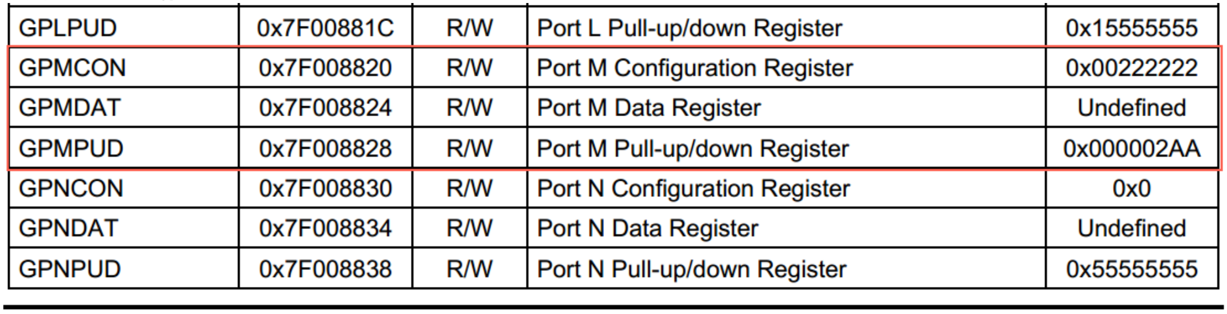
下图为OK6410的LED对应的电路


NLED2
NLED1
NLED3
NLED4
GPM4
GPM5
U1-C
U22
W23
U18
W24
U19
XHIADDR5/KPCOL5/XMUIINPACKATA/GPL5
XHIADDR4/KPCOL4/XM0RSTATA/GPL4
XHIADDR3/KPCOL3/XM0RSTATA/GPL3
XHIADDR2/KPCOL2/CF_ADDR2/GPL2
XHIADDR1/KPCOL1/CF_ADDR1/GPL1
XHIADDR0/KPCOL0/CF_ADDR0/GPL0
XHINTR/BUF_DIR/GPM5
XHIOEN/CF_IORDY/EINT27/GPM4
XHIWEN/CF_IOWR/EINT26/GPM3
XHICSN_SUB/CF_IORD/EINT25/GPM2
XHICSN?CE_CF0/EINT23/GPM0
XHICSNMAIN/CE_CF1/EINT24/GPM1
W25
V22
Y23
Y24
AA23
V18
XHIDATA17/EINT22/GPL14
XHIDATA16/EINT21/GPL13
M25
N17
N23

可知LED使用的GPIO如下表

LED1	GPM0
LED2	GPM1
LED3	GPM2
LED4	GPM3

二、配置GPM寄存器



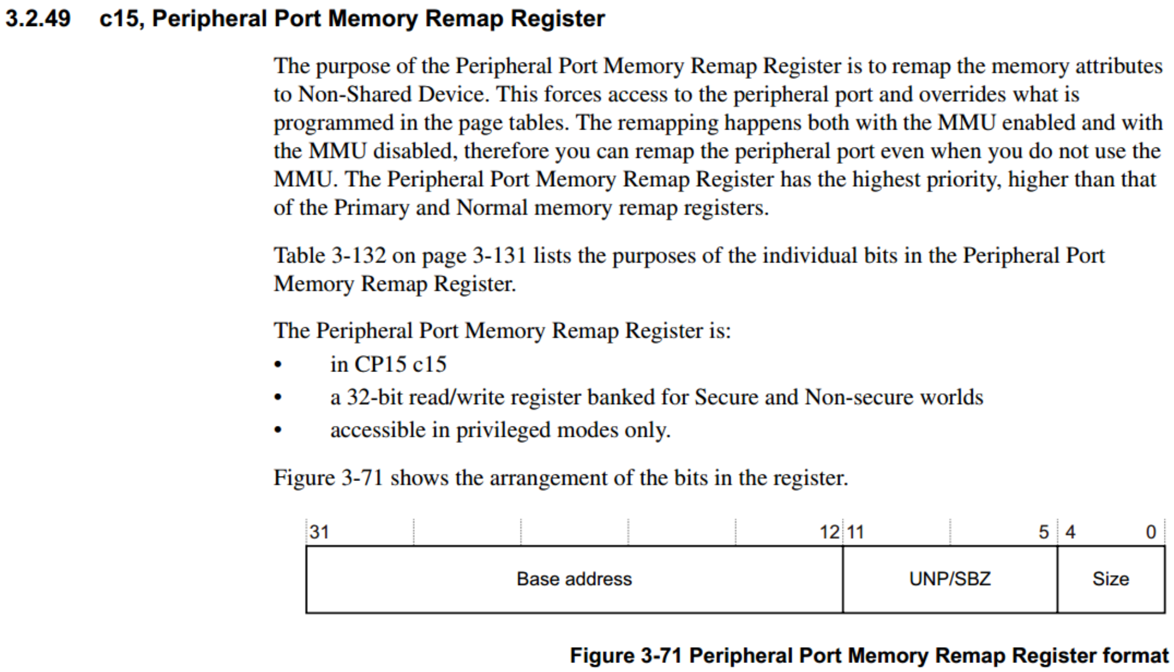
GPLPUD	0x7F00881C	R/W	Port L Pull-up/down Register	0x15555555
GPMCON	0x7F008820	R/W	Port M Configuration Register	0x00222222
GPMDAT	0x7F008824	R/W	Port M Data Register	Undefined
GPMPUD	0x7F008828	R/W	Port M Pull-up/down Register	0x000002AA
GPNCON	0x7F008830	R/W	Port N Configuration Register	0x0
GPNDAT	0x7F008834	R/W	Port N Data Register	Undefined
GPNPUD	0x7F008838	R/W	Port N Pull-up/down Register	0x55555555

```
#define GPMCON 0x7f008820
#define GPMDAT 0x7f008824
#define GPMPUD 0x7f008828
led_on:
        ldr r0, =GPMCON
        ldr r1, =0x00001111
        str r1, [r0]

        ldr r0, =GPMDAT
        ldr r1, =0b001010
        str r1, [r0]

        mov pc, lr
```

三、对外设进行操作时需要先对外设基地址初始化（6410）



3.2.49 c15, Peripheral Port Memory Remap Register

The purpose of the Peripheral Port Memory Remap Register is to remap the memory attributes to Non-Shared Device. This forces access to the peripheral port and overrides what is programmed in the page tables. The remapping happens both with the MMU enabled and with the MMU disabled, therefore you can remap the peripheral port even when you do not use the MMU. The Peripheral Port Memory Remap Register has the highest priority, higher than that of the Primary and Normal memory remap registers.

Table 3-132 on page 3-131 lists the purposes of the individual bits in the Peripheral Port Memory Remap Register.

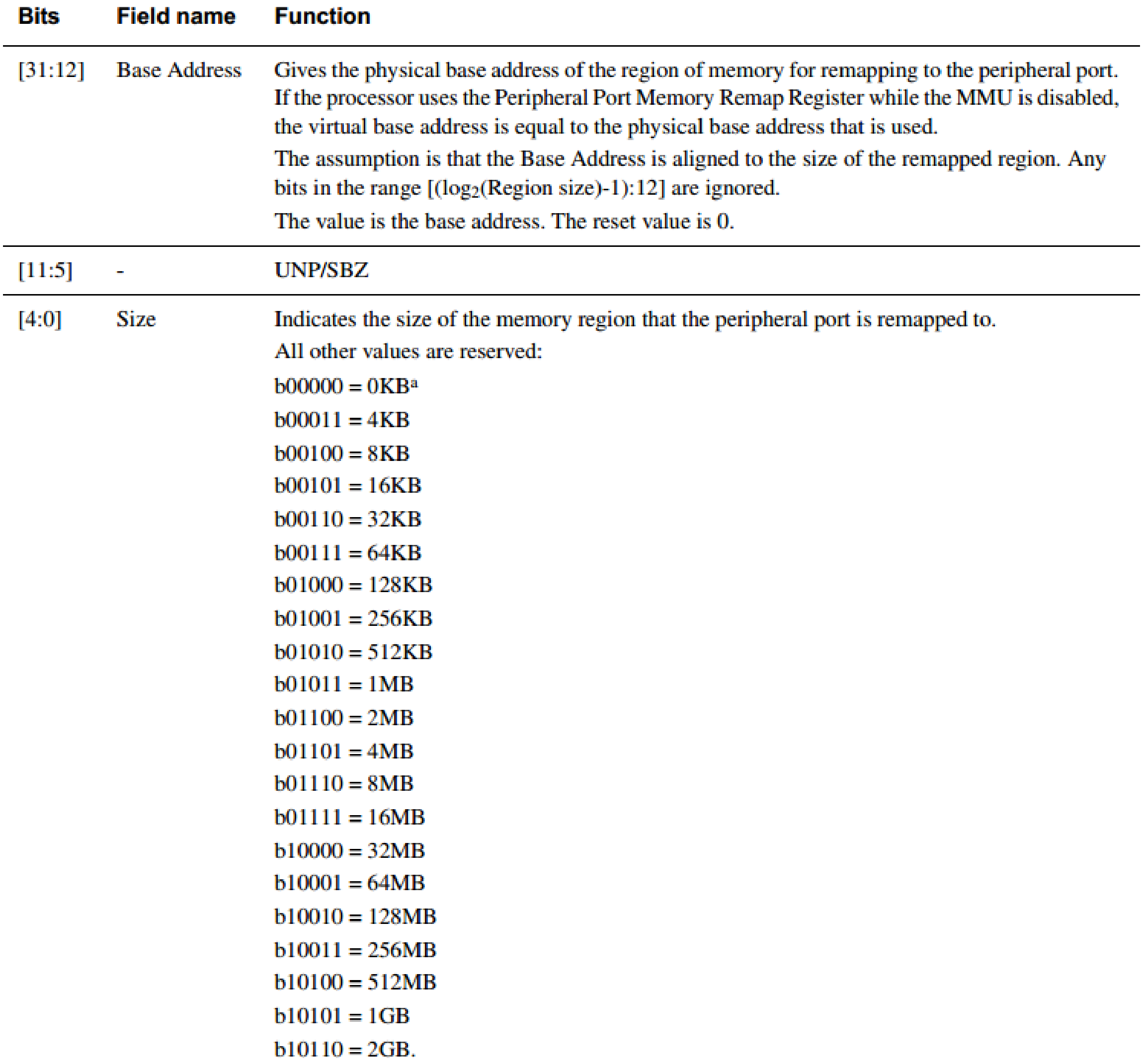
The Peripheral Port Memory Remap Register is:

- in CP15 c15
- a 32-bit read/write register banked for Secure and Non-secure worlds
- accessible in privileged modes only.

Figure 3-71 shows the arrangement of the bits in the register.

Figure 3-71 Peripheral Port Memory Remap Register format

设置外设基地址为0x70000000,大小为256MB



Bits	Field name	Function
[31:12]	Base Address	Gives the physical base address of the region of memory for remapping to the peripheral port. If the processor uses the Peripheral Port Memory Remap Register while the MMU is disabled, the virtual base address is equal to the physical base address that is used. The assumption is that the Base Address is aligned to the size of the remapped region. Any bits in the range [(log$_2$(Region size)-1):12] are ignored. The value is the base address. The reset value is 0.
[11:5]	-	UNP/SBZ

[4:0]	Size	Indicates the size of the memory region that the peripheral port is remapped to.
		All other values are reserved:
		b00000 = 0KB[a]
		b00011 = 4KB
		b00100 = 8KB
		b00101 = 16KB
		b00110 = 32KB
		b00111 = 64KB
		b01000 = 128KB
		b01001 = 256KB
		b01010 = 512KB
		b01011 = 1MB
		b01100 = 2MB
		b01101 = 4MB
		b01110 = 8MB
		b01111 = 16MB
		b10000 = 32MB
		b10001 = 64MB
		b10010 = 128MB
		b10011 = 256MB
		b10100 = 512MB
		b10101 = 1GB
		b10110 = 2GB.

```
peri_port_setup:
        ldr r0, =0x70000000
        orr r0, r0, #0x13
        mcr p15, 0, r0, c15, c2, 4      @ 256M(0x70000000-0x7fffffff)
        mov pc, lr
```