Antenna Effect Solution using Dynamic Diode Insertion during Cell Placement and Post-Layout

A Dissertation

by

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A dissertation submitted to the faculty of

University of Empresarial in partial fulfillment

of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

University of Empresarial, Costa Rica

June 25, 2010

University of Empresarial
Graduate School

Thus is to certify that I have examined this copy of
a doctoral dissertation
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Peter H. Chen

and have found that it is complete and satisfactory in all respects,
and that any and all revisions required by the final
examining committee have been made.

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1. Abstract

This dissertation presents the solution of antenna effect by dynamic protection diode insertion:

- In the cell placement period: A simplified design process containing solutions to both the antenna effect problem and increasing the efficiency of cell placement for million-gates chip layout.
- In the post-layout period: Three ways of fixing antenna problem are compared.

2. Introduction

Working within the ASIC industry, time to market is very important. With Very Deep Sub-Micron (VDSM) processes, issues with timing enclosure, cell placement efficiency, the antenna effect, signal integrity, etc. have impacted our ability to meet market requirements in a timely manner. By focusing on the design process, two of the major issues, the antenna problem and cell placement efficiency, can be addressed. This dissertation proposes Knowledge Based Priority Placement (KBPP), which utilizes design knowledge to simplify those two issues. The post-layout antenna solution is for chip implementation without KBPP and with antenna problem existed in their layout.

3. Antenna Effect

The antenna problem has existed in the semiconductor industry for more than a decade. In the production of the modern VLSI semiconductor, etching plasma is used to deposit or remove material on wafers. The etching plasma causes destructive charges to be built up on the wafer. This problem is more critical in VDSM VLSI design since thinner oxides are even more susceptible to damage. During wafer manufacturing, aluminum or polysilicon wires in the plasma ambient that are not covered with dielectric collect charges and serve as "antenna." When the potential becomes high enough, it will discharge through the gate dioxide and cause cell damage. Damage can include electrical stress that decreases the breakdown voltage of the gate oxide, resulting in a decreased yield rate during wafer manufacturing. It has been hypothesized that UV light bombardment on the etching plasma during the manufacturing process increases the antenna effect; however, I

have found that it increases the effectiveness of protection diodes since they are the miniature solar cells and they conduct the charge instead of the gate dioxide. [5, 6, 7, 17, 18]

3.1 Possible Solutions

To prevent this, we can dig a drainage trench, reduce the antenna lengths, insert jumpers in the post-layout phase, or connect protection diodes as close to the input ports as possible. The first two options are not feasible as they necessitate changing the design of a completed chip during the manufacturing process. Among these solutions, only post-layout jumper insertion and protection diodes can be used in the physical design period. However, even smart routers are not able to insert jumpers because chips are so dense. Jumpers also cause more time delay than diodes and cause timing enclosure problems. The following calculation shows the timing comparison between jumper and diode insertion approaches. In jumper insertion, each jumper needs at least two vias. In

0.35 μm technology, via resistance is around 10 Ω. In 0.25 μm technology or below (such as 0.18 μm), via resistance is around 100 Ω or more. The bigger the resistance, the worse the timing delay is. This phenomenon is more severe in deeper sub-micron technology.

$$R' = R_s \times \frac{L}{W} \cong 60m\Omega \cong 3-10\Omega, \quad (1)$$

Where:

R_s is the sheet resistance of metal

R' is the resistance of metal with length L.

If we use diode insertion, the diode capacitance is the factor that affects the timing delay. The following equation estimates typical diode capacitance.

$$C' = C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{35.5\mu F/cm}{0.4\times10^{-5}cm} = 0.86\, fF/\mu m^2, \quad (2)$$

Where

C is the capacitance of the original wire

C' and C_{ox} are capacitance of metal with length L

ε_{ox} is the permittivity of diode

t_{ox} is the thickness of the diode.

If we add one jumper (with two vias) and one protection diode for a wire 350-μm long, we have the following estimate timed delay.

$$\tau = (R + R') \times (C + C')$$

$$= R \times C \times (1 + R'/R) \times (1 + C'/C) \qquad (3)$$

Assume a wire with $60\,\Omega$ and 1-pF capacitance. If we compare dropping two vias at $3\,\Omega$ (total $6\,\Omega$) versus dropping a protection diode at 0.86 fF from equation (3), we can see that the delay caused by the protection diode (C' /C $\cong$ 0.86 fF /1pF $\cong 10^{-3}$) is much less than that caused by the jumper insertion [or router option] (R' / R $\cong$ 6 / 60 $\cong$ 0.1). Therefore, the timing delay caused by dropping the diode is negligible.

3.2 Simulation Results

Figures 1 and 2 simulate the inverter with a protection diode during the manufacturing process. The protection diode size also affects the cumulative current. Assume a current pulse is generated from the etching plasma into the input gate. The input gate is protected by a protection diode with area $1\times1\mu m^2$. The plasma current source (Is) is set to the following conditions:

- current amplitude = 10 mA
- period = 20 ns
- pulse width = 5 ns
- 1 ns in both the rising and falling edge
- initial delay 2 ns.

Resistors R1, R2, and R3, are set to 5Ω. Capacitances C1, C2, and C3 are set to 0.75pF. Both N-MOS and P-MOS are tied to ground. Voltages are measured and displayed at node NI and the input port (node N3). Since the protection diode provides

drainage, the plasma current at the input gate is kept to zero (Figure 2).

Figure 3 illustrates the normal operation of a circuit when voltage is applied to the chip. The SPICE model during circuit operations (in Figure 4) shows that the diode does not interfere with the integrity of the signal when a pulse is input through the input gate. The protection diode has an area of $1\times1\mu m^2$. The input current source (Is) is set to the following conditions:

- current amplitude 10 mA
- period 20 ns
- pulse width 5 ns
- 1 ns in both the rising and falling edge
- initial delay 2 ns.

Resistors R1, R2, and R3, are set to 5 Ω. Capacitances C1, C2, and C3 are set to 0.75pF. Both N-MOS and P-MOS are tied to ground. Voltages are measured and displayed at node (I) and the

input port (node N3).

Figure 4 shows the protected by diode is open during the normal operation, *i.e.*, the protection diode is a dummy device during the normal circuit operation. In Figure 4, the shift between the solid line V (NI) and the dotted line V (N3) is caused by the capacitance and resistance between them. The area of the diode (e.g., increasing the diode size from 1 μm^2 to $3\times10^{14}\mu m^2$) has a negligible effect. The leakage currents introduced by the protection diode are discussed in previous papers [3, 5].

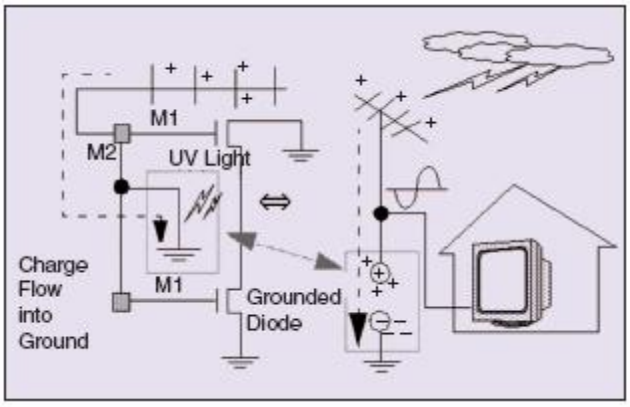

Figure 1. Analogy of protection diode fixing antenna effect

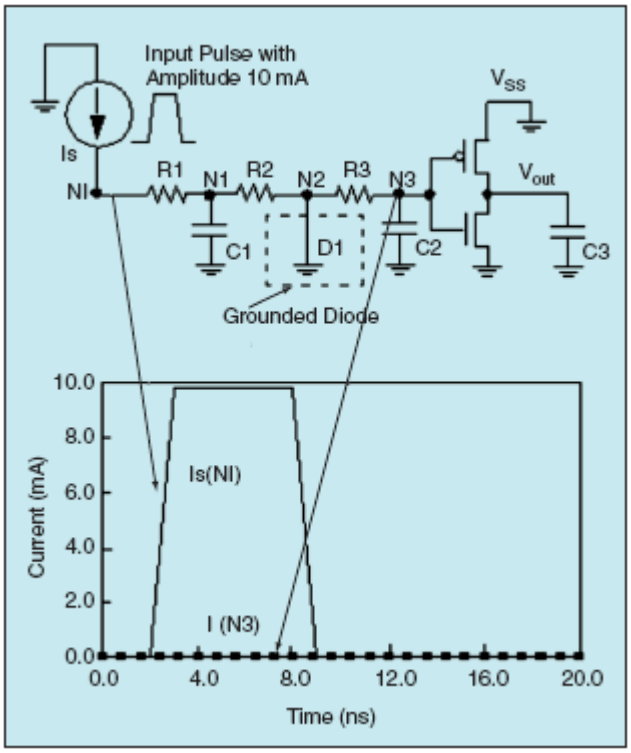

Figure 2. Protecting the input port during manufacturing

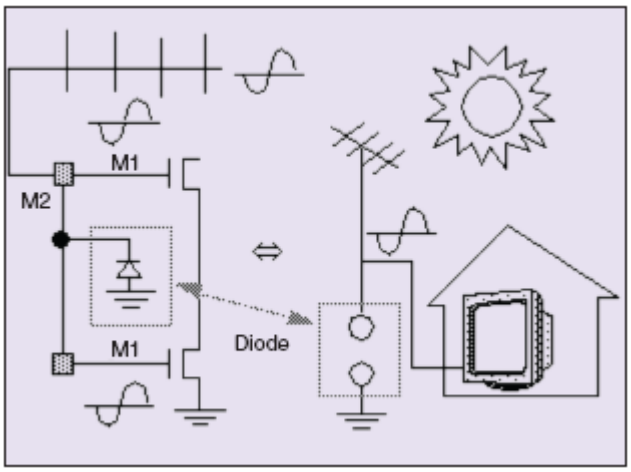

Figure 3. Analog of normal circuit operation

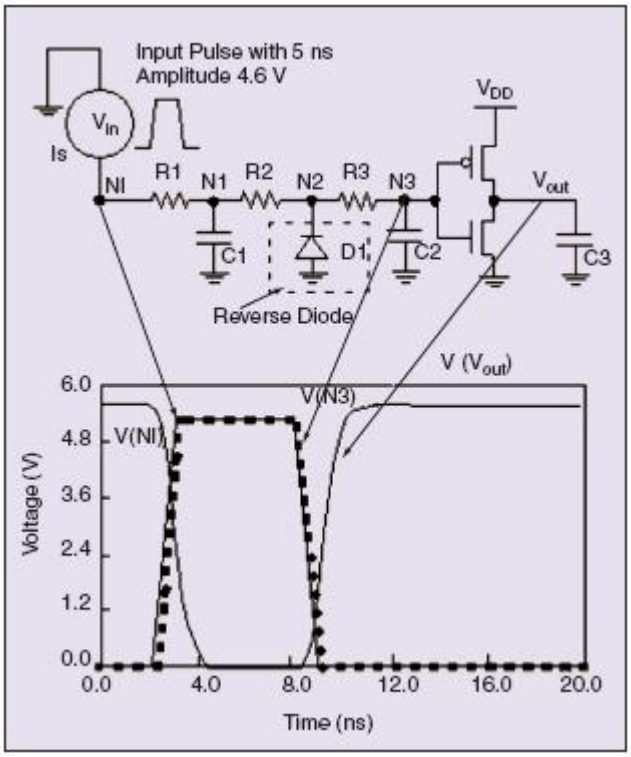

Figure 4. Diode is open during normal circuit operation

3.3 Antenna Ratio

Note that the antenna rule violation definition is foundry and process specific. Using a typical $0.25\,\mu m$ (five-metal) process design rules as an example, the antenna ratio is defined using the total perimeter area of metal wire as the numerator and the gate area as the denominator.

$$\text{Antenna ratio} = \frac{[2 \times (L1 + W1) \times t]}{W2 \times L2}, \quad (4)$$

Where:

$L1$ Is the floating metal length connected to gate

$W1$ is the floating metal width connected to gate

t is the metal thickness

$W2$ is he connected transistor chancel width

$L2$ is the connected transistor channel length

The antenna ration of a typical $0.25\,\mu m$ contact (CO) and via1-via4 is:

$$\text{Antenna ratio} = \frac{\text{total contact (via) area}}{W2 \times L2}, \quad (5)$$

The thickness of M1-M4 is 5,700 $\mathring{A}$. The thickness of M5 is 9,900 $\mathring{A}$. Figure 5 shows the dimension definition of antenna ratio of a typical 0.25 μm process.

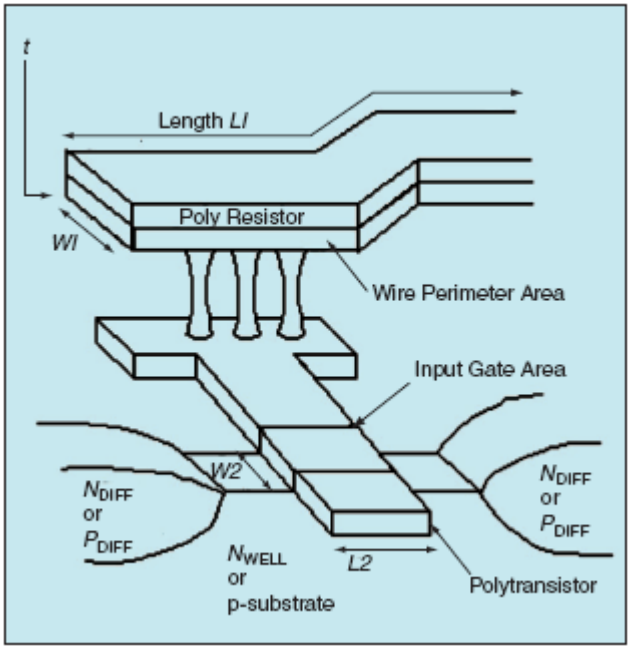

Figure 5. Dimension definition of antenna ratio

4. Protection Diode

Protection diodes are categorized as N-Diode with N+ ion implant mask layer (N-IMP) or P-diode with (P+ ion implant) mask layer (P-IMP) in this work. Figure 6 shows the top view of the protection diode structure.

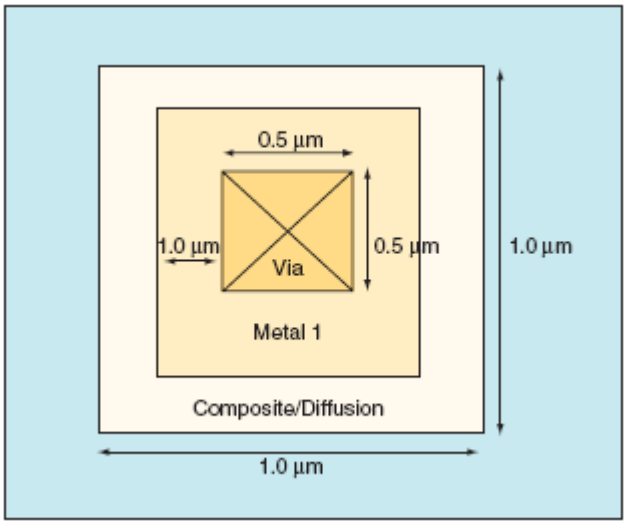

Figure 6. Protection diode top view

Figure 7 and Figure 8 show the side view of a P-Diode for the P-MOS process and an N-Diode for the N-MOS process, respectively. N-IMP, P-IMP, and DIFF are the fundamental mask layers. PDIFF and NDIFF are derived from these fundamental mask layers. Both types of protection diode can be

dynamically dropped after the placement is done. Since the protection diode is very small $(1\times1\mu m^2)$ compared to the cell size, it is not difficult to find empty area (N-MOS or P-MOS) to drop the protection diode or readjust a little bit of the cell location to get the space after the final placement.

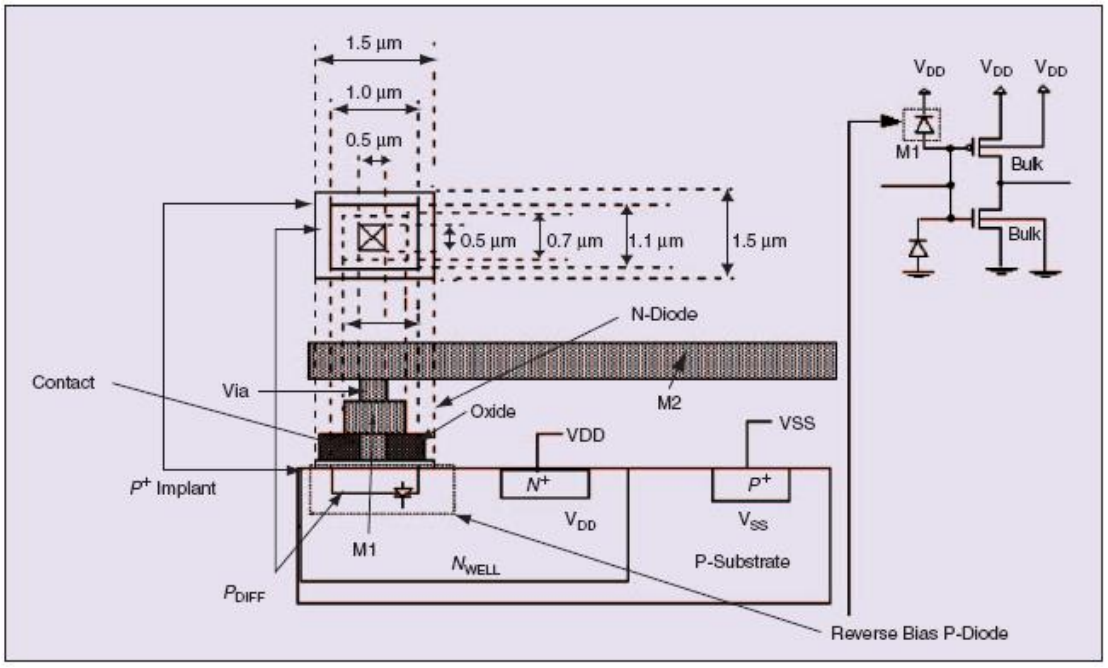

Figure 7. P-Diode structure for P-MOS process

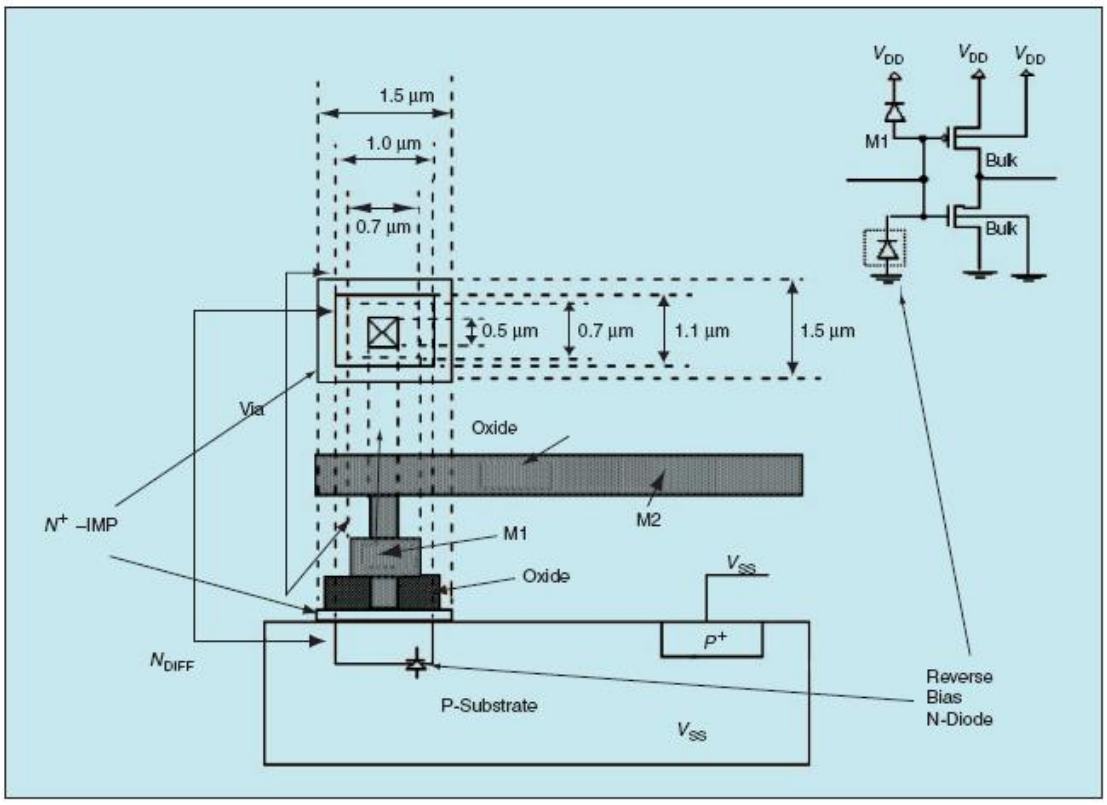

Figure 8. N-Diode structure for N-MOS process.

4.1 Diode Slicing

The purpose of diode slicing is to make sure the extra inserted diodes are fine through the examination of process engineer. Figures 9 and 10 show the cross-section of a diode. Figure 9 shows a cross-section of an N-diode just before entering into the tungsten plug (contact). The diffusion stain (the dark black area on N-COMP) shows that the diffused junction is big enough for current drainage. Figure 10 shows the same N-Diode on a

different die through the center of the tungsten plug. The N-COMP area is not stained. Figures 9 and 10 show the contact are correctly touching N-COMP.

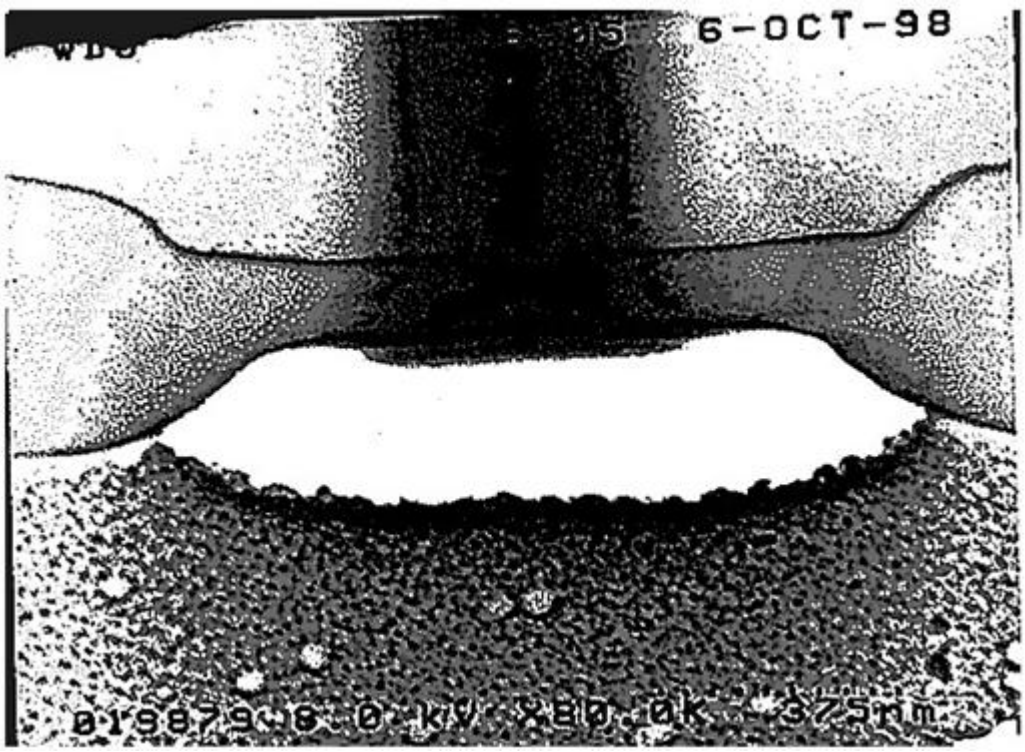

Figure 9. Cross-section of contact before entering into the tungsten plug

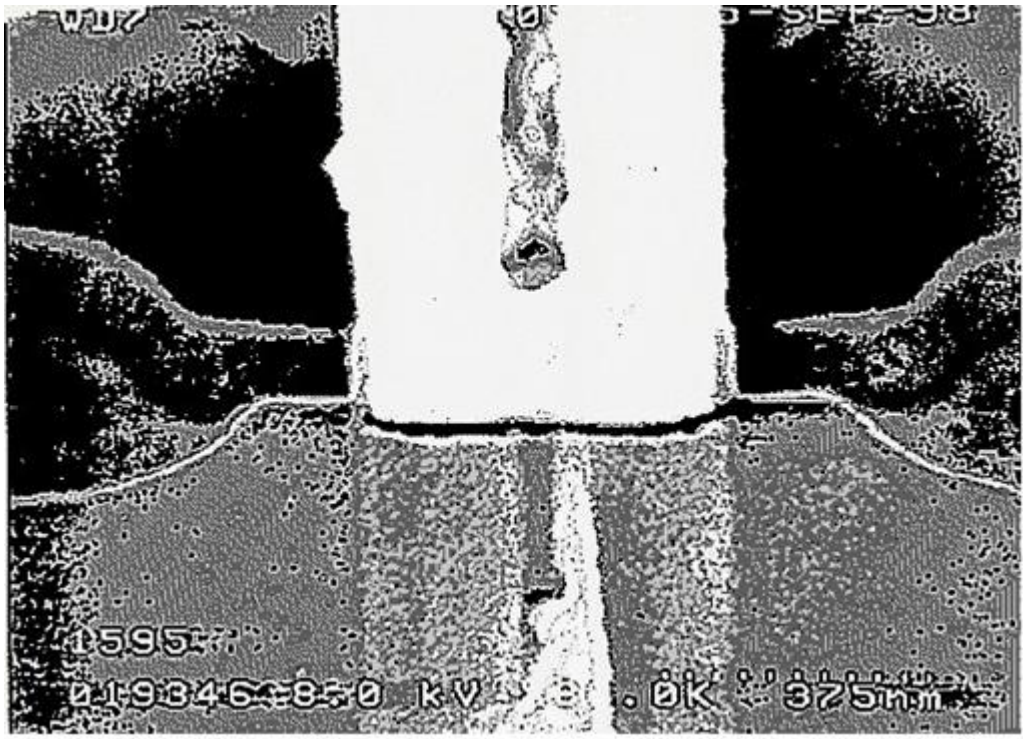

Figure 10. Cross-section of contact with tungsten plug

4.2 Diode Characterization

Figure 12 shows the N-diode's characterization. Three diode sizes (0.25, 1.0, and 25 μm^2) are compared. They all have the same clamped voltages, e.g., -10V. We determine the appropriate diode size based DRC rule. In this work, we use $1.1\mu m \times 1.1\mu m$ for $0.35\,\mu m$ process.

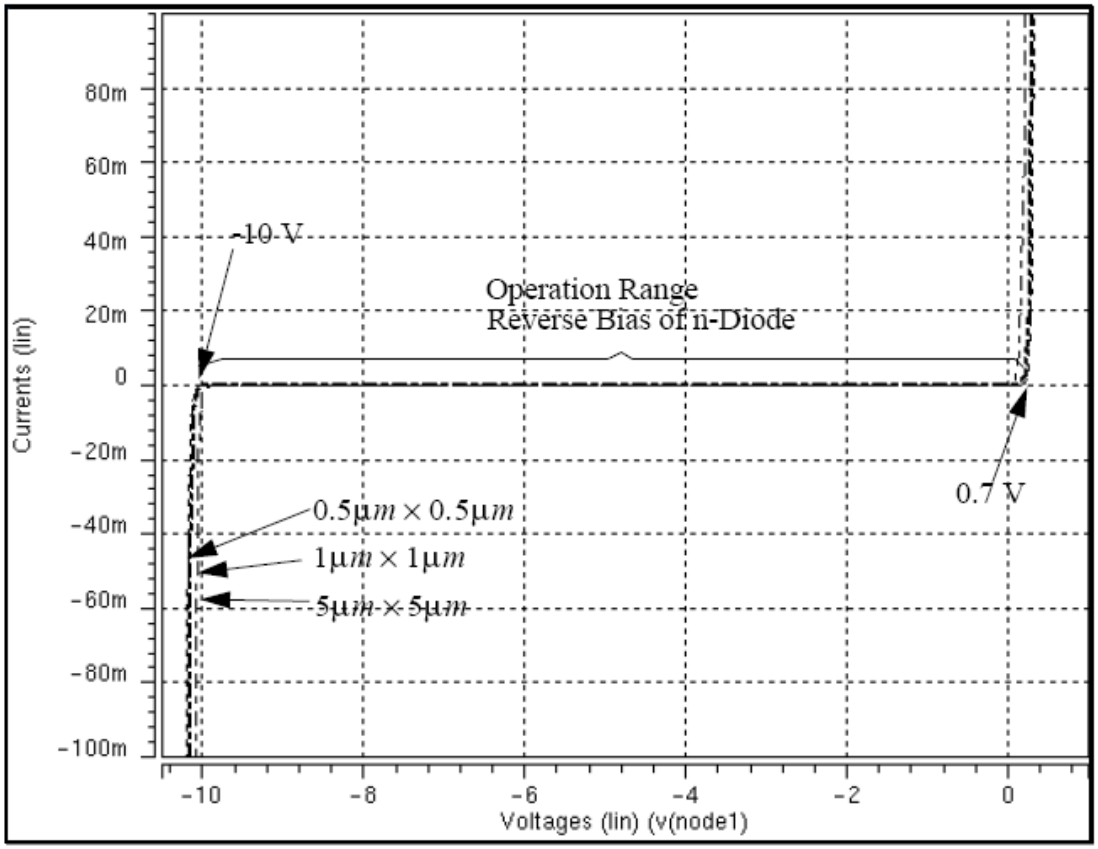

Figure 11. Reverse bias of N-diode operation diagram

Figure 12 shows SPICE results of P-diode with the same clamped voltage, e.g., -10V as the N-diode shown in Figure 11; except the leakage currents are different. The leakage current shown in Figure 12 for P-diode of 0.35 μm process, are as follows:

1. P-diode 225 nA and N-diode 290nA for diode area $0.5\mu m \times 0.5\mu m$
2. P-diode 900 nA and N-diode 1.2 μA for diode area $1\mu m \times 1\mu m$

3. P-diode 22.5 μA and N-diode 29 μA for diode area $5\mu m \times 5\mu m$

From Figure 11 and 12, we observe that the signal transmission is not destroyed or degraded during the normal operation. Both diode can be used for antenna fixing.

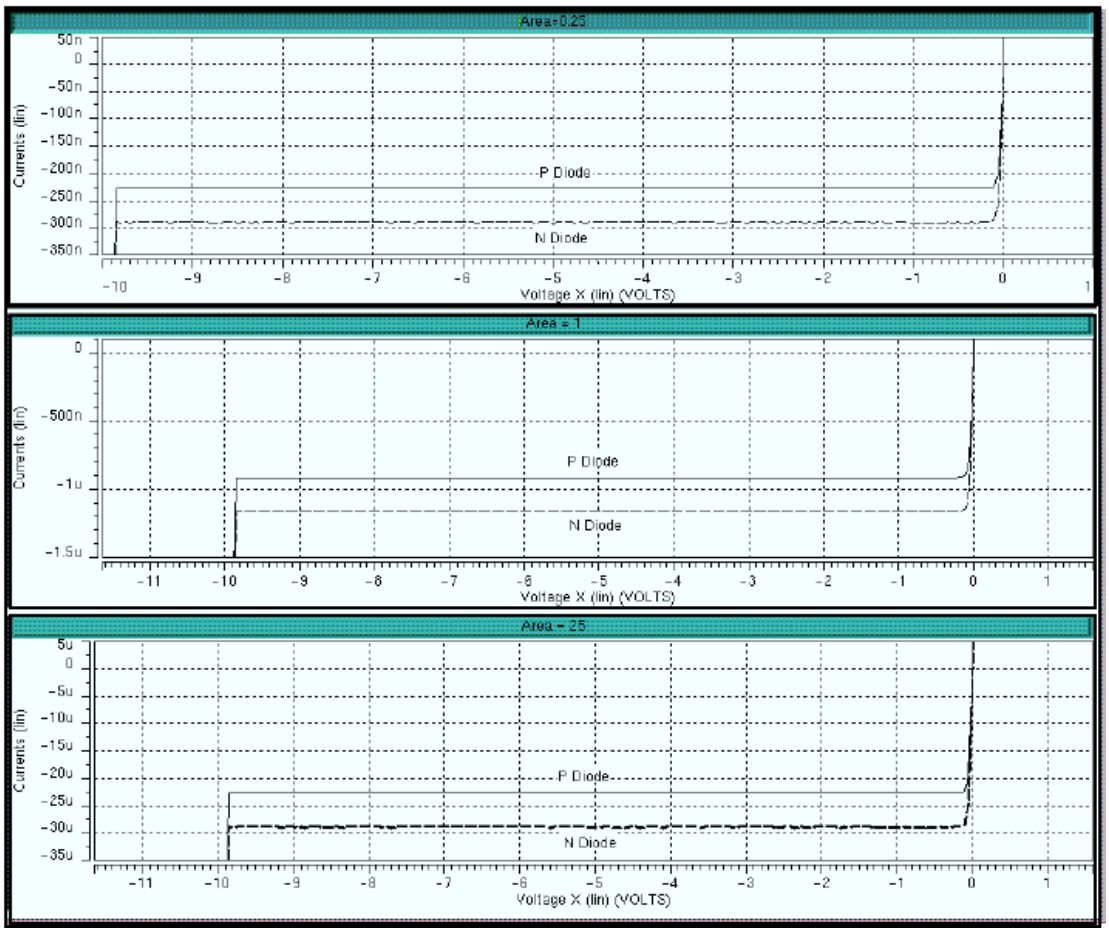

Figure 12. P-diode and N-diode leakage current for size 0.25, 1.0, and 25.0 um

4.3 Diode Leakage

Protection diode solutions are not without disadvantages, however. Currently, cell library vendors embed 1-3 protection diode(s) on each input pin. Because each standard cell contains multiple input pins, million gates chip designs would then contain several million protection diodes. According to our experience the majority of those diodes are not used. In addition to increasing manufacturing costs, the capacitance of each diode produces a very small leakage current, decreasing chip performance and leading to timing degradation. In fact, we experienced timing degradation up to 60% or worse, i.e., a desired 100 MHz chip may operate at 33.3 MHz when millions of diodes are employed. In fact, we have reduced the number of protection diodes needed from millions to hundreds by dropping them as needed at locations of antenna violations. Therefore, the post-layout dynamic protection diode dropping approach seems to increases efficiency in both performance and cost. However, due to the post-layout nature, even the reduced number of diodes is difficult to place on a congested design resulting in a

failure to fix the antenna problem after the routing is done. The inserted diodes also increase the manufacturing cost. How to minimize the number of diode insertion is another subject for future study.

5. Area, Voltage, and Temperature Effect of Protection Diode

The operating conditions of area, voltage, and temperature affect the protection diode. The simulation tools are eldo and adit by Mentor Graphics. Both tools are based on Berkeley BSIM4 and show the same results.

This section shows the drain current results of the n-type protection diode the following operation conditions:

1) DC sweep from-10V to 10V (area factor from 0.0001 to 1).

2) Area effect of antenna drain current

3) Voltage effect of antenna drain current

4) Temperature effect of antenna drain current

- Voltage = -6v, temp = -25, 0, 500 degree C
- Voltage = 0v, temp = -25, 0, 500 degree C
- Voltage = 6v, temp = -25, 0, 500 degree C

In order to drain the unwanted current from the plasma during the munufacture, the drain current should be as high as possible.

5.1 DC sweep and Area Effect

Figure 13 shows DC sweep from-10V to 10V with area factor (AF) from 0.0001 to 1.

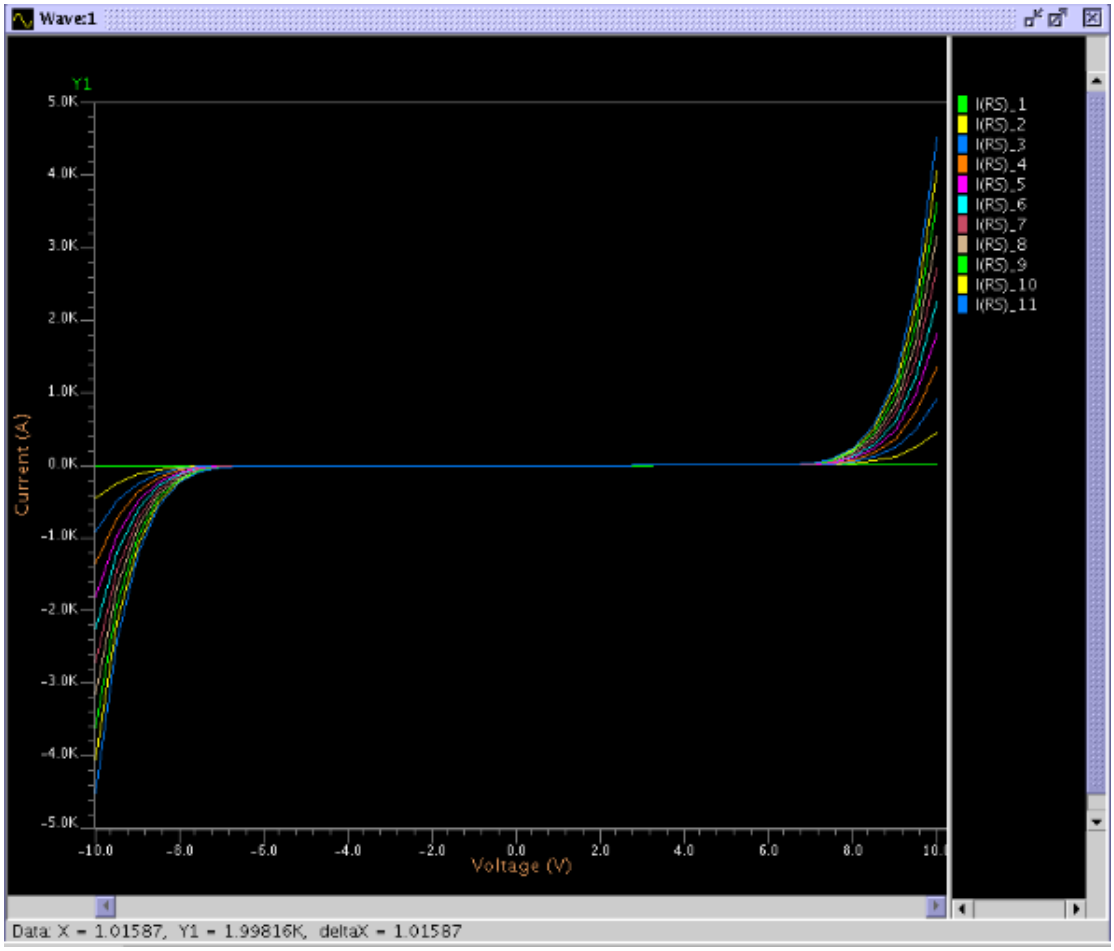

Figure 13. Drain current with DC sweep and area factor

5.2 Area effect of antenna drain current

Figure 14 shows the simulation result of drain current with area factor (0.0001, 0.005, 0.01) of 0.25um n-protection diode. The SPICE Model is set to Level 3, i.e., Fowler-Nordheim Model.

The Area Factor (AF) is 0.0001, 0.005, 0.01, respectively, at temperature 25 degree C and clamped voltage -10V.

Note: Berkeley Level =1 cannot model the area effect due to simulation tool limitation.

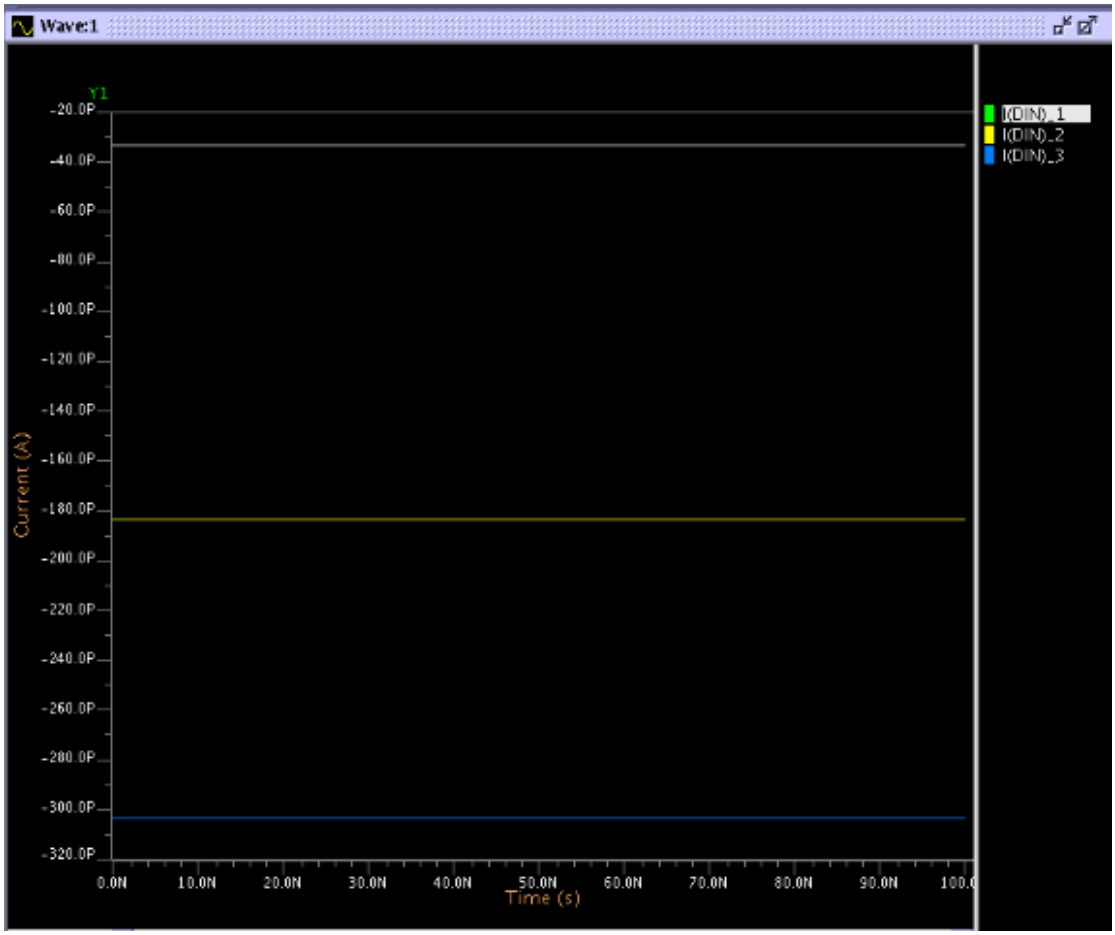

Figure 14. Drain current with area factor

5.3 Drain Current of Voltage Effect

Figure 15 shows the drain current results with clamped voltage = -10V, -5V, 0V, 5V, 10V across the n-type protection diode at

temperature 25 degree C and Area Factor = 1.

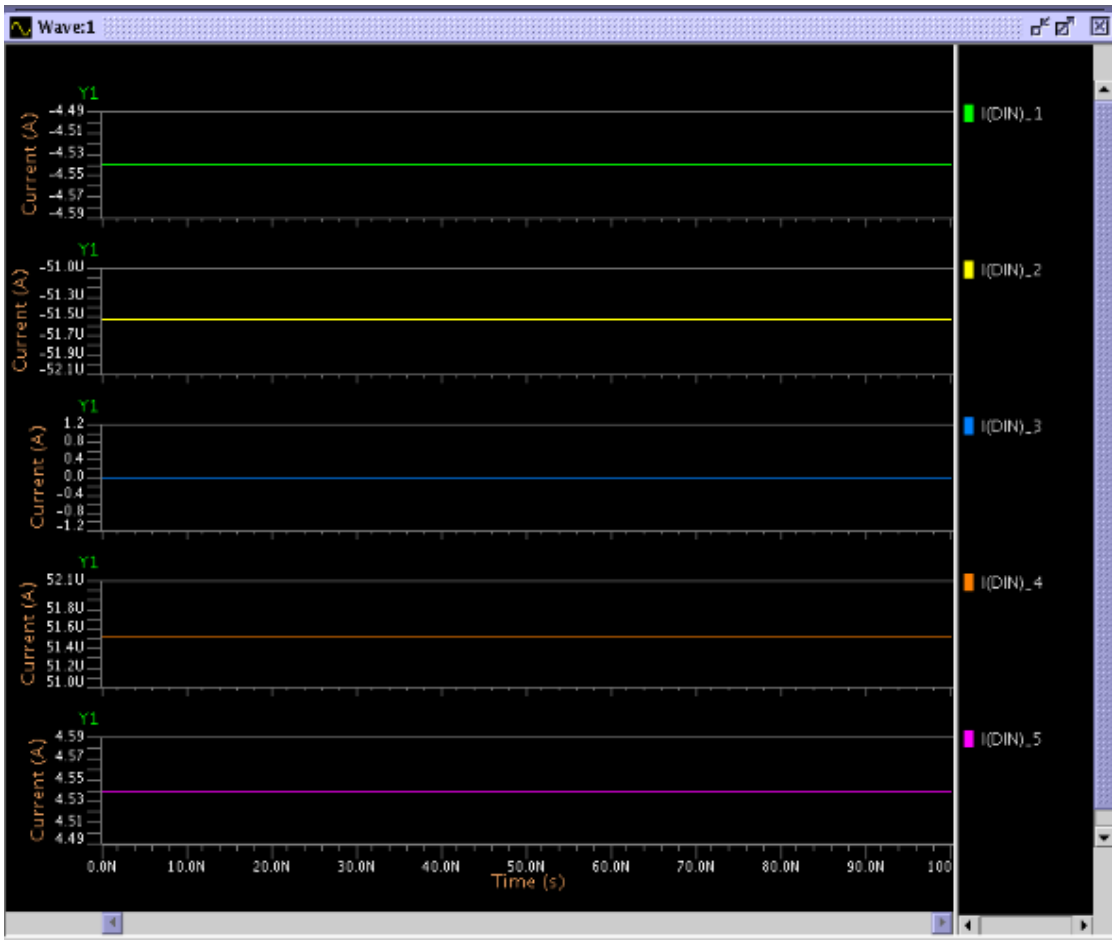

Figure 15. Drain current with clamped voltages (-10 to 10V)

5.4 Drain Current Temperature Effect

Due to Level =3 (Fowler-Nordheim model cannot modeling the temperature effect), I use Berkeley Level=1 instead.

Figure 16, 17, and 18 show the drain currents with temperatures at -25, 0, 500 degree C with clamped voltages of -6v (reverse

bias), 0v (no bias), and 6v (forward bias) across the n-type protection diode, respectively.

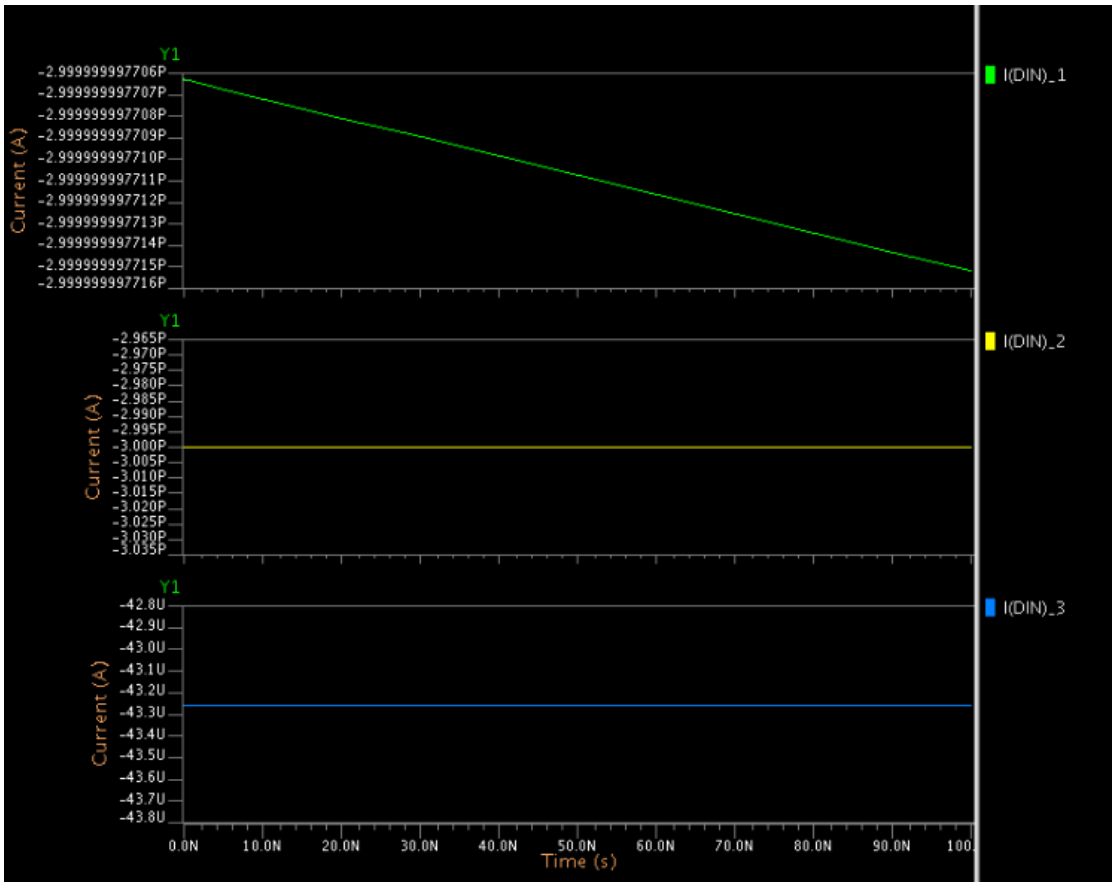

Figure 16. Drain current of temperatures -25, 0, 500 C (at -6V)

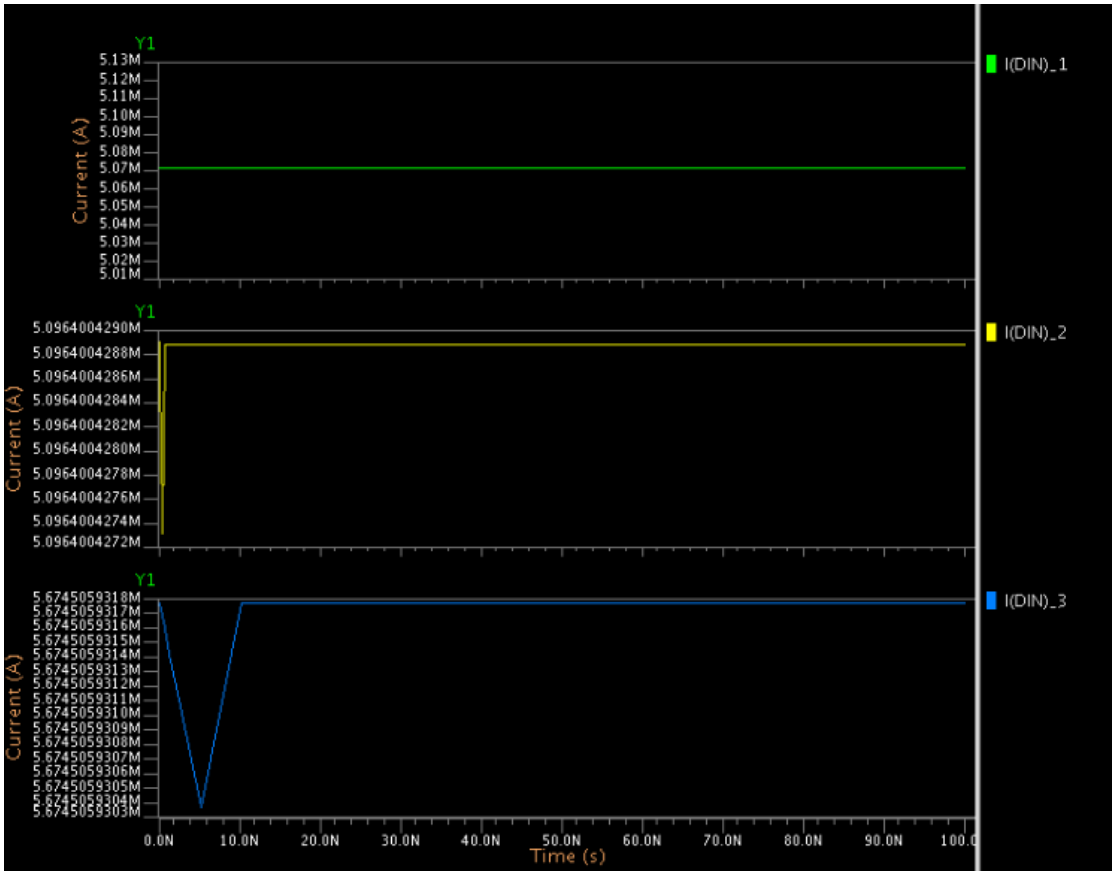

Figure 17. Drain current of temperatures -25, 0, 500 C (at 0V)

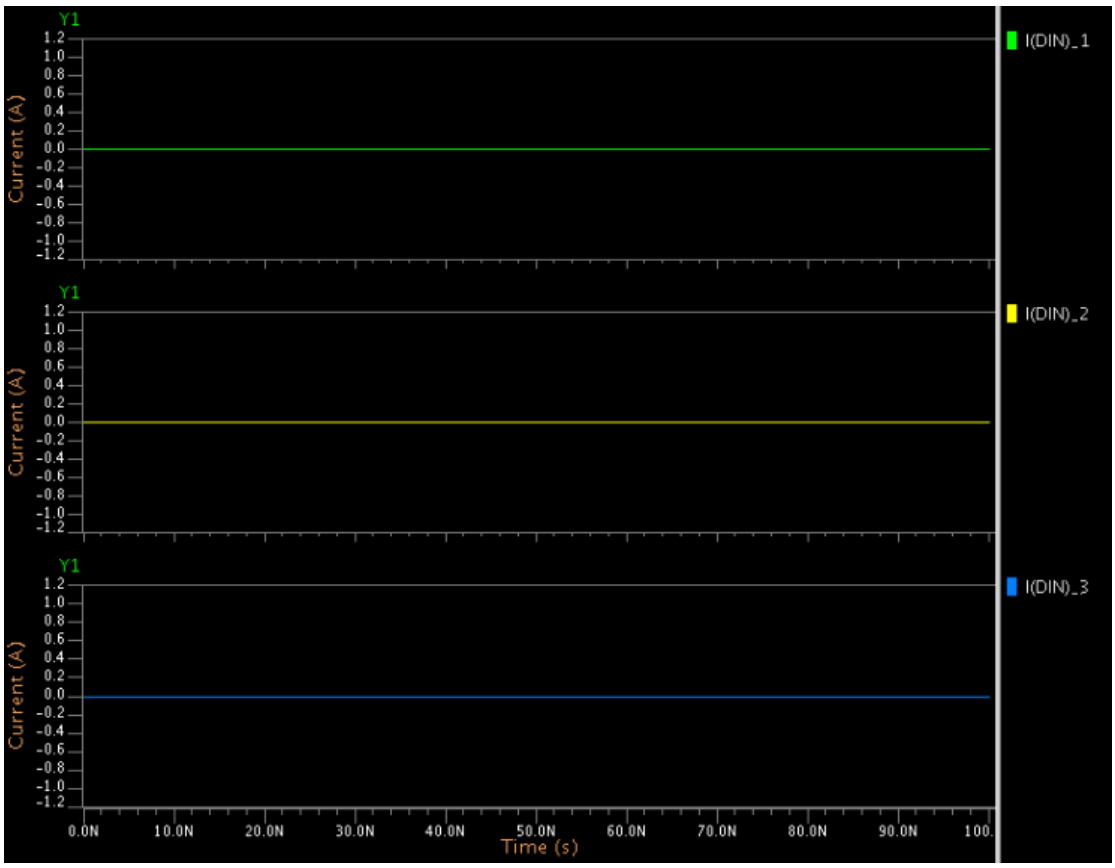

Figure 18. Drain current of temperatures -25, 0, 500 C (at 6V)

6. Proposed Antenna Solution

The antenna effect problem should be solved after final cell placement and before routing. Protection diodes are very small (about $1\times1\mu m^2$) compared to the standard cell size. They are easily inserted between the rows, cells, or anywhere in the design. At this phase, we can adjust cell location and avoid congestion or rerouting (which is extremely time consuming and difficult in the post layout phase). It is possible to reasonably predict where antenna problems will arise. By enclosing each input and output pin within a bounding box and calculating the half-perimeter [4, 10], we can pinpoint values that will cause antenna violations. Note that in situations of multiple fanout (one output pin drives several input pins) the summation of multiple half perimeters will be required. Even if this method of estimating antenna violations is not 100% accurate, congestion will be so much reduced that any violations discovered in the post-layout phase will be corrected much more easily.

6.1 Cell Placement Fundamentals

In order to avoid wasted space in the hierarchical design, our hierarchical design blocks are flattened into the top level which contains 1.2 million logic gates. Only the third party library blocks such as DAC, PLL, and memory blocks are still kept. Commercial tools using generic approaches (such as, quadratic programming, genetic algorithm, genetic evolution, or simulated annealing) have been unable to fully optimize efficiency with these approaches. Quadratic programming without constraints results in overlapped cells. [10, 17] Constrained quadratic programming requires linearization of the constraints by taking the Taylor expansion of the constraints. For blocks with more than 25 modules, it is not practical to solve linear equations with these linearized constraints for millions of cell modules. In addition, the constrained quadratic programming can be used to solve rectangular modules, but not the rectilinear modules common to ASIC design. [4]

Cell placement currently can take from several days to several

months since cell placement and routing are NP-problems and the time to solve them grows in an exponential manner. For the same reason, the tools exhaust memory resources resulting in core dump problems. Both these issues negatively affect time to market. Mathematicians continue to struggle for a solution to the NP-problem. This is not the approach I choose to take. Instead, I attempt to use a heuristic approach to simplify the existing problem domain. In other words, it is possible to use knowledge of design and design constraints to simplify the process without solving the NP problem.

[1, 2, 6, 7, 9, 11, 12, 14, 17, 18, 19, 20]

6.2 Proposed Solution for Fast Cell Placement

This work proposes a simplified model that uses IO-constraints based on the given package type. This method is not suitable for initial prototyping or other situation where the IO position is unknown. Using the circuit levelization offset and the algebraic median of the associated IO position, the initial cell placement is obtained. Circuit levelization determines:

1) the possible row numbers for each cell

2) the maximum number of siblings for each cell

3) the maximum level for each net by traversing the netlist connectivity from IO input to IO output.

The final placement is prioritized by timing constraints and is determined through combinatorial annealing. The annealing area is bounded by multiple fanout, i.e., determining the column position inside each row based on the timing cost function; and by multiple circuit levels, i.e. determining the row number inside each column based on the timing cost function.

6.3 Combinatorial Annealing Model

Assume the standard cells (or gates) are positioned at the center of each cell. Knowledge Based (Restricted Area) Annealing is used to find the best sub-optimal solution for cell location within the rows, for a cell belonging to a single circuit level, or within an area for a cell belonging to multiple circuit levels. Some

other annealing techniques can be combined with restricted area annealing.

The total wire length between gates is:

$$\frac{1}{2}\left[\sum_{i=1}^{M}\sum_{j=1}^{N_M}\left[c_{ij}\cdot\left(x_i-x_j\right)^2+c_{ij}\cdot\left(y_i-y_j\right)^2\right]\right], \qquad (6)$$

The total wire length between gates and I/Os (boundary constraints) is:

$$\frac{1}{2}\left[\sum_{i=1}^{M_{io}}\sum_{k=1}^{N_{io}}\left[c_{ik}\cdot\left(x_i-x_k\right)^2+c_{ik}\cdot\left(y_i-y_k\right)^2\right]\right], \qquad (7)$$

Where:

c_{ij} =1 if $i \neq j$, c_{ij} = 0 if $i = j$

M is the number of gates

N_M is the number of nets in each gate

N_{io} is the number of gates connected to the IOs

c_{ij} is the weighting of the net

The timing constraints for a critical net from source register (*s*) to destination register (*d*) can be estimated by the half-perimeter during the placement period:

$$t_{\min} \le \sum_{i=1}^{N_{rc}} R_i C_i + \sum_{i=1}^{N_g} \text{gate}_i + \text{ant\_del} \le t_{\max} . \quad (8)$$

In equation (8), the first term is the *RC* delay of this critical path. The delay calculator can be either Elmore or Asymptotic Waveform Evaluator (AWE). [4] The capacitances are calculated from the estimated metal distribution of each layer with the intrinsic, coupling, and fringe capacitances. The second term is the gate delay in the selected critical path. The term "ant_del" represents the delay caused by the protection diode insertion. The delay data can be roughly estimated by the half-perimeter method or calculated from pre-routing. Protection diode delay can be estimated by equation (5) with $R2 = 0$ and $C2 = 10^{-3}$ if only one protection diode is

dropped in the specified critical net. Equations (6), (7), and (8) can be rearranged with parameters defined as above into:

Minimize:

$$\frac{1}{2}\left[\sum_{i=1}^{M}\sum_{j=1}^{N_M}\left[c_{ij}\cdot\left(x_i-x_j\right)^2+c_{ij}\cdot\left(y_i-y_j\right)^2\right]\right]$$

$$+\frac{1}{2}\left[\sum_{i=1}^{M_{io}}\sum_{k=1}^{N_{io}}\left[c_{ik}\cdot\left(x_i-x_k\right)^2+c_{ik}\cdot\left(y_i-y_k\right)^2\right]\right]. \qquad (9)$$

Subject to:

$$t_{\min}\le\sum_{i=1}^{N_{rc}}R_iC_i+\sum_{i=1}^{N_g}\text{gate}_i+\text{ant\_del}\le t_{\max}. \qquad (10)$$

The final cell placement is annealed using (9) and (10).

7. Knowledge Based Priority Placement (KBPP)

Figures 19 and 20 show the traditional (generic) design flow versus the proposed Knowledge Based Priority Placement (KBPP) design flow. In the generic design flow, timing constraints and IO constraints are optional. In KBPP, the timing constraint, IO constraints, and dynamic protection diode insertions are required. KBPP uses the constraints as pre-knowledge to determine the cell's locations to replace the traditional quadratic programming approach, which is time consuming and results in overlapped cell locations.

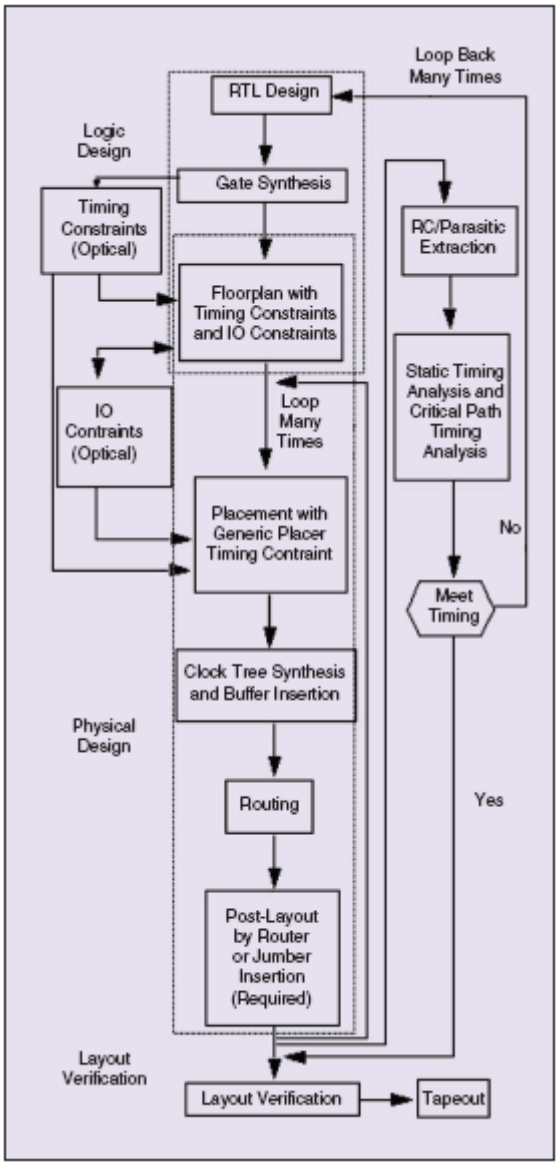

Figure 19. Traditional flow

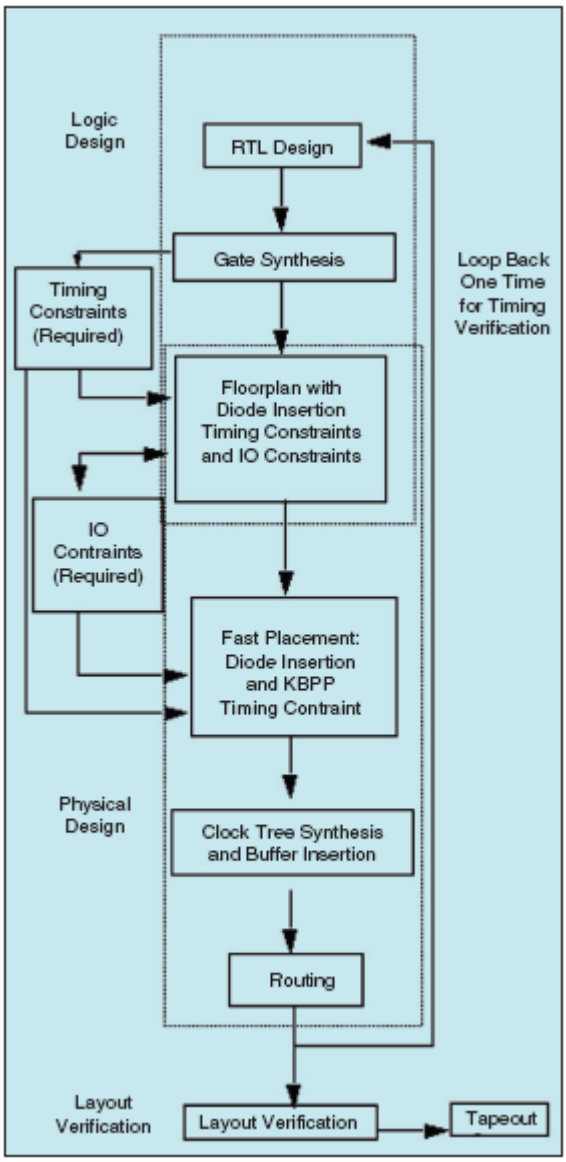

Figure 20. KBPP flow

7.1 Floorplanning and Timing Constraint

1) Carefully design the top-level pin orientations and location of large blocks, such as memory, DAC, PLL, and datapaths. Blocks should be placed near the top-level boundary and their pins placed along the sub-block boundaries that do not overlap

the top-level boundary. Top-level pins should be placed along the boundary away from the overlapping area, also. Determination of IO locations and directions is the most critical step at the beginning of chip layout. It is necessary to perform several IO-layouts and placements to examine the routing congestion in both rows and columns. Once the locations are determined, revised chips should maintain the IO-locations.

2) For prototype chip designs, carefully constrain the IO position with the designer and with floorplanning tools based on connectivity. After the IO position is set on the prototype, subsequent revisions do not need to go through this step.

3) Generate the timing constraint for the critical net and check whether or not it is reasonable. The timing constraint for all critical paths should be prioritized, e.g., from one register (dstw) to the RF register is 8 *n*s, tstd register to HIF block is 7.8 *n*s, etc. Those critical paths should be prioritized (by logic design) and placed within a bounded region (in physical design).

4) Add protection diodes to nets with antenna violations (Figure. 21). The typical size for the protection diode (or a tap) is about $1\mu m^2$ which is very small compared to the typical standard cell size (e.g., JK-Flip Flop size $35\times10\mu m^2$). The protection diode (either n-protection diode or p-protection diode) should be attached as close to the input port as possible. The antenna violation wire can be determined by traversing the placement cell location with the netlist associated with them. The protection diodes should never be dropped on power and ground rails. The dropped protection diode and JK-Flip Flop are shown in Figure 21 and 22.

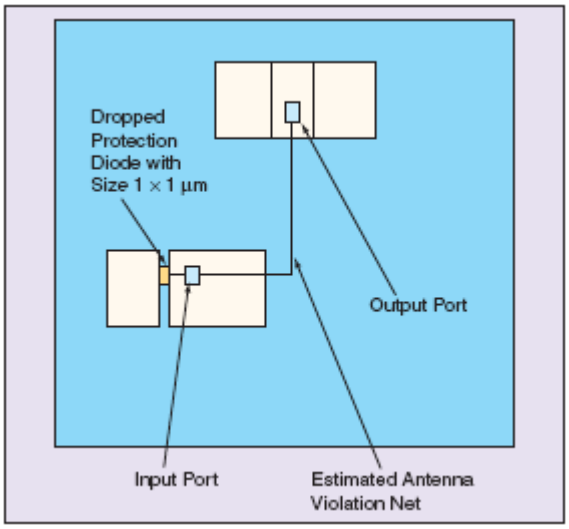

Figure 21. Protection diode insertion during cell placement

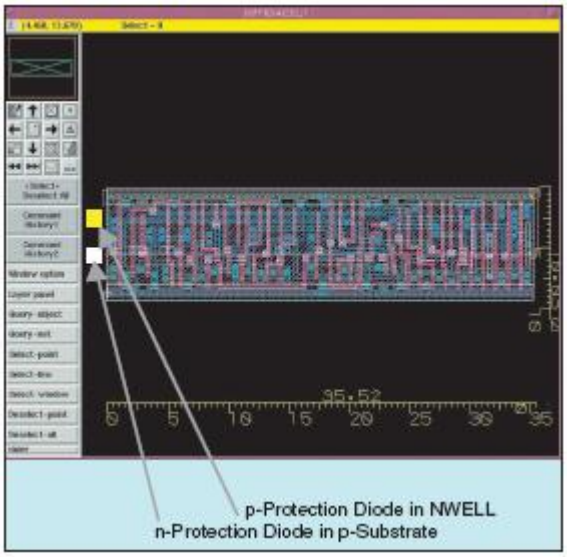

Figure 22. n-/p-protection diode insertion in cell placement

7.2 Cell Levelization

In KBPP, the cells are arranged by Horizontal Levelization and Vertical Levelization (such as VL-1, VL-2, VH-1, VH-2, etc.) while traversing the netlist as shown in Figure 23. Due to the different paths traversing, each cell can have different of circuit levels. Those circuit levels are stored in linked lists. If the cell is a single circuit level, row number for this cell is fixed. If the cell contains multiple circuit level, the final cell placement performs the restricted area refinement based on multiple circuit levels.

7.3 Initial Placement

Assume the IO and macros location / directions are properly floor planned. The locations of initial cell positions are obtained by simple algebraic median plus the level offset of the cell. If the maximum number of rows for any cell associated with a specific net exceeds the given number of rows, multiple columns or rows are required to place the cells. The multiple columns for a specified net can be determined by the following equation:

$$MUL\_col = round\left(\frac{Cir\_level}{Max\_col}\right) + 1, \quad (11)$$

Where:

- MUL_col is the column number will be placement for the specified net.
- Cir_level is the number of the circuit level after the circuit levelization.
- Max_col: is the maximum column specified by the user.

Cell congestion along one row can be treated in the same way. Figure 24 shows the initial placement with the cell levelization.

7.4 Analyze the Placement with Histogram

Analyze the vertical congestion, horizontal congestion, vertical cell area occupancy, and horizontal cell area occupancy. This data provides direction for iterative placement improvement. This step is mainly useful for refining cases of highly asymmetrical or highly fanned out circuitry.

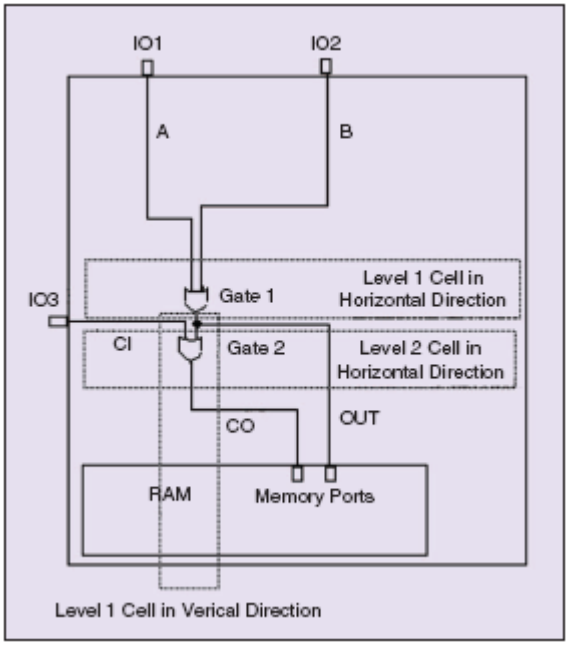

Figure 23. Cell levelization.

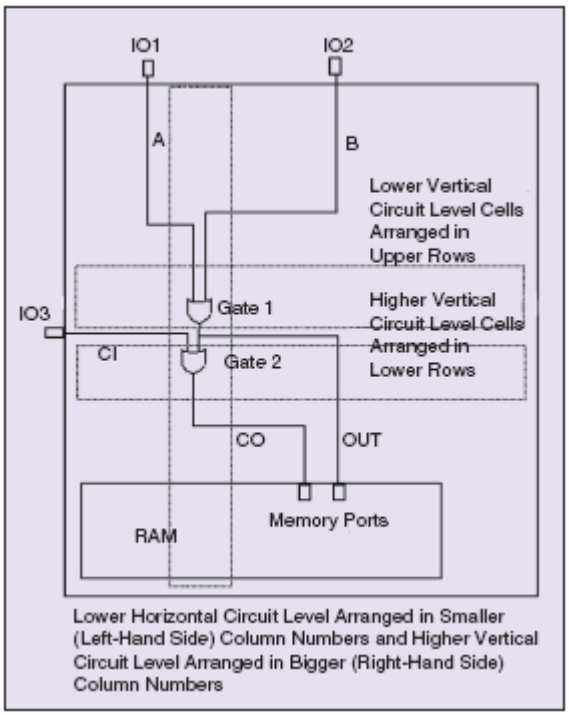

Figure 24. Initial placement with the cell levelization

7.5 KBPP Algorithm

The major KBPP algorithm is summarized as follows:

1. Prioritize the netlist by timing constraints.

2. Traverse each cell by the netlist. Find all the associated IO cells for each net and levelize the cell both vertically and horizontally.

3. Traverse netlist and find cell locations by taking the median of the cell's IO locations and the offset of the circuit levelization.

4. Perform the final placement.

5. Map vertical and horizontal congestion and adjust, arrange, or fold the cell position by modulating the row number. This step is for asymmetric layouts, such as datapath blocks or high fanout circuitry.

6. Traverse net and find antenna violation locations. Estimate wire length using the half perimeter of the bounding box. [4] Place a protection diode at the input port of cells associated with the antenna violations.

7. Perform clock synthesis and routing.

7.6 Post-Layout Antenna Fix

There should be no antenna problem since protection diodes are added during the placement period. If antennae exist, dynamically drop protection diodes to fix the antenna net. Some extension wire can be added to provide more space to add protection diodes. A smart router, which re-route the antenna violation net, can also be tried. Start from the top of the input port of the topmost layer and route down to the output port. Figure 25 shows the dropping protection diode during post-layout using extension wire due to congestion.

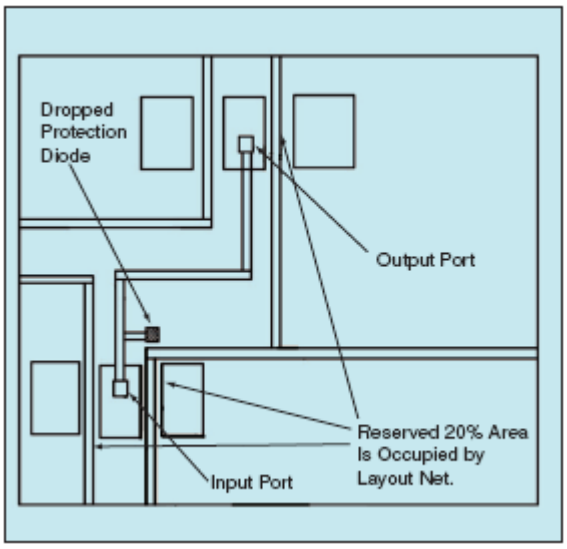

Figure 25. Dropping protection diode using extension wire

8. Result Comparison

The following table shows the comparison between the KBPP with post-layout antenna fixing and quadratic placer.

Table 1. Result Comparison.

	Post-layout jumper insertion with smart router	Post-layout dynamic protection diode insertion	KBPP
Circuit placement time	5 hours (Sun Sparc with 8 CPUs)	4–6 hours (Sun Sparc with 8 CPUs)	20 min on a PC
Antenna violations	Fixed 156 violations. two remaining	Fixed 160 with five remaining. Router has difficulty to find the reroute space.	All fixed.
Chip area	10% reserved for congestion.	5% reserved for congestion.	0% extra area reserved for antenna fixing
Timing requirement	Not met	Met. Best timing delay in critical net 6.2 ns.	Met

8.1 Chip Example

This work uses two chip designs to illustrate the differences of the generic approach and the KBPP approach. The first design is the hierarchical design containing one DAC block, one PLL, and about 10 hierarchical glue logic blocks. Each level of modules contains around 100K-300K cells. The generic solution is able to handle it on each level of hierarchy properly. The second design is flattened containing 2-DAC blocks, 3-PLLs, and approximately 250K more glue logics than the first example.

The number of gates on the top level is about 1.2 million. Flattening the design allow the chip to hold 25% more circuitry than with the hierarchical design. However, the generic solution is not able to handle cell placement. The resulting cell placement could not resolve timing violations. [4] In addition, the process took too long.

Figures 26 and 27 show the Teralogic designs used as test cases. A Sun-Sparc™ workstation with 8 CPUs running in round robin fashion at 400 MHz with 14 GB of main memory per thread was used to perform the first two approaches to cell placement and antenna fixing. The KBPP placement was performed on a PC and the results were transferred in Physical Design Exchange Format (PDEF) or Top Design Format (TDF) to the workstation. [4, 7, 8] In the hierarchical chip, since the number of cells on the top level is within generic can handle, both the generic and KBPP approaches are working fine. For the flatten type of chip with about 1.2 million cells (standard cells, filler cells, IOs, macros, pad cells, IO filler cells) on the top, the generic

approach is not able to handle it properly. KBPP or other in house tool using the simple cut approach can meet the requirements.

Figure 26. Teralogic HDTV hierarchical chip done by KBPP

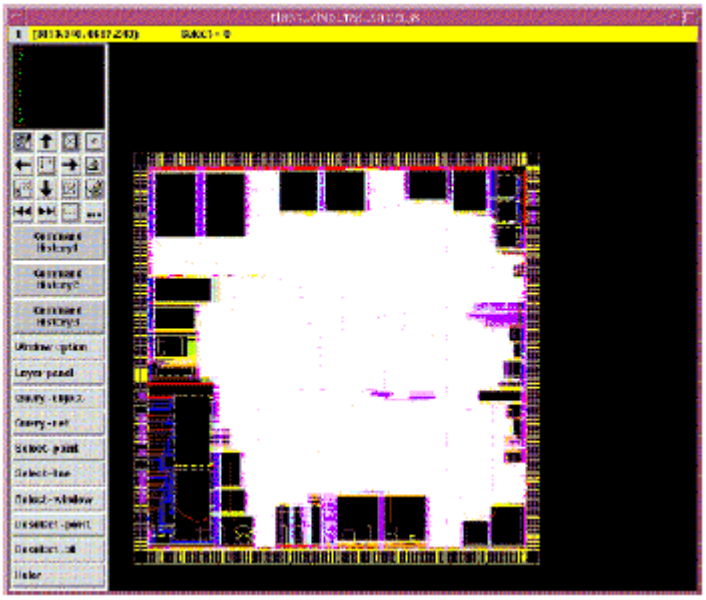

Figure 27. A Teralogic HDTV flatten chip done by KBPP

9. Post-Layout Antenna Solution

If chip implemented without KBPP and with antenna problem, the post-layout antenna fixing is required. This section describes three ways to fix antenna problems during the post-layout: (1) diode dropping, (2) jumper insertion, and (3) diode dropping with extension wires.

9.1 Overall Flow of Post-Layout Antenna Solution

Figure 28 shows the overall flow for fixing antenna problems by dynamic diode dropping and jumper insertion.

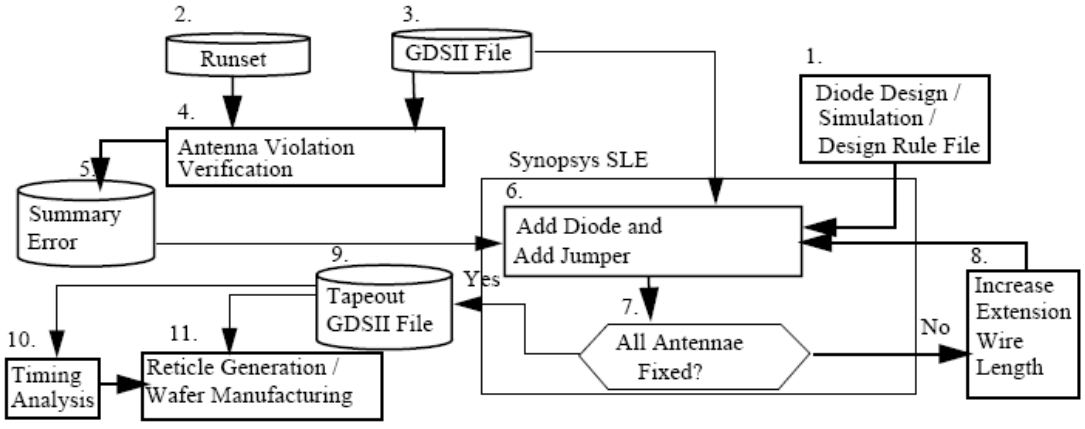

Figure 28. Overall Flow for Post-Layout Antenna Solution

9.2 Procedures for Post-Layout Antenna Fixing

The procedures for post-layout antenna fixing are illustrated below:

1. Make sure the rule file specifications follow your process design rules and DRC rules.
2. Bring up the tool for antenna fixing.
3. Create the new library or open the existing library.
4. Stream in GDSII file.
5. Import the P-Diode and the N-Diode from the GDSII format or create them from scratch.
6. Open the top level cell.
7. Drop the diodes (P-Diode or N-Diode) without extension wires according to the rule files specified in Step 1.
8. Insert the jumper for the rest of the violation (if there is no space to drop a diode).
9. Increase the extension wire to accommodate a bigger area, for example, 5 μm .
10. (Repeat Step 9 until all the violations are cleaned.)

11. Save the design in a GDSII format.
12. Visually check the diode insertion one-by-one. Search and trace all the diodes which are inserted. Examine the diode structure, location of dropped diodes, and make sure the diodes touch the right layers.

For dense designs, it is hard for tools to find the space to drop the diodes. The extension wire gives more space for diode dropping. The extension wire's width is very important for the design rule. If the extension wire width is too small, it causes notch errors. The right wire has a bigger width (the same as the diode width) and will not cause any DRC error. Figure 29 shows a diode connected to an extension wire.

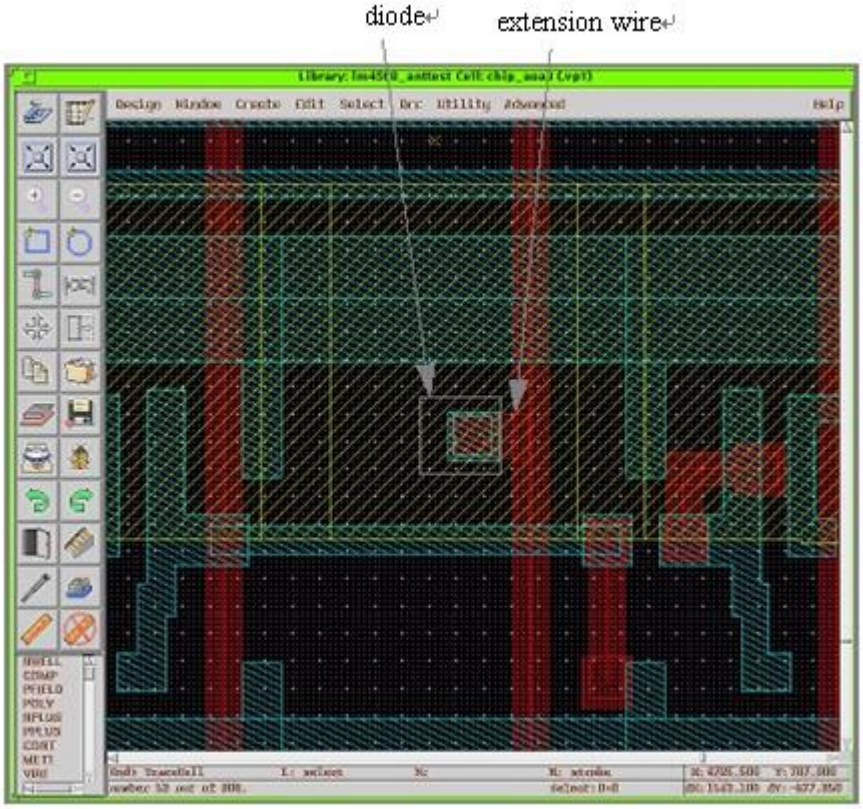

Figure 29. Diode insertion with an extension wire

Table 2 shows some results of 0.35 μm technology. The specification of a maximum antenna ratio is 400 without diode insertion, and the maximum ratio is 5000 with diode insertion. Both design examples in Table 2 are approximately one-quarter of a million gates. Here, we define the dense design as core utilization of more than 90% and the sparse design as core utilization of less than 50%.

For the dense design example, the original number of antenna

violations for Metal 3 is 154. After diode dropping, the number of violations for Metal 3 is reduced to 21. After adding jumpers, the violations for Metal 3 are reduced to 3. Finally, using 20 μm extension wires to drop the diode, the antenna violations are clean. Note that in the topmost metal (e.g., Metal 4), there never have antenna violations. Since after the wire is connected, the charge discharges into the output port.

Normally, Metal 1 also has no antenna violations. This is because Metal 1's resources are occupied by standard cells. Therefore, there is very limited space for the router to generate the antenna problem. Metal 2 violations are very easy to fix, since the tool can always find the space to drop a diode. Metal 3 violations are difficult to fix due to the limited space resources. For some designs with limited routing resources (e.g., when only three metals are used), core utilization is low (e.g., 49%). These designs have lots of space to insert diodes, and most of the violations can be fixed after the first run of diode dropping.

Table 2. Dynamic diode and jumper insertion

Design names	Violation	Diode insertion without exten-sion wires	Add jumper	Diode insertion with 20 ∝μ extension wires
Design 1: dense design	M4: 0 M3: 154 M2: 23 M1: 0	M4: 0 M3: 21 M2: 0 M1: 0	M4: 0 M3: 3 M2: 0 M1:0	M4: 0 M3: 0 M2: 0 M1: 0
Design 2: sparse design	M4: 0 M3: 788 M2: 521 M1: 0	M4: 0 M3: 1 M2: 0 M1: 0	M4: 0 M3: 0 M2: 0 M1: 0	N/A

10. Discussion and Conclusion

KBPP, although introducing no new design theories, makes significant progress toward resolving antenna effect and cell placement issues by analyzing and simplifying the model. The critical net should be considered as the highest priority for placement routing to ensure the timing. The placement speed should be greatly improved by using the constrained locations as pre-knowledge.

Similarly, by using KBPP to anticipate antenna problems and drop protection diodes as needed, efficiency is greatly enhanced. The chips for which this approach was used needed approximately 200-500 protection diodes during the placement period, reducing the chip size by 25% without causing any congestion, timing degradation, or decrease in chip performance.

This work focuses on using existing constraints and knowledge

to optimize efficiency and does not address timing optimization by buffer insertion or gate resizing. This knowledge-based cell placement approach was first tested in datapath and memory cell placement, although no example of the datapath placement is provided within this work.

11. Acknowledgement

Thanks Professor Vincent Tsong-Liang Huang help, my father's financial support, and my wife's financial and spiritual supports. This dissertation if finally finished.

I am glad that I finally fulfilled the promise to my father, my wife Irene, and my four kids (Jessica, Jason, Jasmine, and Jonathan). My father passed away in 2008. He supported my PhD study and had never seen my completion. My wife takes care of kids and allows me focusing on my work and study in the past twenty years. They all want to see a clear educational model of my family.

In addition, I would like to thank the following companies and people:

- LSI Logic datapath and Sun Java chip projects for fast placer implementations.
- National Semiconductor audio chip project for resolving the

antenna problem.

- Teralogic HDTV project for the fast placer verificaiton.
- Avanti accepted my antenna solution and implemented into Hercules and Apollo.
- Synopsys accepted this antenna solution in 1996-2002.
- IEEE / ISQED and IEEE / Devices and Circuits Magazine published antenna and KPBB methodology, respectively.
- My technical writer, Stacy Austin, carefully reviewed and reorganized my writing and challenged me with effective questions.
- LSI Logic Dr. John Shively taught physical design and placer implementation.

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13. Appendix