Discharge-Path-Based Antenna Effect Detection and Fixing for X-Architecture Clock Tree

Journal:	*IEEE Transactions on Very Large Scale Integration Systems*
Manuscript ID:	TVLSI-00341-2009.R1
Manuscript Type:	Brief
Date Submitted by the Author:	21-Dec-2009
Complete List of Authors:	Tsai, Chia-Chun; Nanhua University, Computer Science and Information Engineering Kuo, Chung-Chieh; National Taipei University of Technology, Computer and Communication Engineering Lee, Trong-Yen; National Taipei University of Technology, Electronic Engineering Hsu, Feng-Tzu; National Taipei University of Technology, Computer and Communication Engineering
Key Words:	Antenna effect, discharge path, jumper insertion, layer assignment, X-architecture clock tree

Discharge-Path-Based Antenna Effect Detection and Fixing for X-Architecture Clock Tree

***Abstract*—Antenna effect is a phenomenon in the plasma-based nanometer process and may influence the manufacturing yield of VLSI circuits. For a given X-architecture clock tree that connects *n* clock sinks, we consider the antenna effect and propose a discharge-path-based antenna effect detection method. To fix antenna violations, we apply the jumper insertion technique, and moreover, a layer assignment method is presented for reducing the jumper and via counts. Different from other works, the delay of inserted vias is considered in delay calculation, and a wire sizing procedure is employed for skew compensation. The proposed PADJILA algorithm runs in $O(n^2)$ to obtain an antenna-safe X-clock tree. Experimental results on benchmarks show that our approach achieves significant reductions of 48.21%, 0.02%, 0.02%, and 20.35% in terms of inserted jumpers, delay, power consumption, and via count, respectively, than existing works.**

***Index Terms*—Antenna effect, discharge path, jumper insertion, layer assignment, X-architecture clock tree.**

I. Introduction

As the feature sizes shrink into the nanometer scale, the manufacturing yield on very-large-scale-integration (VLSI) circuits is becoming a crucial challenge. In the manufacturing process, conductors (such as polygon and metal) not covered by a shielding layer of oxide are directly exposed to the plasma and act like antennas to collect charges. The amount of such charging is proportional to the plasma-exposed area [1]. When a gate oxide connects the charged metal wires, the Fowler-Nordheim (F-N) tunneling current may damage the gate oxide through a discharge path, as shown in Fig. 1(a). This phenomenon is called the antenna effect.

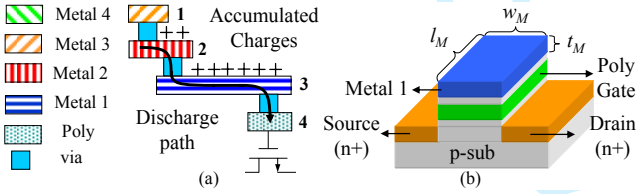


Fig. 1. (a) Antenna effect is occurred due to accumulated charges may damage the gate oxide through a discharge path. (b) An NMOS.

The antenna ratio (*AR*) is defined as the ratio of the exposed antenna area to the gate oxide area [2-3], and it should be controlled under a threshold value for antenna effect avoidance. In the design manual of TSMC [4], the exposed antenna area and gate oxide area are defined as side-wall area $A_{s,metal}$ and polygon area A_{poly}, respectively. For area calculation, $A_{s,metal}$ and A_{poly} are respectively formulated as $2(w_M+l_M)t_M$ and $w_M l_M$, where w_M, l_M, and t_M are the width, length, and thickness of a conductor, as shown in Fig. 1(b). The manual indicates that the required *AR* of $A_{s,metal}/A_{poly}$ is 400, and thus the upper bound for antenna effect, denoted as L_{max}, is derived as 200μm. If a metal wire or the concatenated metal wires is longer than L_{max}, an antenna effect will be occurred [1, 5, 6, 10]. In Fig. 1(a), the total exposed wire area of the gate oxide is calculated from poly to metal 2, and the discharge path is the sum of segments 2-4 [11-13]. When the discharge path is longer than L_{max}, it has an antenna violation.

Krishnan *et al.* [14] presented a consequence of competition between reducing *AR* and increasing gate area and indicated that the

antenna failure depends on plasma/oxide parameters when antenna area is fixed. Simon *et al*. [15] considered the time of metal etching process and proposed an improved *AR* model. Verret *et al*. [16] observed that the ratio of the capacitance per unit area of the gate capacitor to that of the antenna capacitor is more important than *AR*. Therefore, they presented a new model to predict the antenna effect.

There are three general techniques for fixing antenna violations. 1) Insert a jumper to break or shorten the antenna-violation wire [1, 5]. 2) Assign the antenna-critical wire with higher layer [13]. 3) Embed protection diodes on the input ports of standard cells [6]. Because the third technique may cause layer congestion problem, extra capacitances on wires, and leakage power, the other two techniques are more popular for physical synthesis tools to achieve an antenna-safe layout.

In a VLSI system, a clock tree connects all the clock sinks for the system synchronization with minimum clock delay and skew. These sinks are the clock input ports of standard cells or intellectual properties (IPs). Consequently, the antenna effect of the sinks in a clock tree should be addressed. X-architecture clock trees have recently been developed [7-9] that perform better in delay, cost, and power consumption compared with general Manhattan architecture clock trees. Unfortunately, the works [7-9] ignored the antenna effect which is one of DFM issues. In this paper, we propose a discharge-path-based antenna effect detection method for a given X-architecture clock tree. The detection method first obtains the total discharge path for each clock sink. Then, jumpers are correctly inserted to fix antenna violations. In addition, we present a layer assignment method that provides layer candidates to antenna-critical wires and modifies their layers to reduce jumper and via counts. After fixing antenna violations, the antenna-safe X-clock tree consumes more vias than the given X-clock tree. The clock delay is increased, and the clock skew is not zero anymore [10] due to the delay of inserted vias is considered in delay calculation. Hence, a wire sizing technique is applied to achieve zero skew. Experimental results indicate that our approach has more improvements in jumper and via counts, clock delay, and power consumption than existing works.

Section II formulates the problem of antenna effect detection and fixing for a given X-clock tree. Section III presents the proposed algorithm and discusses each procedure in detail. Experimental results on benchmarks are reported in Section IV. Finally, the conclusion is given in Section V.

II. Problem Formulation

An X-clock tree connects a set of clock sinks, and the clock sinks may be damaged due to the accumulated charges. To address the antenna effect of a clock tree, Tsai *et al.* [10] first defined the antenna avoidance problem for X-clock trees. If a metal wire is longer than L_{max} and not routed on the top layer, the jumper insertion (JI) technique will be applied to fix the antenna violation. A jumper needs vias to connect the top layer, and the delay of inserted vias would degenerate the clock performance. To reduce the number of required jumpers, they combine jumper insertion and layer assignment (JILA) techniques to assign antenna-critical wires with the top layer. The portion of X-clock tree and its corresponding layout shown in Figs. 2(a) and 2(b) are taken as an example to present the antenna effects. In the layer configuration of the X-clock tree, horizontal and vertical wires are assigned with metals 1 and 2, as well as, diagonal (±45°) wires are assigned with metals 3 and 4, respectively. JI [10] detects the X-clock tree and gets that the wire connecting bending point $P_B(s_7, s_8)$ and sink s_7 (s_8) is longer than L_{max}. In Figs. 2(c) and 2(d), two jumpers are separately inserted into two antenna-critical wires for antenna avoidance, and the two wires are cut shorter than L_{max} by switching the parts of wires to the top layer (i.e., metal 4). The two jumpers totally need eight vias.

As aforementioned in Section I, antennas collect charges and damage clock sinks through discharge paths. In Fig. 2(b), the segments 1-3 and 5-8 are the antennas for s_8 and s_7 since they are surrounded by the segments 4 and 9 assigned with the highest layer (i.e., metal 3). The discharge paths dp_1, dp_2, and dp_3 may damage s_7 and s_8. If we directly take dp_1 and dp_2 as the total

discharge path of s_7, the common segment 6 will be counted twice to result overestimation. Thus, the common segments should be considered during the determination of the total discharge path of a sink. As shown in Figs. 2(e) and 2(f), a jumper is inserted to fix the antenna violation because the total discharge path of s_7, the sum of segments 5-8, is longer than L_{max}. The inserted jumper only needs two vias due to the antenna-critical wire is switched to metal 2 by the jumper and then switched back to metal 1. On the other hand, s_8 is antenna-safe since dp_3 is the sum of segments 1-3 and shorter than L_{max}. Comparing Figs. 2(d) and 2(f), JI [10] inserts an extra jumper and consumes six more vias. The comparative result shows that detecting antenna effects with discharge paths is more accurate.

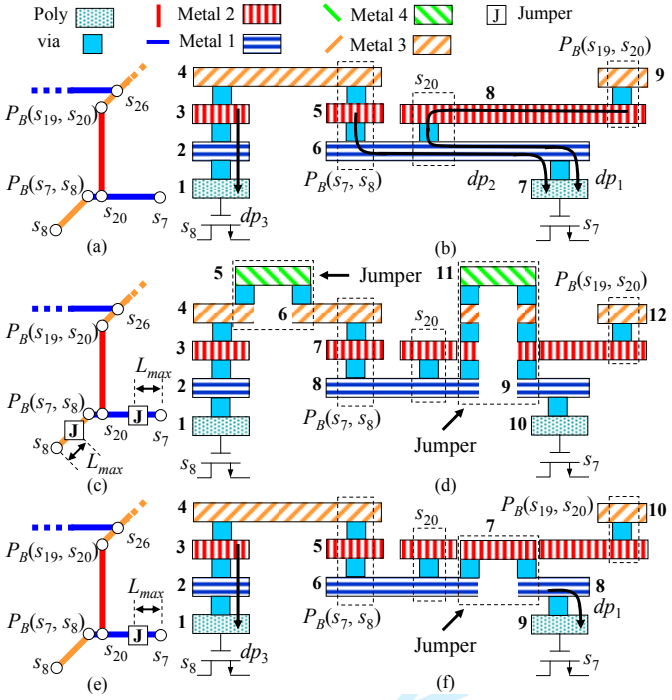


Fig. 2. (a) A portion of X-clock tree. (b) Three discharge paths respectively affect s_7 and s_8. (c) JI [10] inserts two jumpers to fix antenna violations. (d) The two jumpers totally need eight vias. (e) One jumper is inserted using discharge paths for detection. (f) The jumper just needs two vias.

With the above discussion, the problem of antenna effect detection and fixing for an X-architecture zero-skew clock tree is formulated as follows.

Given an X-architecture zero-skew clock tree with a set of clock sinks $S = \{s_1, s_2, \ldots, s_n\}$, a layer configuration of metal 1 to metal 4, and an upper bound for antenna effect L_{max}, the objective is to detect antenna effects and to fix all the antenna violations with minimum jumpers and zero skew.

III. Discharge-Path-Based Antenna Effect Detection and Fixing

Fig. 3 shows the proposed algorithm of discharge-path-based antenna effect detection and fixing antenna violations with jumper insertion and layer assignment techniques, called PADJILA, for a given X-clock tree. For a sink $s_i \in S$ in the given X-clock tree, if the segment connecting s_i, denoted as $e(s_i)$, is on the top layer of layer configuration, denoted as L_{top} (in this work, L_{top} is metal 4), s_i will be antenna-safe (lines 2-3). Otherwise, the antenna effect detection procedure of *DischargePath*(s_i) is applied to obtain the total discharge path of s_i, denoted as $DP(s_i)$ and each path $dp_i \in DP(s_i)$. When obtaining the total segment of $DP(s_i)$, denoted as $e_{total}(s_i)$, the common segment is removed by using the procedure of *ComSeg*($e_{total}(s_i)$, $\forall e_i \in dp_i$) to avoid overestimation (lines 5-7). Next, we compare the length of $e_{total}(s_i)$, denoted as $|e_{\text{total}}(s_i)|$, and the upper bound for antenna effect L_{max} (line 8). If $|e_{total}(s_i)|$ is

longer than L_{max}, the jumper insertion procedure of *InsertJumper*(s_i) will insert a jumper to fix s_i and count the vias of s_i, denoted as $via_{original}$ (lines 9-10). Moreover, the layer assignment procedure of *LayerAssignment*(s_i) is introduced for reducing jumper and via counts and gets the layer candidates $Layer_{can}(s_i)$ for s_i (line 11). After that, $Layer_{can}(s_i)$ is assigned to $e(s_i)$, and then the reduced vias of s_i, denoted as $via_{modified}$, is obtained (line 12). If $via_{modified}$ is less than $via_{original}$, we will remove the inserted jumper and assign $Layer_{can}(s_i)$ to $e(s_i)$ for via reduction (lines 13-14). Finally, the *WireSizing*(s_i) procedure adjusts the width of wire connecting s_i to achieve zero skew (line 18).

Algorithm: ***PADJILA***
Input: *A given X-architecture zero-skew clock tree with a set of clock sinks S, layer configuration, and upper bound for antenna effect* L_{max}
Output: *An antenna-safe X-architecture zero skew clock tree with minimum jumper and via counts*

```
1  for each s_i in S
2  { if e(s_i) = L_top
3    { s_i is antenna-safe; }
4    else
5    { DP(s_i) = DischargePath(s_i); /* Obtain the total discharge path of s_i */
6      for each dp_i ∈ DP(s_i)
7      { e_total(s_i) = e_total(s_i) + dp_i – ComSeg(e_total(s_i), ∀e_i∈dp_i);
         /* Obtain the total segment of DP(s_i). */
8        if |e_total(s_i)| > L_max
9        { InsertJumper(s_i);
10         via_original = #via(s_i); /* Count #vias. */
11         Layer_can(s_i) = LayerAssignment(s_i); /* Get layer candidates. */
12         via_modified = #via(s_i); /* Assign Layer_can(s_i) to e(s_i) and count #vias. */
13         if via_modified < via_original
14         { Remove jumper and assign Layer_can(s_i); }
15       }
16     }
17   }
18   WireSizing(s_i);
19 }
```

Fig. 3. The proposed *PADJILA* algorithm.

A. Discharge-Path-Based Antenna Effect Detection – DischargePath(s_i)

Some notations used in *DischargePath*(s_i) are shown in Fig. 4 . In a given X-clock tree, s_i is one of clock sinks in S, and its paired sink is s_i's brother $B(s_i)$. The tapping point [17] of s_i and $B(s_i)$ is defined as their father $F(s_i)$. Segments connecting bending point and s_i, $B(s_i)$, and $F(s_i)$ are respectively denoted as $e(s_i)$, $e(B(s_i))$, and $e(F(s_i))$. The layer of $e(s_i)$ is denoted as $e(s_i)$.layer.

s_i	Clock sink ∈ S.
$B(s_i)$	s_i's brother due to it is paired with s_i.
$F(s_i)$	s_i's father due to it is the tapping point of s_i and $B(s_i)$.
$e(s_i)$	Segment connects s_i and bending point.
$e(B(s_i))$	Segment connects $B(s_i)$ and bending point.
$e(F(s_i))$	Segment connects $F(s_i)$ and bending point.
$e(s_i)$.layer	Layer of $e(s_i)$.

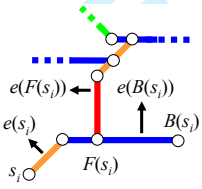


Fig. 4. Notations used in *DischargePath*(s_i).

Fig. 5 shows the discharge-path-based antenna effect detection procedure of *DischargePath*(s_i). For a given sink s_i, we first compare $e(s_i)$.layer and $e(B(s_i))$.layer to get the highest layer, denoted as $L_{high}(s_i)$, (line 1). Then, three cases of $e(s_i)$.layer are defined for obtaining the total discharge path of s_i, denoted as $DP(s_i)$.

Case 1) $e(s_i)$.layer > $e(B(s_i))$.layer (lines 2-7): If $e(F(s_i))$.layer is higher than $L_{high}(s_i)$ and $F(s_i)$ locates on $e(s_i)$, $e(s_i)$ will be moved to $dp_k \in DP(s_i)$ (lines 3-4). Otherwise, s_i is antenna-safe (lines 5-6) due to the charges accumulated on $e(B(s_i))$ are not enough to damage s_i.

Case 2) $e(s_i)$.layer = $e(B(s_i))$.layer (lines 8-16): If $e(F(s_i))$.layer is higher than $L_{high}(s_i)$, both $e(s_i)$ and $e(B(s_i))$ will be moved to $dp_k \in DP(s_i)$ (lines 9-10). On the other hand, if $e(F(s_i))$.layer is equal to $L_{high}(s_i)$, $e(s_i)$ and $e(B(s_i))$ will be moved to $dp_k \in DP(s_i)$. Then, *DischargePath*($F(s_i)$) is required (lines 11-13) because more charges are accumulated on $e(F(s_i))$.

Case 3) $e(s_i)$.layer < $e(B(s_i))$.layer (lines 17-29): If $e(F(s_i))$.layer is higher than $L_{high}(s_i)$, we will check $F(s_i)$ locates on $e(s_i)$ or not. If it does, $e(s_i)$ will be move to $dp_k \in DP(s_i)$ (lines 19-20). Otherwise, $e(s_i)$ and $e(B(s_i))$ are moved to $dp_k \in DP(s_i)$ (lines 21-22). On the other hand, if $e(F(s_i))$.layer satisfies the interval constraint, $e(s_i)$.layer ≤ $e(F(s_i))$.layer < $L_{high}(s_i)$, and $F(s_i)$ locates on $e(s_i)$, $e(s_i)$ will be moved to $dp_k \in DP(s_i)$. Then, *DischargePath*($F(s_i)$ is required (lines 24-26). Otherwise, only $e(s_i)$ is moved to $dp_k \in DP(s_i)$ (lines 27-28).

```
Procedure: DischargePath(s_i)
Input: A sink s_i
Output: Total discharge path of s_i
1  L_high(s_i) = Max( e(s_i).layer, e(B(s_i)).layer );
2  if e(s_i).layer > e(B(s_i)).layer  /* Case 1 */
3  {  if e(F(s_i)).layer > L_high(s_i) and F(s_i) locates on e(s_i)
4     {  Move e(s_i) to dp_k ∈ DP(s_i);  }
5     else
6     {  s_i is antenna-safe;  }
7  }
8  else if e(s_i).layer = e(B(s_i)).layer  /* Case 2 */
9  {  if e(F(s_i)).layer > L_high(s_i)
10    {  Move e(s_i) and e(B(s_i)) to dp_k ∈ DP(s_i);  }
11    else if e(F(s_i)).layer = L_high(s_i)
12    {  Move e(s_i) and e(B(s_i)) to dp_k ∈ DP(s_i);
13       DischargePath(F(s_i));                    }
14    else
15    {  s_i is antenna-safe;  }
16 }
17 else  /* Case 3, e(s_i).layer < e(B(s_i)).layer */
18 {  if e(F(s_i)).layer > L_high(s_i)
19    {  if( F(s_i) locates on e(s_i) )
20       {  Move e(s_i) to dp_k ∈ DP(s_i);  }
21       else
22       {  Move e(s_i) and e(B(s_i)) to dp_k ∈ DP(s_i);  }
23    }
24    else if e(s_i).layer ≤ e(F(s_i)).layer < L_high(s_i) and F(s_i) locates on e(s_i)
25    {  Move e(s_i) to dp_k ∈ DP(s_i);
26       DischargePath(F(s_i));        }
27    else
28    {  Move e(s_i) to dp_k ∈ DP(s_i);  }
29 }
```

Fig. 5. The *DischargePath*(s_i) procedure.

A portion of X-clock shown in Fig. 6(a) is taken as an example for Case 1. Notably, s_{13} is paired with s_{14}, and s_{23} is the tapping point of s_{13} and s_{14}, s_{13} and s_{23} are respectively denoted as $B(s_{14})$ and $F(s_{14})$. Because $e(s_{14})$.layer and $e(B(s_{14}))$.layer are metals 3 and 1, then $L_{high}(s_{14})$ is metal 3 (lines 1-2). Additionally, $e(F(s_{14}))$.layer is metal 2, and $F(s_{14})$ does not locates on $e(s_{14})$, so s_{14} is antenna-safe (line 6). In Fig. 6(b), only $dp_1 \in DP(s_{14})$ affects s_{14} and equals the sum of segments 1-3. Since segments 1-3 are too short to collect enough charges, s_{14} is antenna safe.

The other Case 3 is introduced with s_{13} shown in Fig. 6(a). Notably, s_{14} and s_{23} are respectively denoted as $B(s_{13})$ and $F(s_{13})$. $L_{high}(s_{13})$ is metal 3 due to $e(s_{13})$.layer and $e(B(s_{13}))$.layer are metals 1 and 3 (lines 1 and 17). Because $e(F(s_{13}))$.layer is metal 2, as well as, $F(s_{13})$ not only satisfies the interval constraint of [metal 1, metal 3) but also locates on $e(s_{13})$, $e(s_{13})$ is moved to $dp_1 \in DP(s_{13})$ (lines 24-25). In Fig. 6(b), $dp_1 \in DP(s_{13})$ is the sum of segments 5-7, and $dp_1 \in DP(s_{13})$ can be simplified as segment 6, i.e., $e(s_{13})$, since segments 5 and 7 are short enough to be neglected. Then, *DischargePath*($F(s_{13})$) is required (line 26), where $F(s_{13})$ is s_{23}. *DischargePath*(s_{23}) obtains that $e(s_{23})$.layer, $e(B(s_{23}))$.layer, and $e(F(s_{23}))$.layer are metals 2, 4, and 1, respectively.

DischargePath(s_{23}) moves $e(s_{23})$ to $dp_1 \in DP(s_{23})$ (lines 28-29). Due to $dp_1 \in DP(s_{23})$ is the sum of segments 8 and 10, and segment 10 is short enough to be neglected, $dp_1 \in DP(s_{23})$ is simplified as segment 8, i.e., $e(s_{23})$. Finally, we get that $DP(s_{13})$ is the sum of $e(s_{13})$ and $e(s_{23})$. Because $DP(s_{13})$ is longer than L_{max}, a jumper is inserted to fix s_{13} shown in Fig. 6(c), and $DP(s_{13})$ is reduced as the sum of segments 7-8 shown in Fig. 6(d).

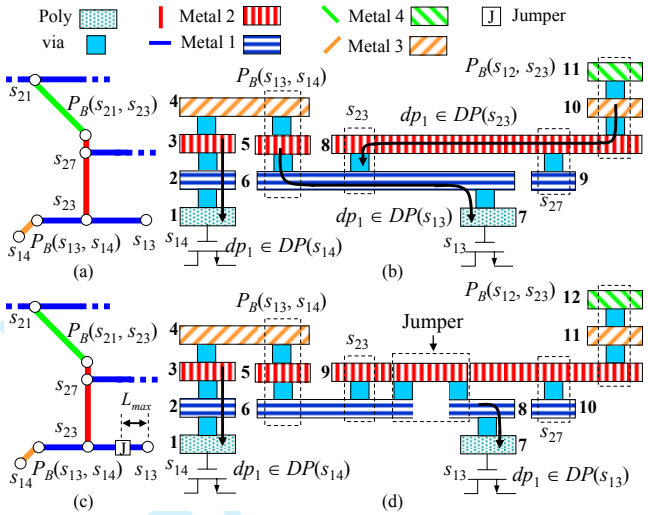


Fig. 6. (a) A portion of X-clock tree. (b) $DP(s_{13})$ and $DP(s_{23})$ damage s_{13}. (c) A jumper is inserted to fix s_{13}. (d) $DP(s_{13})$ is reduced.

B. *Layer Assignment – LayerAssignment*(s_i)

Fig. 7 shows the layer assignment procedure of *LayerAssignment*(s_i) to obtain layer candidates for an antenna-critical wire $e(s_i)$ and to reduce the jumper and via counts in advance. For a sink s_i, if $e(B(s_i))$.layer is equal to L_{top}, $e(B(s_i))$.layer will be returned (lines 1-2). Otherwise, we have to compare the layers of $e(B(s_i))$ and $e(F(s_i))$ (lines 3-14). If $e(B(s_i))$.layer is higher than $e(F(s_i))$.layer, the layer candidates will be $e(B(s_i))$.layer to L_{top} (lines 4-5). On the other hand, if $e(B(s_i))$.layer is equal to $e(F(s_i))$.layer, *LayerAssignement*(s_i) will return $e(B(s_i))$.layer+1 to L_{top} (lines 6-7). For other cases, we check $F(s_i)$ does locate on $e(s_i)$ or not. If it does, the layer candidates will be $e(F(s_i))$.layer to L_{top} (lines 9-10). Otherwise, we assign $e(B(s_i))$.layer+1 to L_{top} to $e(s_i)$ (lines 11-12).

```
Procedure: LayerAssignment(s_i)
Input: A sink s_i
Output: A set of layer candidates for e(s_i).layer
1  if e(B(s_i)).layer = L_top
2  { return e(B(s_i)).layer; }
3  else
4  { if e(B(s_i)).layer > e(F(s_i)).layer
5    { return e(B(s_i)).layer to L_top; }
6    else if e(B(s_i)).layer = e(F(s_i)).layer
7    { return e(B(s_i)).layer+1 to L_top; }
8    else
9    { if F(s_i) locates on e(s_i)
10     { return e(F(s_i)).layer to L_top; }
11     else
12     { return e(B(s_i)).layer+1 to L_top; }
13   }
14 }
```

Fig. 7. The *LayerAssignment*(s_i) procedure.

We take Figs. 8(a) and 8(b) as examples for explanation. The inserted jumper needs two vias to cut $e(s_6)$ by switching it to metal 3 for a short length (i.e., segment 4) and then switching it back to its original layer. Besides, s_6, $P_B(s_4, s_6)$, s_4, and s_{18} respectively need two, one, one, and three vias. Therefore, $via_{original}$ is nine. In *LayerAssignment*(s_6), s_4 and s_{18} are denoted as $B(s_6)$ and $F(s_6)$.

Since $e(B(s_6))$.layer is metal 3 and higher than $e(F(s_6))$.layer (i.e., metal 2), the procedure obtains that $Layer_{can}(s_6)$ are metals 3 and 4 (lines 4-5). We temporarily remove the inserted jumper and then assign $Layer_{can}(s_6)$ to $e(s_6)$. When assigning metal 3 to $e(s_6)$, $via_{modified}$ is seven because s_6, s_{18}, and s_4 need three, one, and three vias, respectively. In contrast, $via_{modified}$ is equal to $via_{original}$ when assigning metal 4 to $e(s_6)$. Finally, we remove the jumper and assign metal 3 to $e(s_6)$ due to one jumper and two vias are reduced.

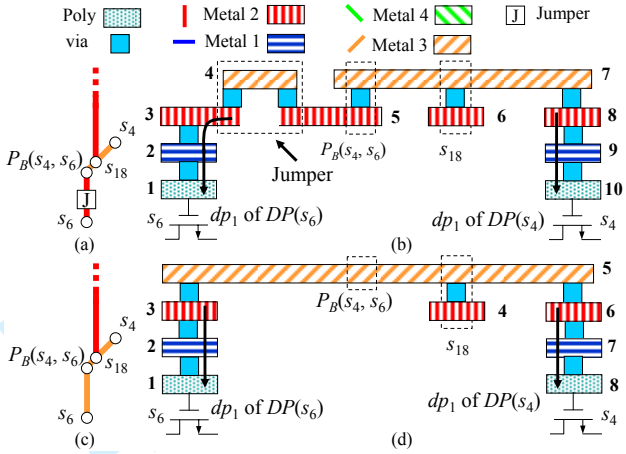


Fig. 8. (a) A jumper is inserted to fix s_6. (b) The jumper needs two vias. (c) Assign $e(s_6)$ with metal 3. (d) One jumper and two vias are reduced compared with (a).

C. *Zero Skew Compensation – WireSizing*(s_i)

After fixing antenna violations, the clock skew is not zero anymore due to the delay of inserted vias. We apply the wire sizing technique to achieve zero skew. The pair of sinks (s_{13}, s_{14}) shown in Fig. 6(c) is taken as an example to explain the technique. When inserting a jumper to fix s_{13}, the via count of s_{13}, denoted as $\#via_{13}$, is increased from one to three since the jumper needs two vias, as shown in Fig. 6(d). On the other hand, $\#via_{14}$ is five because s_{14} and $P_B(s_{13}, s_{14})$ respectively need three and two vias.

Fig. 9(a) shows the equivalent model of the pair of sinks (s_{13}, s_{14}) shown in Fig. 6(c), which includes the wires and the inserted vias. We use the fitted Elmore delay (FED) [18] model to calculate the clock delay and the delay of inserted vias is considered in delay calculation. Based on the model, Fig. 9(b) shows the equivalent circuit of a wire e_i with width w_i and length l_i. The sheet resistance, unit area capacitance, and fringing capacitance are denoted as r, c_a, and c_f, respectively. In Fig. 9(b), n-vias is modeled as a π-model circuit for via delay calculation, where n is via count. Both via resistance and capacitance are two-times of wire resistance and capacitance [19].

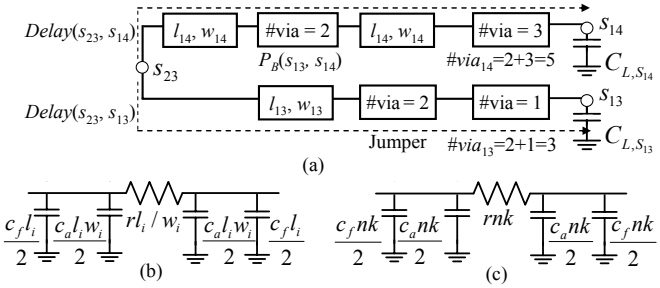


Fig. 9. (a) The equivalent model of the pair of sinks (s_{13}, s_{14}) shown in Fig. 6(c). The equivalent circuits of (b) e_i and (c) n-vias based on the FED model.

We take the equivalent model of the paired sinks (s_{13}, s_{14}) shown in Fig. 9(a) as an example to explain how to derive the width of $e(s_{13})$, denoted as w_{13}, for skew compensation. First, s_{14} is antenna-safe and does not require any jumper. Based on the FED model, $Delay(s_{23}, s_{14})$ with via delay consideration is formulated as follows.

$$Delay(s_{23}, s_{14}) = \sum_{i \in P(s_{14})} r(\frac{l_i}{w_i})\left[\frac{(Dc_a w_i + Ec_f)l_i}{2} + FC_{load,\,i}\right] = r(\frac{l_{14}}{w_{14}} + via_{14}k)\left[\frac{Dc_a(l_{14}w_{14} + via_{14}k) + Ec_f(l_{14} + via_{14}k)}{2} + FC_{L,S_{14}}\right], \quad (1)$$

where $P(s_{14})$ is the set of tree edges those are along the path from s_{23} to s_{14}. The coefficients D, E, and F are obtained by the curve fitting technique [18]. In (1), $C_{load,i}$ is the load capacitance and defined as follows.

$$C_{load,\,i} = \begin{cases} \sum_{j \in T(n_i)} \left[\frac{(Dc_a w_j + Ec_f)l_j}{F} + C_{load,\,j}\right] & \text{for node } n_i \\ C_{L,S_i} & \text{for sink } s_i, \end{cases} \quad (2)$$

where $T(n_i)$ is the set of tree edges at the downstream of node n_i.

Next, we formulate $Delay(s_{23}, s_{13})$ and let the two delays be equal to each other to derive w_{13} as follows.

$$\begin{aligned} &Delay(s_{23}, s_{13}) = Delay(s_{23}, s_{14}) \\ &r(\frac{l_{13}}{w_{13}} + via_{13}k)\left[\frac{Dc_a(l_{13}w_{13} + via_{13}k) + Ec_f(l_{13} + via_{13}k)}{2} + FC_{L,S_{13}}\right] = Delay(s_{23}, s_{14}) \\ &w_{13} = \left(-b \pm \sqrt{b^2 - 4ac}\right)/2a, \end{aligned} \quad (3)$$

where

$$\begin{aligned} a &= \frac{r via_{13} k Dc_a l_{13}}{2} \\ b &= r\left[\frac{Dc_a l_{13} + Ec_f via_{13}k}{2} l_{13} + via_{13}k(\frac{Dc_a + Ec_f}{2} via_{13}k + FC_{L,S_{13}})\right] - Delay(s_{23}, s_{14}) \\ c &= r l_{13}\left[\frac{Dc_a via_{13}k + EC_f(l_{13} + via_{13}k)}{2} + C_{L,S_{13}}\right]. \end{aligned}$$

D. *Time Complexity Analysis*

For a given X-clock tree with a set of n clock sinks, each clock sink is detected by the proposed PADJILA algorithm shown in Fig. 3, and the *for* loop runs in $O(n)$. In the *for* loop, the *DischargePath* procedure obtains the total discharge path for a sink in $O(k)$ due to a sink has at most k-discharge paths. The remaining procedures (i.e., *InsertJumper*, *LayerAssignment*, and *WireSizing*) respectively insert jumpers to fix antenna violations, obtain layer candidates for assignment, and adjust wire width to achieve zero skew in constant time. Finally, the time complexity of PADJILA is $O(n^2)$.

IV. Experimental Results

The proposed algorithm has been implemented in C++ and performed on a Windows machine with 1.7GHz Pentium-4 processor and 512MB memory. Table I lists the FED model with 130nm fabrication parameters [18] for delay and power calculation, and the upper bound for antenna effect L_{max} is measured by wirelength and set as 200μm [10].

TABLE I Technology Parameters

Tech. (nm)	#Layers	Delay Model	r (Ω/μm)	c_a (fF/μm)	c_f (fF/μm)	D	E	F	F_{clk} (Hz)	V_{dd} (v)	L_{max}(μm)
130	4	FED	0.623	0.00598	0.043	1.12673ln2	1.10463ln2	1.04836ln2	100M	1.2	200

Table II lists the results of jumper insertion. Notably, layer assignment technique is not applied here. Both JI [10] and the proposed PADJI algorithms first apply PMXF algorithm [9] to construct the initial X-clock trees of all the benchmarks [20]. Then, they separately detect antenna effects and insert jumpers to fix antenna violations. The percentage ratio is defined as JI/PMXF or PADJI/PMXF. As listed in Table II, PADJI averagely inserts 46.12% less jumpers than JI and respectively has better performance

of 0.09%, 0.10%, and 46.19% in terms of delay, power, and via count. Moreover, the proposed wire sizing technique can maintain the zero skew property after fixing antenna violations. Comparing with PMXF, PADJI achieves antenna-safe X-clock trees and slightly increases 0.07% in delay, 0.07% in power, and 17.21% in via count.

TABLE II COMPARISON OF PMXF [9], JI [10], AND THE PROPOSED PADJI ALGORITHMS BASED ON L_{MAX} = 200μM WITH 130NM FED MODEL

Bench marks	#Sinks	#Inserted Jumpers		Delay (ns)			Skew (ns)			Power (mW)			#Vias		
		JI	PADJI	PMXF	JI	PADJI	PMXF	JI	PADJI	PMXF	JI	PADJI	PMXF	JI	PADJI
Primary1	269	211	79	59.456	59.495	59.483	0.806	0.816	0	174.272	174.341	174.322	1194	2014	1352
Primary2	603	353	305	254.020	254.135	254.113	0.688	0.694	0	412.771	412.895	412.874	2350	3720	2960
r1	267	207	115	310.696	311.018	310.928	0.360	0.389	0	63.340	63.405	63.359	1220	2022	1450
r2	598	439	256	1125.454	1126.724	1125.910	0.859	0.975	0	156.019	156.188	156.067	2846	4646	3358
r3	862	642	378	1803.820	1805.865	1804.441	1.217	1.301	0	210.124	210.368	210.197	4020	6562	4776
r4	1903	1421	815	4804.431	4810.863	4806.244	2.762	3.736	0	487.032	487.646	487.208	9158	14866	10788
r5	3101	2283	1292	8585.707	8597.276	8588.974	3.049	4.162	0	809.903	810.941	810.201	14585	23555	17169
s1423	74	54	20	7.489	7.509	7.492	0.038	0.041	0	6.009	6.039	6.028	351	559	391
s5378	179	137	70	17.915	17.965	17.930	0.033	0.027	0	15.470	15.508	15.490	772	1308	912
s15850	597	414	166	49.893	50.067	50.013	0.124	0.159	0	58.674	58.830	58.722	2711	4399	3043
Average Ratio (%)		-	53.88	-	100.16	100.07	-	-	-	-	100.17	100.07	-	163.40	117.21

Table III lists the results associated with layer assignment technique for reducing jumper and via counts in advance. Comparing with JI and PADJI, the number of inserted jumpers required by JILA [10] and the proposed PADJILA can be effectively reduced. The percentage ratio is defined as JILA/PMXF or PADJILA/PMXF. As listed in Table III, PADJILA averagely inserts 48.21% less jumpers than JILA and respectively achieves reductions of 0.02%, 0.02%, and 20.35%, in delay, power, and via count. Comparing with PMXF, PADJILA slightly increases 0.03% in delay, 0.05% in power, and 0.88% in via count. Fig. 10 shows the full chip and local views of benchmark *r*4 fixed by using the proposed PADJILA algorithm.

TABLE III COMPARISON OF PMXF [9], JILA [10], AND THE PROPOSED PADJILA ALGORITHMS BASED ON L_{MAX} = 200μM WITH 130NM FED MODEL

Bench marks	#Sinks	#Inserted Jumpers		Delay (ns)			Skew (ns)			Power (mW)			#Vias		
		JILA	PADJILA	PMXF	JILA	PADJILA	PMXF	JILA	PADJILA	PMXF	JILA	PADJILA	PMXF	JILA	PADJILA
Primary1	269	12	3	59.456	59.472	59.461	0.806	0.813	0	174.272	174.299	174.281	1194	1520	1200
Primary2	603	8	7	254.020	254.089	254.059	0.688	0.700	0	412.771	412.839	412.813	2350	3107	2364
r1	267	13	7	310.696	310.805	310.784	0.360	0.399	0	63.340	63.360	63.355	1220	1470	1234
r2	598	22	12	1125.454	1125.812	1125.730	0.859	0.909	0	156.019	156.061	156.049	2846	3299	2870
r3	862	37	20	1803.820	1804.302	1804.236	1.217	1.165	0	210.124	210.189	210.175	4020	4702	4060
r4	1903	80	32	4804.431	4806.045	4805.609	2.762	2.551	0	487.032	487.185	487.146	9158	10597	9222
r5	3101	145	71	8585.707	8588.937	8588.136	3.049	3.488	0	809.903	810.178	810.109	14585	17000	14727
s1423	74	0	0	7.489	7.494	7.491	0.038	0.041	0	6.009	6.029	6.027	351	399	351
s5378	179	13	8	17.915	17.937	17.926	0.033	0.030	0	15.470	15.486	15.480	772	1003	788
s15850	597	32	13	49.893	49.958	49.921	0.124	0.143	0	58.674	58.732	58.698	2711	3350	2737
Average Ratio (%)		-	51.79	-	100.05	100.03	-	-	-	-	100.07	100.05	-	121.23	100.88

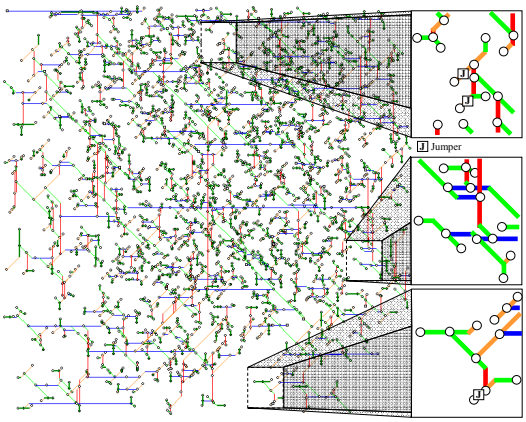


Fig. 10. Full chip and local views of benchmark *r*4 after fixing antenna violations by using PADJILA.

Table IV lists the results of changing the upper bound for antenna effect L_{max} from 200μm to 100μm based on the proposed PADJILA algorithm. The percentage ratio is defined as PADJILA(100μm)/PADJILA(200μm). When L_{max} shrinks, the number of detected antenna violations is increased by 16.55%. In addition, PADJILA on L_{max} = 100μm averagely inserts 12.73% more jumpers than PADJILA on L_{max} = 200μm and slightly increases 0.07% in delay, 0.08% in power, and 10.36% in via count, respectively.

TABLE IV COMPARISON OF THE RESULTS BASED ON L_{MAX} = 200μM AND L_{MAX} = 100μM WITH 130NM FED MODEL

Bench marks	#Sinks	#Antenna Violations		#Inserted Jumpers		Delay (ns)		Power (mW)		#Vias	
		PADJILA (200μm)	PADJILA (100μm)	PADJILA (200μm)	PADJILA (100μm)	PADJILA (200μm)	PADJILA (100μm)	PADJILA (200μm)	PADJILA (100μm)	PADJILA (200μm)	PADJILA (100μm)
Primary1	269	79	101	3	5	59.461	59.482	174.281	174.394	1200	1330
Primary2	603	305	335	7	7	254.059	254.171	412.813	412.959	2364	2689
*r*1	267	115	119	7	7	310.784	310.926	63.355	63.404	1234	1371
*r*2	598	256	267	12	12	1125.730	1126.046	156.049	156.269	2870	3076
*r*3	862	378	387	20	21	1804.236	1804.978	210.175	210.337	4060	4425
*r*4	1903	815	856	32	33	4805.609	4808.613	487.146	487.409	9222	9962
*r*5	3101	1292	1393	71	74	8588.136	8595.251	810.109	811.318	14727	16464
*s*1423	74	20	27	0	0	7.491	7.503	6.027	6.030	351	387
*s*5378	179	70	86	8	9	17.926	17.933	15.480	15.491	788	865
*s*15850	597	166	244	13	16	49.921	50.013	58.698	58.721	2737	3062
Average Ratio (%)		-	116.55	-	112.73	-	100.07	-	100.08	-	110.36

V. CONCLUSION

Antenna effect is one of the DFM issues in nanometer process. For a given X-clock tree, we present a discharge-path-based antenna effect detection method and fix antenna violations with the integration of jumper insertion and layer assignment techniques. The proposed PADJILA algorithm outperforms the comparative work within one second for each benchmark. Experimentally, shrinking the upper bound for antenna effect in advanced process would cause more inserted jumpers for antenna avoidance. Our extended work is to combine other DFM issues and crosstalk reduction for X-clock trees.

REFERENCES

[1] T. Y. Ho, Y. W. Chang, and S. J. Chen, "Multilevel routing with jumper insertion for antenna avoidance," *Integration, the VLSI Journal*, vol. 29, no. 4, pp. 420-432, Jul. 2006.

[2] H. C. Shin and C. Hu, "Thin gate oxide damage due to plasma processing," *Semiconductor Science and Technology*, vol. 11, no. 4, Apr. 1996, pp. 463-473.

[3] G. S. Hwang and K.P. Giapis, "On the dependence of plasma-induced charging damage on antenna area," in *Proc. Int. Symp. Plasma-Induced Damage*, May 1999, pp. 21-23.

[4] *TSMC 0.18μm Design Manual*, Document number TA-10A5-4001, pp. 67-68.

[5] B. Y. Su and Y. W. Chang, "An optimal jumper-insertion algorithm for antenna avoidance/fixing," *IEEE Trans. on CAD*, vol. 26, no. 10, pp. 1818-1829, Oct. 2007.

[6] Z. W. Jiang and Y. W. Chang, "An optimal network-flow-based simultaneous diode and jumper insertion algorithm for antenna fixing," *IEEE Trans. on CAD*, vol. 27, no. 6, pp. 1055-1065, June 2008.

[7] W. Shen, Y. Cai, J. Hu, X. Hong, and B. Lu, "High performance clock routing in X-architecture," in *Proc. IEEE Int. Symp. Circuits and Systems*, 2006, pp. 2081-2084.

[8] C. H. Wang and W. K. Mak, "λ-geometry clock tree construction with wire length and via minimization," in *Proc. IEEE Int. Symp. VLSI-DAT*, Apr. 2007, pp. 124-127.

[9] C. C. Tsai, C. C. Kuo, J. O. Wu, T. Y. Lee, and R. S. Hsiao, "X-clock routing based on pattern matching," in *Proc. IEEE Int. SOC Conf.*, Sept. 2008, pp. 357-360.

[10] C. C. Tsai, F. T. Hsu, C. C. Kuo, J. O. Wu, and T. Y. Lee, "X-clock tree construction for antenna avoidance," in *Proc. IEEE Int. Conf. Solid-State and Integr.-Circuit Tech.*, Oct. 2008, pp. 2248-2251.

[11] H. Shirota, T. Sadakane, M. Terai, and K. Okazaki, "A new router for reducing antenna effect in ASIC design," in *Proc. IEEE Custom Integrated Circuits Conf.*, May 1998, pp. 601-604.

[12] Peter H. Chen, "Beat the competition - a knowledge-base design process addressing the antenna effect and cell placement," in *IEEE Circuits and Device Magazine*, May/June 2004, pp. 18-27.

[13] D. Wu, J. Hu, and R. Mahapatra, "Antenna avoidance in layer assignment," *IEEE Trans. on CAD*, vol. 25, no. 4, pp. 734-738, Apr. 2006.

[14] A. T. Krishnan, S. Krishnan, and P. Nicollian, "Impact of gate area on plasma charging damage: the "reverse" antenna effect," in *Proc. Int. Electron Devices Meeting*, Dec. 2002, pp. 20.6.1-20.6.4.

[15] P. Simon, J-M. Luchies, W. Maly, "Antenna ratio definition for VLSI circuits," in *Proc. Int. Symp. Plasma-Induced Damage*, May 1999, pp. 16-20.

[16] D. P. Verret, A. Krishnan, and S. Krishnan, "A new look at the antenna effect," *IEEE Trans. on Electron Devices*, vol. 49, no. 7, pp. 1274-1282, July 2002.

[17] R. S. Tsay, "An exact zero-skew clock routing algorithm," *IEEE Trans. on CAD*, vol. 12, no. 2, pp. 242-249, Feb. 1993.

[18] A. I. Abou-Seido, B. Nowak, and C. Chu, "Fitted Elmore Delay: a simple and accurate interconnect delay model," *IEEE Trans. on VLSI*, vol. 12, no. 7, pp. 691-696, 2004.

[19] T. Y. Ho, Y. W. Chang, S. J. Chen, and D. T. Lee, "Crosstalk- and performance-driven multilevel full-chip routing," *IEEE Trans. on CAD*, vol. 24, no. 6, pp. 869-878, June 2005.

[20] VLSI CAD Laboratory, University of California, San Diego, "Bounded-skew clock tree routing version 1.0," May 2000, http://vlsicad.ucsd.edu/GSRC/bookshelf/Slots/BST/.

Dear Prof. Niraj Jha,

Editor-in-Chief, IEEE Transactions on VLSI Systems

We resubmit the major revision of the manuscript TVLSI-00341-2009 titled "Discharge-Path-Based Antenna Effect Detection and Fixing for X-Architecture Clock Tree." as a brief manuscript for your consideration published in the IEEE Transactions on VLSI Systems. We appreciate all the reviewers' valuable comments on this paper. Their remarks are very helpful to improve our work.

We have incorporated all the reviewers' comments into the revised manuscript as possible. The revised manuscript has been reduced to 11 pages and whose corrections are explained as follows.

- All the formulas, figures, and tables using Elmore delay model are removed due to the model may overestimate wire delay.
- All the sentences are carefully checked and corrected to make the manuscript concise.
- The references [1, 2, 3, 16, 17, 22, 29, and 31] in original manuscript are removed to make the manuscript concise, and the references [5, 7, 20, 21, 25, 26, 27, are 28] are changed to [4, 12, 10, 9, 18, 19, 8, and 20] in the revised manuscript, respectively. The references [23 and 30] discuss the same topic and are written by same author, so we remove [23] and change [30] to [17].
- To discuss the diode insertion technique, we quote the latest work [19] and change it to [6], as well as, remove the references [16-18] written by the same group of researchers.
- The reference [8] is removed because it is the preliminary version of [9], and the reference [9] is changed to [1]. Similarly, the references [10, 11, 12] are removed, and the reference [13] is changed to [5].
- The reference [14] is removed, and the reference [15] is changed to [13] for consistency.

The form for response to reviewers is attached next six pages. We hope this manuscript can meet yours and reviewers' standard. For any question, please contact me via e-mail. Thank you for handling this paper. We are looking forward to hear from you soon.

Sincerely yours,

Chung-Chieh Kuo
Graduate Institute of Computer and Communication
National Taipei University of Technology
E-mail: s4419014@ntut.edu.tw

Response to Reviewer's Comments

For Reviewer 1

General remarks

1. English is very bad. The paper contains numerous awkward sentences and grammatical errors – it is impossible to list them all.

– **All possible grammatical and writing style errors in English in the revised manuscript have been corrected and tried our best.**

2. The paper organization is poor. It is hard to extract the relevant information.

– **We have reorganized the revised manuscript. Section I, Introduction, includes the definition of antenna effect and three general strategies in current literatures, and then gives the motivation for X-clock tree with antenna effect consideration and our contribution. Section II, Problem Formulation, presents the latest solutions for X-clock tree with antenna avoidance and their weaknesses, and then formulates the problem. Section III, Delay model, in original manuscript is removed, especially for all the formulas, tables, and figures using Elmore delay model due to the model may overestimate wire delay. Section IV, Experimental Results, shows the comparison of the existing works and our approach. Section V, Conclusion, states our contributions and future work.**

3. The authors should explain the differences between this submission and the 2 prior papers they have published on the same topic [20][21].

– **The references [20, 21] in the original manuscript have changed to [10, 9] in the revised manuscript, respectively. In the fifth paragraph in Section I on page 2, we have given the introduction, i.e., "X-architecture clock trees have recently been developed [7-9] that perform better in delay, cost, and power consumption compared with general Manhattan architecture clock trees. Unfortunately, the works [7-9] ignored the antenna effect which is one of DFM issues." to point out the result and shortcoming of [9].**

– **In the first paragraph in Section II on page 2, we have stated the contribution of [10], i.e., "To address the antenna effect of a clock tree, Tsai *et al.* [10] first defined the antenna avoidance problem for X-clock trees. If a metal wire is longer than L_{max} and not routed on the top layer, the jumper insertion (JI) technique will be applied to fix the antenna violation. A jumper needs vias to ..." We take a portion of X-clock tree and its corresponding layout shown in Fig. 2 (on page 3) to discuss the difference between [10] and our work in the second paragraph in Section II on pages 2-3. Additionally, we compare [10] and our work with ten benchmark circuits reported in Tables II and III (on page 9). Experimental results show that our work performs better than [10] in terms of inserted jumpers, delay, skew, power, and via count.**

4. Some essential references are missing, for example:

[a] H. C. Shin and C. Hu, "Thin gate oxide damage due to plasma processing", Semicond. Sci. Technol. 11 (1996) 463–473.

[b] A.T. Krishnan, S. Krishnan, and P. Nicollian, "Impact of Gate Area on Plasma Charging Damage: The "Reverse" Antenna Effect," International Electron Devices Meeting, pp. 20.6.1-20.6.4, December 2002.

[c] G.S. Hwang and K.P. Giapis, "On the Dependence of Plasma-Induced Charging Damage on Antenna Area," Proceedings of the International Symposium on Plasma-Induced Damage, pp. 21-23, May 1999.

[d] P. Simon, J-M. Luchies, W. Maly, "Antenna ratio definition for VLSI circuits", 1999 4th International Symposium on Plasma Process-Induced Damage, 1999, pp. 16-20.

[e] D.P. Verret, A. Krishnan, and S. Krishnan, "A New Look at the Antenna Effect," IEEE Transactions on Electron Devices, Vol. 49, No. 7, pp. 1274-1282, July 2002.

4. The authors should provide a more meaningful discussion and a better explanation of the layout factors that contribute to antenna effects. For example, such information can be found in [c][d][e]. Other relevant publications exist. The area ratio used in this paper may not be a proper metric for controlling antennas [d][e].

– **We have added the above references, which are respectively numbered as [2, 14, 3, 15, 16], into our reference list on page 11 in the revised manuscript. In the first and second paragraphs in Section I on page 1, we introduce the antenna effect with a simple layout shown in Fig. 1 and discuss the definition of antenna ratio. The summary of [a]-[e] is stated as "The antenna ratio (*AR*) is defined as the ratio of the exposed antenna area to the gate oxide area [2-3], and it should…" in the beginning of the second paragraph in Section I on page 1, and "Krishnan *et al.* [14] presented a consequence of competition…" in the third paragraph in Section I on pages 1-2.**

– **According to the TSMC 0.18μm Design Manual [4], it defines and reports antenna effect as the area ratio or antenna ratio. The works [1, 5, 6, 10] applied the definition to detect antenna violations, and we also employ the area ratio for antenna effect detection. Hence, the metric should be practical and proper for controlling antenna avoidance.**

5. It is not clear what makes the antenna avoidance problem for a clock routed in X-geometry different from that routed in Manhattan geometry.

– **The difference between X-geometry and Manhattan geometry is that X-geometry can route metal wires in diagonal, horizontal, and vertical directions to perform better than Manhattan geometry in delay, cost, and power consumption. Antenna effect is tightly related to the conductor length, but not to the routing structure geometry. Because X-geometry clock tree construction is a new trend, we address antenna avoidance problem for an X-clock tree.**

6. It appears that the authors assume the same model for antenna violation for clock and signal nets. If so, it is not clear how the jumper insertion for a clock differs from that for a signal net. It appears that in the case of a clock net, after jumper insertion, a standard process of skew tuning will follow. The jumper insertion strategy does not consider this, so the procedures for clock and signal nets appear to be the same. This point should be clearly explained.

– **In a VLSI system, a clock tree connects all the clock sinks for the system synchronization with minimum clock delay and zero skew. When inserting jumpers for a clock tree, extra vias are required for connecting the adjacent layers. After that, the antenna-safe clock tree consumes more vias than the given clock tree. Via is modeled as a π-model circuit for via delay calculation, as shown in Fig. 9 on page 7. Therefore, the clock delay is increased, and the clock skew is not zero anymore due to the delay of inserted vias is considered in delay calculation. To prevent fault functions induced by different clock times, we apply a wire sizing technique to achieve zero skew (i.e, skew tuning) after inserting jumpers, as discussed in Section III C on page 7.**

7. The paper would be more readable if the authors first explained the procedures in high-level terms and then provided more details.

– **We have reorganized the proposed algorithm and given the overview associated with line numbers in detail in the beginning of Section III on pages 3-4. Then, the detail of each procedure is stated in the Section III on pages 4-8.**

8. Section III on delay models is confusing. It is unclear what is the purpose of bringing up the delay modeling problem before explaining the jumper insertion. The authors talk about modeling the delay of ei, but the expressions are given as delay(i). This is confusing. The expressions for Elmore delay and fitted Elmore delay are given. It is unclear what the purpose of stating both expressions is.

– **Because one of other reviewers also suggested us to remove the expression of Elmore delay to make the manuscript concise, we have removed all the formulas, tables, figures, and experimental results based on Elmore delay model in the revised manuscript. In our work, all the results are only based on fitted Elmore delay (FED) model introduced in Section III C on page 7.**

9. Section IV A is very confusing. Many details are given without proper explanation/motivation. The pseudo code is hard to follow.

– **Section IV A in the original manuscript has been arranged to Section III A in the revised manuscript. The comparative study and motivation of this work are stated in Section II on page 2. Moreover, we modify the pseudo codes shown in Fig. 3 on page 4 for easy reading and introduce the used notations with a simple portion of X-clock tree shown in Fig. 4 on page 5. Then, we state the three cases of our antenna detection method shown in Fig. 5 with explanations associated with line numbers in the second paragraph in Section III A on pages 4-5. Finally, we discuss the usage of the detection method with an example shown in Fig. 6 on page 6.**

10. It is unclear what are the contributions of this paper.

– **In this work, we propose a discharge-path-based antenna effect detection method and insert jumpers to fix the antenna violations (in Section III A on pages 4-6). Moreover, we present a layer assignment technique that provides layer candidates to antenna-critical wires and modifies their layer for jumper and via counts reduction (in Section III B on pages 6-7). Different from the existing works, we consider the delay of inserted vias in clock delay calculation and apply a wire sizing technique to achieve zero skew for an antenna-safe X-clock tree (in Section III C on pages 7-8). Comparing with the work [10] under ten benchmark circuits, the experimental results show that our approach achieves significant reductions of 48.21%, 0.02%, 0.02%, and 20.35% in terms of inserted jumpers, delay, power consumption, and via count, respectively (in Tables II-III on page 9). Additionally, we change the upper bound for antenna effect L_{max} from 200μm to 100μm to demonstrate that the number of antenna violations is increased when L_{max} shrinks (in Table IV on page 10).**

11. Table I is difficult to understand. Why would a reader care to know the coordinates of the clock sink positions?

– **We have removed this table in the revised manuscript. (The original idea of the table is to provide the coordinate of each clock sink and let the interested readers can follow our proposed detection method to calculate the total discharge path for each clock sink. In addition, they can clearly see the difference between our approach and other existing works.)**

12. It is unclear what the purpose of the experiments is and what they demonstrate. Self-comparisons to other tools written by the same group of researchers are not very convincing. Results presented in terms of 6-digit numbers are difficult to comprehend. Perhaps scaling would help.

– **We propose a new antenna effect detection method, as well as, reduce jumper and via counts with a layer assignment technique that provides layer candidates to antenna-critical wires. To evaluate our approach, the study [10], which is the first work addressing the antenna avoidance problem for X-clock trees, should be taken for comparison. We also compare our approach with [9], which constructs an X-clock tree without considering any DFM issue, to show the slight increasing resource utilization for achieving an antenna-safe X-clock tree. Additionally, we have scaled our experimental results listed in Table II-IV on pages 9-10 in the revised manuscript for easy comprehension.**

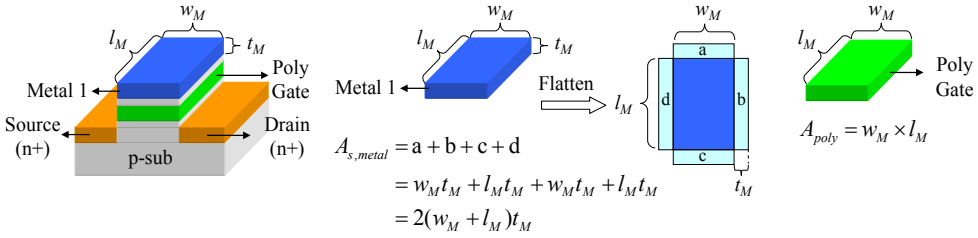
Some detailed remarks

1. The authors say on page 1 that "Chen and Koren [4] proved that the amount of such charging is proportional to the plasma-exposed area." [4] is a paper on channel routing and no proof that the amount of charging is proportional to the plasma-exposed area can be found in this paper. In addition, no such concept as "antenna ratio" can be found in that paper.

– **We have corrected it as "The amount of such charging is proportional to the plasma-exposed area [1]" in the revised manuscript. Please check the statement in Section I on page 1.**

2. If As,metal is the plasma-exposed area, and Apoly is the gate oxide area, I do not understand why As,metal and Apoly are computed as 2(wM+lM)tM and wMlM where w, l and t correspond to width, length and height of a wire. Again, the authors quote [4], but no such discussion/concepts can be found in [4].

– **The antenna ratio is defined as the ratio of the exposed antenna area to the transistor gate oxide area. In the TSMC 0.18μm Design Manual [5], the exposed antenna area and gate oxide area are defined as side-wall area $A_{s,metal}$ and polygon area A_{poly}, respectively. For area calculation, $A_{s,metal}$ and A_{poly} are respectively formulated as $2(w_M+l_M)t_M$ and $w_M l_M$, where w_M, l_M, and t_M are the width, length, and thickness of a conductor. We take a simple case shown as follows for explanation in detail.**



3. What is the "model of antenna strength caused by conductors"? The authors refer to it on page 2.

– **We have removed the statement in the revised manuscript and given the clear definition of antenna effect as the ratio of the exposed antenna area to the gate oxide area.**

4. On page 2, the authors say: "As shown in Fig. 1(b), the manufacturing process supports four metal layers and all the interconnects are manufactured in the order of poly, metal 1, metal 2, metal 3, and metal 4. Obviously, metal 3 is the topmost layer of this structure." Isn't metal 4 the topmost layer? I am confused.

– **Fig. 1(b) in the original manuscript is modified as Fig. 1(a) in the revised manuscript. In the figure, because the gate is not connected to metal 4, the highest layer for the gate is metal 3 not metal 4. Notably, metal 4 is the top layer of layer configuration.**

5. Page 2 – you use the word "ration" instead of "ratio".

– **We have corrected the typo on page 2 in the revised manuscript.**

6. Page 3: "However, the approach detects all the antenna violations with the topmost layer of layer configuration instead of the discharge paths those connect gates." I cannot parse this sentence.

– **We have corrected the sentence, i.e., "To address the antenna effect of a clock tree, Tsai *et al.* [10] first defined the antenna avoidance problem for X-clock trees. If a metal wire is longer than L_{max} and not routed on the top layer, the jumper insertion (JI) technique will be applied to fix the antenna violation." in Section II on page 2 in the revised manuscript.**

7. Page 4: "Figure 3(b) is the cross-section view of Fig. 3(a)." Fig. 3(a) illustrates a symbolic representation of a portion of a clock tree. You cannot have a cross-section view of an abstract graph.

– **We have corrected them in the revised manuscript, and Fig. 2 (i.e., Fig. 6 in the original manuscript) is employed for explanation and comparative study on page 3.**

For Reviewer 2

Replace Reference [6] P. H. Chen with his latest/better publication,

[6] Peter H. Chen, "Beat the Competition - A knowledge-Base Design Process Addressing the Antenna Effect and Cell Placement," IEEE Circuits and Device Magazine, May/June 2004, pp. 18-27.

This is the same author and similar paper but with complete antenna solution.

– **We have replaced the reference [6] in the original manuscript and changed it to [11] on page 11 in the revised manuscript.**

For Reviewer 3

This paper presents a new scheme to detect and fix antenna violation for X-clock trees. The proposed method is sound and effective. I recommend the authors to address the following issues:

1. Why do you select X-Architecture clock trees? Is there a fundamental reason that prevents you from extending your approach to more generic clock trees? Please comment on that.

– **Clock trees are generally routed on Manhattan architecture, which allows wires be routed in vertical and horizontal directions. Recently, X-architecture routing structure has received much attention from both industry and academia because it can route wires in diagonal, vertical, and horizontal directions to contribute more improvements on delay, cost, and power consumption compared with Manhattan architecture. In the revised manuscript, we add the references [7-8] those address X-architecture zero-skew clock tree construction. Antenna effect is tightly related the conductor length, but not for the routing geometry. Since X-architecture routing structure for a clock routing is a**

new trend, so we address antenna avoidance problem for an X-clock tree. Of course, the proposed approach can handle the other generic clock trees.

2. The organization of the paper can be improved. I recommend you to add a "background" section to discuss manufacture-induced antenna effects. Your paper currently has two parts, i.e., page 2 and page 4, to discuss such a topic. You should combine them. Also please use a separate section to discuss related work, i.e., schemes that detect and fix antenna violations.

– **We have reorganized the original manuscript and stated the background of antenna effect in the first and second paragraphs in Section I on page 1 in the revised manuscript. Moreover, we discuss the related works in Section II on pages 2-3 and take Fig. 2 (i.e., Fig. 6 in the original manuscript) as an example to explain how to detect and fix antenna violations with the existing work and our approach, respectively.**

3. Why do you use two timing models? I recommend you to use FED only since it is more accurate. You can remove the ED part to make the paper concise.

– **Since FED model is more accurate than ED model and the comparative work [10] uses FED model to calculate clock delay, we have removed all the formulas, tables, figures, and results based on the ED model in the revised manuscript to make the paper concise. The equivalent model/circuit and formulas of FED model are presented in Section III on pages 7-8. Additionally, the parameter and experimental results of the FED model are reported in Table I-IV on pages 8-10.**