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Fixing Antenna Problem by Synopsys SLE

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- Introduction
  - Antenna explanations
  - Antenna ratio definitions
  - Antenna check out violation by verification tools
  - Comparison of diode dropping and jumper insertion methods
  - Diode characterizations and structures
  - Diode dropping, jumper insertion, and diode dropping with extension wire
  - Chip-level protection diode dropping for blocks
  - Diode timing delay checking by RC extraction and SPICE Simulation
  - Diode structure verification by slicing

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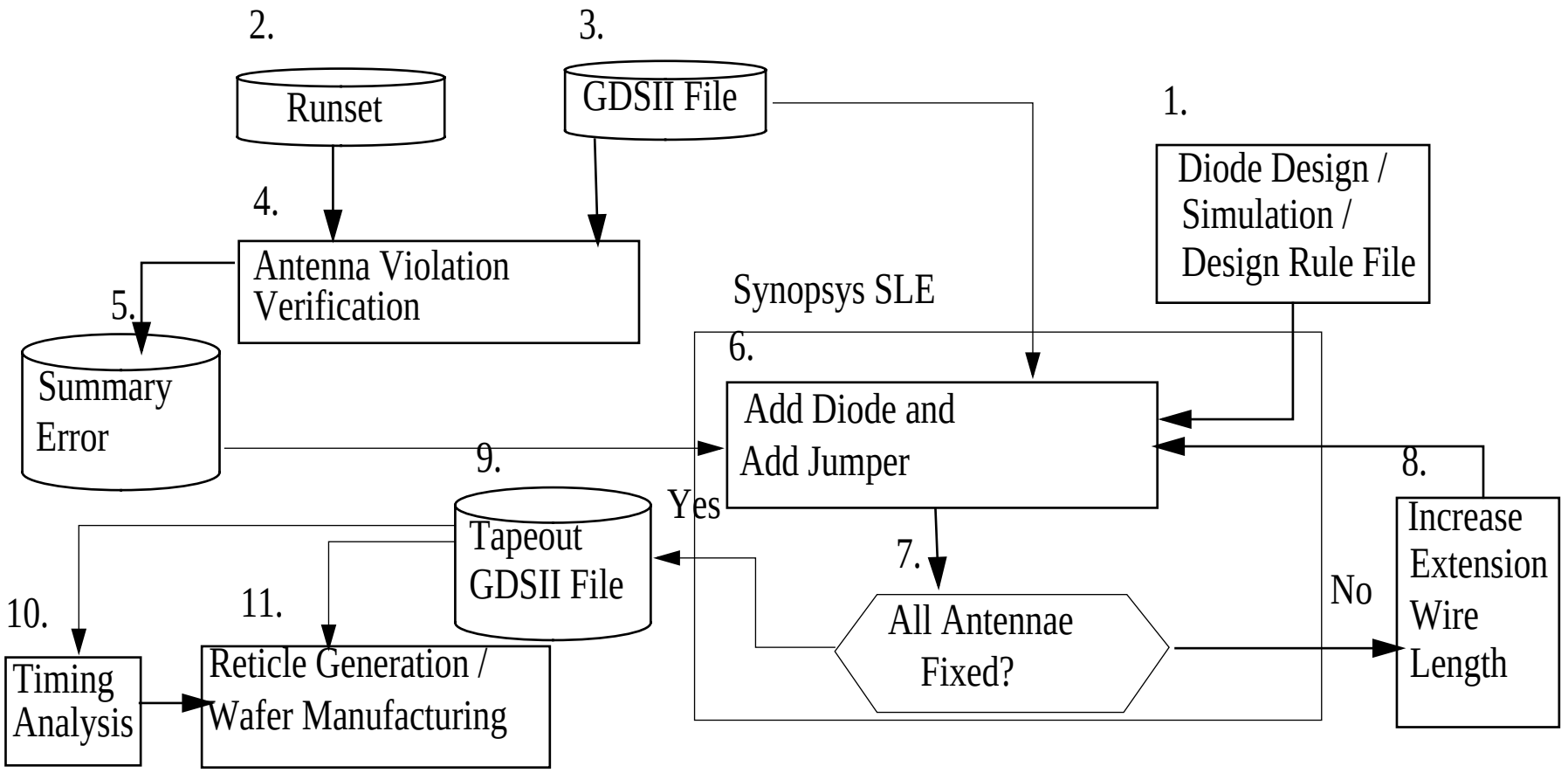
- Flow Chart for Fixing the Antenna Problem



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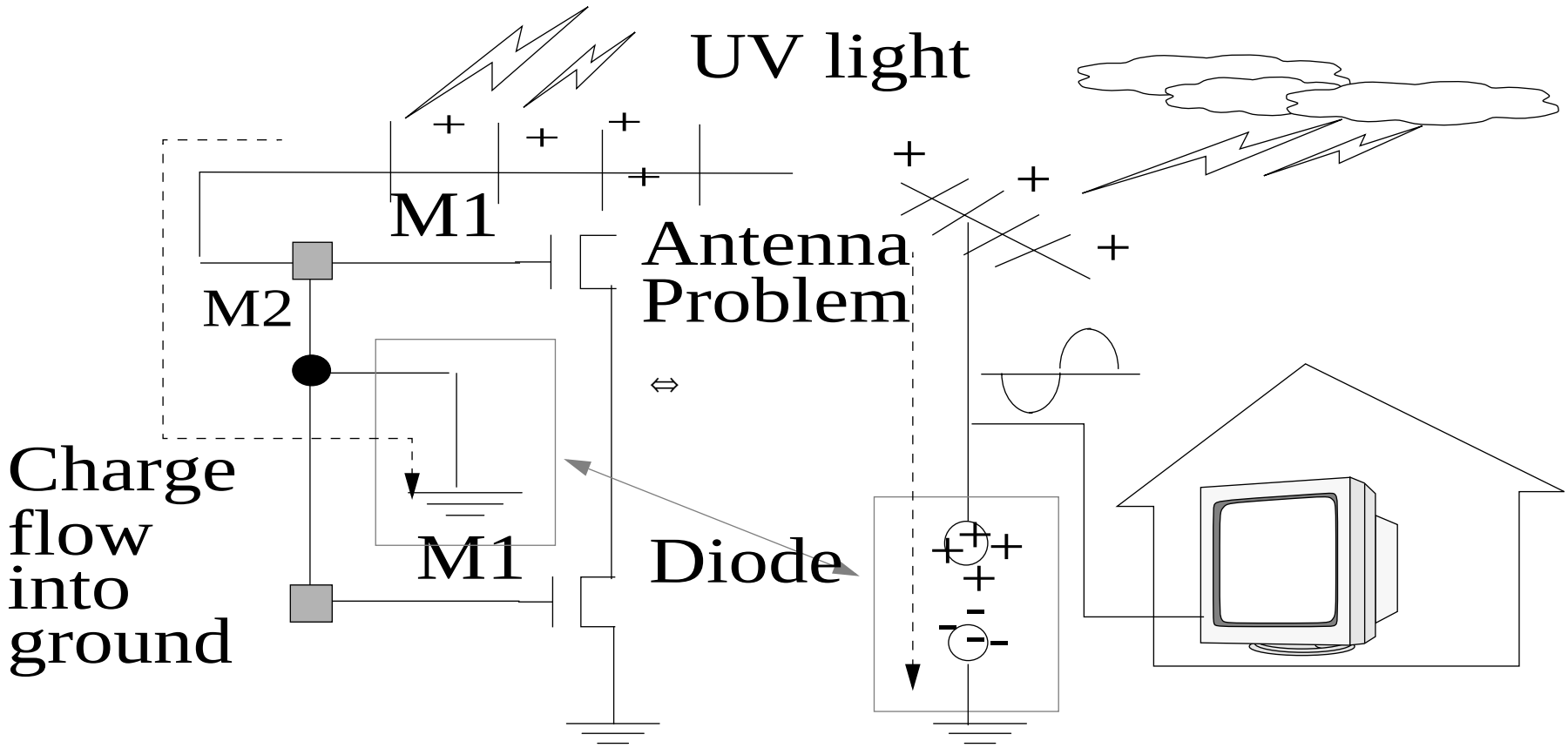
- Antenna During Manufacturing



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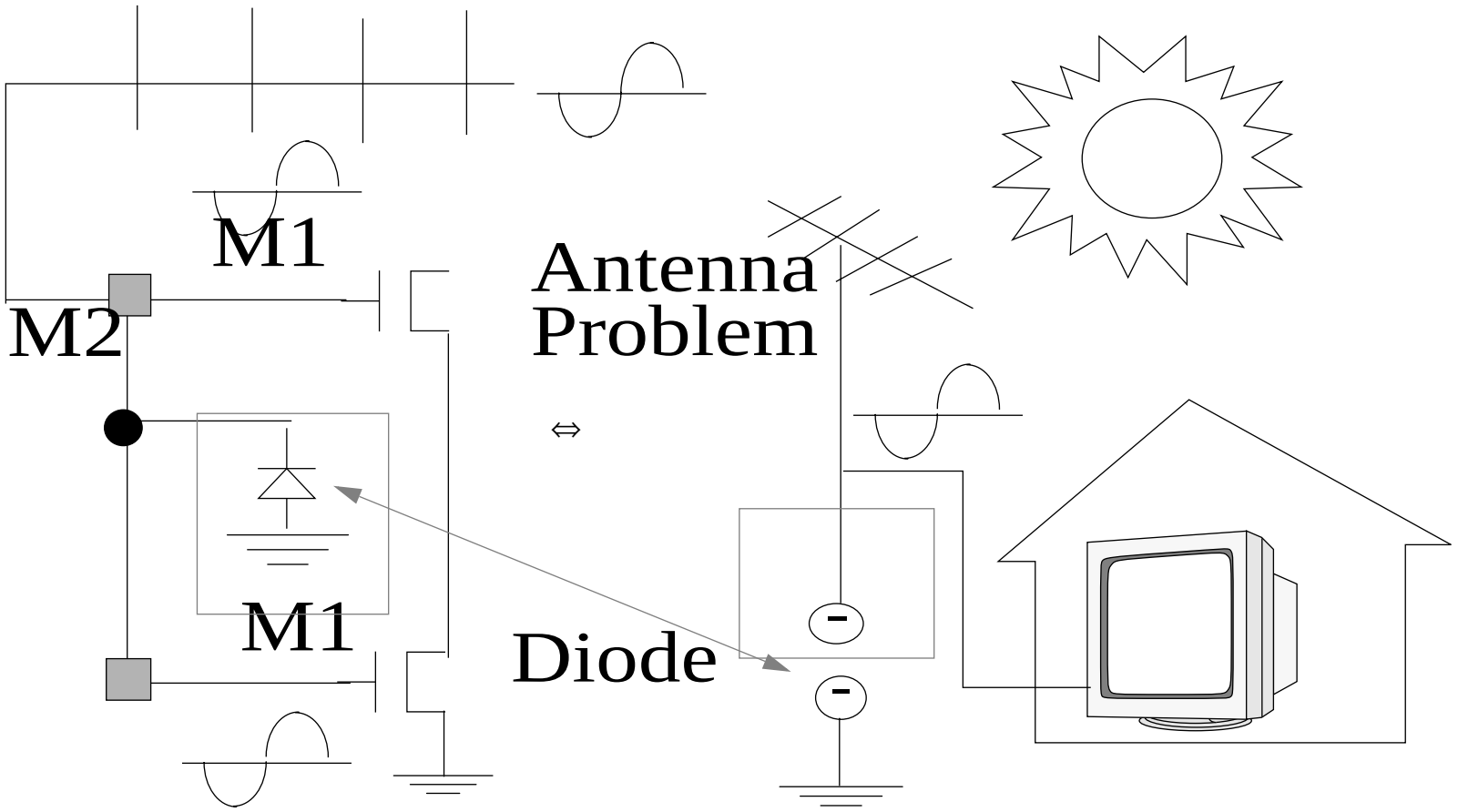
- Antenna During Normal Operation



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- Antenna Ratio Definition

The antenna ratio of a particular net is defined as:

$$\text{Antenna Ratio} = \frac{\text{Total Wire Area}}{\text{Total Input Port Area}}$$

Note that the antenna rule violation definition is foundry and process specific. For example, TSMC design rules (0.18 μm) uses total perimeter area of metal wire vs. gate area.

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- Antenna Rule Checking
  - The violated position of the wire: The (x, y) position of which the antenna ratio of the wire exceeds the specified antenna ratio, e.g, 400.
  - Error flattened: Since the wire is connected to every module, it should not be hierarchical. Therefore, the errors should be flattened. Set the error flattened option if the tool is a hierarchical verification tool. If the verification tool is not hierarchical, you do not need to set this option.
  - Chip level: At the chip level, since each block's antenna problem is fixed, we only need to consider the interconnection among the blocks. Since the whole chip may be very large (e.g., 1 million gates), to check the whole chip antenna violation might take a long time (several days on a SUN® Ultra-SPARC workstation). If the chip is too big, chip-level antenna violations can be avoided by putting a protection diode on every input pin.

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- Three Solutions for Antenna Problem
  - Router options: Break signal wires and routes to upper levels.
  - Embedded protection diode: Add protection diodes on every input port for every standard cell.
  - Dynamic dropping diode after placement and route: Fixing only the wire with the antenna violation which will not waste routing resources. reverse diodes.

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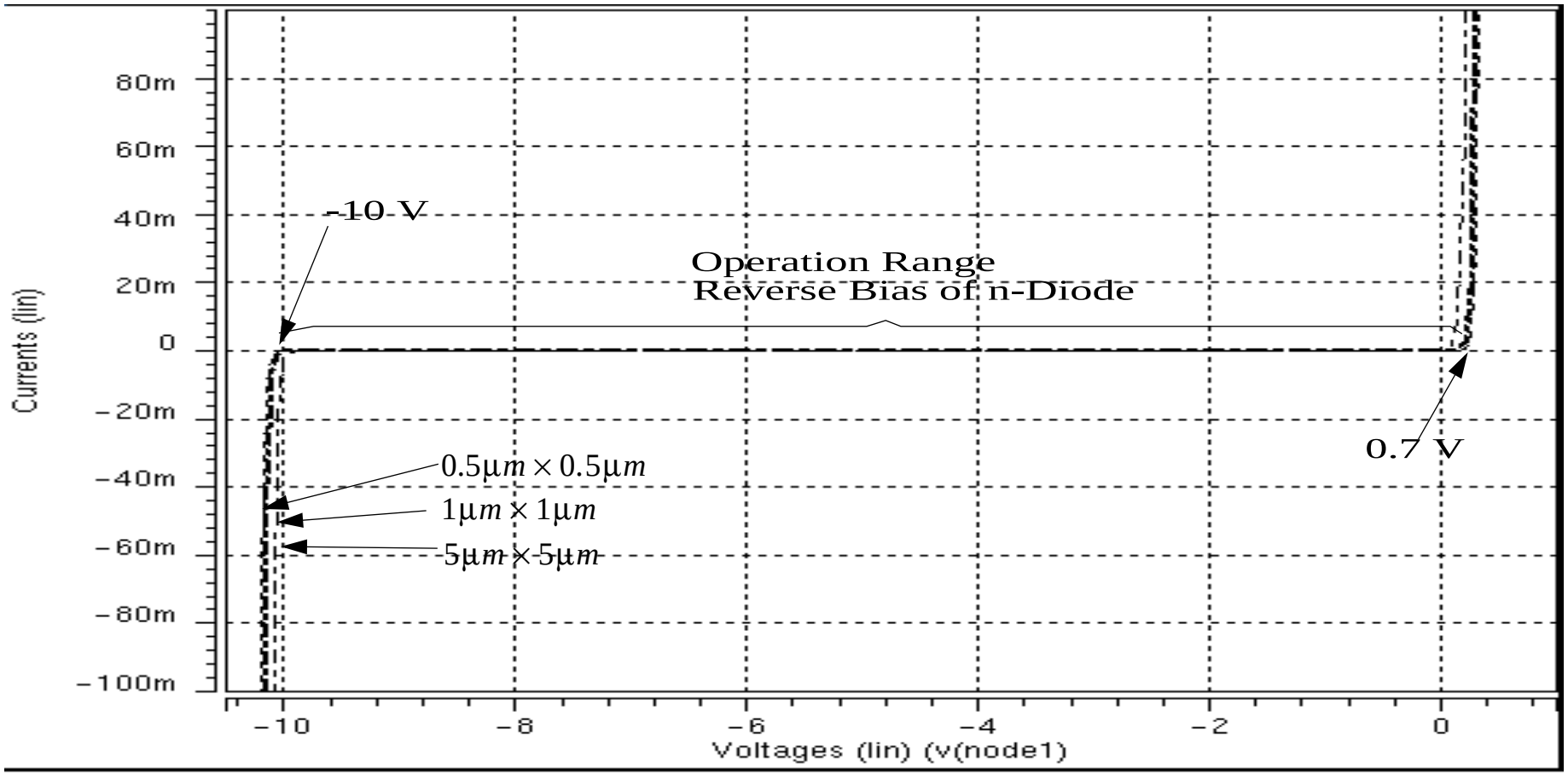
- The Leakage Current vs. Different Diode Area



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- Different Approaches Comparison

Table 1: Comparison of three approaches

Impact	Jumper	Embedded Diode	Dynamic Dropping Diode
Cell Area	No	Yes	No
Routability/Chip Size	Yes	Yes	No
Completeness	No	No	Yes
Timing	Most	More	Least

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- Jumper Insertion Timing Impact: Each jumper needs at least two vias. In the 0.35 μm technology, via resistance is around 10 Ω. In 0.25 μm technology or above, via resistance is around 100 Ω or more.

$$R' = R_{\square} \times \frac{L}{W} \cong 60\text{m}\Omega \times \frac{L}{W} \cong 3 - 10\Omega$$

Where:

$R_{\square}$ **: The sheet resistance of metal.**

R'**: The resistance of metal with length** L**.**

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- Diode Insertion Timing Impact:

  Diode Capacitance

$$C' \cong C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{34.5\mu F/cm}{0.4 \times 10^{-5} cm} = 0.86 fF/\mu m^2$$

  Where:

  C' and C_{ox}: **Capacitance of the diode**

  ε_{ox}: **Permittivity of diode and** t_{ox}: **Thickness of the diode**

  Time Constant:

$$\tau = (R + R') \times (C + C') = R \times C \times \left(1 + \frac{R'}{R}\right) \times \left(1 + \frac{C'}{C}\right)$$

  Where: τ: **Time delay of metal with diode/via.**

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- Timing Impact

  For 0.35 μm design with 350 μm wire, the formula is as follows:

$$\frac{R'}{R} = \frac{5}{60} \gg \frac{C'}{C} = \frac{1fF}{10pF}$$

  Where:

  τ: Time delay of metal with diode/via.

  For 0.35 μm design with 350 μm wire, the formula is as follows:

$$\frac{R'}{R} = \frac{5}{60} \gg \frac{C'}{C} = \frac{1fF}{10pF}$$

  From the Time Constant formula, we know the timing delay is negligible.

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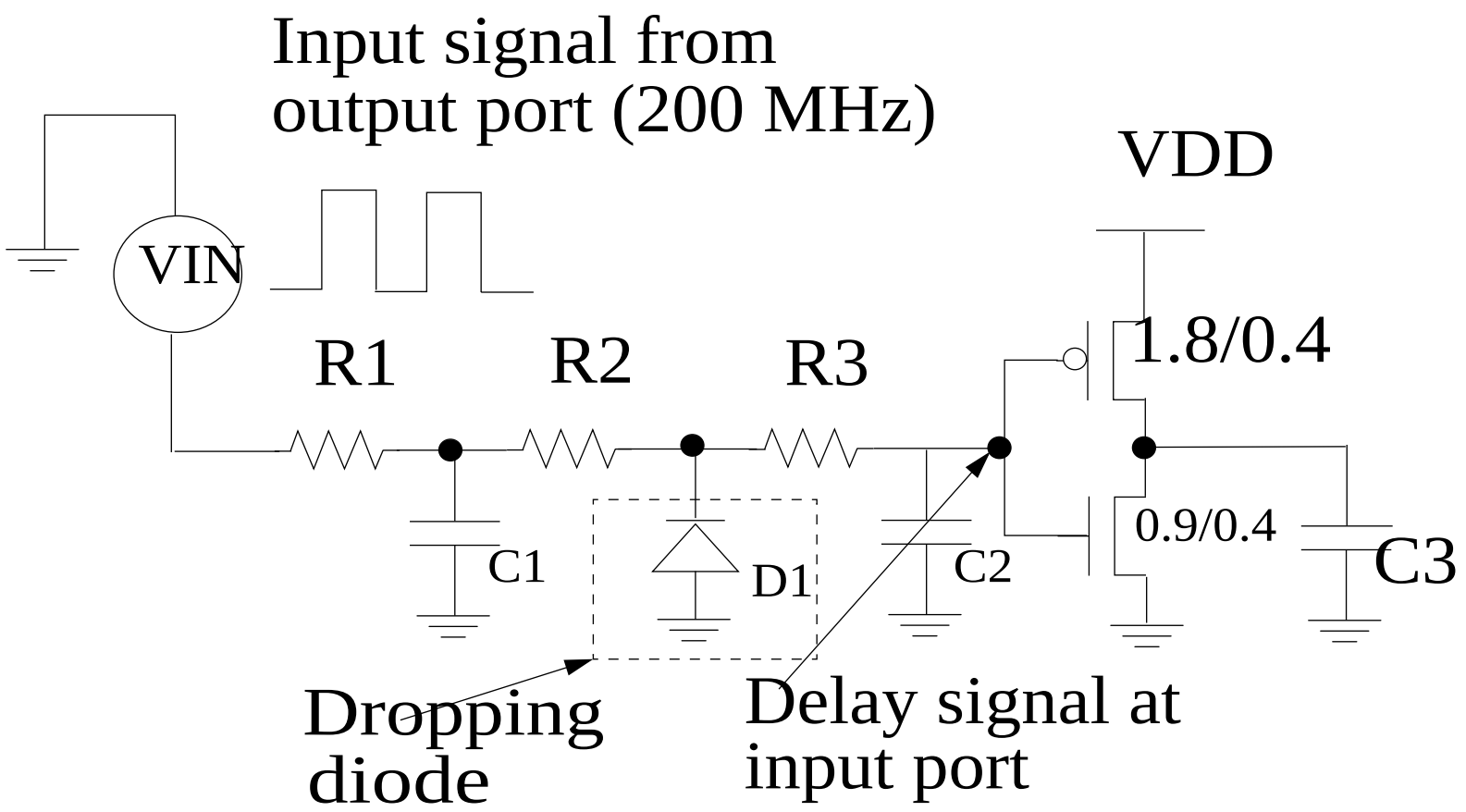
- SPICE Simulation for Diode Insertion



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- Advantages of The Dynamic Diode Dropping Approach

  - The designers may insert diodes within a given physical design tool flow. SLE's approach is post P&R. Its main advantage, flow-wise, are:
  - works with users' existing physical design flow
  - the only way to solve antenna violations for mixed-signal / analog designs. Since analog circuit design can not routed with P&R tool.
  - Least timing degradation (better than embedded)
  - Least waste of chip area during manufacturing
  - Least impact on routability. The jumper only approach is unusable on very dense chips.

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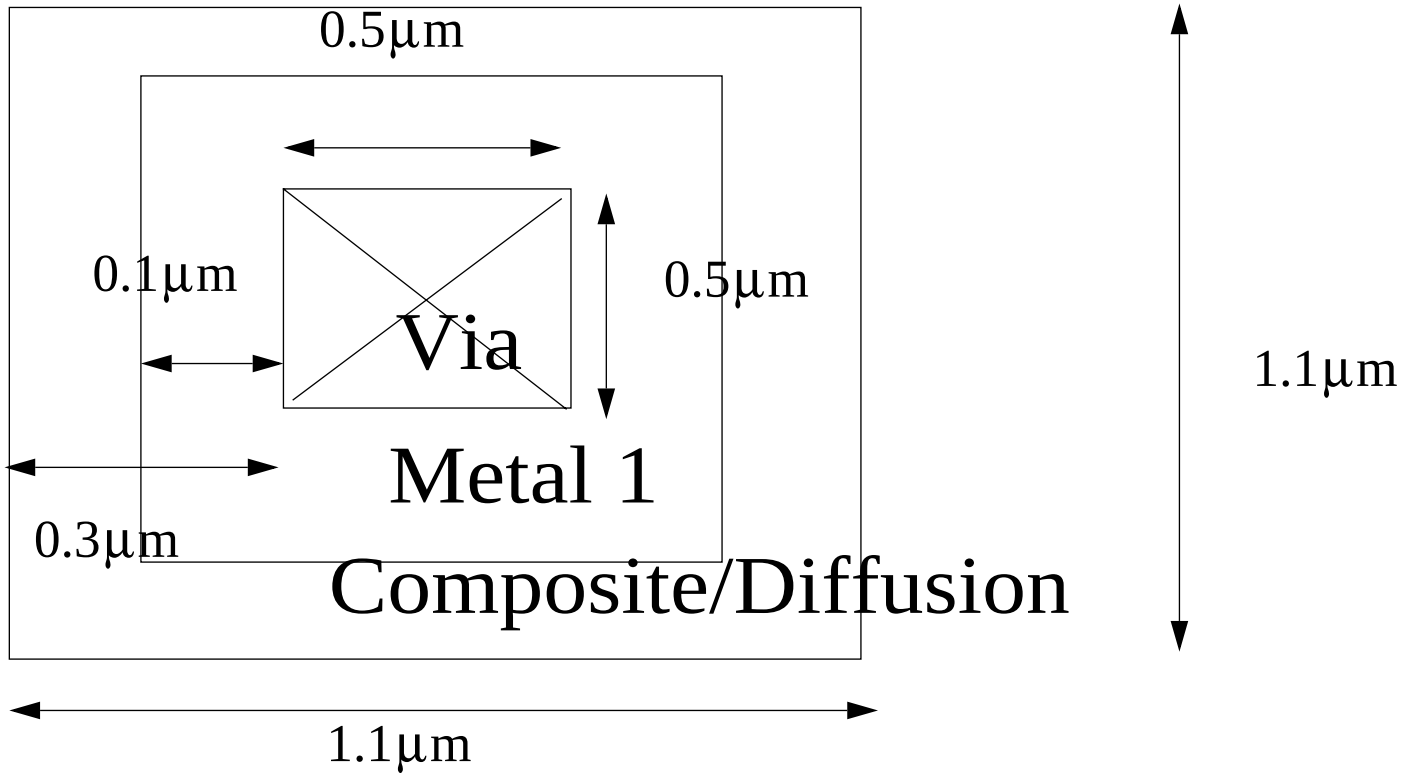
- Diode Structure



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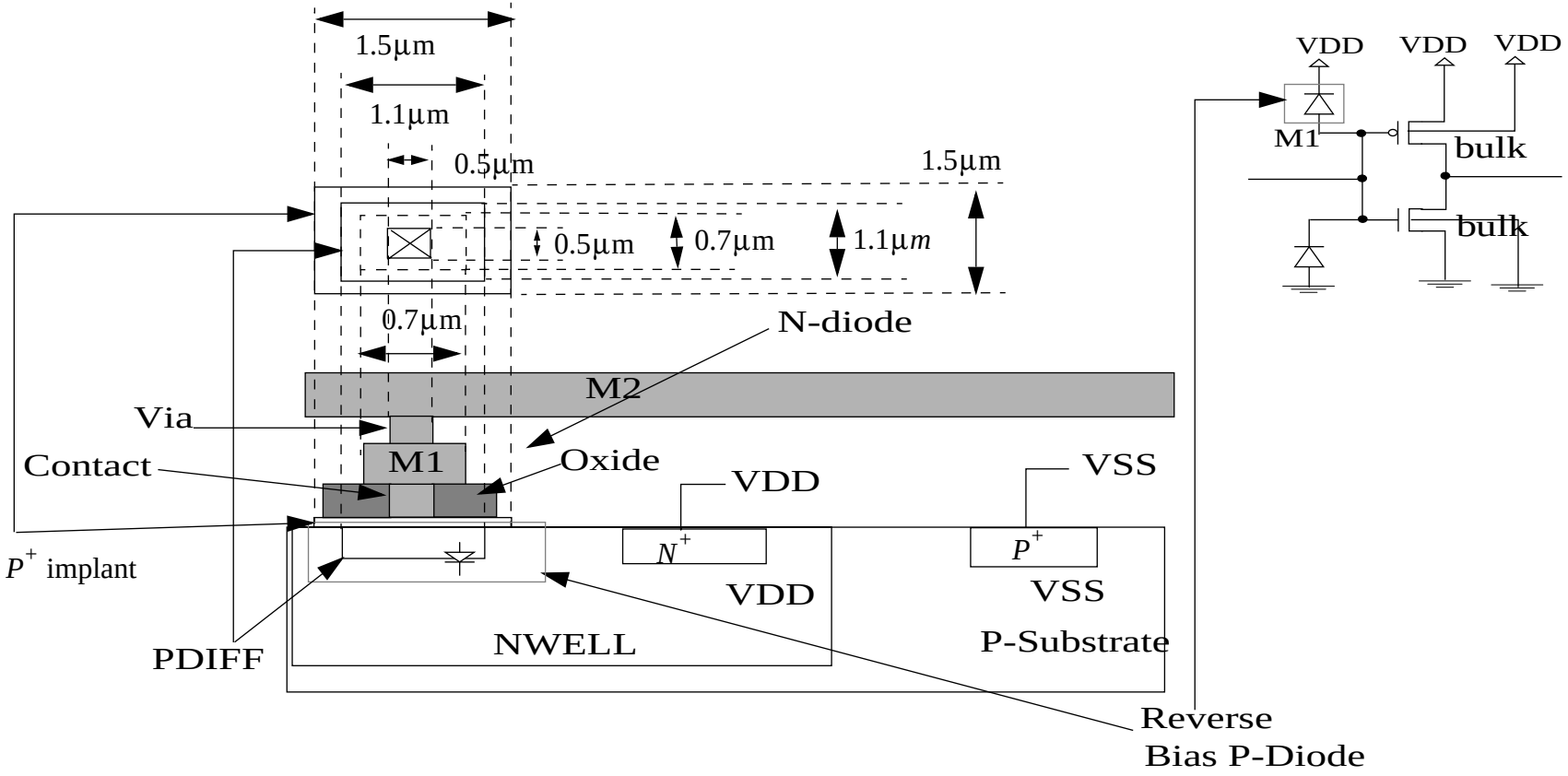
- P-Diode with P-IMP (P^+ implant)



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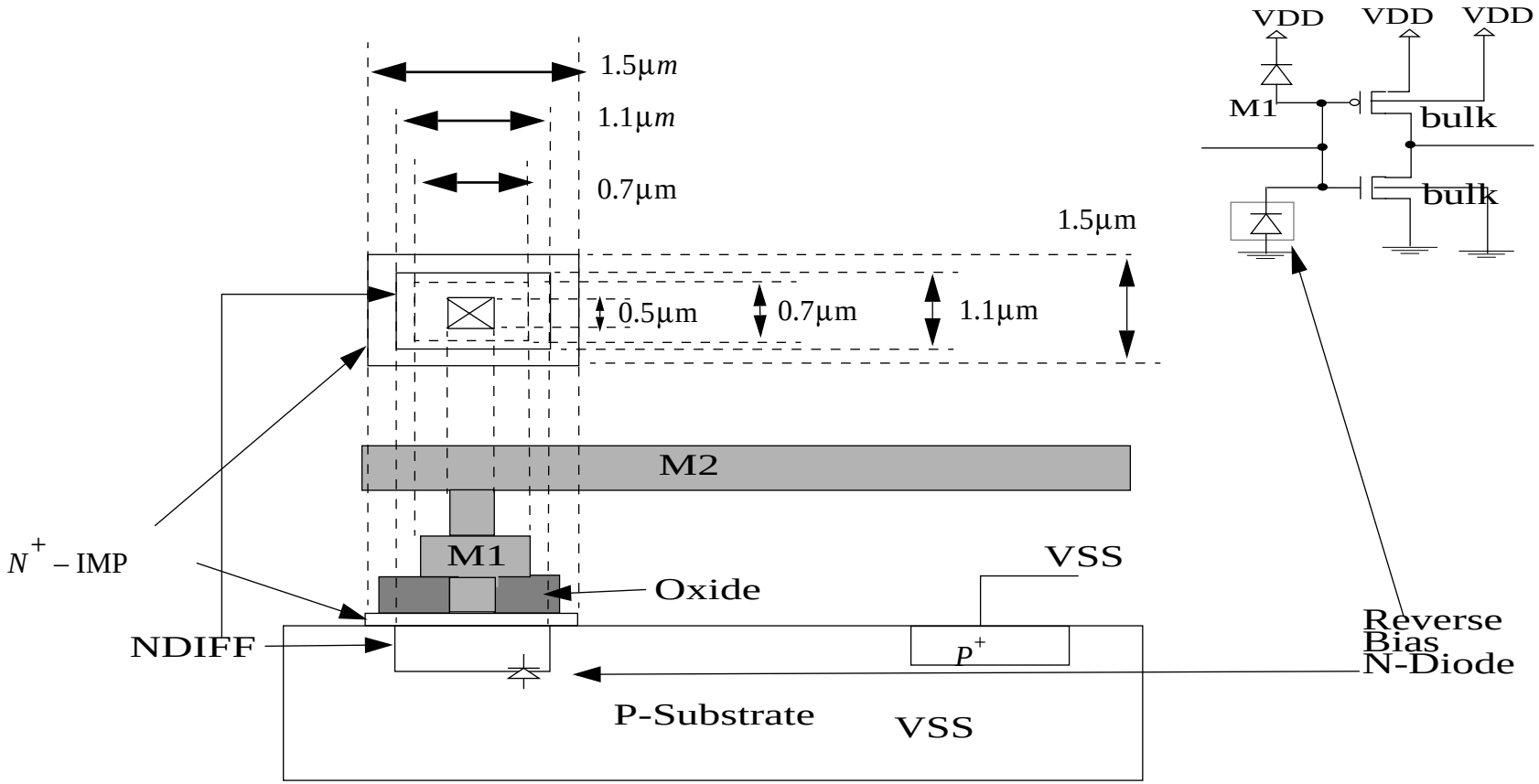
- N-Diode with N-IMP (N^+ implant)



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- Procedures for Fixing Antenna Violations

1. Make the rule file specifications.
2. Bring up the tool for antenna fixing.
3. Create the new library and stream in GDSII file.
4. Import the P-Diode and the N-Diode and open the top level cell.
5. Drop diodes w/o extension wires per Step 1.
6. Insert the jumper for the rest of the violation
7. Increase the extension wire to accommodate a bigger area.
8. (Repeat previous step until all the violations are cleaned.)
9. Save the design in a GDSII format.
10. Visually check the diode insertion.

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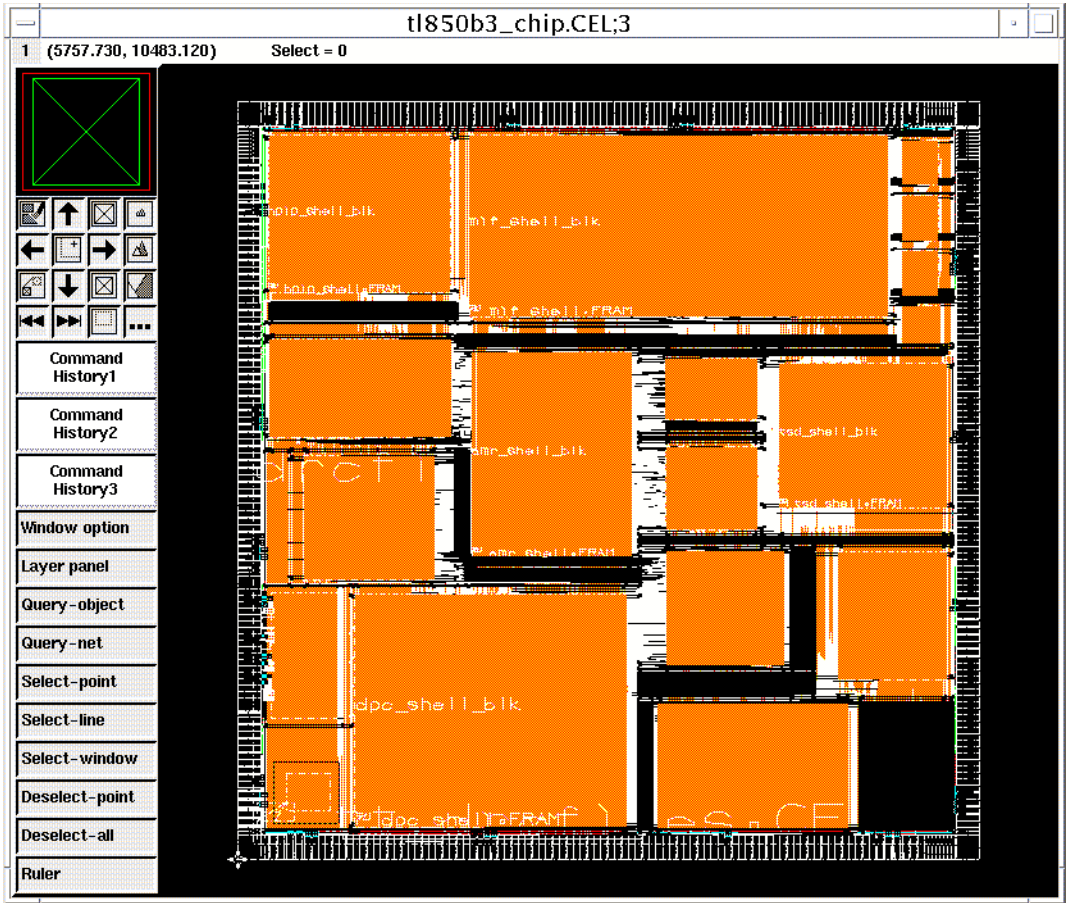
- Tapeout Chip Example



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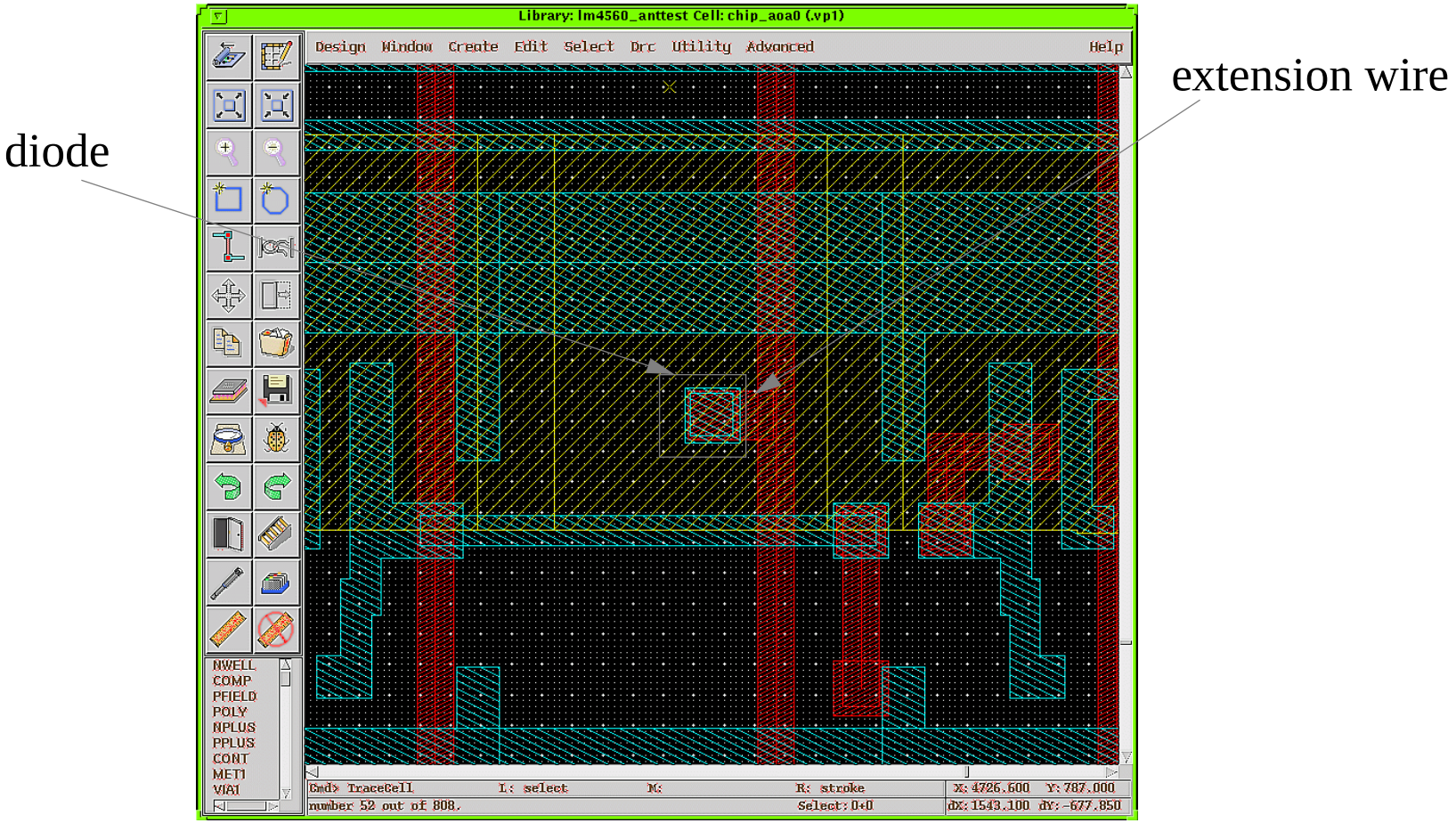
- Extension Wire Example



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- Antenna Fixing Results

Table 2: Dynamic diode and jumper insertion

Design names	Violation	Diode insertion without extension wires	Add jumper	Diode insertion with 20 μm extension wires
Design 1: dense design	M4: 0 M3: 154 M2: 23 M1: 0	M4: 0 M3: 21 M2: 0 M1: 0	M4: 0 M3: 3 M2: 0 M1:0	M4: 0 M3: 0 M2: 0 M1: 0
Design 2: sparse design	M4: 0 M3: 788 M2: 521 M1: 0	M4: 0 M3: 1 M2: 0 M1: 0	M4: 0 M3: 0 M2: 0 M1: 0	N/A

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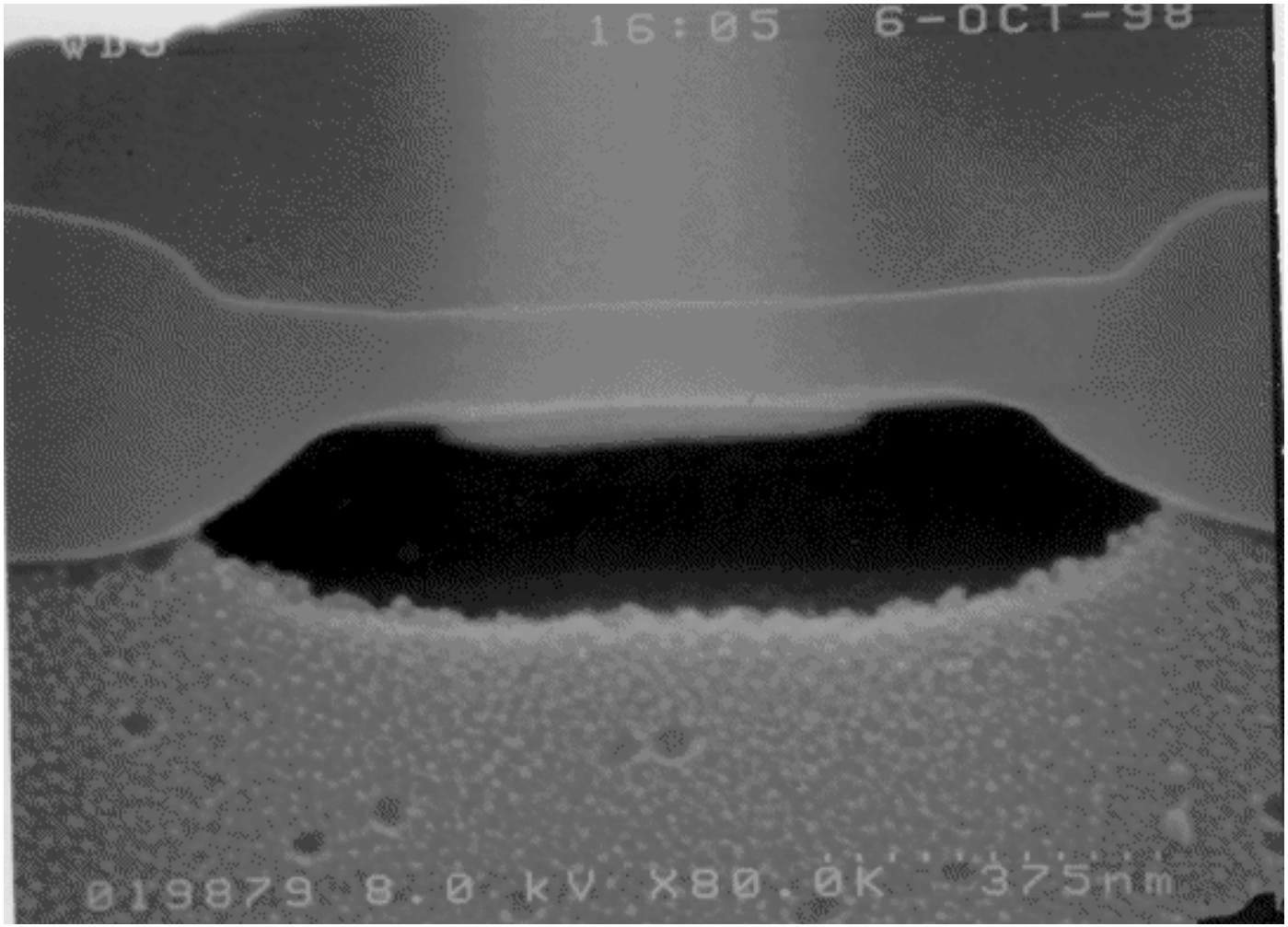
- Diode Verification: Before Tungsten Plug insertion



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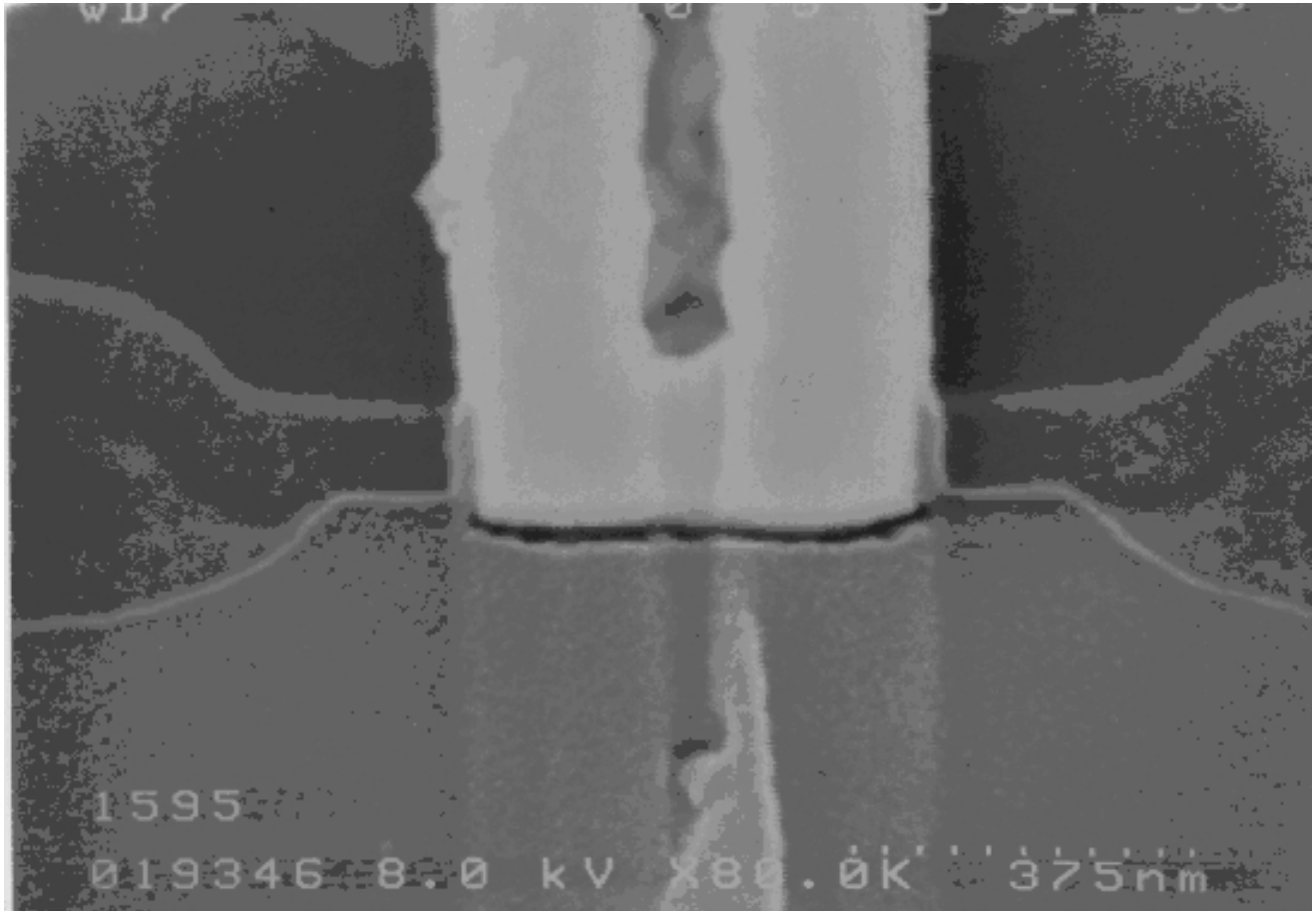
- Diode Verification: After Tungsten Plug



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- Conclusions

For dense designs (core utilization of more than 90%), dynamic diode dropping, jumper insertion, and dropping diodes with extension wires are three approaches which can be used to solve antenna violations. For design engineers, try to loosen up core utilization 5% to 7%, in order to leave some margin for diode and jumper insertion approaches.

For sparse designs (core utilization less than 50%), diode dropping alone is flexible enough to solve antenna problem. The three approaches proposed in this paper can be used successfully to solve most antenna violation problem.

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- Recommendations

This article do not consider the effect of diode insertion for clock net and memory blocks. Since the clock net is balanced tree structure, diode insertion will affect the skew and timing degradation problem. Therefore, diode insertion to clock net and memory block are not recommended. SLE can be improved to avoid the clock and critical net diode insertion.

This paper's approach can be applied to both block level and top level's antenna fixing. Timing delay can be verified from the RC extraction and SPICE tools. The timing delay caused by diode insertion is within 0.02% for critical net (the longest nets in design, such as clock net). DRC and LVS are verified after fixing antenna problems. If the tool does not generate the transistor level netlist, diode insertion can not be checked. In LVS checking, just check for short circuits only.