Hybridization Methodology for Finding Maximum Capacitance of Mixed Signal Design

Peter H. Chen, Harrison Liu, Jerry Hong, Jim H. Wang, and Sam Lee

Faraday Technology Corporation
10-2 Li-Hsin First Road
Science-Based Industrial Park
Hsinchu, Taiwan 300, ROC

{pchen, hcliu, cnhong, jhwang, lees}@faraday-tech.com

Abstract

This paper proposes a generic working methodology, *i.e.*, hybridization of strength interpolation and partial circuit extraction and SPICE simulation, Input Insertion, and whole IP simulation for finding the maximum capacitance of IPs. The main subjects include the IP block library to standard cell library mapping, Table of Inverter Set, IP Table, IP vs. Inverter Set Interpolation, and Partial Circuit Extraction and SPICE Simulation. The automation of the maximum loading capacitance (maximum capacitance) search for inout (input/output) pin and output pin of Intellectual Property (IP) blocks can estimate 75% of the maximum capacitance in a practical and fast manner via the interpolation of a group of candidate inverters (Inverter Set) without running SPICE Simulation. The Partial Circuit Extraction and SPICE simulation is used to obtain the maximum capacitance for 24.9% of ASIC pins. The remaining non-ASIC external IO pins are about 0.1%. Due to circuitry complication, debugging, and verification reasons associated with these external IO pins, circuit extraction is not recommended. The maximum capacitance of IO pins of Pulse Width Modulation (PWM) IPs is estimated by Input Insertion and SPICE simulation, and that of Universal Serial Bus (USB) IPs is calculated by whole IP block and SPICE simulation, respectively. The Forward and Backward Trees are used to store the temporary and final Max Loading Capacitance.

Table of Contents

Table of Figures

1.0 Introduction

Using SPICE simulation to get the maximum capacitance for each inout pin and output pin of an IP is very time consuming. For example, it takes 4-5 days for Synopsys's HSPICE simulation or 1-2 hours for ADiT's Turbo Mode to get a timing delay for PLL [3]. The time required to identify the maximum capacitance is much longer (by months) since the task involves more steps of SPICE simulation. It is therefore impractical to obtain the maximum capacitance for PLL and other IPs through the SPICE simulation.

Currently, Faraday institutes four ways to determine the maximum capacitance for an ASIC design, i.e., IP vs. Inverter Set Interpolation, Partial IP Circuit [1, 2, 3, 5] Simulation. If the first way does not qualify, the second one will be used instead. The hybridization of the above two ways covers 100% of the digital inout / output pins for an ASIC design. For IPs with non-ASIC pins (IPs with external IO pins from external devices), two additional ways are employed, i.e., Simulation of Input Insertion of IO Cells and whole IP simulation.

The analog output pins of IPs are ignored since they do not drive the digital block, i.e., they do not have slew rate and maximum capacitance. The external driving output pins are embedded in specified IO cells. The maximum capacitances for those pins (about 0.2% of all inout and output pins of IPs) are parsed directly from the specified IO cells.

The Inverter Set with varieties of strength is a good candidate as the basis of interpolation for IPs. However, there are some restraints for maximum capacitance search. In more detail, the device names (such as N_18_LL, P_18_LL, N_18_G2, or P_18_G2) must be the same for the IPs selected; the IP length must be the same or within the tolerance range (-10% to +2%) to the Inverter Set; and the total width of the device connected to the output pin must be shorter than that of the Inverter Set. If the foregoing criteria are not matched, then the partial circuit will be extracted and the SPICE simulation will be performed.

2.0 IP Interpolation and Inverter Set

For mobility concern, the PMOS size is normally set to be 2.5 to 3 times bigger than the NMOS size. These size variations differ from design to design. Due to this reason, the algorithm picks the smallest strength of Inverter Set of the NMOS and PMOS comparison and finds the maximum capacitance from the associated Inverter Set.

Figures 1 and 2 show the relationship between the selected IP and the Inverter Set with different strengths, i.e., INV1 through INV12.

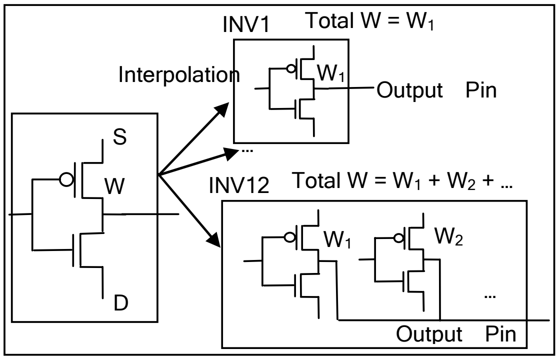

Figure 1. Schematic View of IP Interpolation.

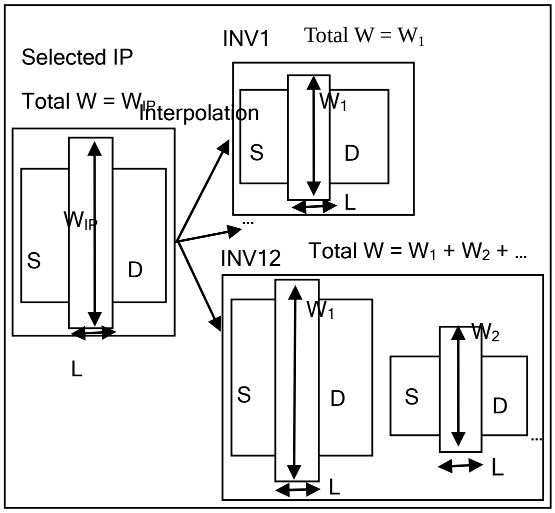

Figure 2. Layout view of IP Interpolation.

The symbols in Figures 1 and 2 are defined as follows:
L: Channel length of N-MOS or P-MOS
W: Channel width of N-MOS or P-MOS
S: Source
D: Drain
Total W: Sum of channel width of N-MOS or P-MOS

2.1 Exception of Interpolation

This interpolation method only applies to any IP blocks that use identical or similar channel length of the Inverter Set within an ASIC design. It does not apply to all IP blocks. Specifically, the following situations must be met to use this interpolation method: 1) the device name must be the same, 2) the gate length must be the same or within the -10% to +2% tolerance, and 3) the total width of IP must fall within the range of total width of each member of the Inverter Set.

As a rule of thumb, the length tolerance for IPs adopting this method is -10% to +2% based on Faraday designers' estimation. Any devices with a length beyond this tolerance will have a bigger driving strength (shorter electron moving path). This implies that the IP tolerance is more conservative than that of the Inverter Set. For example, for 0.18 µm technology, using a bigger length of 0.19 µm to drive the inout or output pin will not be suitable for Inverter Set with a channel length of 0.18 µm. The tolerance of the IP in this instance is 5.5%, which is outside the tolerance of -10% to +2%.

2.2 IP, Cell Library, and Inverter Set Mapping

In each technology, every IP has its associated standard cell library for ASIC design. In order to map IP libraries to standard cell libraries, the relations between the IP libraries and the standard cell libraries should be defined. Table 1 shows the mapping of IP libraries to standard cell libraries and Inverter Sets. The directory structure of IP library and standard cell library is shown in Figure 3.

Table 1. IP Mapping Table.

Process (µm)	IP Library	Standard Cell Library	Inverter Set
0.18	fsa0l_v	fsa0a_l	inv1.cir … inv12.cir
0.13	fsc0g_v	fsc0g_d	invcgd.cir … invggd.cir
0.09	fsd0l_v	fsd0l_d	invcld.cir … invgld.cir

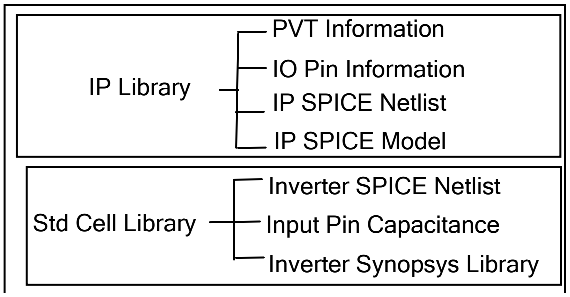

Figure 3. Directory Structure of IP Library and Standard Cell Library.

2.3 Inverter Set and Pin Set

As shown in Figure 4, the Inverter Set and the Pin Set are the dynamic allocated tables to hold the information of inverter and pin, respectively. Each Table holds one set of information for inverter and pin. The IP Library data are stored in Synopsys Liberty Format and retrieved via the Synopsys Liberty-API [1, 2, 3, 5].

Table 2 shows the Maximum Capacitance of Inverter Set with NMOS and PMOS Lengths of 0.18 µm, respectively.

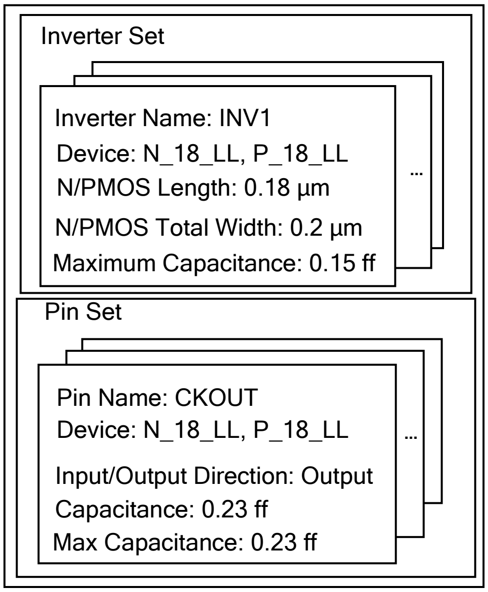

Figure 4. Data Member of Inverter Set and Pin Set.

Table 2. Max Capacitance of Inverter Set.

Inverter	NMOS Width	PMOS Width	Max. Cap. (BC/TC/WC)
inv1	1.211	1.571	0.356148/0.365933/0.429577
inv2	1.993	2.713	0.622911/0.639639/0.749577
inv3	3.216	4.492	1.03755/1.06705/1.25146
inv4	4.238	6.296	1.45539/1.49749/1.75689
inv6	6.32	9.42	2.1566/2.21731/2.60193
inv8	8.468	12.408	2.8412/2.92085/3.42721
inv12	12.5	18.1	4.15877/ 4.28216/5.0299

2.4 Algorithm

Figure 5 shows the algorithm for maximum capacitance searching for all the IPs.
This algorithm is explained as below.

1. Read the input information of IP Library and Standard Cell Library by parsing the directories as described in Figure 3. Build the table of IP libraries to standard cell libraries by parsing the given IP libraries to standard cell libraries information.

2. Ignore the analog inout / output pin. Parse the maximum capacitance of external driving output pins (about 0.2% of all inout / output pins) from specified IO Cell. Some of the IPs at Faraday, such as Universal Serial Bus (USB), Pulse Width Modulator (PWM), and Regulator (REG), contain external output pins. Otherwise, use the following steps to find the maximum capacitance for digital inout / output pins for ASIC design.

3. Read information from IP Libraries. Build the output pin and inout pin table for IP libraries. The table contains pin names, capacitances and maximum capacitances. The capacitances are obtained from RC extraction. The maximum capacitances are the subject matter of concern in this paper. Then build the device names (e.g., N_18_LL / P_18_LL or N_33_LL / P_33_LL).

Build the length (e.g., 0.18 µm) of each device. Build the summation of the width for each device.

4. Set up information for Inverter Set (e.g., INV1, INV2, …, INV12). Build the device names (e.g., N_18_LL and P_18_LL). Build the length (e.g., 0.18 µm) of each device. Build the summation of the width for each device.

5. Loop each inout and output pin table of the IP. Check for compliance of the interpolation criteria, i.e., same device name, same device length or device length within tolerance, and IP's driving strength less than the Inverter Set's. Note that the device names can be N_18_LL, P_18_LL, N_33_LL, P_33_LL, and so on. The IPs must be of the same length (0.18 µm, 0.09 µm, etc.) or be within the tolerance of the Inverter Set. Then interpolate the width of IP within the width of the Inverter Set. Pick the smallest width of the NMOS and PMOS interpolation.

6. For each inout pin and output pin, if the interpolation criteria are met, put the maximum capacitance data obtained from Inverter Set into the IP maximum capacitance data. If not, start the Partial Circuit Extraction and SPICE Simulation.

7. Write the three corners (Best, Typical, and Worst) of the IP library.

2.5 Example

This section demonstrates an example of the algorithm.

Given a PLL, the following steps are used to determine the maximum loading capacitance for the output pin CKOUT.

1. Open the SPICE model of PLL, and search for the output pin CKOUT. We have:

   MX_1 CKOUT … L=0.180U W=4.000U N_18_LL

   MX_2 CKOUT … L=0.180U W=4.000U N_18_LL

   MX_1 CKOUT … L=0.180U W=3.000U P_18_LL

   MX_2 CKOUT … L=0.180U W=3.000U P_18_LL

   MX_3 CKOUT … L=0.180U W=3.000U P_18_LL

   MX_4 CKOUT … L=0.180U W=3.000U P_18_LL

2. We have Total Width (TW) for 2 NMOS (TW) = 8.0U and TW for 4 PMOS = 12.0U with the same L = 0.18 U for PLL.

3. Build the strength table inverter set from the standard cell library as follows:

   inv1: NMOS TW =1.211U; PMOS TW=1.571U

   inv2: NMOS TW= 1.993U; PMOS TW= 2.713U

   inv3: NMOS TW= 3.216U; PMOS TW = 4.492U

inv4: NMOS TW = 4.238U; PMOS TW = 6.286U

inv6: NMOS TW = 6.32U; PMOS TW= 9.42U

inv8: NMOS TW = 8.46U; PMOS TW = 12.40U

inv12: NMOS W = 11.33U; PMOS TW = 18.1U

4. Interpolate PLL from the above Inverter Set (inv1 to inv12). We have inv8 as the best fit.

5. Find maximum one for maximum capacitance from inv8 library. We have the maximum loading capacitance for the pin CKOUT as 3.42721 pF.

If you have any other inout / output pin, repeat steps 1 to 5 until all the inout / output pins are done.

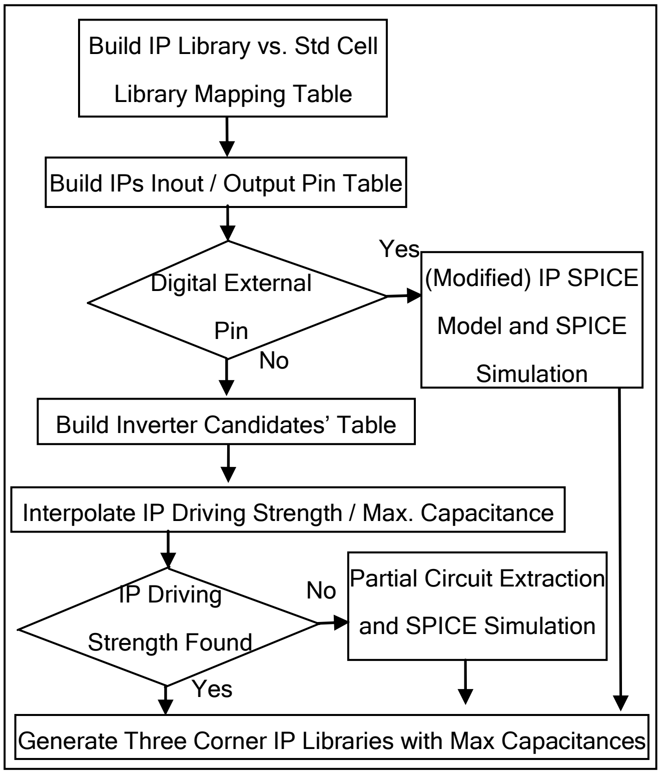
Build IP Library vs. Std Cell Library Mapping Table
Build IPs Inout / Output Pin Table
Digital External Pin
Yes
No
(Modified) IP SPICE Model and SPICE Simulation
Build Inverter Candidates' Table
Interpolate IP Driving Strength / Max. Capacitance
IP Driving Strength Found
No
Yes
Partial Circuit Extraction and SPICE Simulation
Generate Three Corner IP Libraries with Max Capacitances

Figure 5. Flowchart of Max. Capacitance Search.

2.6 Result

Table 3 shows the maximum capacitance of Best Condition (BC), Typical Condition (TC) and Worst Condition (WC) for Analog-to-Digital Converter (ADC). This IP is one of 153 IPs under test. About 75.1% (897 pins out of 1194 pins) of Faraday's IPs are eligible to use IP vs. Inverter Set Interpolation. The IP Library Name is fsa0b_v (0.18 µm) and the IP Name is adc020ha0l [4]. In this example, all the output pins (DRDY, O0-O7) match the interpolation rules and maximum capacitances are found.

Table 3. Max Capacitance by Inverter Set Interpolation.

Output Pin	Output Max. Cap. [BC/TC/WC] (fF)
DRDY	0.622911 / 0.639339 / 0.749577

O0-O7	0.622911 / 0.639339 / 0.749577

3.0 Partial Circuit Extraction

25% of the pins failed to obtain the maximum loading capacitances by the Interpolation of Inverter Set due to device mismatch, length mismatch, excessive width, and the like. To perform SPICE simulation against the 25% remainder is impractical insofar as the length of run-time is concerned. Partial circuit extraction is a good mechanism to cut down the SPICE run-time. In partial circuit extraction, the last two levels of circuits are extracted. At Faraday, those circuits are categorized as inverters and very few are transmission gates in USB and latches in DLL. For the output pin connected to transmission gate in USB, we perform the IP simulation. For the output connected to latches (such as DLL), we extracted one level of inverter and then perform the simulation. Figure 6 shows an example of two-level extraction of inverters. The latch circuit can be identified by two different inputs from two P-MOS or N-MOS in the second level of circuitry. Figure 7 shows the latch circuit example with two different inputs RB and Data. When RB is High, T1 is Open (Off) and T2 is Short (On). The circuits are double layer of inverters at the operation mode of the data latch.

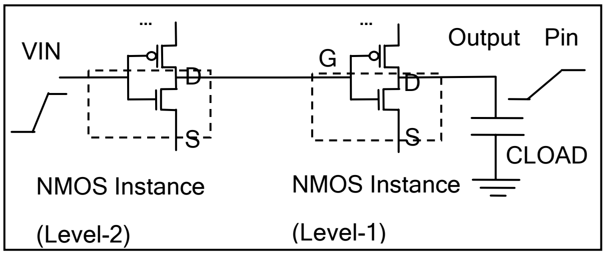

Figure 6. Extraction of Last Two Circuit Levels for General IPs.

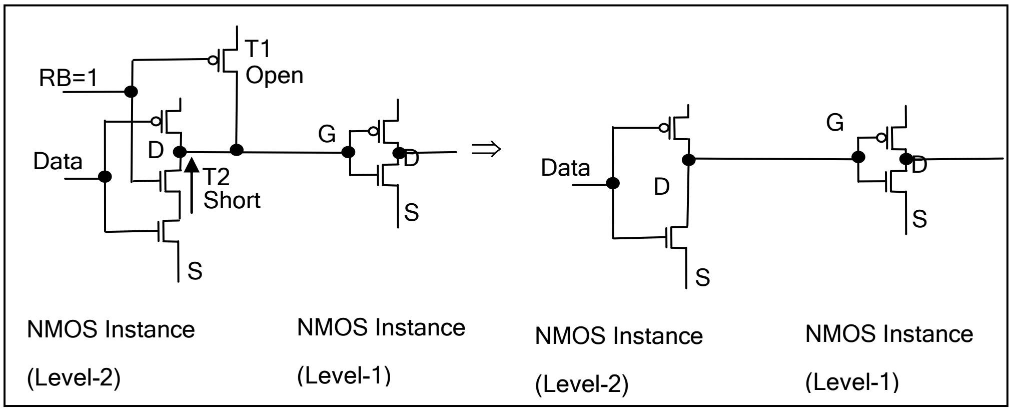

Figure 7. Identification of Latch Circuit.

3.1 Algorithm

The algorithm for Partial Circuit Extraction is as follows:

1. Build the first level of pin set from output / inout pins.

2. Search for all the devices that have the Source and Drain connected to the level-1 pin set. Build the level-1 device sets.

3. Build the level -2 net set by the gate name of the level-1 devices.

4. From the gate of the level-1 device sets, search for the level-2 devices (with the Source and Drain connected to the level-2 net set). Build the level-2 device sets.

5. Set the input VIN, sweep the output pin loading for each corner, and measure the slew rate.

6. From the SPICE result, find the maximum output capacitance according to the criterion of slew rate at 1 nsec.

7. Use following formula for approximating the maximum capacitance at the slew rate of 1 nsec.

   $$MaxL_{i,lm} = L_{i,lm,j-1} + (L_{i,lm,j} - L_{i,lm,j-1})/(SR_{i,lm,j} - SR_{i,lm,j-1}) \cdot (SR_{i,lm,j} - 1.0) \quad \ldots (1)$$

   Where:

   $MaxL$: Maximum Loading Capacitance

   L : Loading Capacitances

   SR : Measured Slew Rate

   i: inout or input pin index

   lm: Library Corner (BC, TC, WC)

   j: Loading Capacitance / Slew Rate index

8. If the loading capacitance is too small to meet the 1 nsec of Slew Rate criterion, then double the loading capacitance and repeat Steps 5-7 until the 1 nsec of Slew Rate criterion is met.

3.2 Result

Table 4 shows an example of the best corner of Faraday's ADC030 (Analog to Digital Converter) for the input voltage Vinput (rise time = 0.2, fall time = 0.2, width = 12.3, and period = 25 nsec). Sweep the output pin DI0 with loading capacitances (start 0.0pF, stop 10.0pF, and step 10.0 pF) and measure the slew rate at the output pin DI0. The maximum capacitance at 1 nsec slew rate (interpolated based on slew rates of 0.2027 nsec and 1.85 nsec for 0pF and 10pF, respectively) is 5.17752 pF from Partial Circuit Extraction and Simulation within 2 seconds vs. 5.3376 pF after 7 days of whole IP simulation with 97% accuracy.

Table 4. Loading Capacitance by Partial Circuit Extraction and SPICE Simulation for Output Pin DI0 at Best Corner.

Loading Capacitance (pF)	Slew Rate (nsec)
0.0	0.2027
10.0	1.85
…	…

Figure 8 shows an example of RCV output pin extracted by the same algorithm. The inputs VIN and VIN1 are set to have opposite waveform according to USB specification [1, 2, 5]. Similarly, the pins VON and VOP of USB can be processed the same way as RCV. There are two external driving pins for USB, i.e., DN and DP, which are not within the ASIC concern. Table 5 shows a similar result. The maximum capacitance of RCV can be calculated by Equation (1).

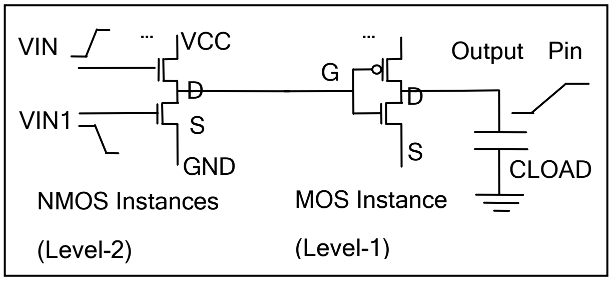

Figure 8. Extraction of Last Two Circuit Levels for RCV of USB.

Table 5. Loading Capacitance by Partial Circuit Extraction and SPICE Simulation for Output Pin RCV of USB at Best Corner.

Loading Capacitance (fF)	Slew Rate (nsec)
0.0	0.05324
10.0	1.42
	…

4.0 Digital External IO by Input Insertion and SPICE Simulation

At Faraday, only two IPs contain the external IO, i.e., USB and PWM. Figure 9 shows a Pulse Width Modulator (PWM) converts the voltage levels (e.g., 3, 4, 5 Volts at pin VOUT) into pulse widths (e.g., 3, 4, 5 nsec at pin EXT).

The pins EXT, PD_PMOS, and TEST_PIN are external digital output pins for PWM, respectively. Here, VREF, TA, TB, and TC are analog output pins of PWM and are not of concern. Figure 8 shows the power, input, and output pins of PWM, in which the VOUT is set to 6 V.

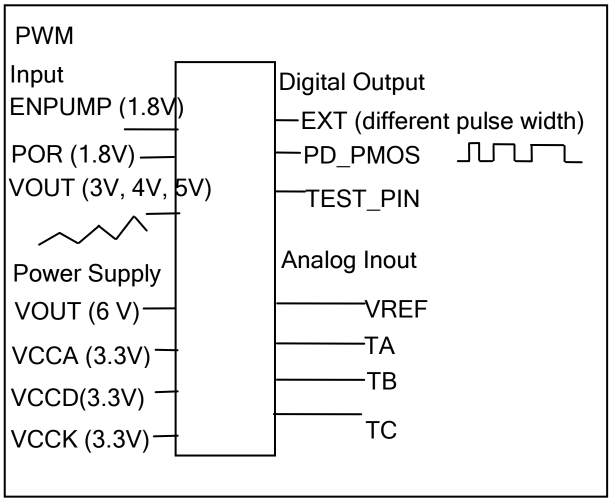

Figure 9. PWM Power Supplies, Input, and Digital/Analog Output.

Figure 10 shows simplified interconnection of pin PD_PMOS for PWM. The input of last instance is disconnected while the other setting of the PWM remains unchanged. The input slew is inserted at the input of IO cell connected to the output.

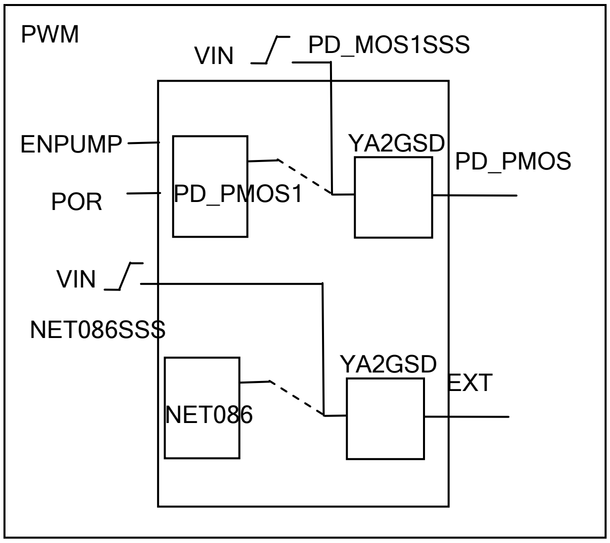

Figure 10. Interconnection of PD_PMOS for PWM.

4.1 Algorithm

The following algorithm performs Modified SPICE Model as shown in Figure 9.

1. Inside the IP Model, locate the top level IP name (e.g., PWM). Inside the IP, find the IO cell (e.g., YA2GSD) that connects to the external output pin (e.g., PD_PMOS).

2. Find IO input port location and maximum argument: In the IO cell library, find the IO cell (e.g., YA2GSD). Find the input pin location (e.g., 5) with key word “I” (input port) of IO cell (e.g., YA2GSD) and the maximum argument number (e.g., 7) of IO cell. This input pin location is the argument location of an IO instance. Store the IP arguments.

3. Find the input connection of IO instance: In the IP library, check the IO cell (e.g., YA2GSD) instance. If the IO input pin name (e.g., PD_PMOS) is on the current IO cell instance, then connect the IO input pin to IO cell. From the argument number (e.g., 5), we can find the input name (e.g., PD_PMOS1) of IO cell.

4. Disconnect the input to IO instance and add the new input (e.g., PD_PMOS1SSS) for the IO instance: Open the IP library. Disconnect the input pin name by adding another pin name (e.g., PD_PMOS1SSS). This is a newly added pin. Find the input name (e.g., PD_PMOS1) of the IO, change the input name into the newly added input (e.g., PD_PMOS1SSS). Store the new input port.

5. Generate the above SPICE file. Include the above SPICE file from test bench. Instantiate the IP instance and IP arguments.

6. Set up the global powers (e.g., VCCA, VCCD, VCCK).

7. Set the input VOUT and input VIN for the newly added pin (e.g., PD_PMOS1SSS), sweep the output pin loading for each corner, and measure the slew rate at the output pin (e.g., PD_PMOS).

8. Repeat steps 1-7 for all the external inout / output pins for three corners.

5. 0 Digital External IO by Full IP SPICE Simulation

Figures 11 and 12 show the definition and setting of USB IP. The maximum capacitance of output pin RCV and the maximum capacitances of inout pins VOP and VON are obtained by inverter interpolation and partial circuit extraction. However, the external IO pins DP and DN are specified in the USB 1.1 [1, 5].

SP = 1 (VCCK): Full Speed with DP pulled up.

Maximum capacitance specification: With Input Slew Rate of 12 MHz at 0.2 nsec, fix 50 pF for PD (or DN), and sweep DN (or DP) loading capacitance 200, 100, and 80 pF for BC, TC, and WC, respectively, as opposed to USB specification of 50 pF.

SP = 0: Low Speed with DN pulled up.

Maximum capacitance specification: With Slew Rate of 1.5 MHz at 0.2 nsec rising edge, fix 600 pF for PD (or DN), and sweep DN (or DP) loading capacitance 1200, 800, and 200 pF for BC, TC, and WC, respectively, as opposed to USB specification of 600 pF.

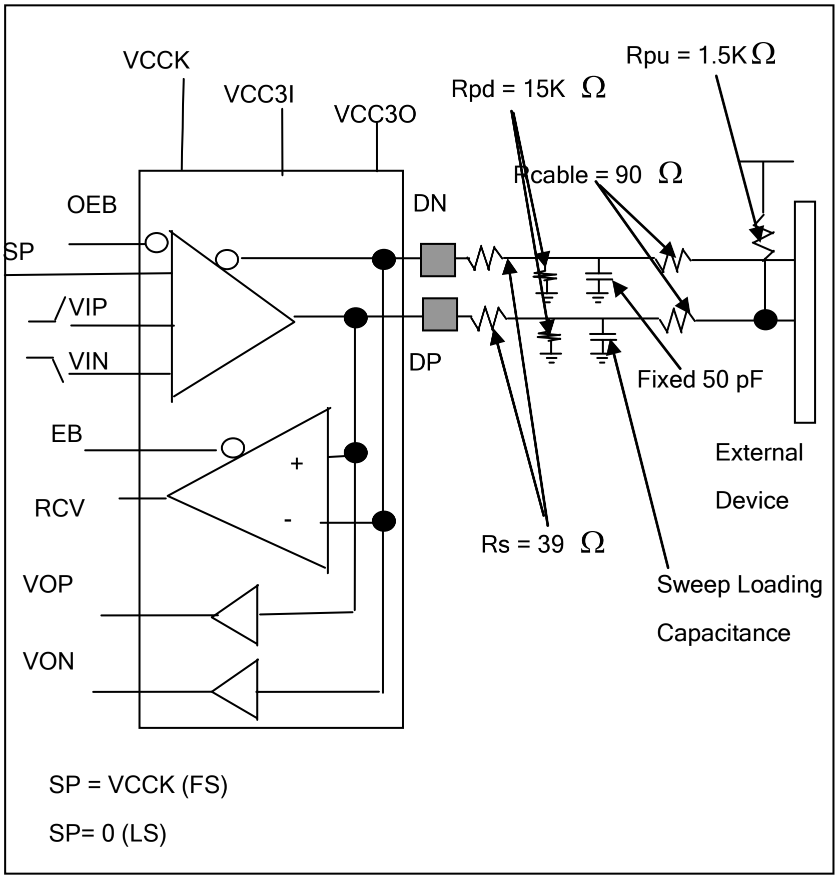

Figure 11. Full IP SPICE Simulation for Full Speed (SP = 1) of USB.

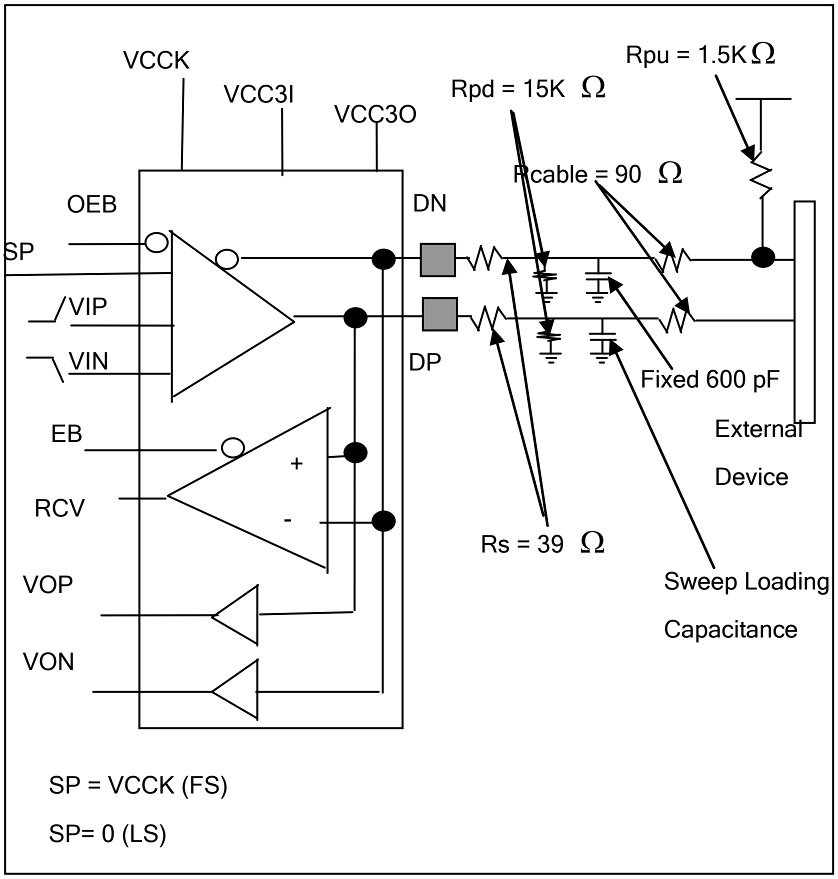

Figure 12. Full IP SPICE Simulation for Low Speed (SP = 0) of USB.

6.0 Max Capacitance of Synopsys Liberty Format

The characterized maximum capacitance of each output and inout pin is added to the Synopsys Library Format. The Data structure of Synopsys Liberty Format for IP is modeled as Figure 13. This paper proposes two Pin Trees to represent the Forward and Backward timing paths, respectively. These Tree Models are used to represent the Forward and Backward Liberty Format. The Forward Tree is for SPICE Testbench Generation, Network Computing Submitted Task Control (license, submitted, not submitted, and re-submitted) and Running Status Control (done, error, and running), and Non-Timing Related Input/Inout Pin of Liberty Format. Each testbench is created by Forward Pin Tree Structure.

The maximum capacitance of each forward path is obtained by sweeping the loading capacitance and is then assigned under the Forward Pin Tree. For instance, the final maximum capacitance of output pin DN is obtained by taking the minimum of each path under the same input pin. In the example shown in Figure 14, the maximum capacitance for output pin DN is obtained from min (Max Cap DN0 and Max Cap DN1 of input pin VIN, and Max Cap DN2 and Max Cap DN3 of input Pin OEB). The maximum capacitances are then stored under the output pin of Backward Pin array. The Backward Pin Tree is used for Output Pin and Timing Related Liberty Format.

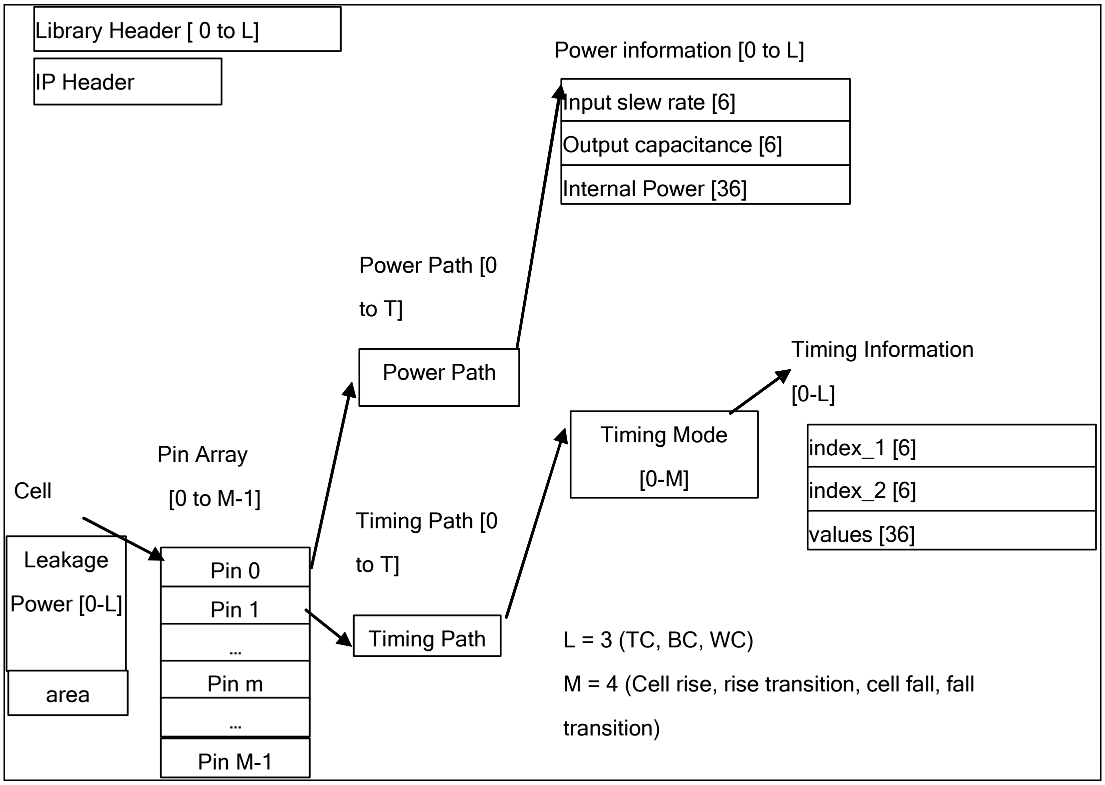

Figure 13. MxCAE Data Model.

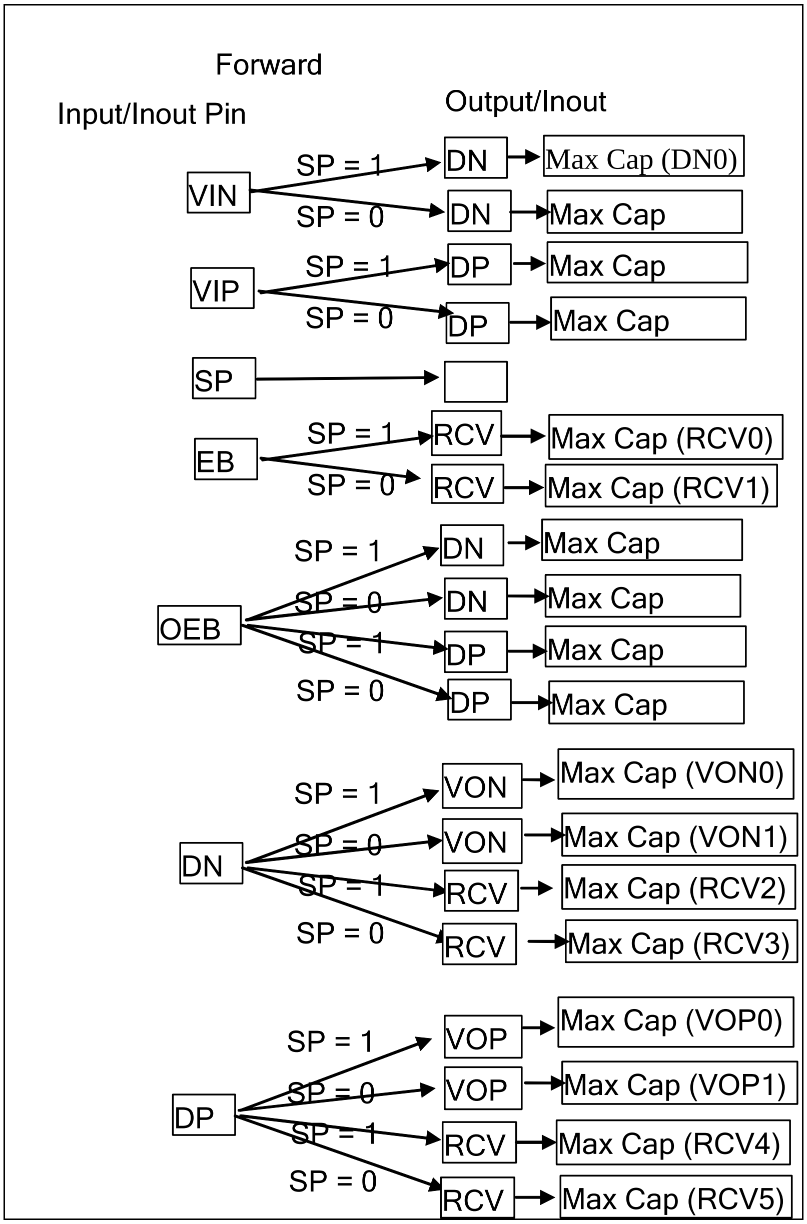

Figure 14. Forward Pin Tree of USB by MxCAE Model.

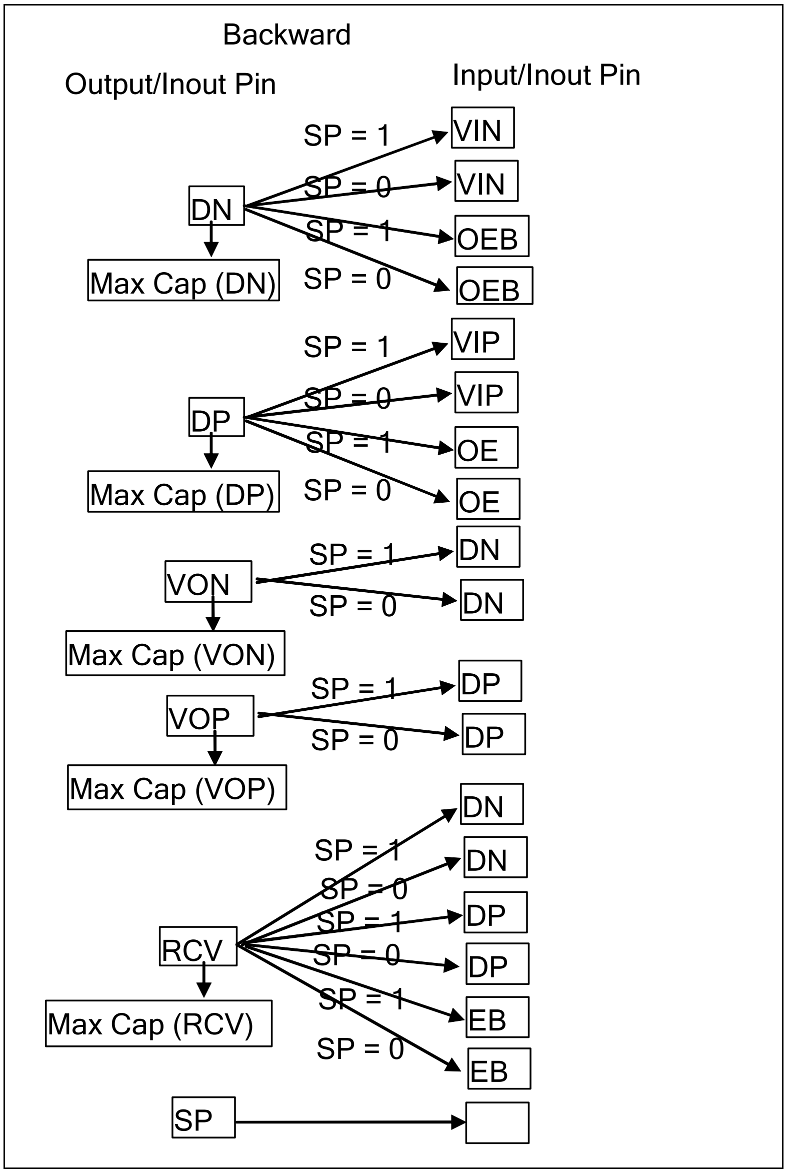

Figure 15. Backward Pin Tree of USB by MxCAE Model.

6.1 Forward and Backward Pin Tree Algorithm

The Forward Pin Tree is constructed by Traversing the Behavioral Model (Verilog) of IP and verified by traversing of SPICE Model of IP. The number of path from both Verilog and SPICE should be the same [1, 2, 5]. The following shows the construction of the Backward Pin Tree algorithm and the constrction of the maximum capacitances and etc.

1. Construct the Top Level of Backward Pin Tree:

    1.1 Loop for Input/Inout Pins of Forward Pin Tree.

        1.1.1 Loop for each Related Pin (or Path) of each Input/Inout Pin of Forward Pin Tree.

            1.1.1.1 Construct the Output Pins of Backward Pin Tree from the Related Pin of the Forward Pin Tree.

```
2. Construct the Path of Backward Pin Tree:
    2.1 Loop for the Output Pins of Backward Pin Tree.
        2.1.1 Loop for Input/Inout Pins of Forward Pin Tree.
            2.1.1.1 Loop for each Related Pin (or Path) of each Input / Inout Pin of Forward Pin Tree.
                2.1.1.1.1 If the Related Pin name of Forward Pin Tree is same as the Output/Inout
                Pin name of Backward Pin Tree, then construct the Related Input/Inout Pin name (or
                path) and associated attributes (timing, power) of Backward Pin Tree.
3. Construct the Max Capacitance of Backward Pin Tree
    3.1 Loop for the Output Pins of Backward Pin Tree.
        3.1.1 Loop for each Related Pin (or Path) of each Input / Inout Pin of Backward Pin Tree.
            3.1.1.1 Loop for Input/Inout Pins of Forward Pin Tree.
                3.1.1.1.1 Loop for each Related Pin (or Path) of each Input / Inout Pin of Forward
                Pin Tree.
                    3.1.1.1.1.1 Calculate the minimum of all maximum loading capacitances of all
                    related pin (path) under the same Input / Inout Pin of the Forward Pin Tree.
                    3.1.1.1.1.2 Store the minimum value as the maximum capacitance of the
                    Output/Inout Pin of the Backward Pin Tree.
```

7.0 Conclusion

The result of this research shows that only about 75% of the IPs under test can use the Maximum Capacitance Searching strategy. The remaining 25% need to go through the SPICE Simulation. As stated earlier, it is impractical to run the SPICE Simulation for an entire IP for maximum loading capacitance determination. Therefore, Partial Circuit Extraction of the last one or last two levels is necessary to cut down the run-time. The result of max capacitance is within accuracy 90% or above of whole IP simulation by this hybridization methodology. However, the runtime is cut from weeks into within the seconds.

8.0 Acknowledgement

The authors would like to thank Faraday for the full and valuable support of this project and Ms. Valerie Shih for the careful review and proofreading of this paper.

9.0 References

[1] Peter H. Chen, Steven Chien, and Jim J. Wang, “Automation of IP Characterization and Function Test by HSPICE and Liberty-API,” SNUG, Hsinchu, Taiwan, May 2004.

[2] Peter H. Chen, Steven Chien, Jim J. Wang, and Steve Tsai, “Method for IP Characterization and Path Finding, and Computer Readable Recording Medium for Storing Program,” Patent P2004-007-US-A / 13321 usd1 Pending, June 2004.

[3] Peter H. Chen, Tin-Fu Kuo, and Jim J. Wang, “Benchmarked PLL with ADiT Turbo and SPICE Model with Synopsys HSPICE,” Faraday Internal Research Report, August 2004.

[4] Peter H. Chen and Jim J. Wang, “Result of Maximum Capacitance Search by Inverter Interpolation,” Faraday Internal Research Report, August 2004.

[5] Peter H. Chen, Steven Chien, Harrison Liu, Jerry Hong, and Jim J. Wang, “Method for Finding Driving Strength and Computer Readable Recording Medium for Storing Program,” US/Taiwan Patent P2004-051-TW-A/14900-TW-PA Pending.