Hybridization Methodology for Finding the Maximum Capacitance of IP

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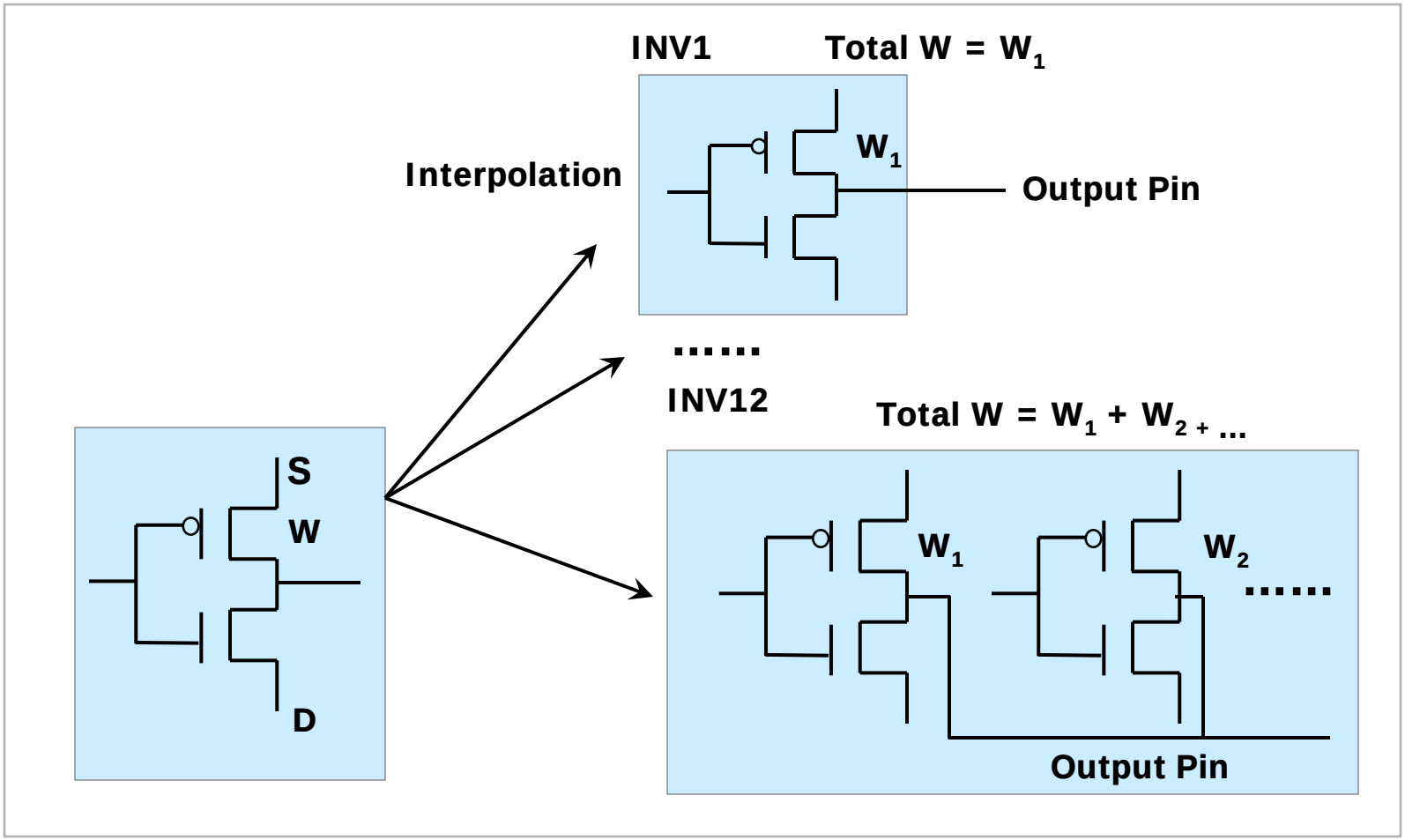
Introduction

- This paper proposes a generic working methodology for finding the maximum capacitance of Intellectual Property (IP). (hybridization of strength interpolation and partial circuit SPICE Simulation)
- 75% of the maximum capacitance can be found via the interpolation of a group of candidate inverters (Inverter Set) without running SPICE Simulation.
- The remaining 25% will be found by Partial Circuit Extraction and SPICE Simulation.

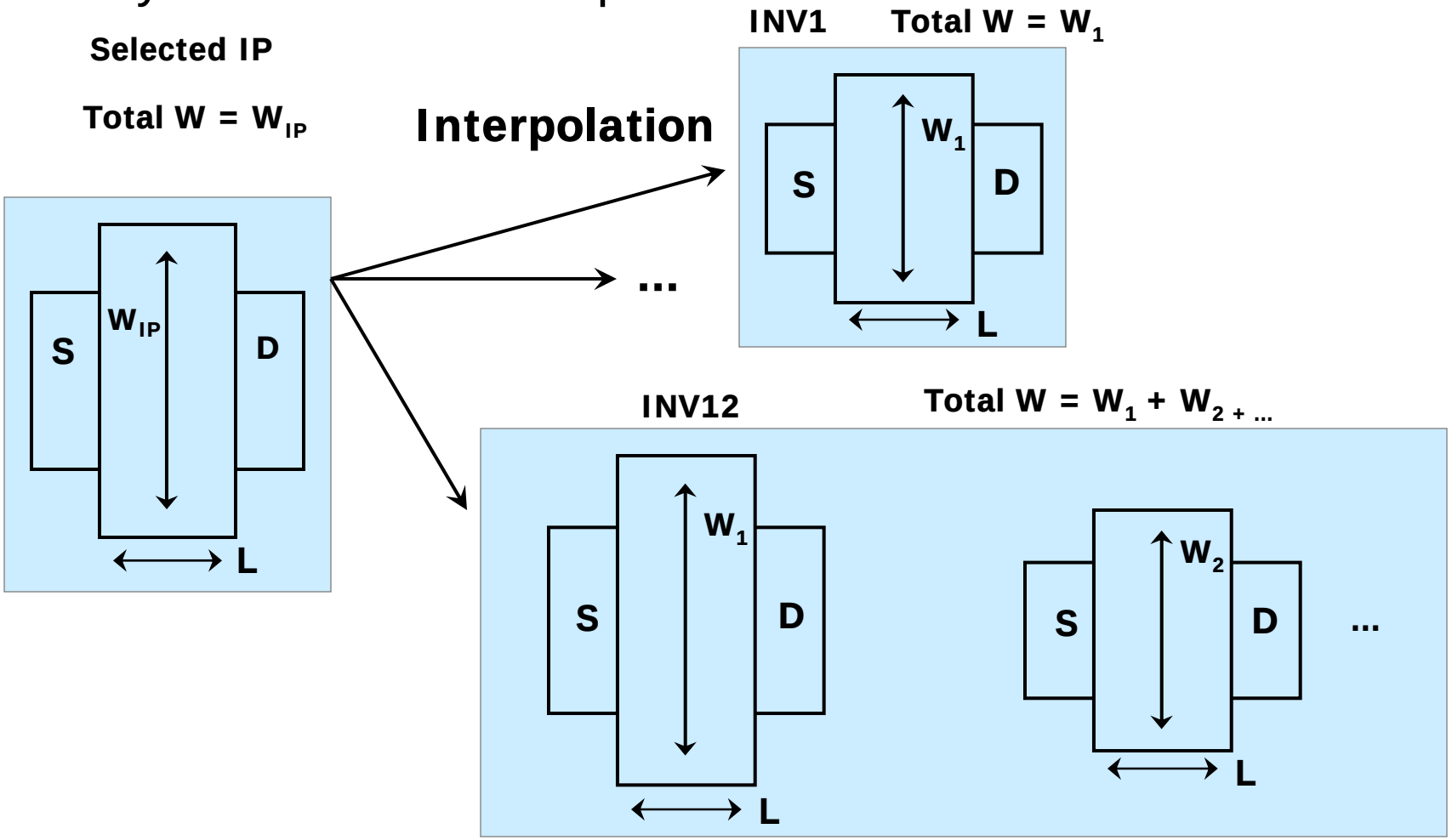
IP Interpolation and Inverter Set

❖ Schematic View of IP Interpolation.



IP Interpolation and Inverter Set

- Layout View of IP Interpolation



Inverter Interpolation Algorithm

- Build up IP Library and Standard Cell Library Information.
- Parse the maximum capacitance of external driving output pins (about 0.2% of all in-out / output pins) from specified IO Cell.
- Build up an IP pin table.
- Build up standard cell inverter set.
- Interpolate the IP from the standard cell inverter set.
- Find the maximum capacitance of IP.

Inverter Interpolation Example

- Open a SPICE model of PLL, search for “CKOUT” pin
  - **MX_1 CKOUT … L=0.180U W=4.000U N_18_LL**
  - **MX_2 CKOUT … L=0.180U W=4.000U N_18_LL**
  - **MX_1 CKOUT … L=0.180U W=3.000U P_18_LL**
  - **MX_2 CKOUT … L=0.180U W=3.000U P_18_LL**
  - **MX_3 CKOUT … L=0.180U W=3.000U P_18_LL**
  - **MX_4 CKOUT … L=0.180U W=3.000U P_18_LL**
- Total width for 2 nmos = 8.0um (on L=0.18um)
- Total width for 4 pmos = 12.0um
- Build up an inverter set table
- Interpolate and find inv8 is the best fit
- Find max cap from inv8 library
- The Max loading cap for CKOUT is 3.42721 pf

Max Cap of Inverter Set

Inverter	NMOS Width	PMOS Width	Max. Cap. (BC/TC/WC)
inv1	1.211	1.571	0.356148/0.365933/0.429577
inv2	1.993	2.713	0.622911/0.639639/0.749577
inv3	3.216	4.492	1.03755/1.06705/1.25146
inv4	4.238	6.296	1.45539/1.49749/1.75689
inv6	6.32	9.42	2.1566/2.21731/2.60193
inv8	8.468	12.408	2.8412/2.92085/3.42721
inv12	12.5	18.1	4.15877/ 4.28216/5.0299

Rules of Interpolation

- Interpolation applies to IP block that uses identical or similar channel length of the Inverter Set within an ASIC design.

- Requirements
  - 1) the device name must be the same type
  - 2) the gate length must be the same or within the -10% to +2% tolerance
  - 3) the total width of IP must fall within the range of total width of each member of the Inverter Set.

Result from Inverter Interpolation

- In this example, all the output pins (DRDY, O0-O7) match the interpolation rules and maximum capacitances are found
- The maximum capacitance of Best Case (BC), Typical Case (TC) and Worst Case (WC) for ADC are shown
- About 75.1% (897 pins out of 1194 pins) of Faraday's IPs can use IP vs. Inverter Set Interpolation.

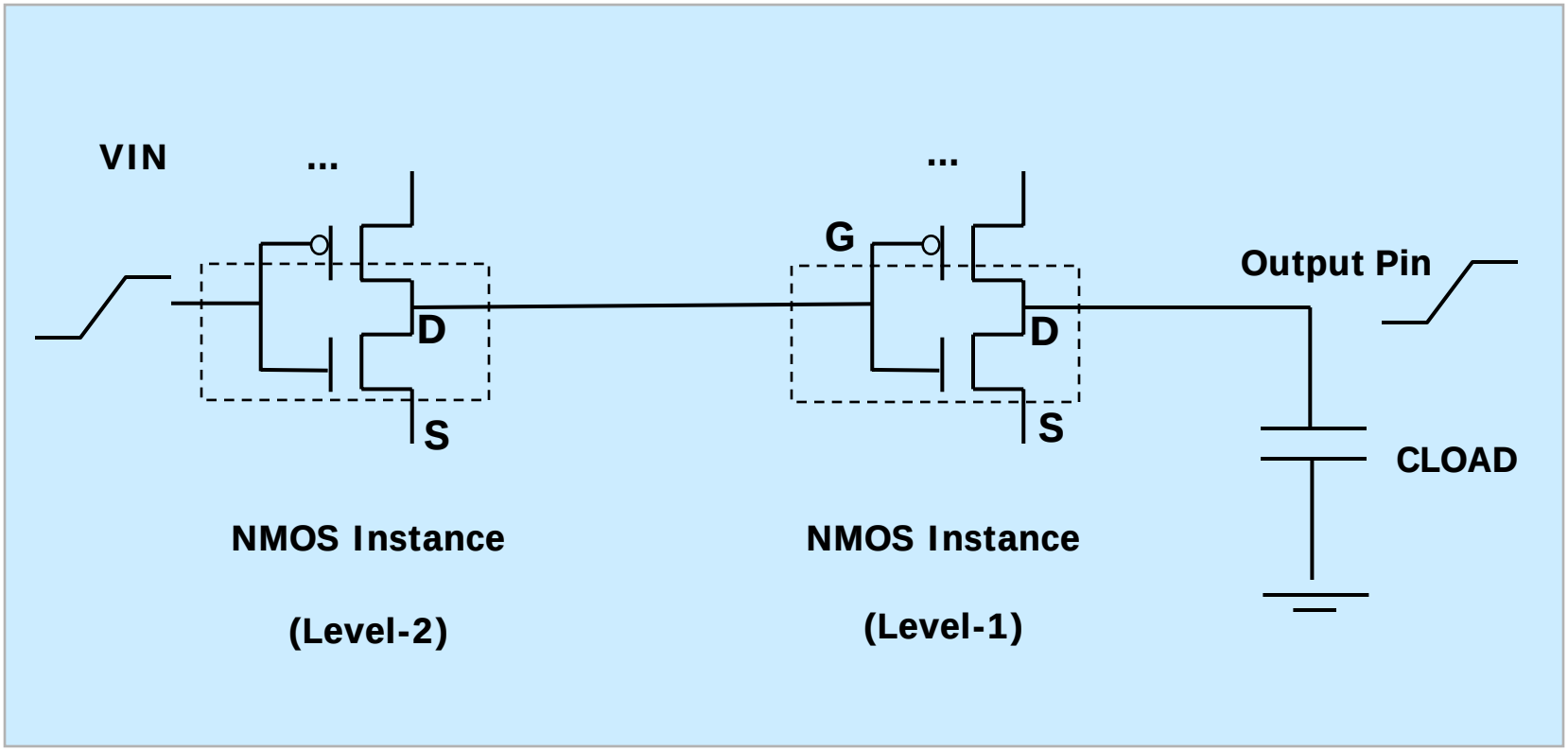
Output Pin	Output Max. Cap. [BC/TC/WC] (fF)
DRDY	DRDY0.622911 / 0.639339 / 0.749577
O0-O7	O0-O70.622911 / 0.639339 / 0.749577

Partial circuit extraction

- What are not able to use Interpolation method
  - Device mismatch
  - Length mismatch
  - Excessive width
- Why partial circuit extraction
  - To cut down spice simulation time
  - Last 2 level of circuits are categorized as inverters and very few are transmission gates in USB and latches in DLL

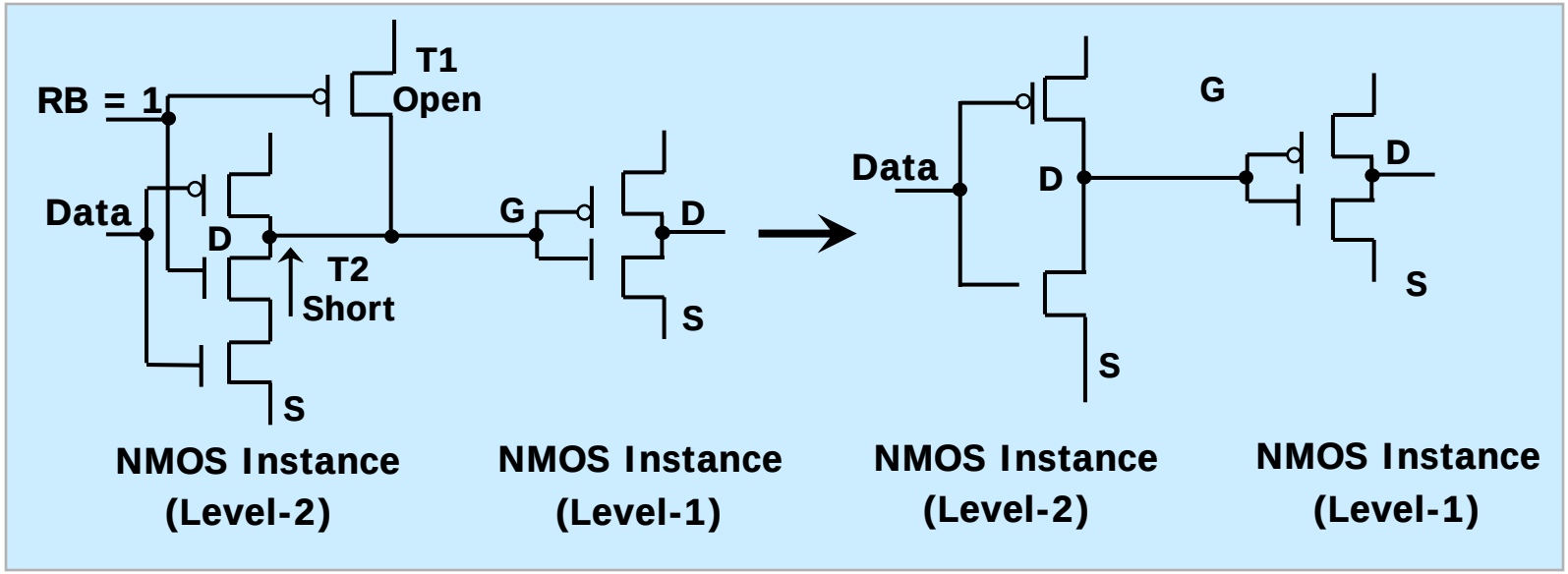
Partial Circuit Extraction

- 25% of pins use Partial Circuit Extraction



Partial Circuit Extraction

- The latch circuit can be identified by 2 Pmos or Nmos in the second level of circuitry
- The circuit is double layer of inverters at the operation mode of the data latch
- When RB is High, T1 is open (off) and T2 is short (on)



Partial Circuit Extraction Algorithm

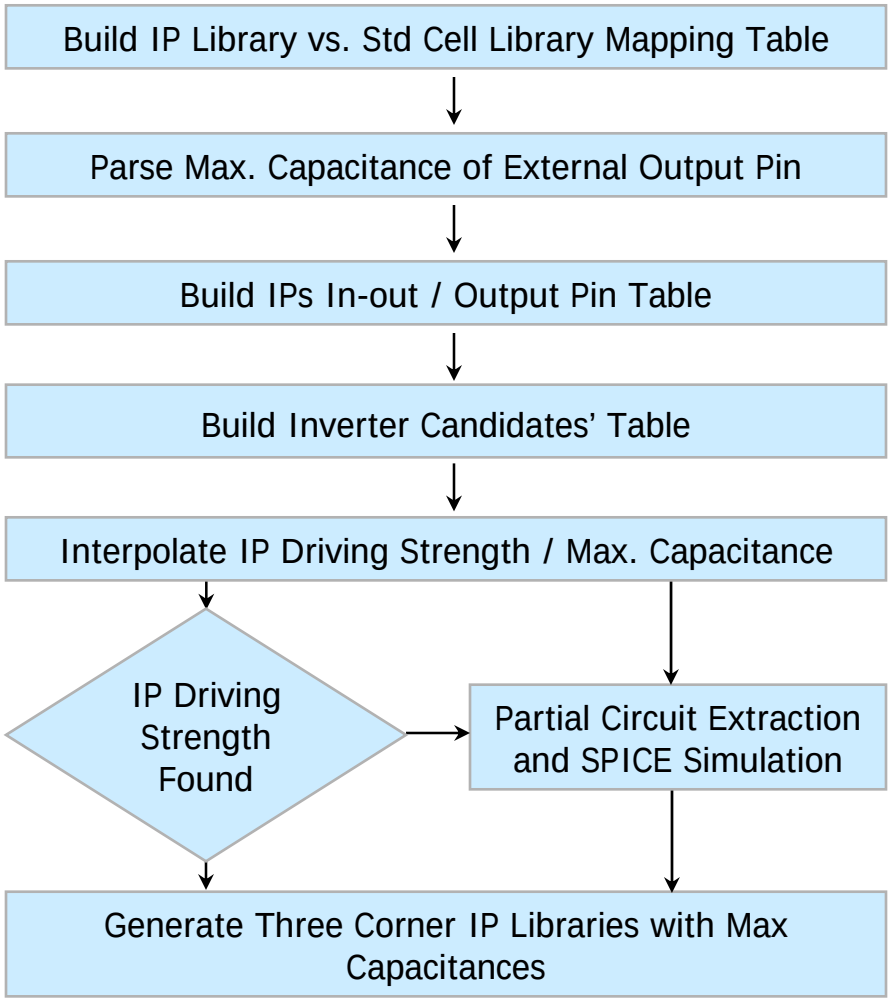
- Build the first level of pin set and the level-1 device sets.
- Build the level -2 net set and build the level-2 device sets.
- Set the input VIN, sweep the output pin loading for each corner, and measure the slew rate.
- Find the maximum output capacitance from SPICE result.
- Interpolate the maximum capacitance
- Double the loading capacitance and repeat SPICE simulation.

Partial circuit extraction

- Example of the best corner of Faraday's ADC030 (Analog to Digital Converter) for the input Vinput (rise time = 0.2ns, fall time = 0.2ns, width = 12.3ns, and period = 25 ns). Sweep the output pin DI0 with loading capacitance [start 0.0pF, stop 10.0pF, step 100.0 fF] and measure the slew rate at the output pin DI0. The interpolated maximum capacitance is 4.73125 fF. (run time 2 sec vs 7 days full chip Spice simulation and get 4.827fF result)
- Loading Capacitance (fF) Slew Rate (nsec)
- 0.0 0.00523
- 10.0 1.85
- ……

Overall Flow

❖ The overall flow shown as follows:



Conclusion

- The result of this research shows that only about 75% of the IPs under testing can use the Maximum Capacitance Searching strategy.
- The remaining 25% need to go through the SPICE Simulation. As stated earlier, it is impractical to run the SPICE Simulation for an entire IP for maximum loading capacitance determination. Therefore, Partial Circuit Extraction of the last one or last two levels is necessary to cut down the run-time from weeks to within 1-2 seconds.
- The result is above 90% accuracy of a whole chip simulation.