A Fast Methodology Flow for IP Input and Max Output Cap Characterization

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Agenda

- Introduction
- Characterization Flow
- Runtime and Accuracy Comparison
- Conclusion

Introduction (I): Current Problem

- It is very common for an IP to have 500K+ transistors. As IP design grows bigger and bigger, the SPICE simulation time grows exponentially, i.e., Non-Polynomial (NP) Problem.
  - It will take weeks to months to run SPICE simulation for input or output capacitance
  - Commercial tools using IV curve or model simplification does not cut enough in the runtime.
- IP designers are responsible for giving the input cap and output cap based on their knowledge, experience, impression, and IP specification
- Input and output cap characterization for IPs using spice-level simulator sounds impossible

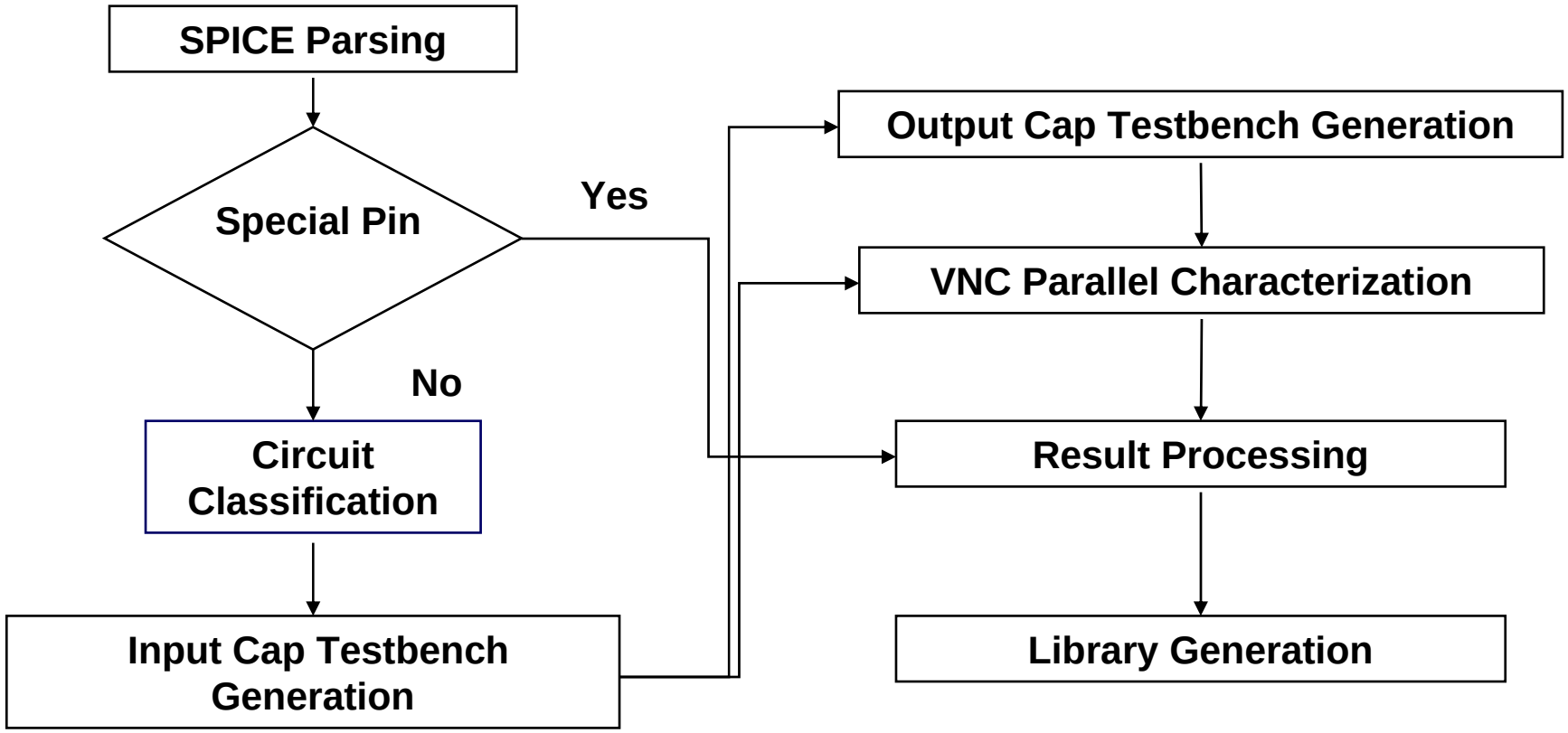
Introduction (II): Tool Problems

- One-corner input cap can be roughly estimated by extraction tool based on physical dimension. It is inaccurate and unconvincing due to lack of simulation model which adapts to any corner of processes and temperatures.
- Current commercial SPICE tools all failed to meet the speed, convergence, price, and accuracy requirement.

Introduction (III): Input and Output Cap Characterization Problem

- This paper proposes a fast and generic algorithm for Intellectual Property (IP), i.e., input cap and output cap characterization with partial circuit extraction and SPICE simulation, for finding the three corners of input cap of an IP
- The proposed algorithm cuts down the run-time from weeks to within seconds without sacrificing accuracy
- The accuracy for the input cap and output cap is 90% or above, which is within the acceptance of IP designers
- It is a part of Faraday IP characterization flow

Methodology Flow Overview



SPICE Parsing

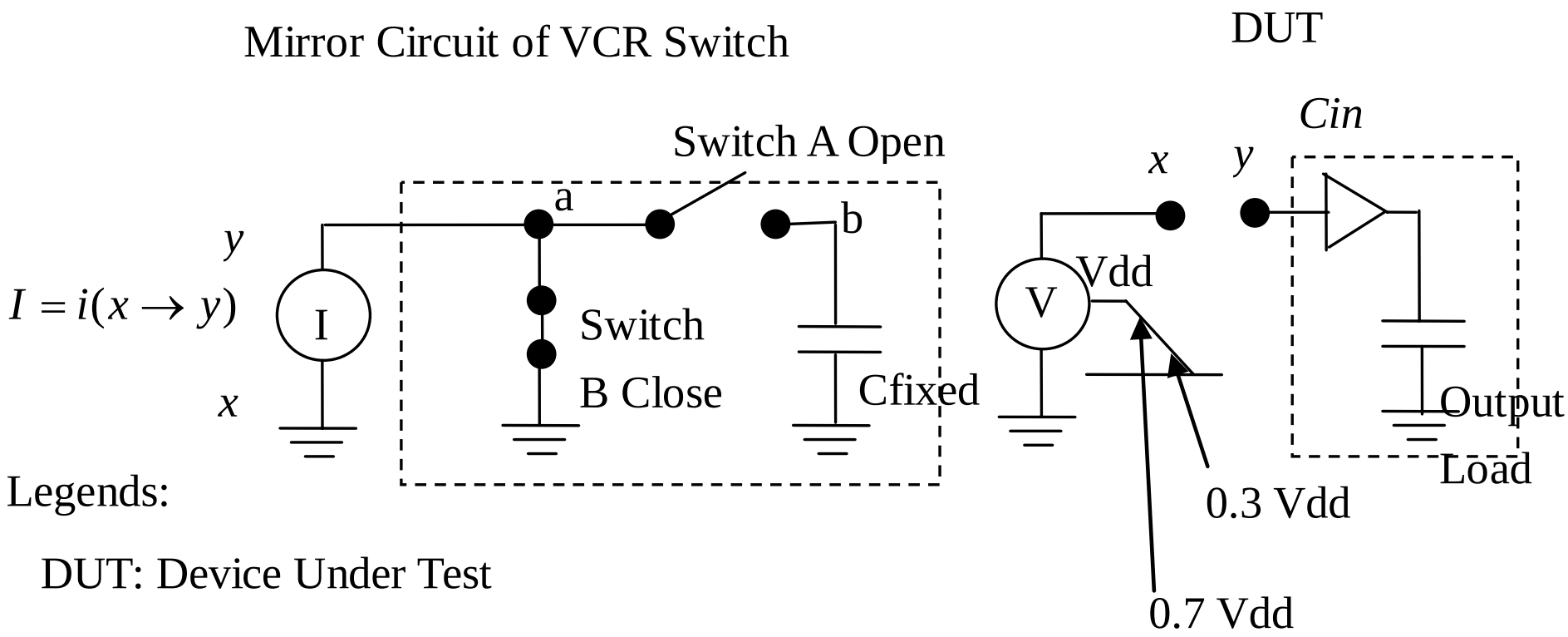
- Lumped LPE SPICE is used for input/output cap characterization
- The SPICE parsing does the following:
  - Parse the SPICE Device Model to map the voltage level to specified technology (0.25-, 0.18-, 0.13-micron, or others).
  - Remove the dummy resistors
  - Setup trimming resistors floating or shorted per IP specification
  - Parse the global ground and power definition
  - Extracts the IP's passing parameters for testbench instantiation

Special Pin

- Special Pins include input, output and IO pins connected to special analog circuits defined at Faraday.
  - Reference Voltage Setup
  - Resistance Setting
  - Voltage Compensation
  - Current Adjustment
  - Trimming Resistor
- The Special pins cannot be characterized by digital methodology.

Input Cap Characterization

Voltage-Controlled Resistance (VCR) for Input Cap



Legends:

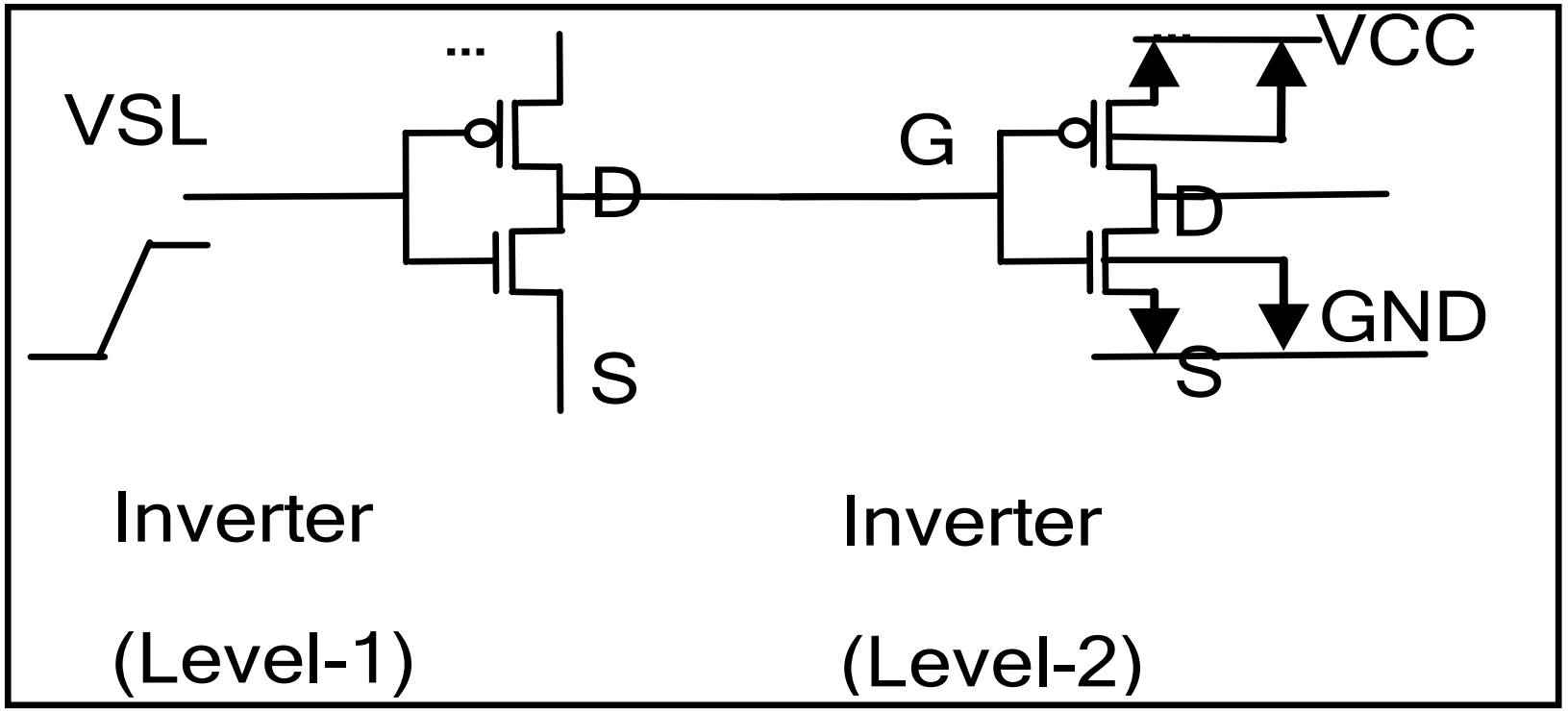
DUT: Device Under Test

VCR: Voltage-Controlled Resistance

$$Cin \equiv \max(Vb) \cdot Cfixed \,/\, 0.4Vdd$$

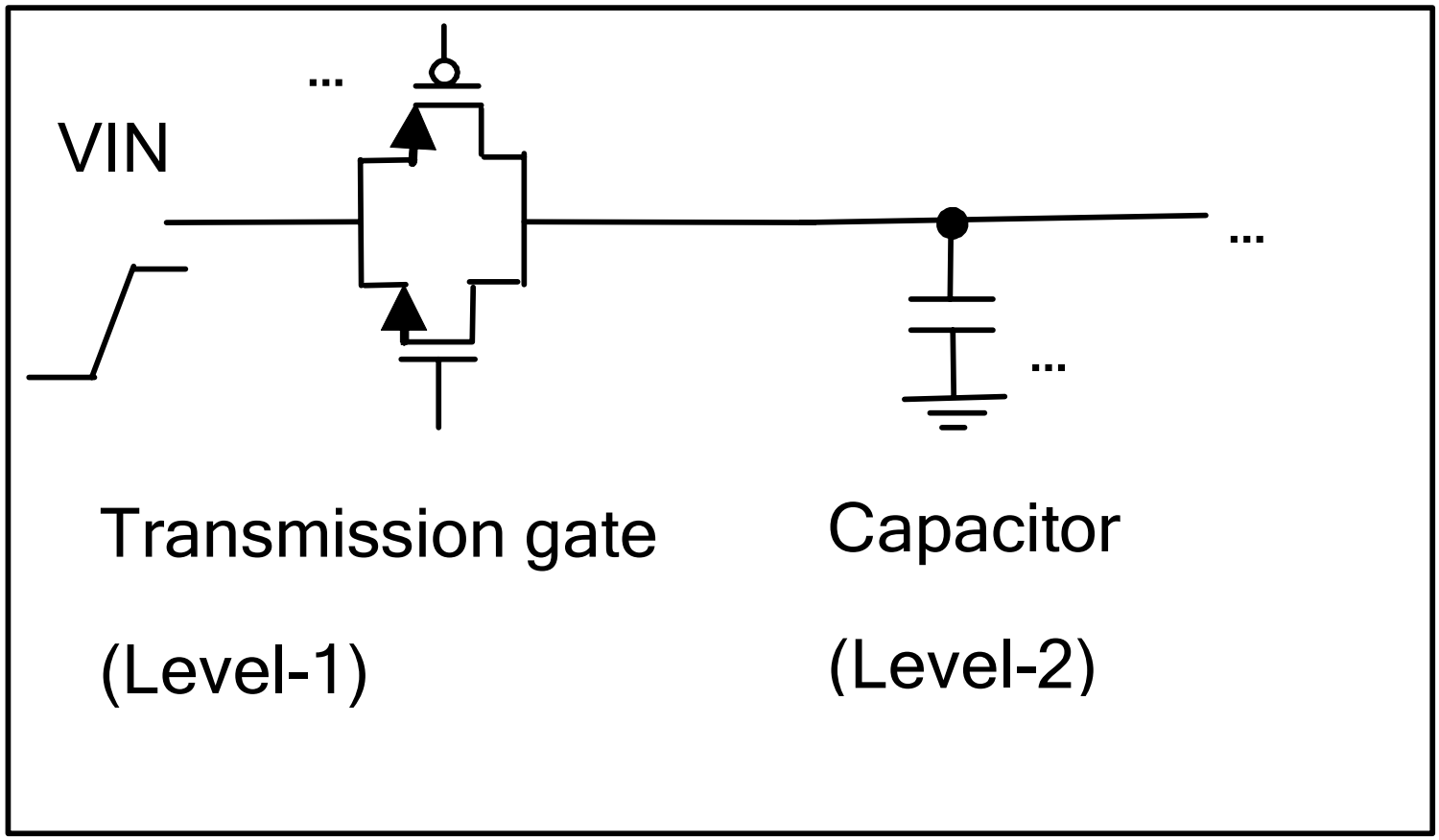
Input Cap: Double Inverter

Double Layers of Inverter



Input Cap: Transmission Gate

Transmission Gate and Capacitor



Input Cap (I): Level 1 Partial Circuit Extraction

- Input Cap Extraction Algorithm:
  - This algorithm extracts input pin connected to the inverter pairs (double inverter), transmission gate (transmission gate / capacitance), and ESD devices.
  - ESD device have no effect on designer but relate to the input / output cap characterization.
- Level-1 Device Extraction:
  1. Loop all the input pins/IO pins and skip the special pins
  2. If the input is connected to gate, then mark the cell type as inverter cell
  3. If the input is connected to source or drain, then mark the cell type as transmission gate and store the SPICE code.
  4. Build the level-1 device set containing device types, associated diode, and capacitances.

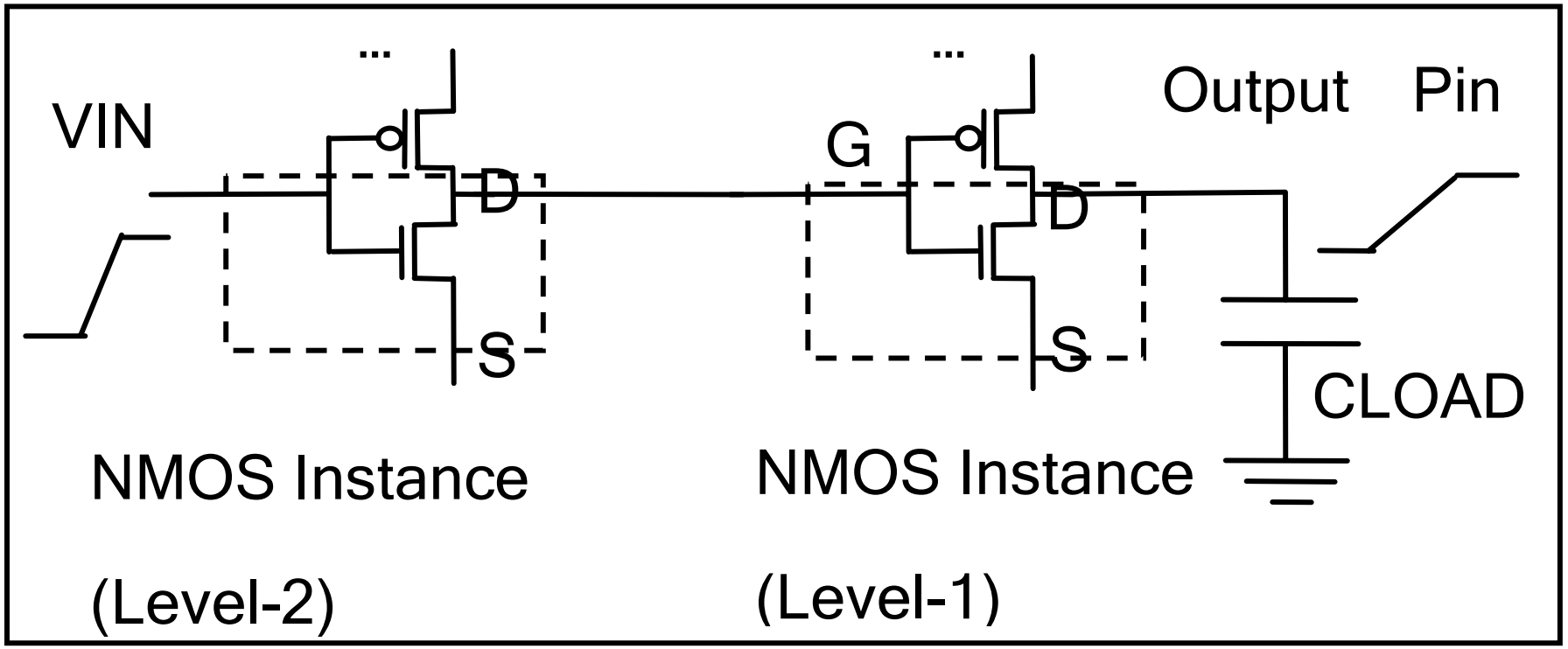
Input Cap (II): Level 2 Partial Circuit Extraction

- Level-2 Device Extraction:
  1. Loop all the input pins/IO pins and skip the special pins
  2. Loop all the level-1 device set
  3. If the level-1 cell type is an inverter, find out all of the devices connected to the output (source and drain) of level-1 devices. Disconnect the devices after level-2 by pulling appropriate voltage level HIGH (VCCA, VCC33A, etc) or Low (GND) with device naming (if no voltage level is specified by the designer)
  4. If the level-1 cell type is a transmission gate, then the level-2 device is a capacitor. One of the capacitor terminals connects to level-1 transmission gate. Ground the other terminals of level-2 device.

Output Cap Characterization

- Faraday uses hybridization methodology for output cap characterization due to the complexity of output circuits
- The hybridization includes interpolation, partial circuit extraction, and IO Instance based simulation
- Output cap needs forward and reverse trees to generate the library
- Differential Inputs are required for some IPs
- IO instance based simulation is used in PWM
- Full-chip simulation is applied to external digital output pins, DP and DN pins, in USB/OTG due to circuit complexity and designer request
- Transmission Gate is also found in data latch circuit for output pin
- Please refer to San Jose SNUG, 2005 for Hybridization Methodology

Output Cap: Double Inverter



Output Cap Partial Circuit Extraction

Output Cap: Level-1 Partial Circuit Extraction:

1. Loop all the output/IO pins and skip the special pins
2. Search for all the devices that have the source and drain connected to the output/IO pins. Build the level-1 device set.
3. Build the level-1 net set with nets connected to gates of level-1 devices

Output Cap: Level-2 Partial Circuit Extraction:

1. Loop all the output/IO pins and skip the special pins
2. Loop all level-1 net set
3. Search for the level-2 devices with source and drain connected to the level-1 net set. Build the level-2 device set.

Distributed SPICE Simulation

- Those testbench objects (input cap and output cap) are distributed / parallel run by all the available Linux machines at Faraday
- Those distributed running tasks are kept tracked by the testbench objects until all the simulations are done
- The testbench objects handle the distributed task status (Queues, Running, Suspend, Done), tool license, tool exit error (0-253) handlings, SPICE converge error, SPICE coding error, status and log file cleanup

Result Processing and Library Generation

- The Input cap is stored in *.mtN file (where N = 0, 1, 2, …) by HSPICE
- The following formula is used to interpolate the maximum capacitance for output cap at the slew rate of 1 nsec

$$MaxL_{i,\,lm} = L_{i,\,lm,\,j-1} + (L_{i,\,lm,\,j} - L_{i,\,lm,\,j-1}) / (SR_{i,\,lm,\,j} - SR_{i,\,lm,\,j-1}) * (SR_{i,\,lm,\,j} - 1.0)$$

- Where:

  $MaxL$: Maximum Loading Capacitance

  L : Loading Cap

  SR : Slew Rate

  lm : BC, TC, WC

  i : inout or input pin index

  j : Loading Capacitance / Slew Rate index

- Please refer to San Jose SNUG 2005 for Library Generation

Runtime and Accuracy Comparison (I)

Method	Runtime	Accuracy
Interpolation	< Seconds	~85%
Circuit Extraction Simulation	Seconds to Minutes	90% - 100%
IO Instance Based Simulation	Minutes to Hours	> 95%
Full-Chip Simulation	Hours to Months	100% or 0% if failed

Runtime and Accuracy Comparison (II): ADC Input Cap

FIP: Full IP Simulation, PCS: Circuit Extraction Simulation, LPE: Layout Parasitic Extraction, TC: Typical Corner, WC: Worst Corner, BC: Best Corner

Pin	Method	Corner	Input Cap (pf)	Runtime (s)	Accuracy
CLK	FIP	BC	0.2009	2814567.52	100%
CLK	CES	BC	0.1913	2.87	95.2%
CLK	FIP	TC	0.1870	2389748.37	100%
CLK	CES	TC	0.1693	2.42	90.5%
CLK	LPE	TC	0.192047	90.02	1.03%
CLK	FIP	WC	0.1806	2073361.24	100%
CLK	CES	WC	0.1680	2.35	93%

Runtime and Accuracy Comparison (III): ADC Output Cap

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FIP: Full IP Simulation, PCS: Circuit Extraction Simulation, TC: Typical Corner, WC: Worst Corner, BC: Best Corner

Pin	Method	Corner	Output Cap (pf)	Runtime (s)	Accuracy
DI0	FIP	BC	18.4865	2464756.21	100%
DI0	CES	BC	19.5033	1.08	105.5%
DI0	FIP	TC	6.98590	2687921.72	100%
DI0	CES	TC	7.23863	1.90	104.3%
DI0	FIP	WC	3.49277	2571362.31	100%
DI0	CES	WC	3.58009	1.82	102.5%

Conclusion (I): Faraday IP Under Characterization

No	IP	Description	No	IP	Description
1	ADC	Analog-to-Digital Converter	8	OSC	Oscillator
2	DAC	Digital-to-Analog Converter	9	PLL	Phase-Locked Loop
3	BG	Bandgap Voltage Reference	10	POR	Power-On High/Low Reset
4	CMP	Comparator	11	PWM	Charge Pump Circuit (Pulse Width Modulator)
5	DEL	Delay Cell	12	VDT	Voltage Detector
6	DLL	Delay-Locked Loop	13	USB/ OTG	Universal Serial Bus / On The Go
7	LVR	Low Voltage Differential Signal Receiver			

Conclusion (II)

- Device extraction and SPICE simulation are tested with 1500 test cases (by pin count) covering about 250 IPs including regular power and low power library for 0.25-, 0.18- and 0.13-micron technology
- The accuracy is around 90%-100% with selected IP.
- The proposed methodology cuts the run-time from several weeks/months to seconds/minutes