Fixing Antenna Problem by Synopsys SLE

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ABSTRACT

Antenna problems have existed in the chip manufacturing industry for more than one decade. It damages the devices and therefore reduces the yield during the wafer manufacturing. This paper describes three ways to fix antenna problems: (1) diode dropping, (2) jumper insertion, and (3) diode dropping with extension wires by using the Synopsys's SLE tool. Many tools try to solve the antenna problem using the router approach by putting jumper in the block level. It might causes extra delay by introducing the jumper. In the chip level, there jumper insertion approach is not suitable due to the chip hierarchy. Synopsys SLE drops the diode dynamically and add jumper insertion to solve the antenna problem successfully in both block level and chip level. The timing degradation effect is a big concern for the diode dropping. We have experienced a number of chips has the timing degradation after the diode insertion. Some investigation are presented in this study including the SPICE simulation and diode slicing. Those SPICE simulation result and diode slicing picture are provided to make sure it si working correctly. We finally find out the diode insertion should be avoided in the memory block or around the critical net, such as clock net. Basic principles of these methods are compared and results are presented. Diode structures, SPIC simulation, and diode slicing are also discussed in this paper.

1.0 Introduction

Antenna problems have existed in the chip manufacturing industry for more than one decade. In this paper, we present a systematic way to describe this problem by Teralogic tl850 chip and fix by using Synopsys SLE. tl850 is a High Definition TV (HDTV) chip designed by Teralogic, inc. and manufactured by Taiwan Semiconductor Manufacturing Corporation (TSMC). This paper includes the following topics:

- Antenna explanations
- Antenna ratio definitions
- Antenna check out violation by verification tools
- Comparison of diode dropping and jumper insertion methods
- Diode characterizations and structures
- Diode dropping, jumper insertion, and diode dropping with extension wires
- Design Rule Checking (DRC) and Logic Versus Schematics (LVS) checking
- Chip-level protection diode dropping for blocks
- Diode timing delay checking by RC extraction and SPICE Simulation
- Diode structure verification by slicing

2.0 Flow Chart for Fixing the Antenna Problem

The overall flow for fixing antenna problems by dynamic diode dropping and jumper insertion is shown in Figure 1.

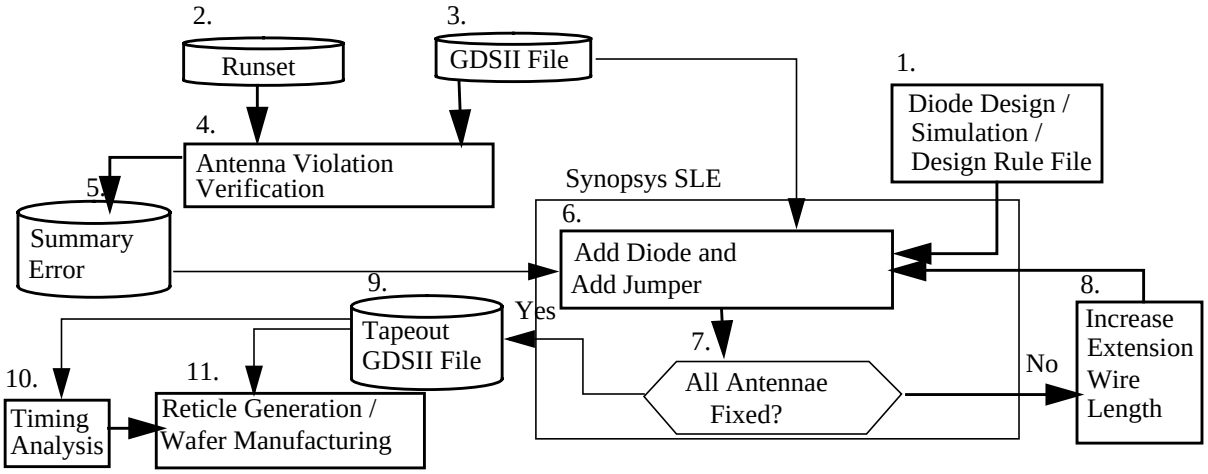

Figure 1. Overall Flow for Fixing Antenna Problems

3.0 Antenna Explanation

During wafer manufacturing, if the wire connected to the input port is too long, the accumulated charges (caused by UV light, etc.) on the long wires that are near the input port damage the device. This reduces the wafer manufacturing yield. Analogies for antenna problems during wafer manufacturing and normal operation are shown as Figures 2 and 3. During manufacturing, diodes which do not connect to any power source are floating devices. These floating devices can be used to discharge accumulated charges on the long wires during wafer manufacturing.

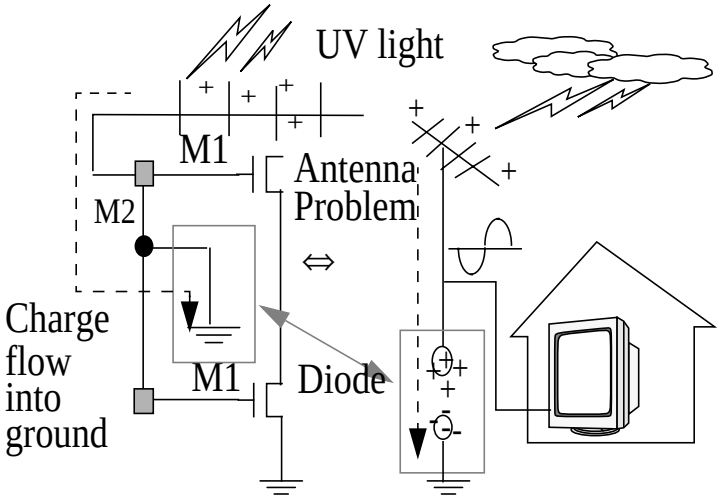

Figure 2. Analogy of antenna problem during manufacturing

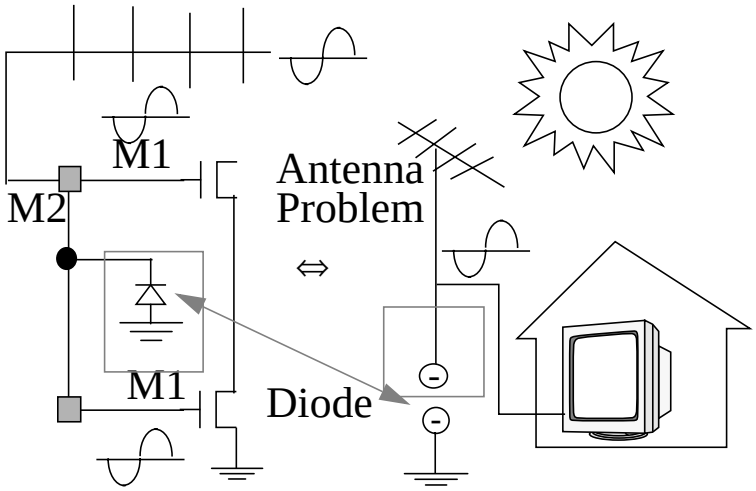

Figure 3. Analogy of antenna problem during circuit normal operation

When wafers are manufactured, these diodes are no longer used as discharging devices. They become reverse bias diodes and act like an open circuit. With very little parallel capacitance to input ports during normal operation, the transmitted signals can maintain their integrity.

In Figures 2 and 3: M1 denotes Metal 1s, which are always small pieces of metal. M2 denote Metal 2s, which may be small or big pieces of metal. Diode locations should be as close to input ports as possible. Diodes are dropped on Metal 2.

4.0 Antenna Ratio Definition

The antenna ratio of a particular net is defined as:

$$\text{Antenna Ratio} = \frac{\text{Total Wire Area}}{\text{Total Input Port Area}}$$

Note that the antenna rule violation definition is foundry and process specific. For example, TSMC design rules ($0.18\ \mu m$) uses total perimeter area of metal wire vs. gate area.

Where:

Total Wire Area: The total area of a wire starts from the input port before reaching the topmost routing layer. (For example, for a five metals process, a wire is started from Metal 1 to Metal 2, and then to Metal 3 (metal 4 and 5 is not used for this example). For this wire, Metal 3 is the topmost layer for this wire. The total wire area is counted from Metal 1 to Metal 2. This is the area that accumulates charges and damages the input port. The area after the topmost layer to the output port is irrelevant to the antenna ratio, since the charges in this area are discharged to the output gate once the connection is established during wafer manufacturing.) The area of Metal 3 is not counted, since once Metal 3 is finished during manufacturing, the whole wire is connected. The charge flows into the output port due to the output port's low impedance.

Total Input Port Area: The total input port area is the total area of the input ports that are connected with this selected net. Figure 4 shows the antenna ratio for Metal 3. The total area of the metal is the summation. The total input port area is the summation of ports 1, 2, and 3.

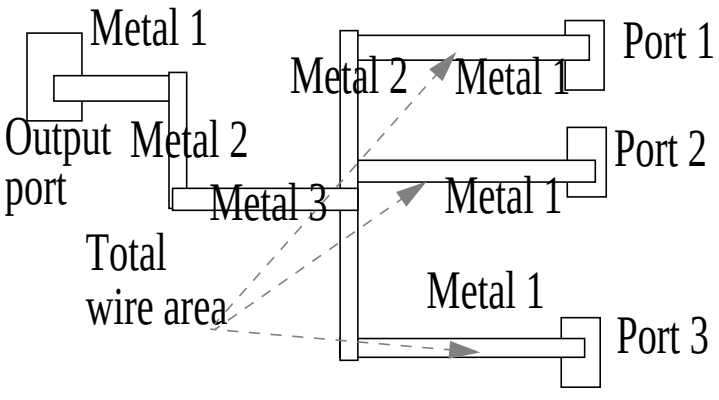

Figure 4. Antenna ratio for metal 3

5.0 Antenna Rule Checking

Use layout verification tools to check antenna errors. The error reports should contain the following information:[4]

1. The violated position of the wire: The (x, y) position of which the antenna ratio of the wire exceeds the specified antenna ratio, e.g, 400.
2. Error flattened: Since the wire is connected to every module, it should not be hierarchical. Therefore, the errors should be flattened. Set the error flattened option if the tool is a hierarchical verification tool. If the verification tool is not hierarchical, you do not need to set this option.
3. Chip level: At the chip level, since each block's antenna problem is fixed, we only need to consider the interconnection among the blocks. Since the whole chip may be very large (e.g., 1 million gates), to check the whole chip antenna violation might take a long time (several days on a SUN® Ultra-SPARC workstation). If the chip is too big, chip-level antenna violations can be avoided by putting a protection diode on every input pin. This can be done very quickly, in general within few seconds to one minute. If the chip is not too big and run time is acceptable, then antenna violation checking and dynamic diode dropping and jumper insertion approaches can still be used.

6.0 Three Solutions for Antenna Problem

The three solutions proposed to solve the antenna problem are described as follows:[2, 3]

1. Router options: Break signal wires and routes to upper levels. This reduces the charge amount for each net during manufacturing. This is called the "jumper approach."
2. Embedded protection diode: Add protection diodes on every input port for every standard cell. However, these protection diodes consume the cell area resources and increase manufacturing costs. Even though the diodes are not necessary, these diodes are always embedded.
3. Dynamic dropping diode after placement and route: Fixing only the wire with the antenna violation which will not waste routing resources. During wafer manufacturing, all the inserted diodes are floating (or ground). Since the input ports are high impedance, the charge on the wire flows through the insert floating/ground diode (composite) instead of flowing into the input port. One diode can be used to protect all input ports that are connected to the same output ports. If the chip is too dense and the tool cannot find the space to drop the diode, jumpers can also be inserted or extension wires near the input ports can be added for diode insertion. In the operation mode, these diodes act like reverse diodes. Within the clamp voltage range, the signals are preserved with very small leakage currents as shown in the Figure 7.

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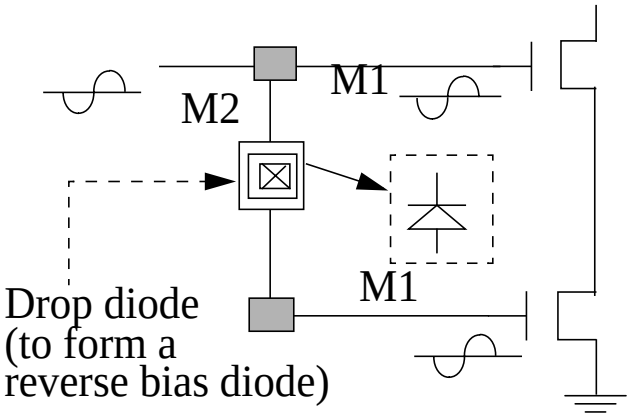

Figure 5. Examples of tool dropping a diode

7.0 Diode Characterization

Figure 6 presents the P-diode's characterization. Three diode sizes (0.25, 1.0, and 25.0 μm^2) are compared. They all have the same clamped voltages (e.g., -10 V). We determined the appropriate diode based on the DRC rule for each process. In this paper, we use the $1.1\mu m \times 1.1\mu m$ for $0.35\mu m$ process.

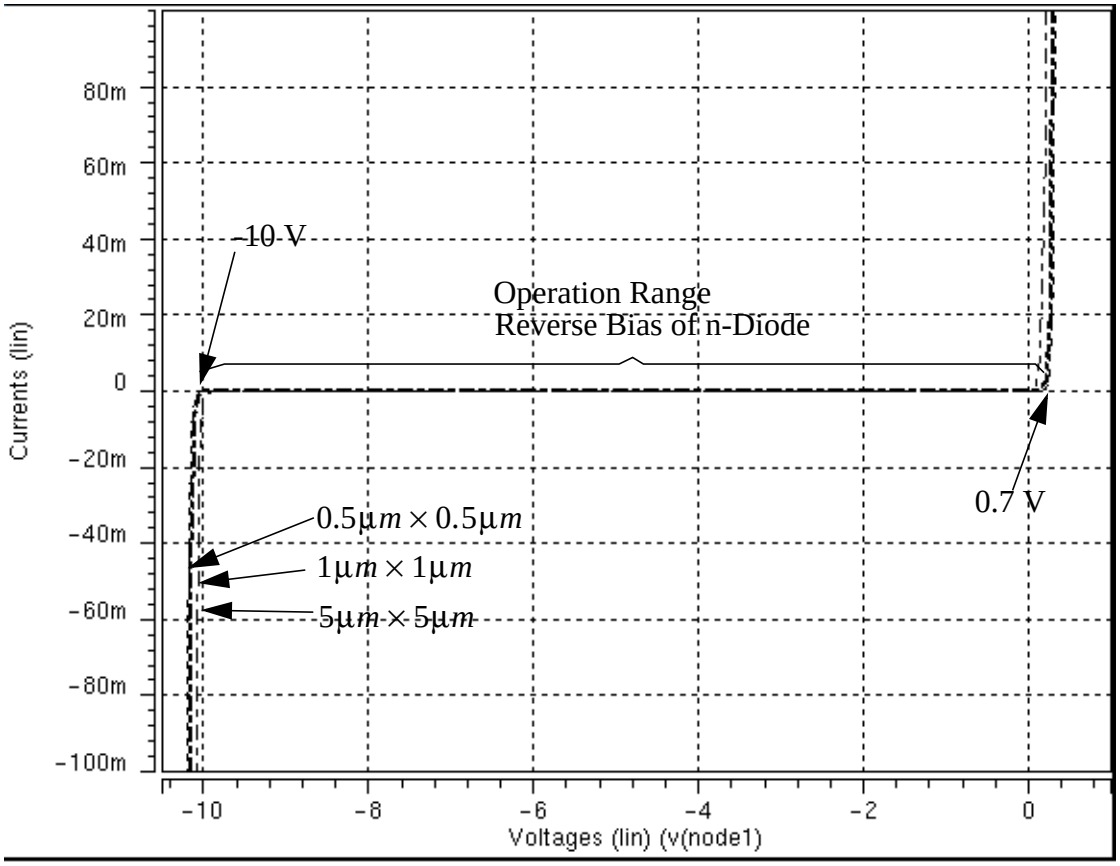

Figure 6. Reverse bias of N-Diode operation diagram

The SPICE simulation results show that the P-Diode has the same clamped voltage (e.g., -10 V) as the N-Diode shown in Figure 6; except the leakage currents are different. The leakage currents, shown in Figure 7 for the $0.35\mu m$ process, are as follows:

1. P-Diode 225 *nA* and 290 *nA* for diode area $0.5\mu m \times 0.5\mu m$
2. P-Diode 900 *nA* and 1.2 μA for diode area $1\mu m \times 1\mu m$
3. P-Diode 22.5 μA and 29 μA for diode area $5\mu m \times 5\mu m$.

From Figure 6 and 7, we observe that the signal transmissions will not be destroyed or degraded during normal operations.

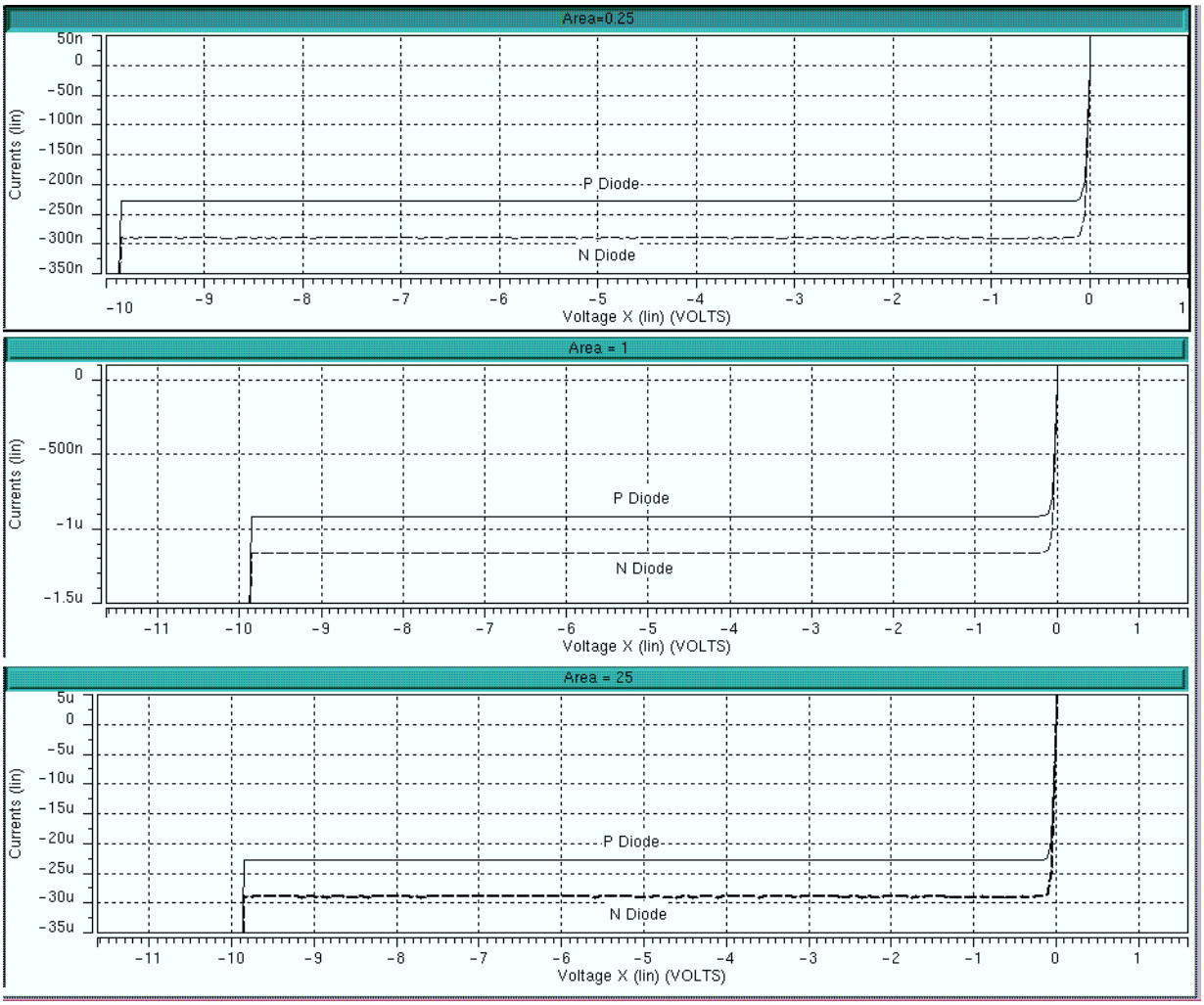

Figure 7. P-Diode and N-Diode leakage currents with diode size 0.25, 1.0, and 25.0 μm^2

8.0 Comparison

Table 1 shows the comparison of the three approaches used to solve antenna problems.

Table 1: Comparison of three approaches

Impact	Jumper	Embedded Diode	Dynamic Dropping Diode
Cell Area	No	Yes	No
Routability/Chip Size	Yes	Yes	No
Completeness	No	No	Yes
Timing	Most	More	Least

9.0 Timing Impact

The following calculation shows the timing comparison between jumper and diode insertion approaches.[1]

1. Jumper Insertion: Each jumper needs at least two vias. In the 0.35 μm technology, via resistance is around 10 Ω. In 0.25 μm technology or above, via resistance is around 100 Ω or more.

$$R' = R_{\square} \times \frac{L}{W} \cong 60\text{m}\Omega \times \frac{L}{W} \cong 3 - 10\Omega$$

Where:

$R_{\square}$: The sheet resistance of metal.

R' : The resistance of metal with length L.

2. Diode Insertion:
   Diode Capacitance

$$C' \cong C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{34.5\mu\text{F}/\text{cm}}{0.4 \times 10^{-5}\text{cm}}$$

$$= 0.86\text{fF}/\mu m^2$$

   Where:

   C : Capacitance of the original wire

   C' and C_{ox} : Capacitance of the inserted diode

   ε_{ox} : Permittivity of diode

t_{ox}: Thickness of the diode

Time Constant Formula:

$$\tau = (R + R') \times (C + C')$$

$$= R \times C \times \left(1 + \frac{R'}{R}\right) \times \left(1 + \frac{C'}{C}\right)$$

Where:

τ: Time delay of metal with diode/via.

For 0.35 μm design with 350 μm wire, the formula is as follows:

$$\frac{R'}{R} = \frac{5}{60} \gg \frac{C'}{C} = \frac{1fF}{10pF}$$

From the Time Constant formula, we know the timing delay is negligible.

In Figure 8, set the following parameters for very long wire:

VIN: 200 MHz input signal from output port

R1: 120 Ω for long wire resistance

C1: 2.4 pF for long wire capacitance

R2: 10 Ω for short wire resistance

D1: N-Diode with area $1.1\mu m \times 1.1\mu m$

C2: 0.2 pF for short wire capacitance

R3: 5 Ω for short wire resistance

VDD: 3.0 V

C3: 1.0 fF for CMOS capacitance

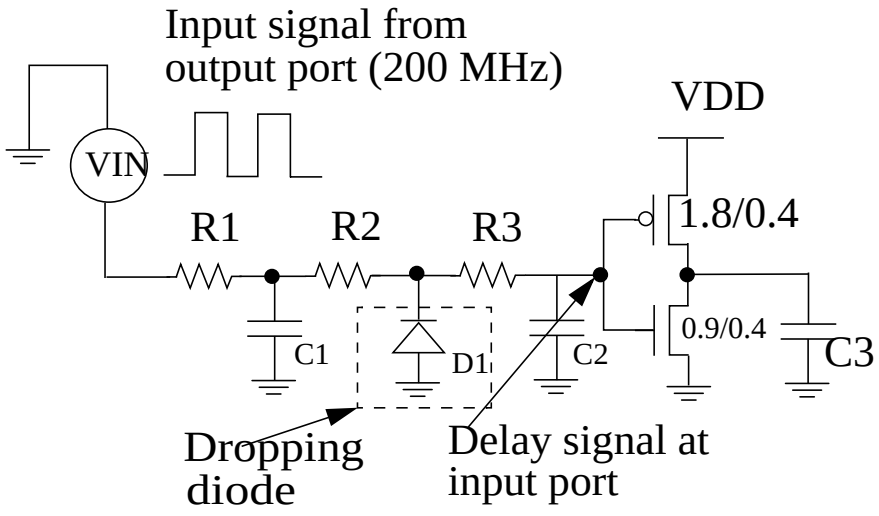

Figure 8. Timing simulation of diode insertion

Figure 9 shows the simulation circuits of timing delay of a very long wire with a 200 MHz input signal (from the output port). This very long wire with an N-Diode (P-Diode) or without a diode

has about 0.3 *nsec* timing delay. The dropping diode's timing effect is negligible. The forward diode has the same time delay as the reverse diode but it drops the maximum amplitude of the signals at some voltage level. Therefore, the forward diode cannot be used to solve the antenna problem.

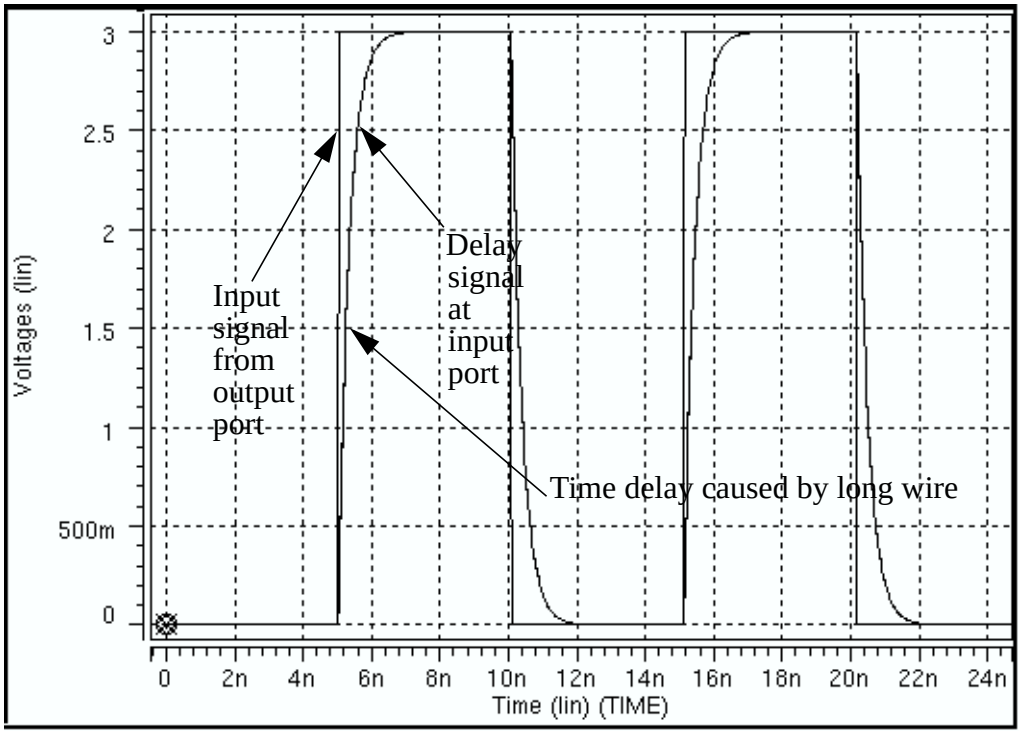

Figure 9. Timing delay simulation of a very long wire with N-diode

Figure 10 shows the result of a medium long wire with the following configurations:

VIN: 200 MHz input signal from output port

R1: 17 Ω for long wire resistance

C1: 5.3 pF for long wire capacitance

R2: 1.0 Ω for short wire resistance

D1: N-Diode with area $1.1\mu m \times 1.1\mu m$

C2: 0.125 pF for short wire capacitance

R3: 0.5 Ω for short wire resistance

VDD: 3.0 V

C3: 1.0 fF for CMOS capacitance

The total wire's timing delay is $0.1ns$. The timing delay caused by this N-Diode is $0.0001ns$, which is negligible. In the real design, the wire's patterns are much more complicated, but the inserted diode's effect is similar.

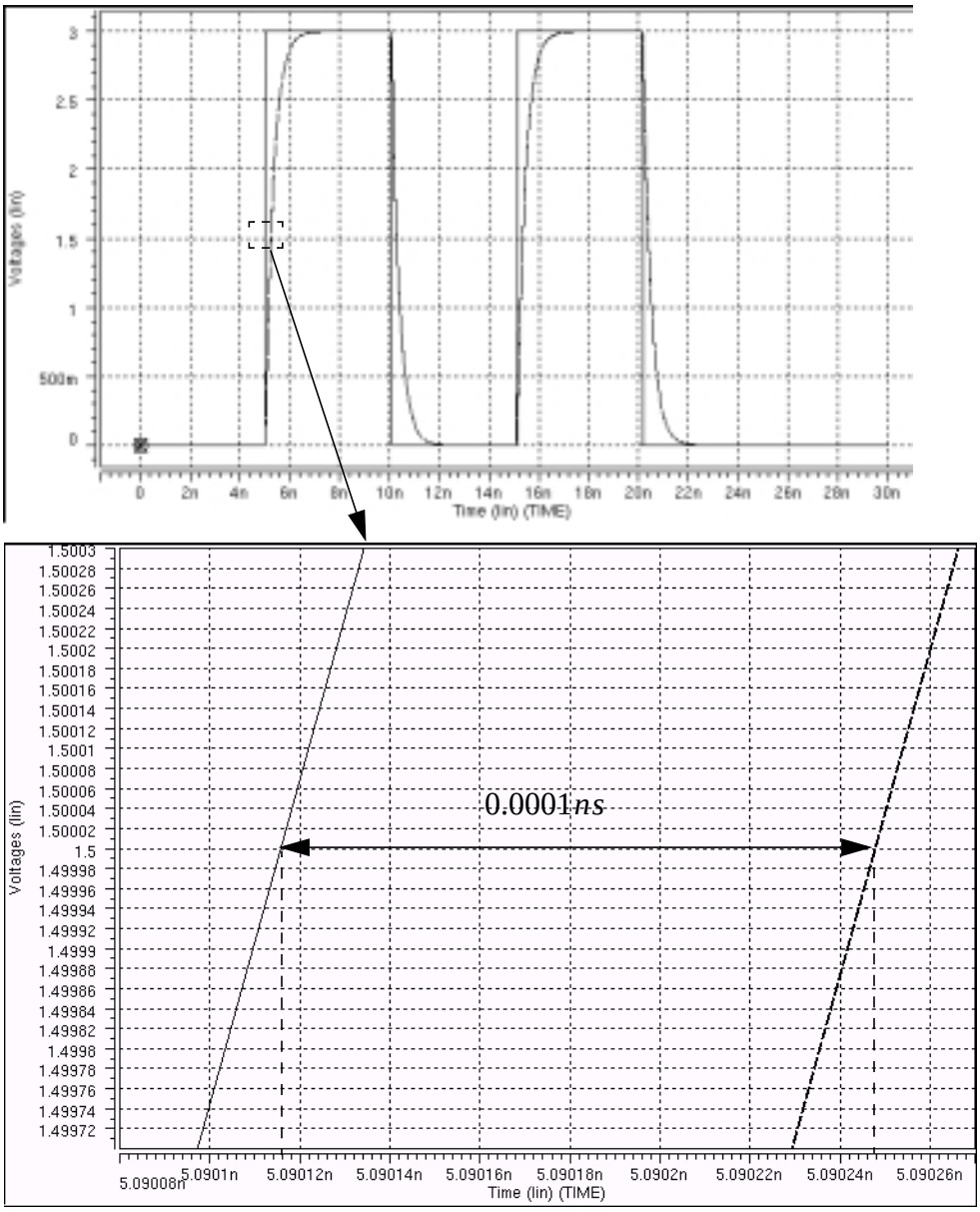

Figure 10. Timing delay simulation of a medium long wire N-diode

10.0 Advantages of The Dynamic Diode Dropping Approach

The designers may insert diodes within a given physical design tool flow. SLE's approach is post P&R. Its main advantage, flow-wise, are:

1. works with users' existing physical design flow
2. the only way to solve antenna violations for mixed-signal / analog designs. Since analog circuit design can not routed with P&R tool.

Figures 8, 9, and 10 show the dynamic diode dropping approach to have the following advantages:

1. Least timing degradation (better than embedded)
2. Least waste of chip area during manufacturing
3. Least impact on routability. The jumper only approach is unusable on very dense chips.

11.0 Diode Structure

Figure 11 shows a top view of diode structure for the 0.35 μm process. A diode is composed by a via, Metal 1, and Composite. Dropping an N-Diode on top of $N^+ - IMP$ within P-Substrate forms a reversed bias diode during normal operation, as shown in Figure 13. Forward diodes degraded the signals; whereas, reverse diodes can preserve the signals during normal operation. Figures 12 and 13 show the reverse bias of a P-Diode and an N-Diode for the P-MOS and N-MOS processes, respectively.

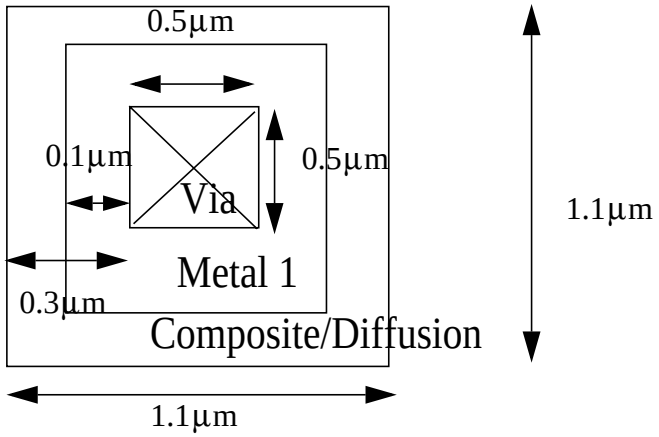

Figure 11. Top view of diode structure

Two kinds of dropping diodes are described as follows:

1. N-Diode with N-IMP (N^+ implant)
2. P-Diode with P-IMP (P^+ implant)

Figures 12 and 13 show dropping a P-Diode for the P-MOS Process and an N-Diode for the N-MOS Process, respectively. Note that transistor part are not shown in both diagrams. NIMP (N^+ implant), PIMP (P^+ implant), and DIFF are the fundamental mask layers. PDIFF and NDIFF are derived from these fundamental mask layers.

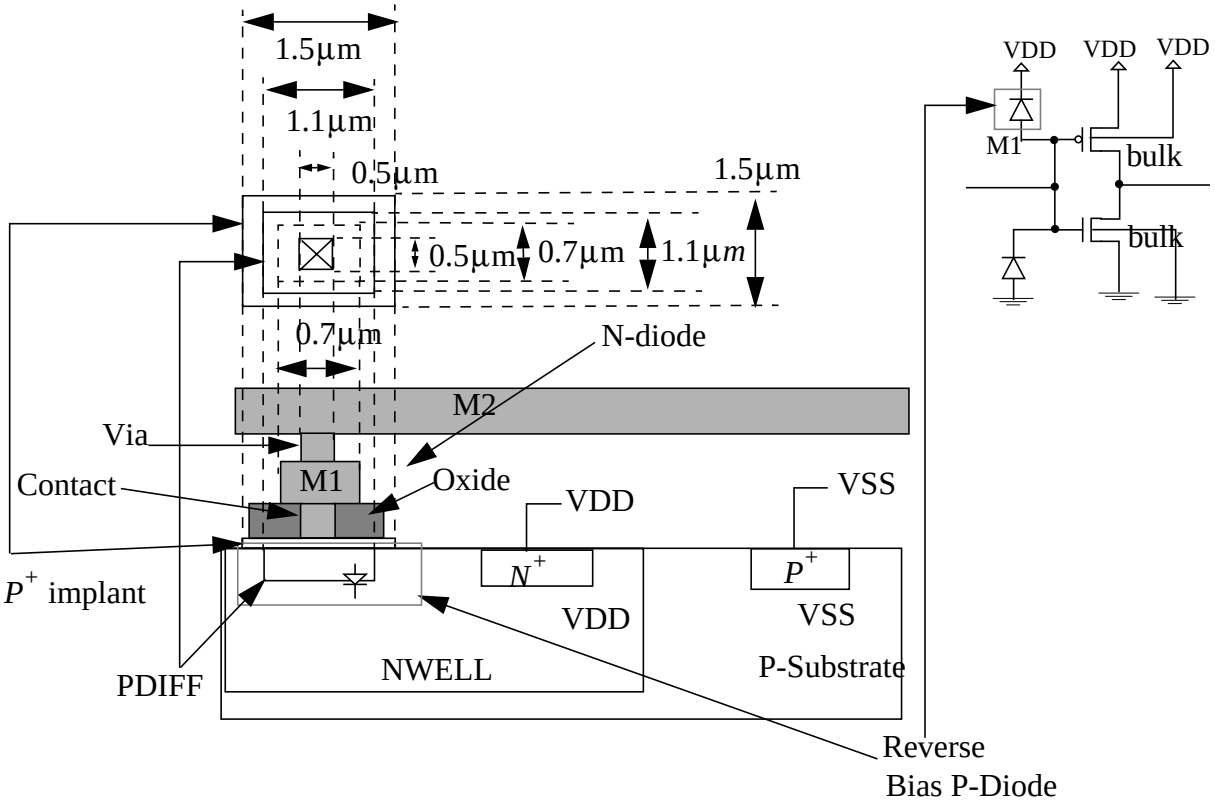

Figure 12. Dynamic dropping P-Diode (PN protection diode) structure for P-MOS Process

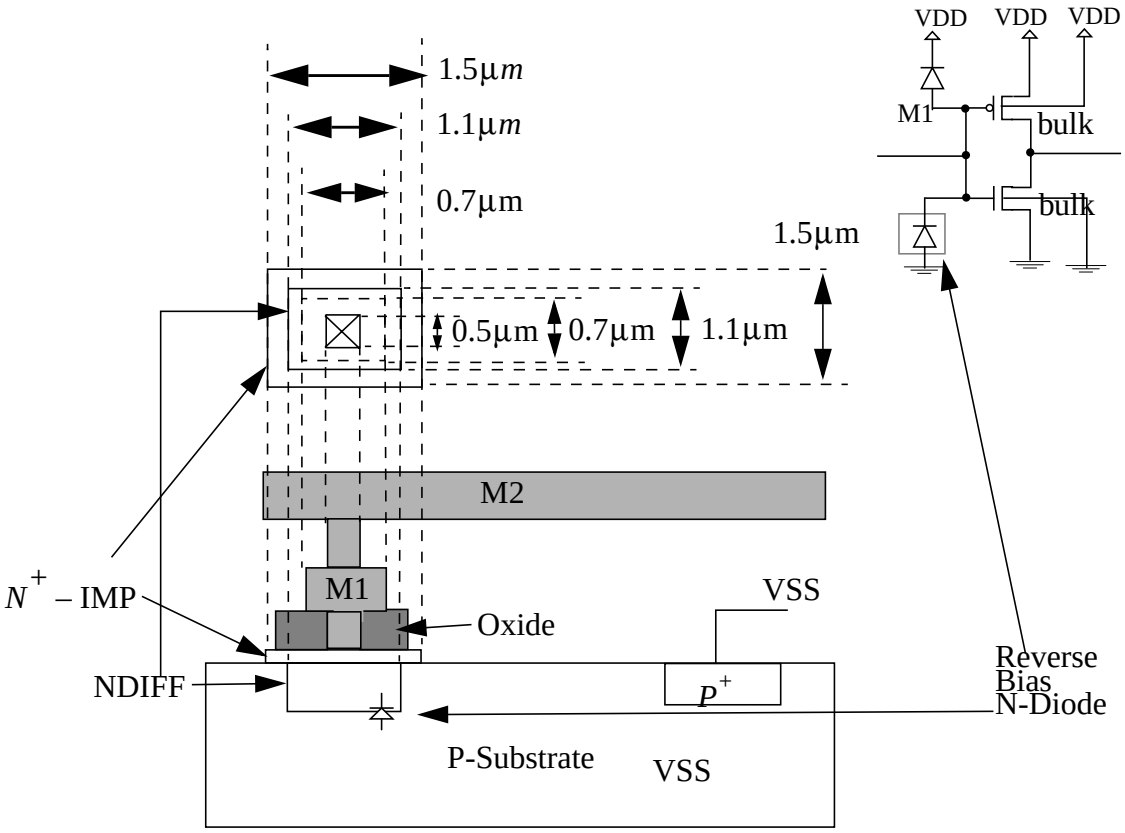

Figure 13. Dynamic dropping N-Diode (NP protection diode) structure for N-MOS Process

12.0 Procedures for Fixing Antenna Violations

The procedure for fixing antenna violations are illustrated below:[4]

1. Make sure the rule file specifications follow your process design rules and DRC rules.
2. Bring up the tool for antenna fixing.
3. Create the new library or open the existing library.
4. Stream in GDSII file.
5. Import the P-Diode and the N-Diode from the GDSII format or create them from scratch.
6. Open the top level cell.
7. Drop the diodes (P-Diode or N-Diode) without extension wires according to the rule files specified in Step 1.
8. Insert the jumper for the rest of the violation (if there is no space to drop a diode).
9. Increase the extension wire to accommodate a bigger area, e.g, 5 µm .
10. (Repeat Step 9 until all the violations are cleaned.)
11. Save the design in a GDSII format.

12. Visually check the diode insertion one-by-one. Search and trace all the diodes which are inserted. Examine the diode structure, location of dropped diodes, and make sure the diodes touch the right layers.

Figure 14 shows a Teralogic tl850 design which fixes antenna violations by dynamic diode dropping and jumper insertion. For dense designs, it is hard for tools to find the space to drop the diodes. The extension wire gives more space for diode dropping. The extension wire's width is very important for the design rule. If the extension wire width is too small, it causes notch errors. The right wire has a bigger width (the same as the diode width) and will not cause any DRC error. Figure 15 shows a diode connected to an extension wire.

Figure 14. Antenna fixed by diode dropping and jumper insertion

13.0Dynamic Diode/Jumper Insertion Results

Table 2 shows some results of 0.35 μm technology. The specification of a maximum antenna ratio is 400 without diode insertion, and the maximum ratio is 5000 with diode insertion. Both design examples in Table 2 are approximately one-quarter of a million gates. Here, we define the dense design as core utilization of more than 90% and the sparse design as core utilization of less than 50%.

For the dense design example, the original number of antenna violations for Metal 3 is 154. After diode dropping, the number of violations for Metal 3 is reduced to 21. After adding jumpers, the

violations for Metal 3 are reduced to 3. Finally, using 20 μm extension wires to drop the diode, the antenna violations are clean. Note that in the topmost metal (e.g., Metal 4), there never are antenna violations. Since after the wire is connected, the charge discharges into the output port. Normally, Metal 1 also has no antenna violations. This is because Metal 1's resources are occupied by standard cells. Therefore, there is very limited space for the router to generate the antenna problem. Metal 2 violations are very easy to fix, since the tool can always find the space to drop a diode. Metal 3 violations are difficult to fix due to the limited space resources.

For some designs with limited routing resources (e.g., when only three metals are used), core utilization is low (e.g., 49%). These designs have lots of space to insert diodes, and most of the violations can be fixed after the first run of diode dropping.

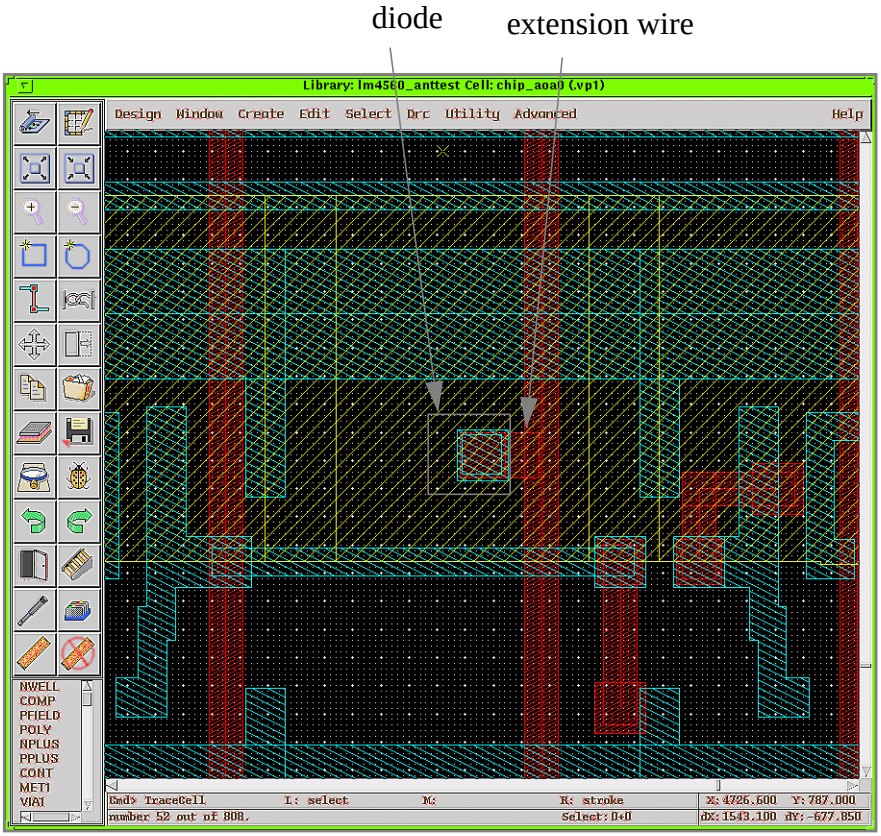

Figure 15. Diode insertion with wire extension

Table 2: Dynamic diode and jumper insertion

Design names	Violation	Diode insertion without extension wires	Add jumper	Diode insertion with 20 μm extension wires
Design 1: dense design	M4: 0 M3: 154 M2: 23 M1: 0	M4: 0 M3: 21 M2: 0 M1: 0	M4: 0 M3: 3 M2: 0 M1:0	M4: 0 M3: 0 M2: 0 M1: 0
Design 2: sparse design	M4: 0 M3: 788 M2: 521 M1: 0	M4: 0 M3: 1 M2: 0 M1: 0	M4: 0 M3: 0 M2: 0 M1: 0	N/A

14.0RC Extraction and SPICE Timing Simulation (Optional)

We need to perform the SPICE analysis to understand the timing impact after the diode insertion. The following steps are used to get the delay information from SPICE.

1. Perform the critical path and longest path from Synopsys Prime Time.
2. Select a path, for example, longest path, starting from one flip-flop (register) and terminated at the other flop-flop (register).
3. Get the RC extraction information, *i.e.*, Standard Delay Format (SDF) information by performing the RC analysis.
4. Extract the selected path RC information including sun-node.
5. Insert the diode into the closest node by examining the layout's diode inserted position by Synopsys SLE.
6. Set the data input and clock waveforms for the triggering the starting register in the selected path.
7. Perform the SPICE analysis by comparing the timing delay before diode insertion and after diode insertion.

The timing impact is negligible.

15.0Diode Slicing

The purpose of the diode slicing is to make sure that the diode that inserted do not cause any leakage current and timing degradation. Figures 16 and 17 show the cross-section of a diode. Figure 16 shows a cross-section of an N-Diode just before entering into the tungsten plug (contact). The diffusion stain (the dark black area on N-COMP) shows that the diffused junction is big enough. Figure 17 shows the same N-Diode on a different die through the center of the tungsten plug. The

N-COMP area is not stained. Figures 16 and 17 show that the contact is touching the N-COMP area correctly.

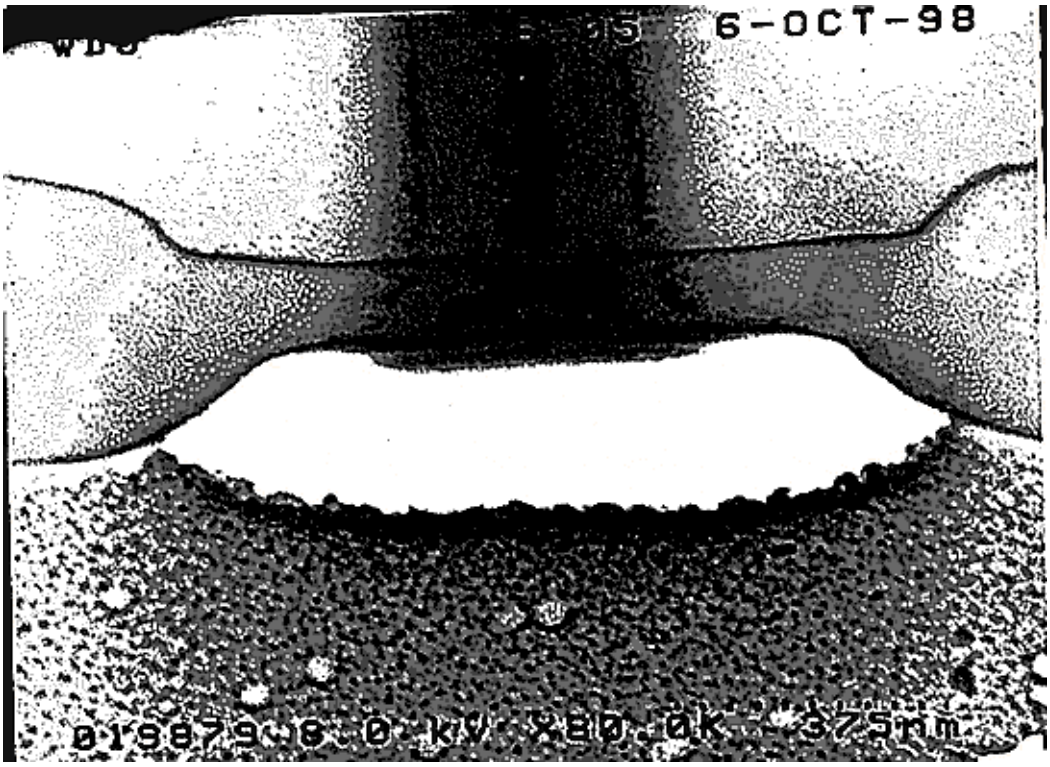

Figure 16. Cross-section of contact before entering into the tungsten plug

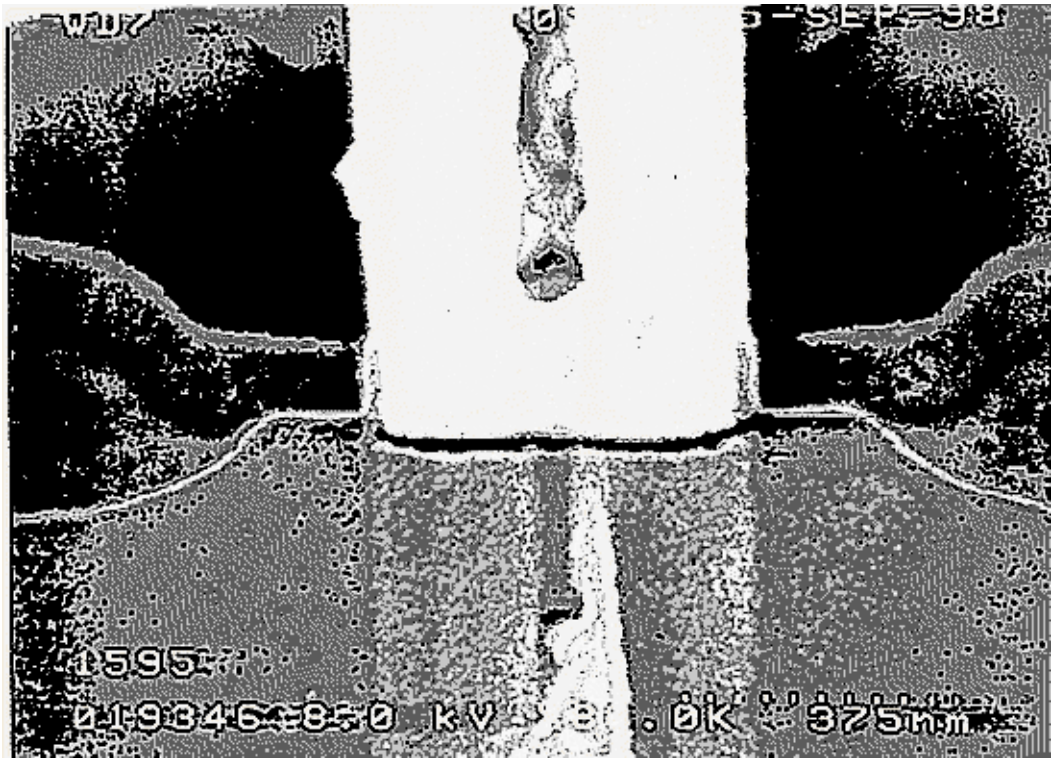

Figure 17. Same contact on a different die through the center of the tungsten plug

16.0 Conclusions and Recommendations

For dense designs (core utilization of more than 90%), dynamic diode dropping, jumper insertion, and dropping diodes with extension wires are three approaches which can be used to solve antenna violations. For design engineers, try to loosen up core utilization 5% to 7%, in order to leave some margin for diode and jumper insertion approaches.

For sparse designs (core utilization less than 50%), diode dropping alone is flexible enough to solve antenna problem. The three approaches proposed in this paper can be used successfully to solve most antenna violation problem.

This article do not consider the effect of diode insertion for clock net and memory blocks. Since the clock net is balanced tree structure, diode insertion will affect the skew and timing degradation problem. Therefore, diode insertion to clock net and memory block are not recommended. The SLE can be improved to avoid the diode insertion for memory block and clock net.

This paper's approach can be applied to both block level and top level's antenna fixing. Timing delay can be verified from the RC extraction and SPICE tools. The timing delay caused by diode insertion is within 0.02% for critical net (the longest nets in design, such as clock net). DRC and

LVS are verified after fixing antenna problems. If the tool does not generate the transistor level netlist, diode insertion can not be checked. In LVS checking, just check for short circuits only.[4]

17.0 Acknowledgments

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