Basic IP Characterizations: Static Powers & I/O Capacitances

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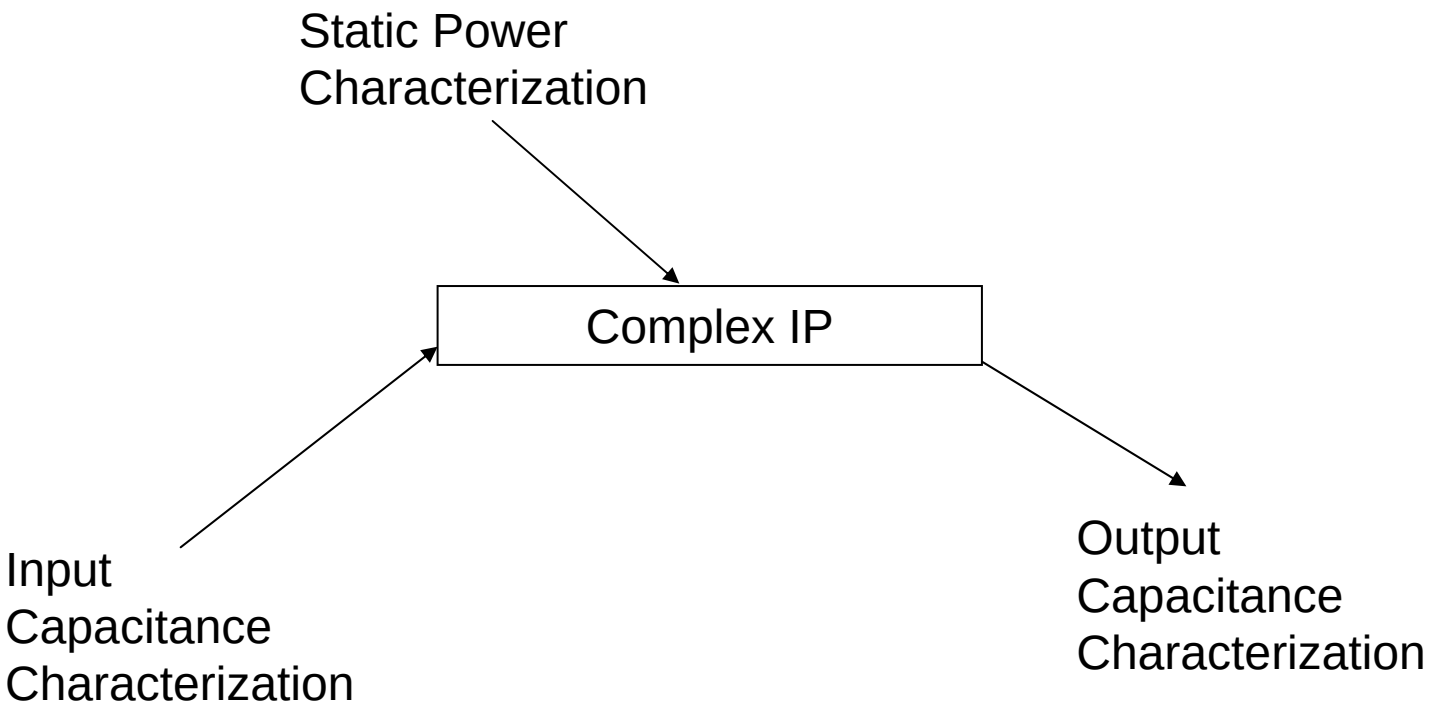
Outlines of The Presentation

1. Scope of Basic IP Characterization
2. Current Challenges of Characterizing Complex IP's
3. Abstract, Highline, and Flow of The Proposed Solution
4. Details of New Static Power Characterization
5. Details of New Input/Output Capacitance Characterization
6. Summary
7. Q and A

Static Power, and Input/Output Capacitance Characterizations



Current Problems of Characterizing Complex IP's

1. Becoming impractical or even impossible to characterize static powers due to state explosion.

   $f(n) = O(2^n)$ for state-dependant leakages,
   while n is the number of input pins

2. Lack of automation for both static power and I/O capacitance characterizations.

3. Single entry result (state independent) of static power in Liberty Library does not meet the synthesis tool requirements.

Proposing Reduction Methodology

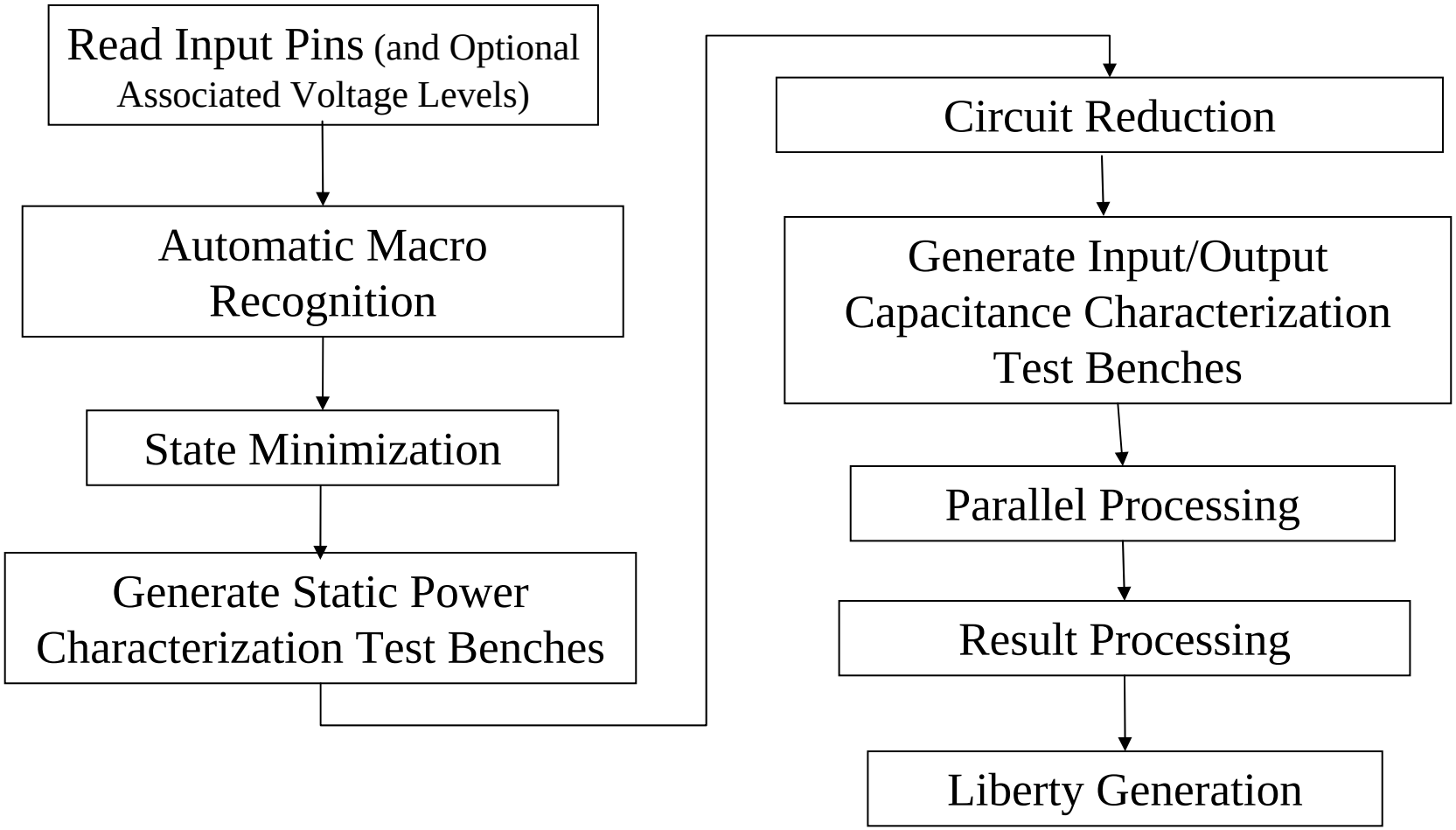
- Static (or leakage) Power Characterization:
  Reducing irrelevant input pins, with
  Automatic Macro Recognition and
  Knowledge-based State Reduction.

- Input / Output Capacitance Characterization:
  Reducing irrelevant circuits, with
  Graph Algorithm for Partial Circuit Extraction.

The Reduction Methodology Is Validated with 2,000+ IP's

No	IP	Description	No	IP	Description
1	ADC	Analog-to-Digital Converter	8	OSC	Oscillator
2	DAC	Digital-to-Analog Converter	9	PLL	Phase-Locked Loop
3	BG	Bandgap Voltage Reference	10	POR	Power-On High/Low Reset
4	CMP	Comparator	11	PWM	Charge Pump Circuit (Pulse Width Modulator)
5	DEL	Delay Cell	12	VDT	Voltage Detector
6	DLL	Delay-Locked Loop	13	USB/ OTG	Universal Serial Bus / On The Go
7	LVR	Low Voltage Differential Signal Receiver			

The New IP Characterization Flow



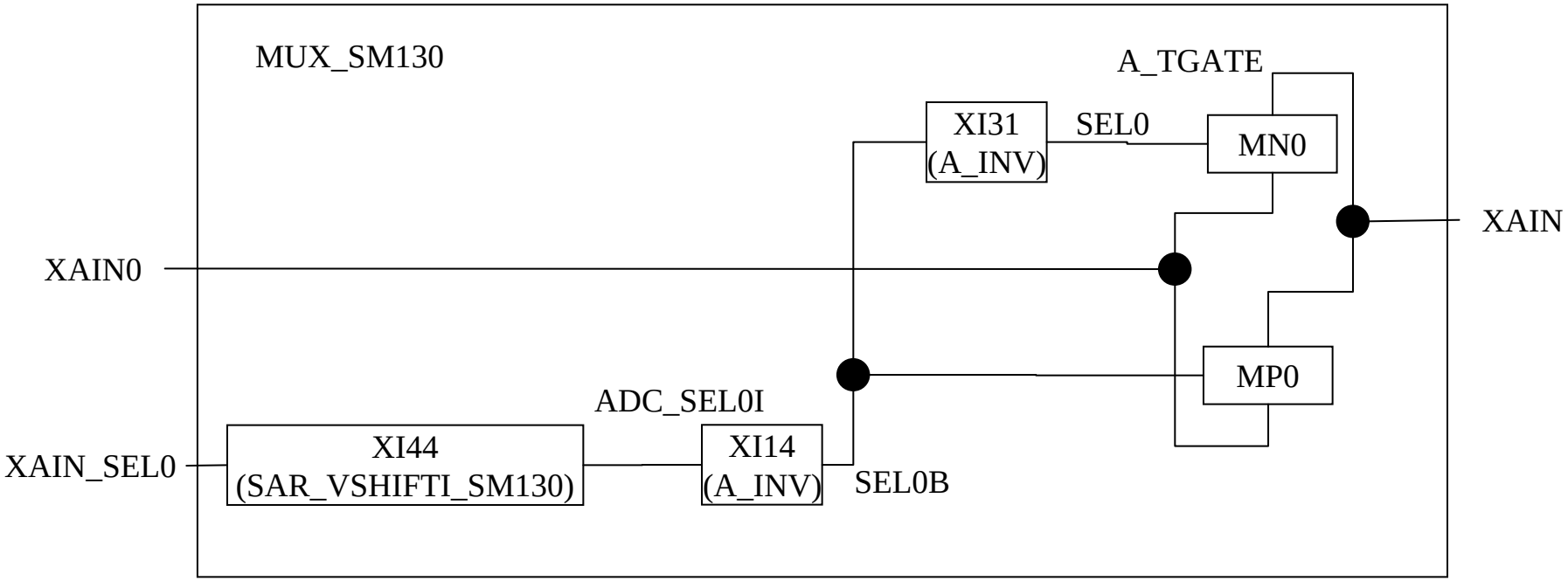
Static Power Characterization with Automatic Macro Recognition

- Head off state explosion, by removing irrelevant inputs before test bench generations.
- Provide complete state-dependant static power information.
- Improve convergent rate from 60's % to 100 %, with automatic fixes of floating nodes.

Leakage Power Attributes in Liberty Library

```
cell (DAC010HA0L) {
    cell_leakage_power : 10.974;
    leakage_power () {
        when : “!VREF * !CLKIN * !PD * !VSL";
        value : 3.2169e+07;
    }
    leakage_power () {
        when : “VREF * !CLKIN * !PD * !VSL";
        value : 10.974;
    }
    …
}
```

"Automatic Macro Recognition" Identifies The MUX in The ADC



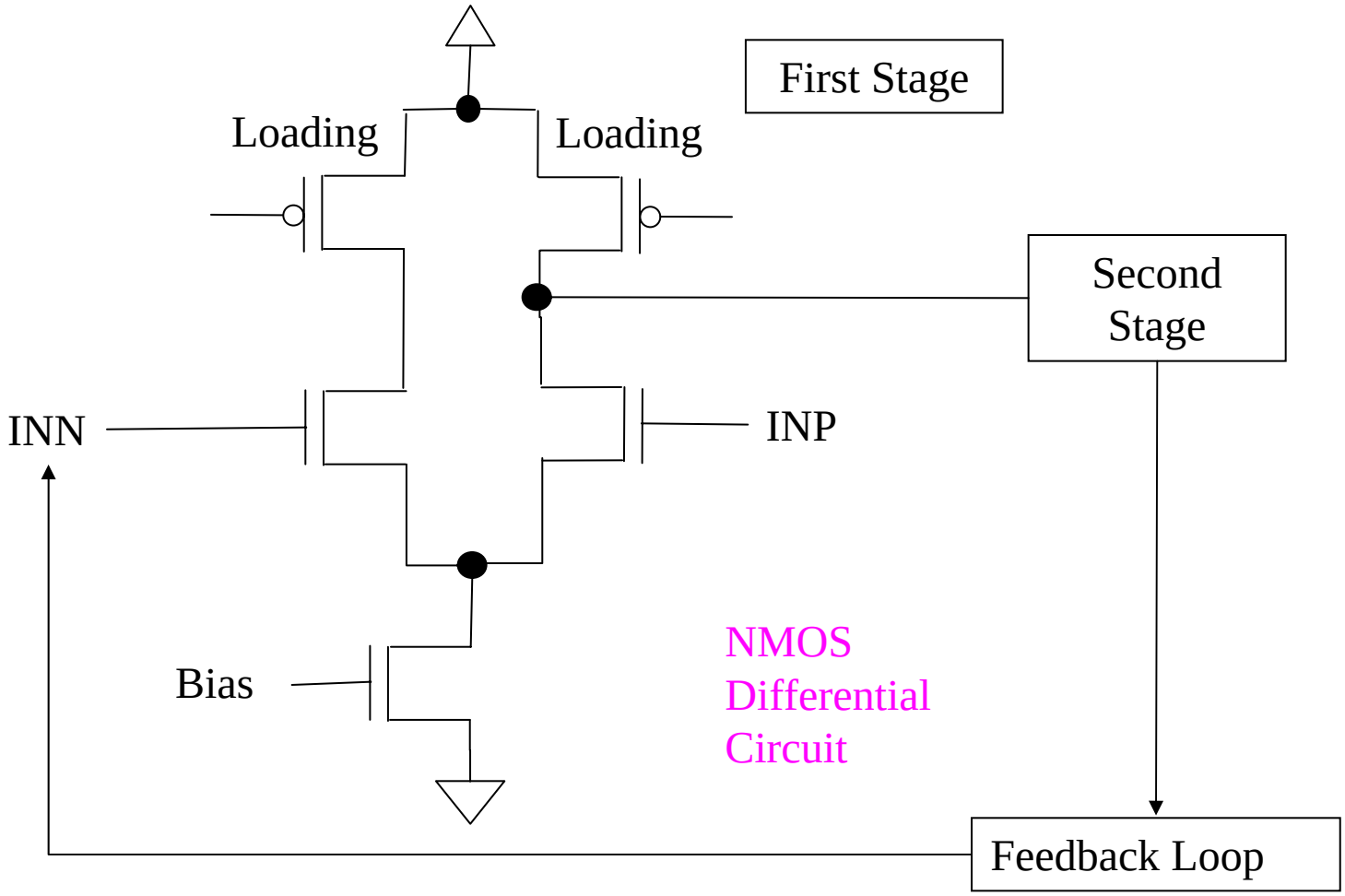
MUX features:

1. One Transmission Gate - A_TGATE
2. One pair of select signals - SEL0 and SEL0B)

Merge Redundant States to Dramatically Reduce Run Time

Methodology	Input Pin	Total Test Bench	Execution Time
Traditional characterization with Initial Conditions	16 inputs: COMP, RSET, VREF, CLKIN, DACIN[0-9], PD, VSL	196,608 (= 2 ** 16 * 3) *3 to cover best, nominal and worst cases	More than 3 hours for a test bench. More than 589,824 hours to complete.
Automatic Macro Recognition	4 inputs: VREF, CLKIN, PD, VSL	48 (= 2 ** 4 * 3) *3 to cover best, nominal and worst cases	Parallel run. Finished within 1 minute for all test benches and 48 entries in liberty.

Automatically Fixes Floating Nodes



I/O Capacitance Characterization with Netlist Extraction

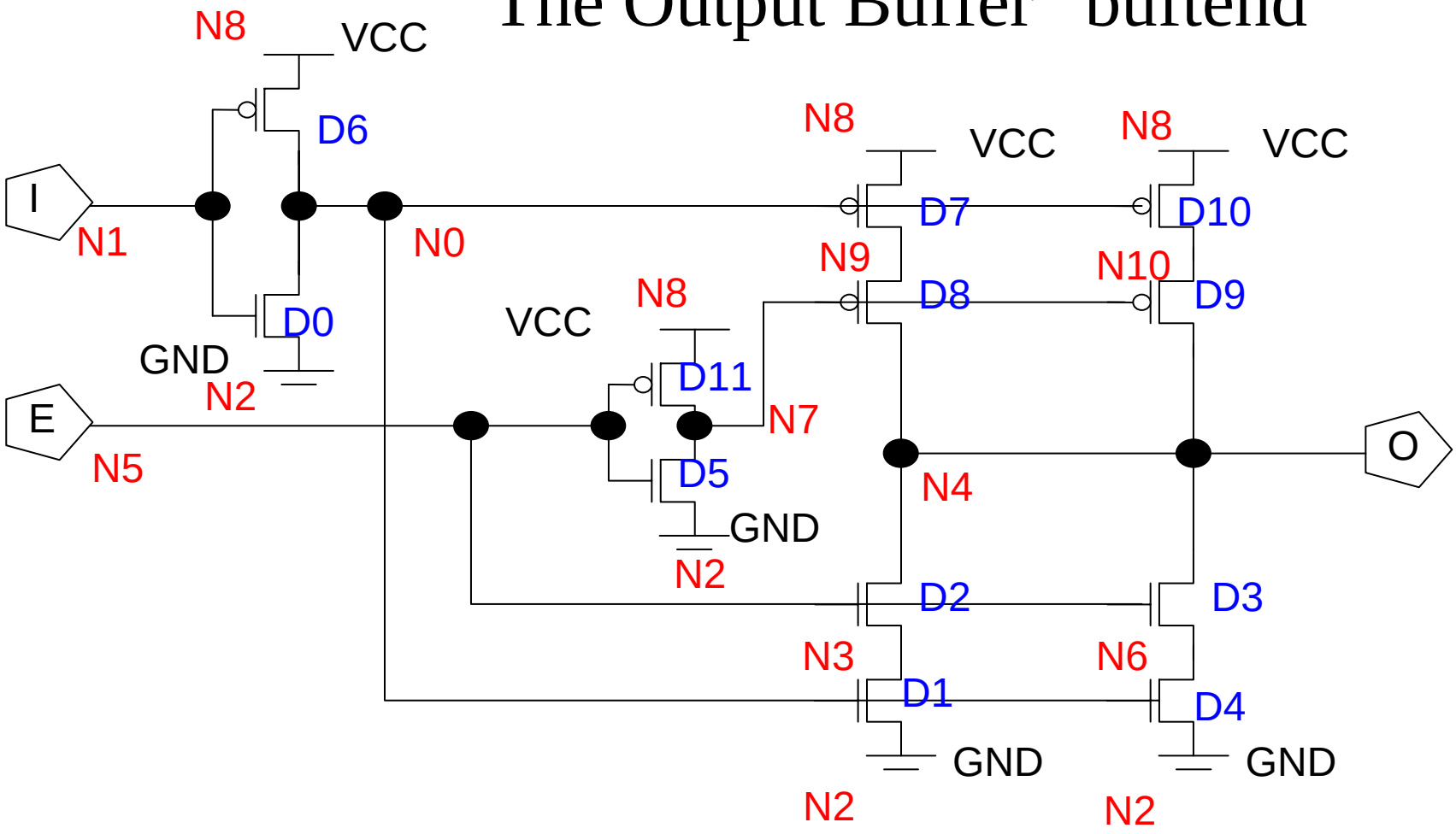
- Accelerate characterization time, by using partial netlist.
- Extract partial netlist, by traversing SPICE netlist with a graph algorithm.
- Achieve 100+ times of characterization throughput, on complex IP's.

Input/Output Capacitance Attributes in Liberty Library

```
cell (DAC010HA0L) {
    pin (VREF) {
        capacitance   :  1 ;
        …
    }
    pin (Z) {
        capacitance   : 0.1    ;
        …
    }
    …
}
```

Extracting Netlist with a Graph Algorithm

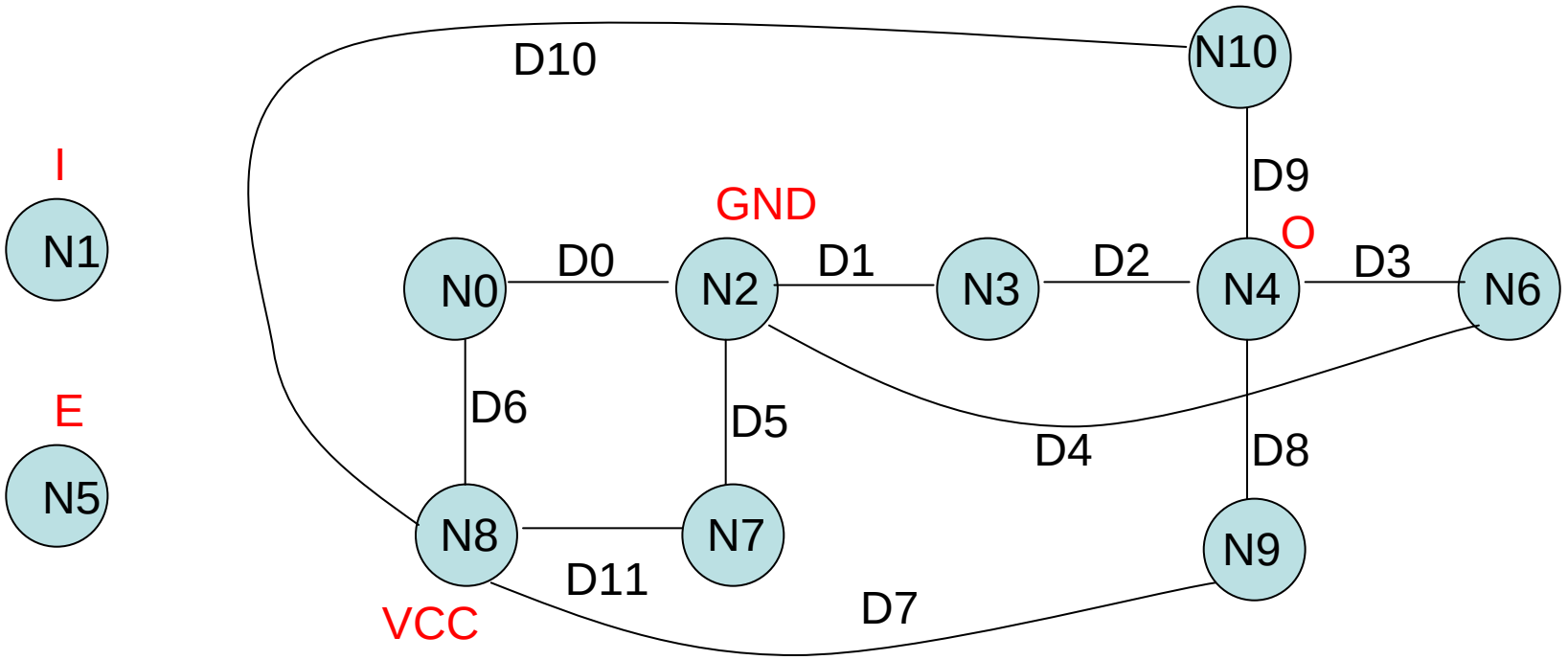
The Output Buffer "buftehd"



Graph Representation of buftehd

- Apply graph theory to traverse the connectivity.
- Consider each node as a vertex. Each device as an edge connecting the vertices. Then, buftehd is a graph.
- To view transistors as edges, ignore the gates. See source and drain as the connected vertex.

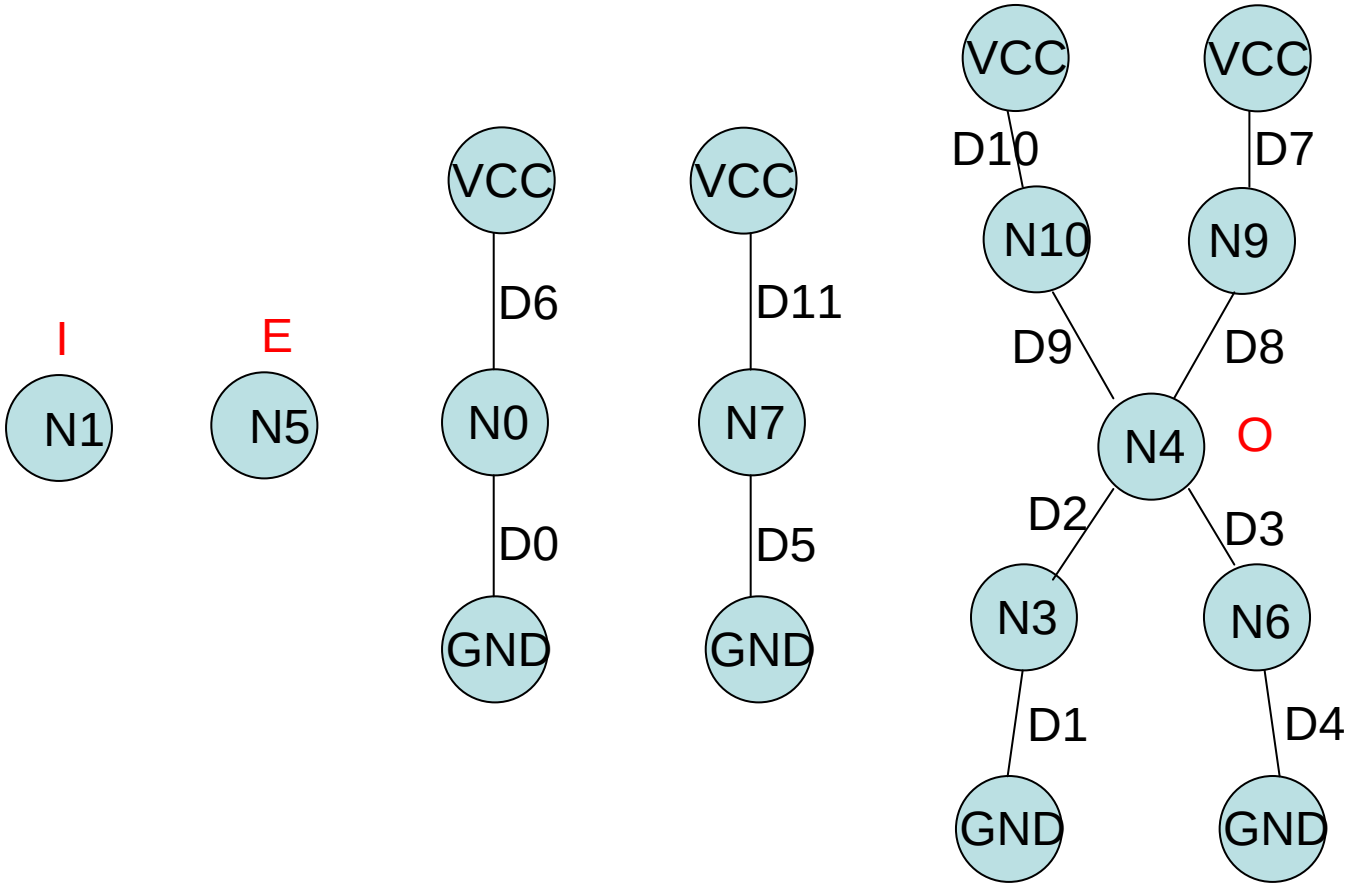
The buftehd Graph



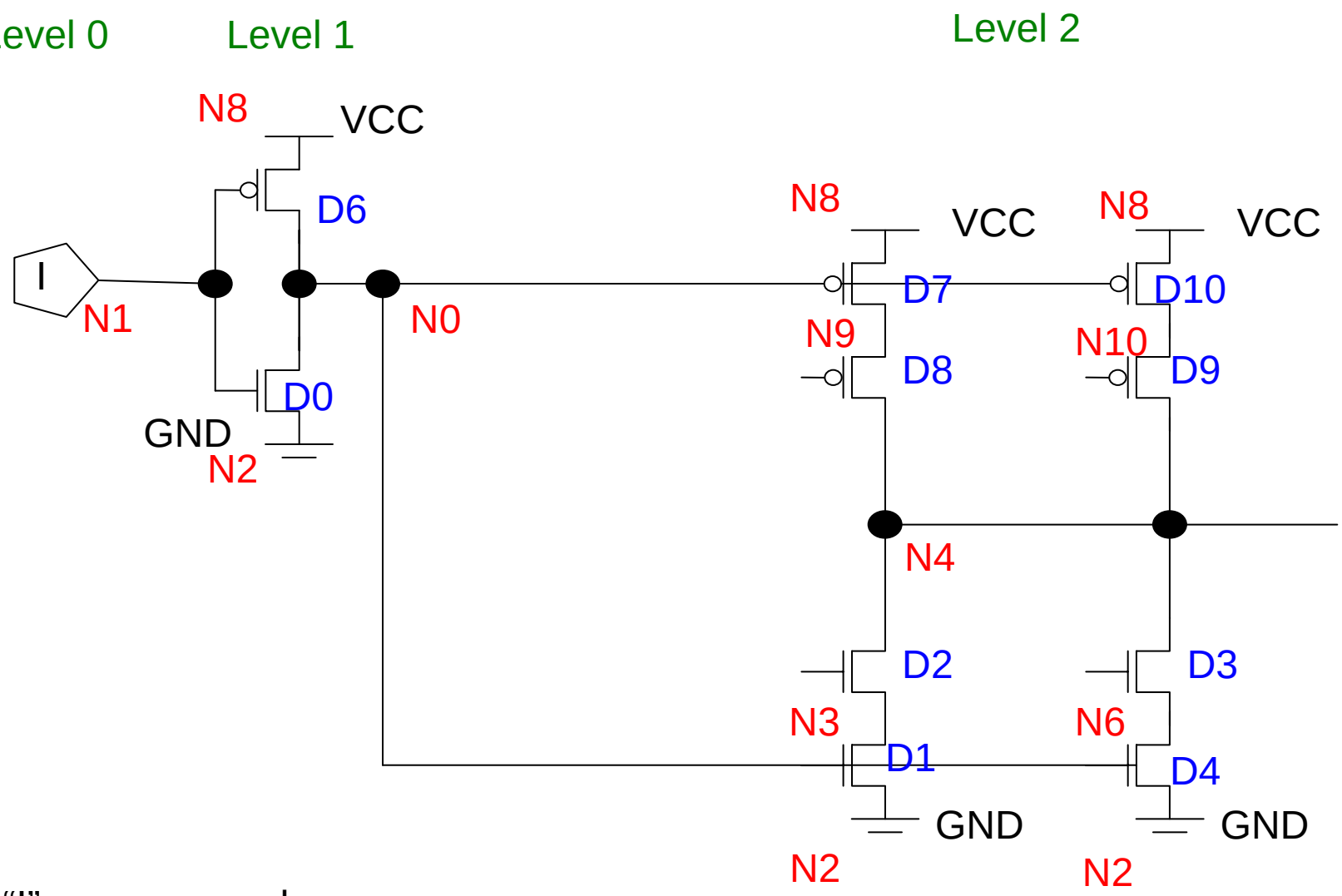
Connected Components of The buftehd Graph

- Use VCC and GND as the articulation points, to divide the graph into connected components.

Connected Components of buftehd, with VCC and GND as cut vertices



Extracted Netlist for Input/Output Capacitance Characterization



Input “I” as an example.

Summary

1. Complex IP's require new methodology to characterize.

2. Exponential performance improvement is achieved for characterizing both static powers and input/output capacitances.

3. State reduction is for static power characterizations.

4. Netlist reduction is for I/O capacitance characterizations.

5. The reduction methodology delivers an accuracy of within 1%, compared against traditional methods.

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