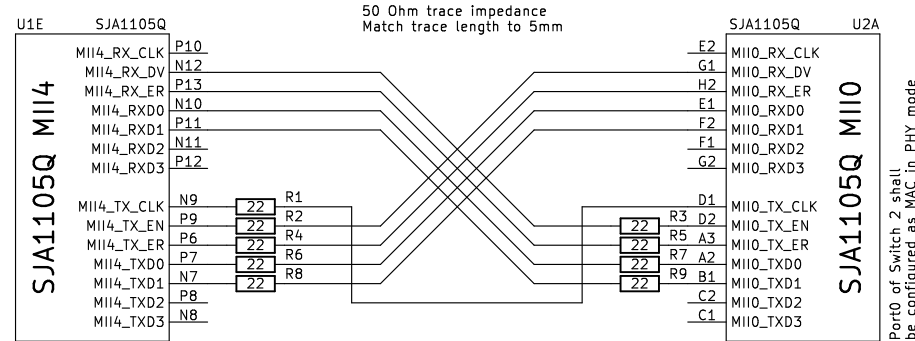
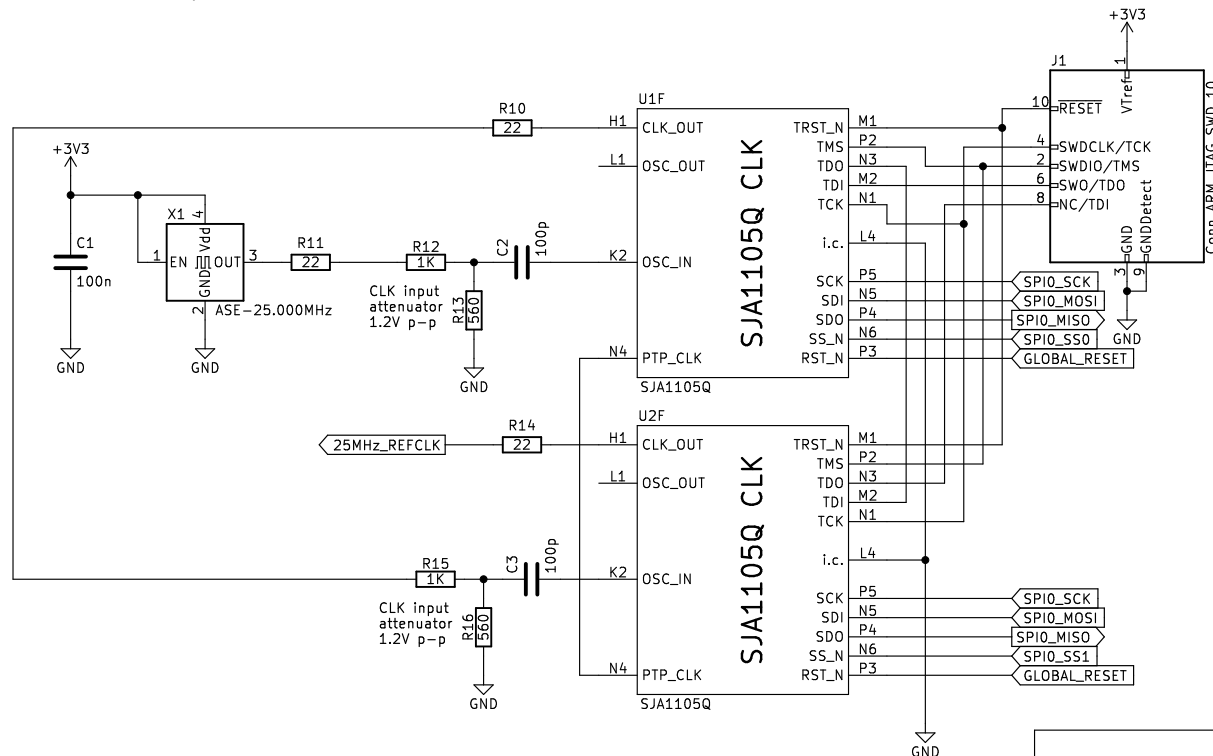


Inter Switch Connection RMII<-->RMII 100MBit



Switch Clock Generation / JTAG Debug



Keep clock lines less than 14 cm, according to "1/3 rise time" rule.
<https://www.altium.com/documentation/altium-designer/interactively-routing-controlled-impedance-pcb>

The ASE-25.000MHz has a 2.8ns rise time, hence 0.93ns trace delay, which equals to 14cm trace length on FR4.

https://github.com/peterheinrich/Open_10Base-T1L_Switch
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Sheet: /SJA1105Q Switch/
File: SJA1105Q_Switch.kicad_sch

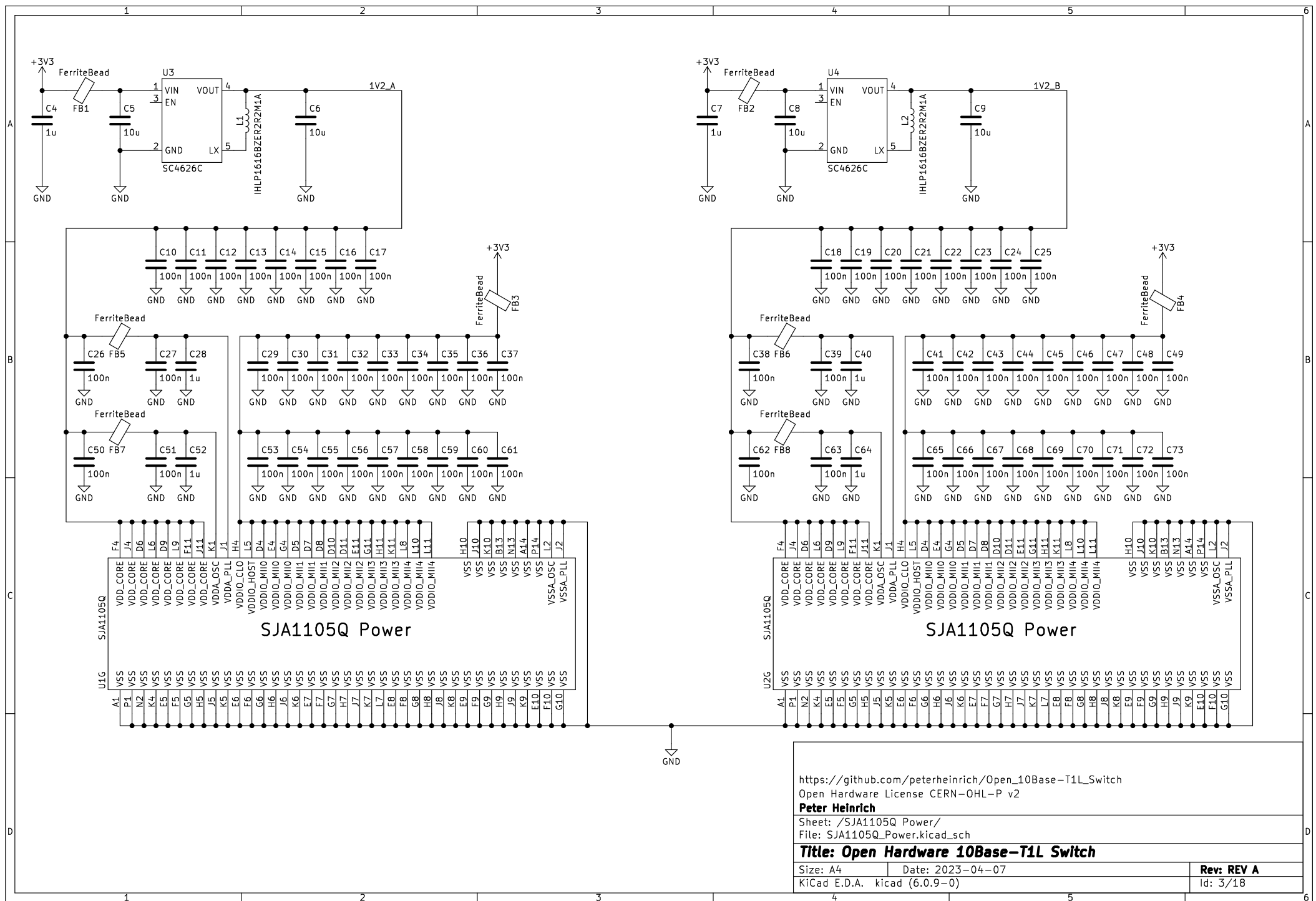
Title: Open Hardware 10Base-T1L Switch

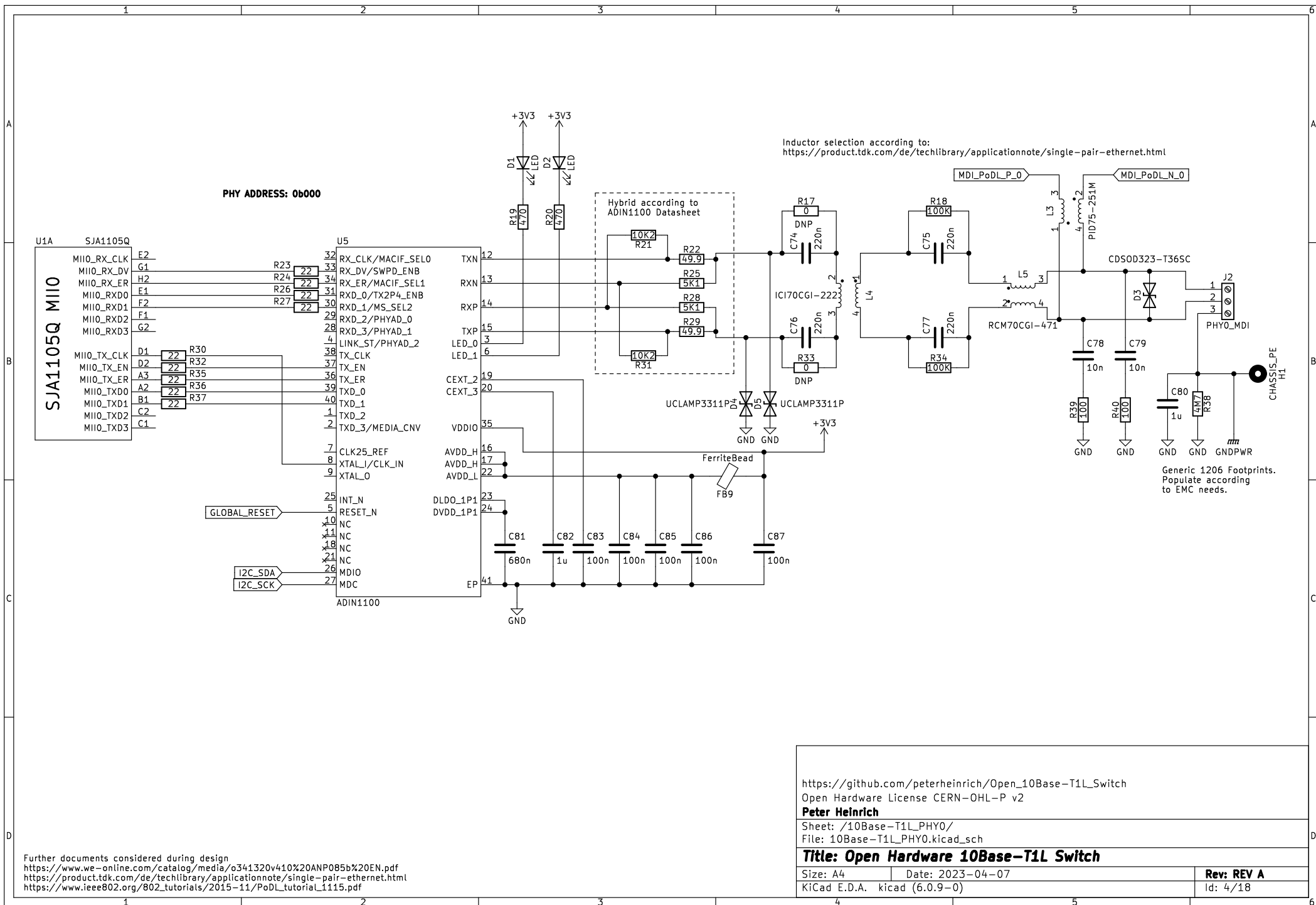
Size: A4 Date: 2023-04-07

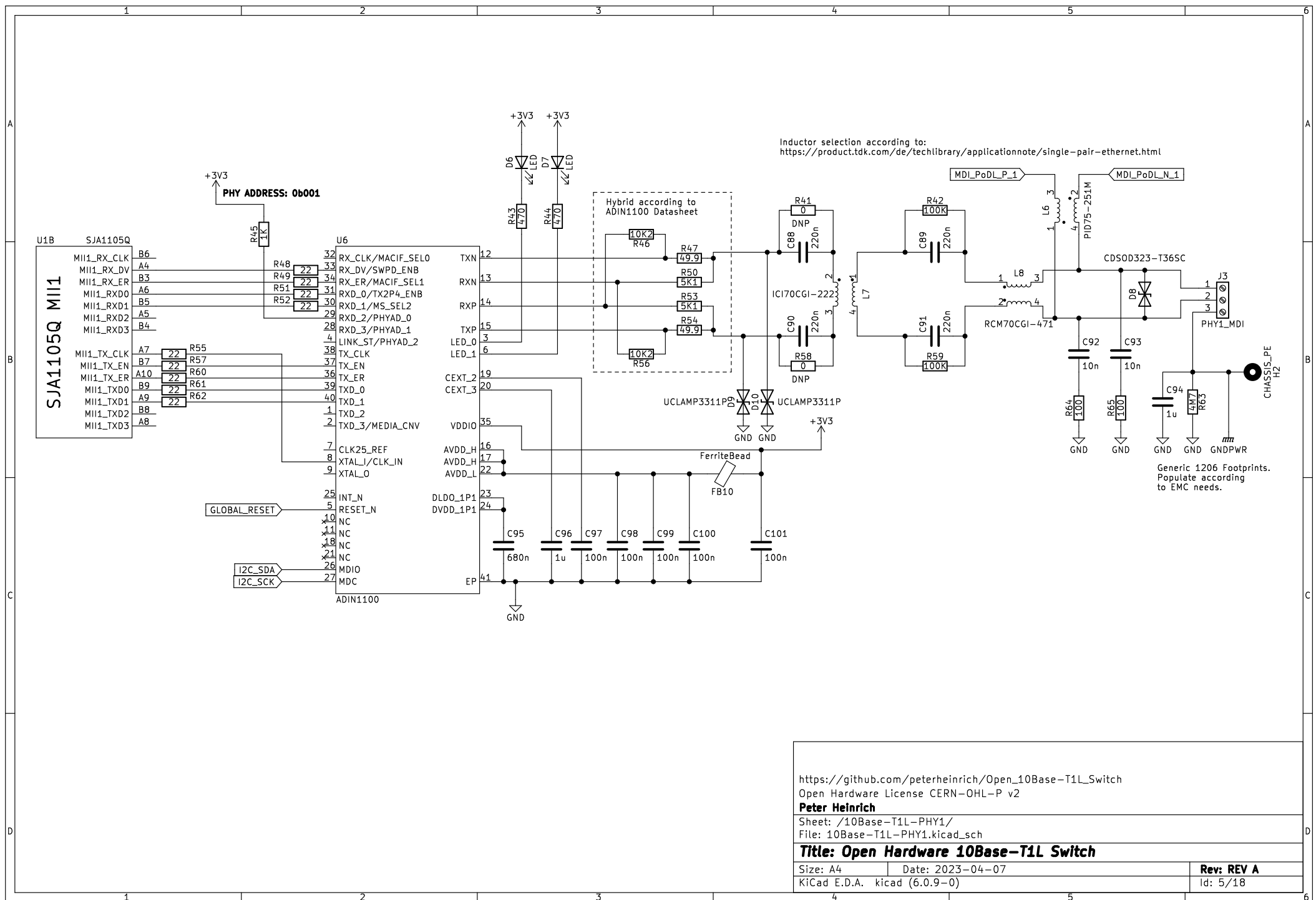
KiCad E.D.A. kicad (6.0.9-0)

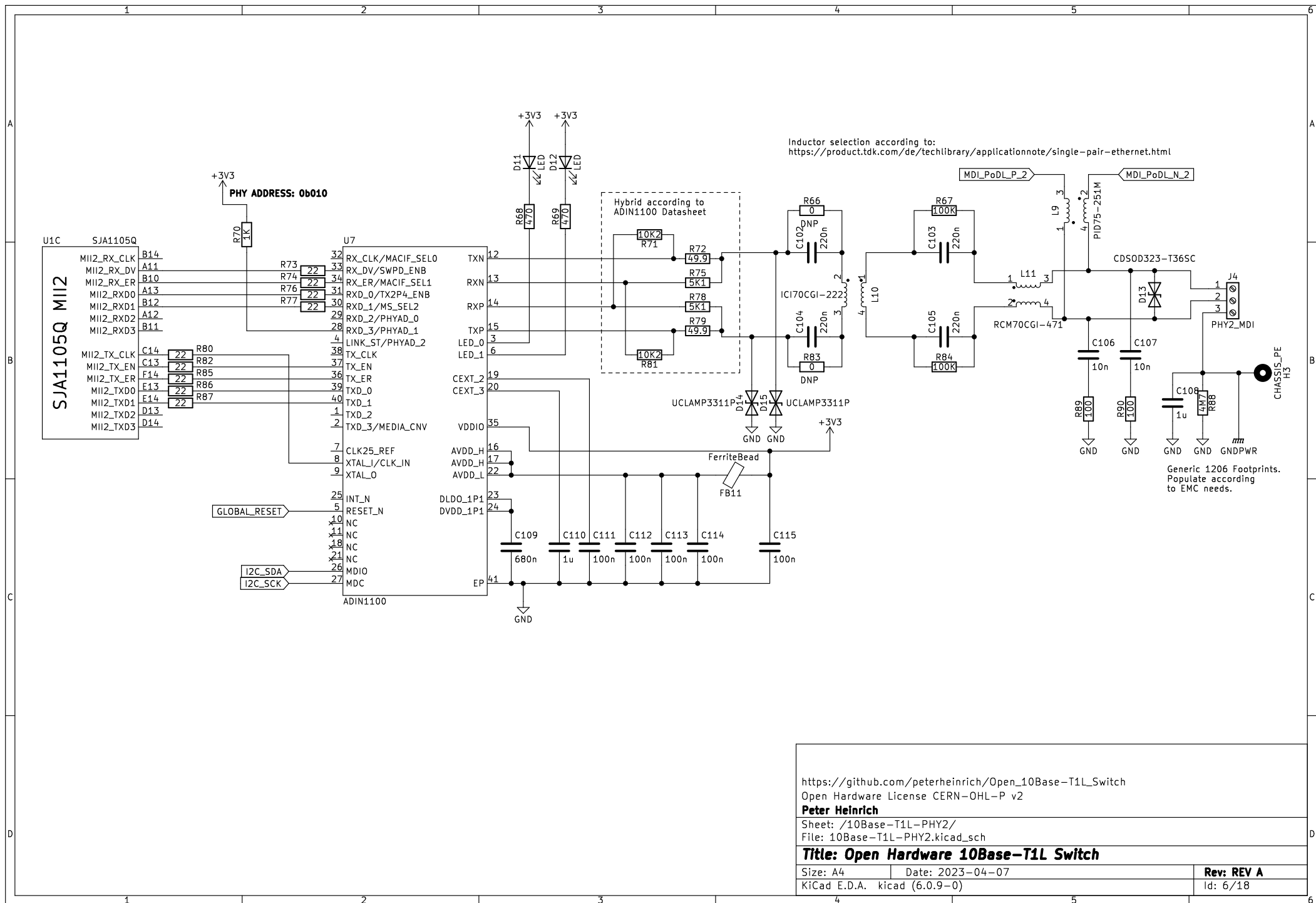
Rev: REV A

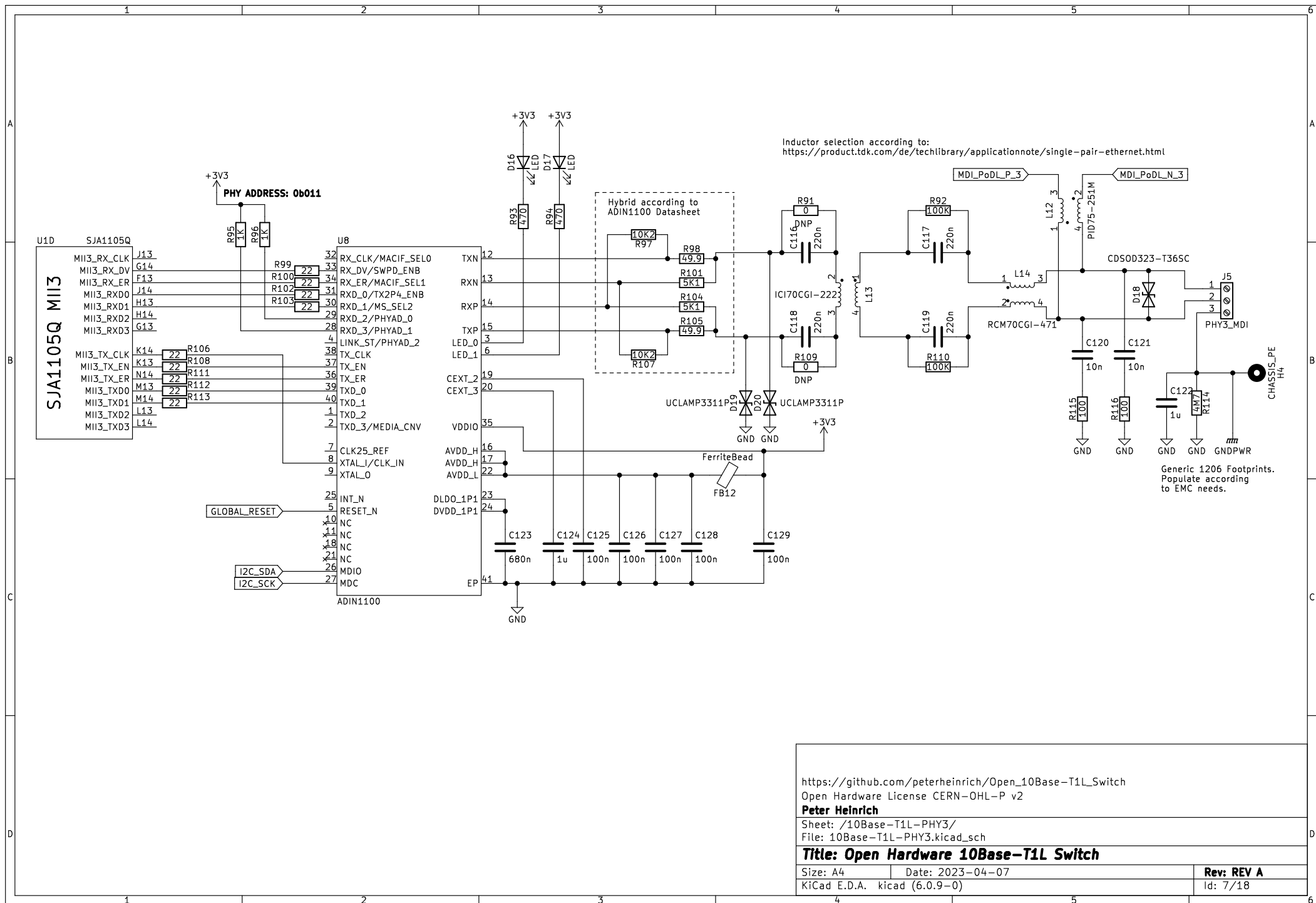
Id: 2/18

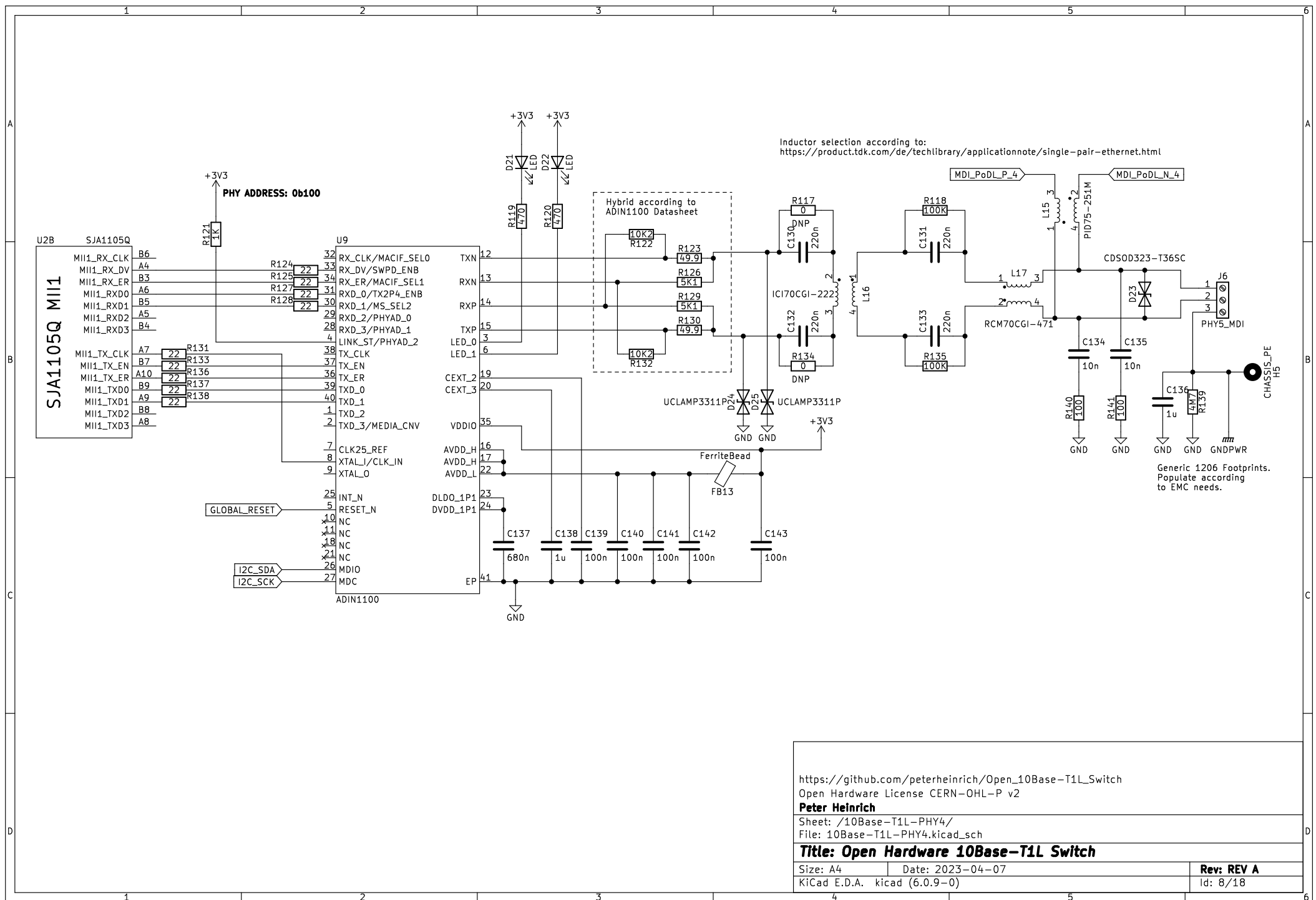


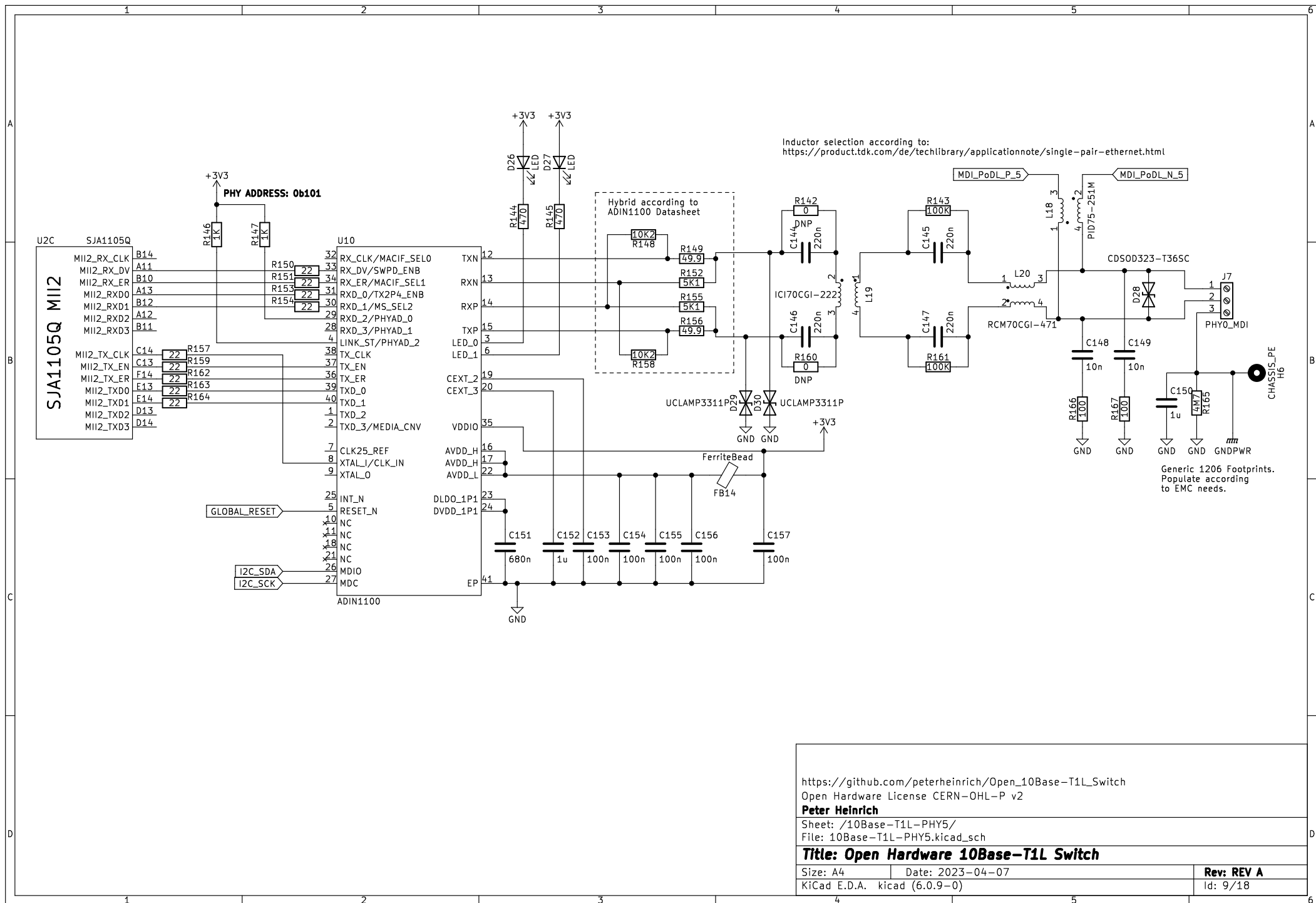












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Sheet: /10Base-T1L-PHY5/
 File: 10Base-T1L-PHY5.kicad_sch

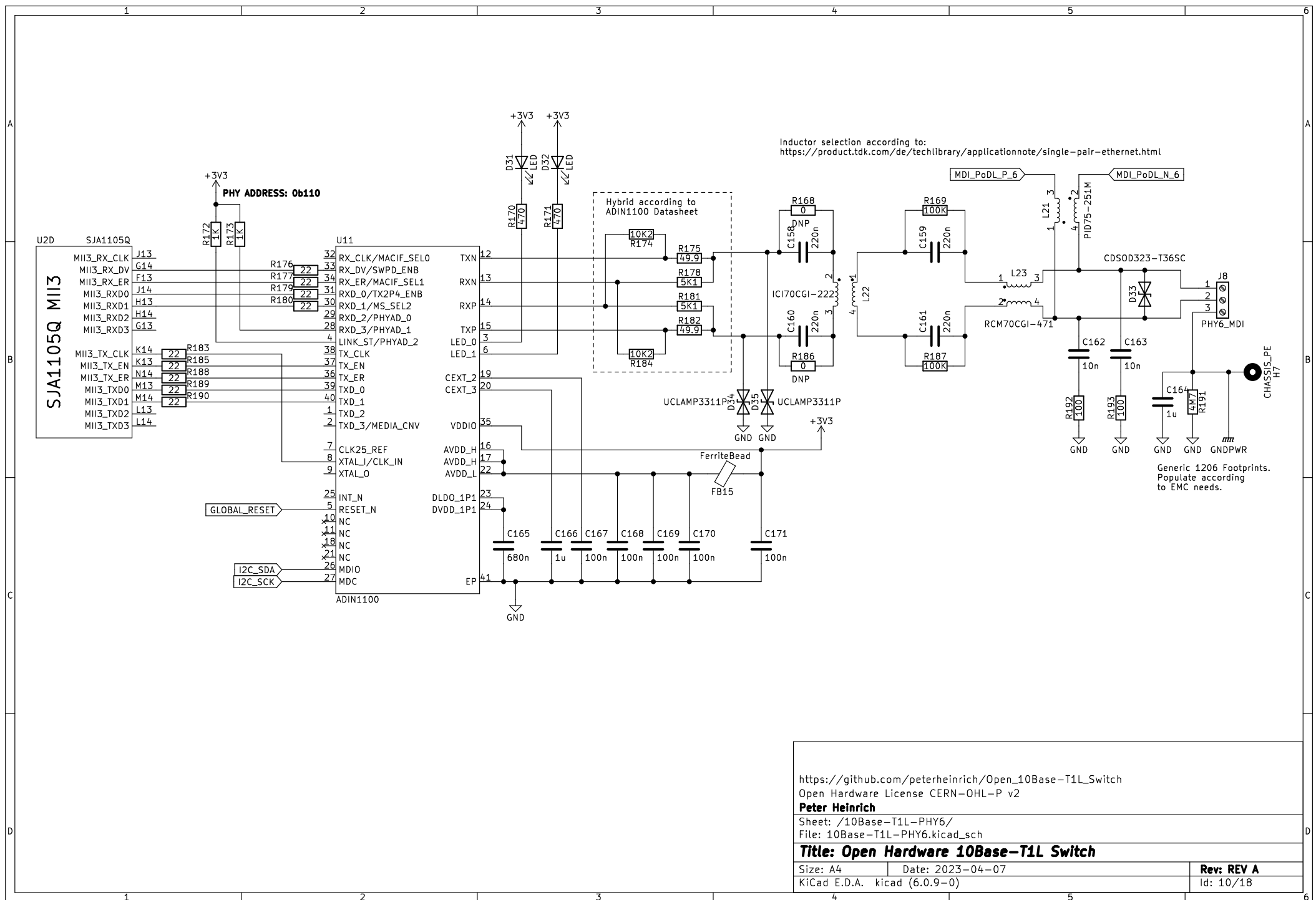
Title: Open Hardware 10Base-T1L Switch

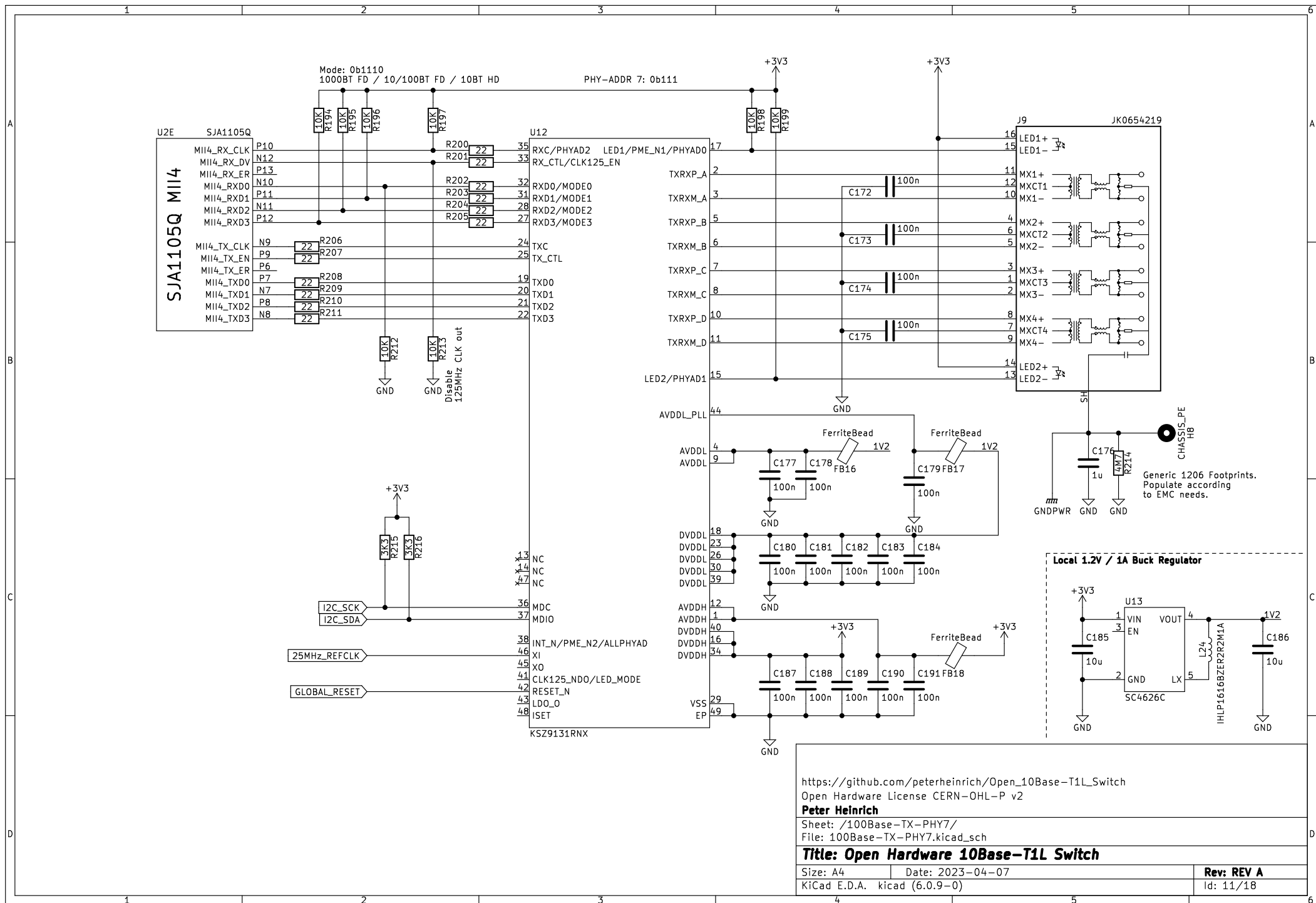
Size: A4 Date: 2023-04-07

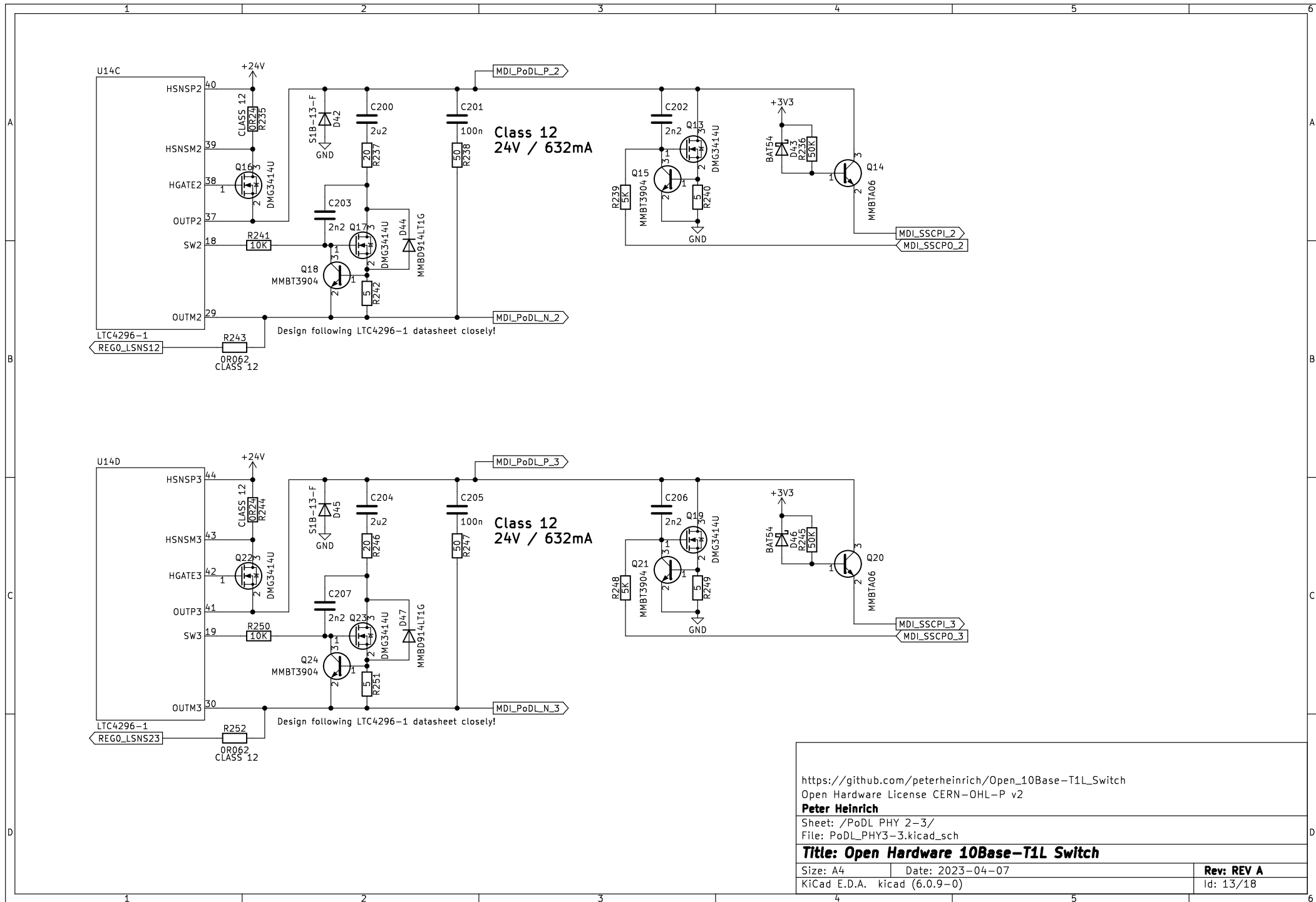
KiCad E.D.A. kicad (6.0.9-0)

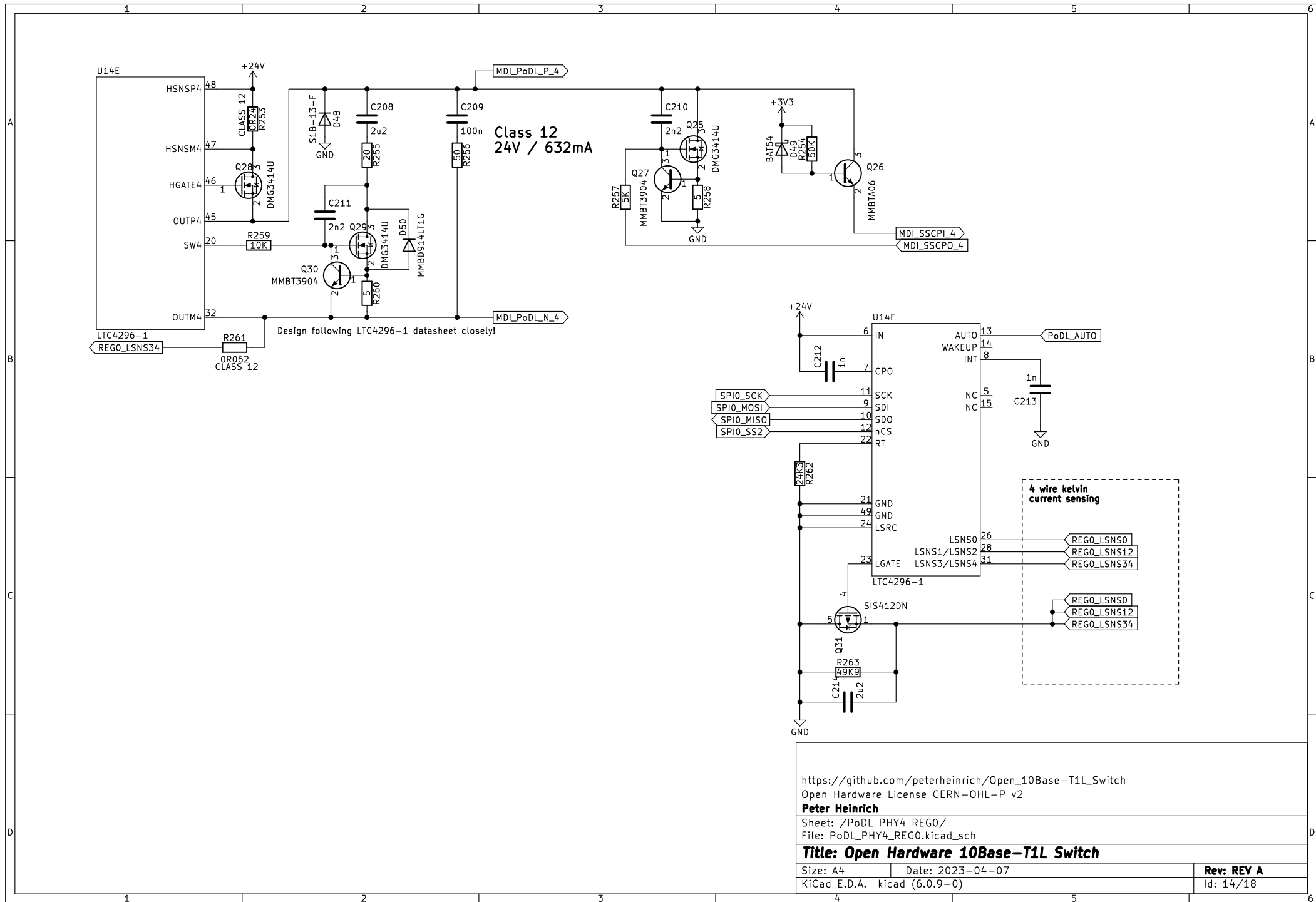
Rev: REV A

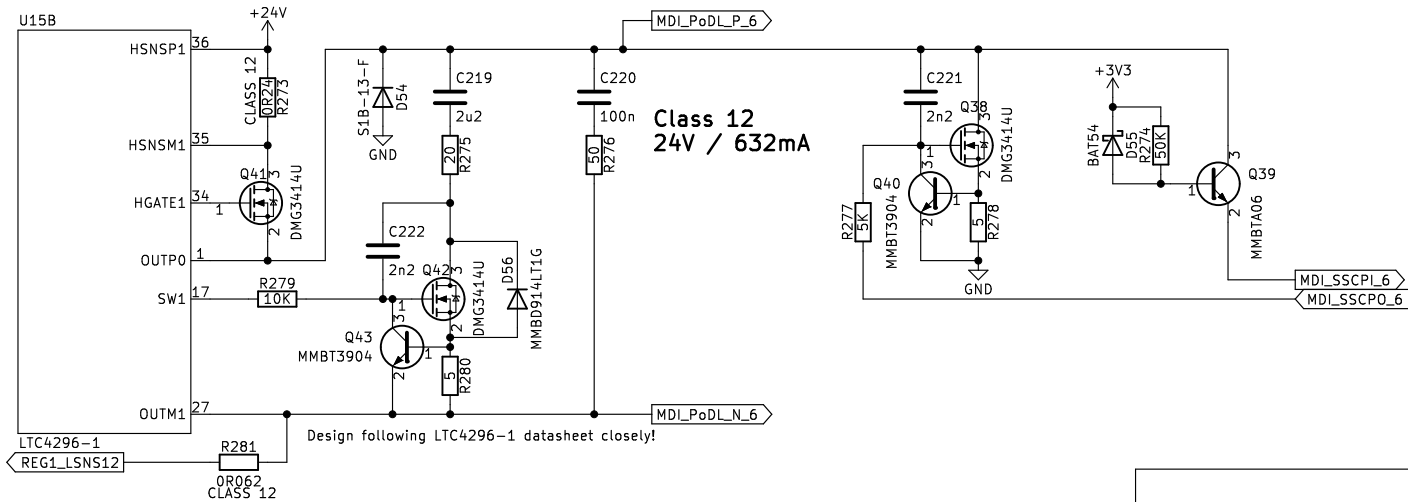
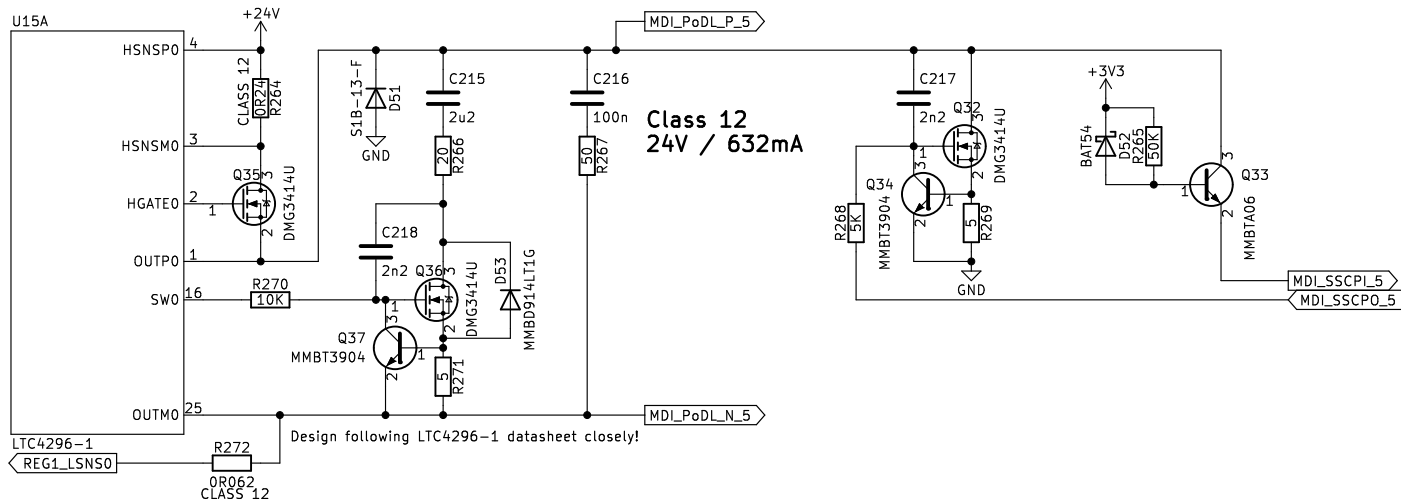
Id: 9/18











https://github.com/peterheinrich/Open_10Base-T1L_Switch
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Sheet: /PoDL PHY 5-6/
File: PoDL_PHY5-6.kicad_sch

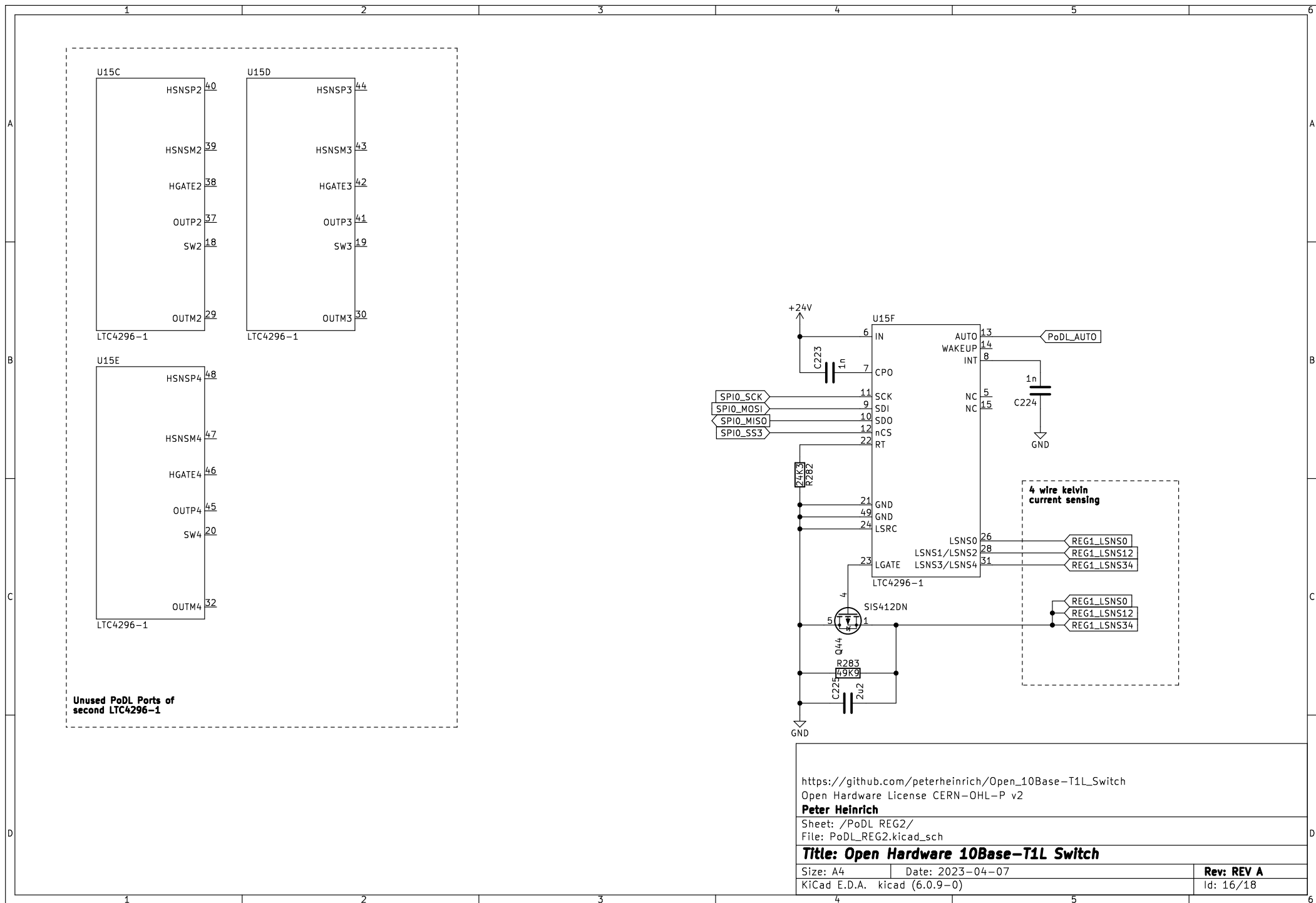
Title: Open Hardware 10Base-T1L Switch

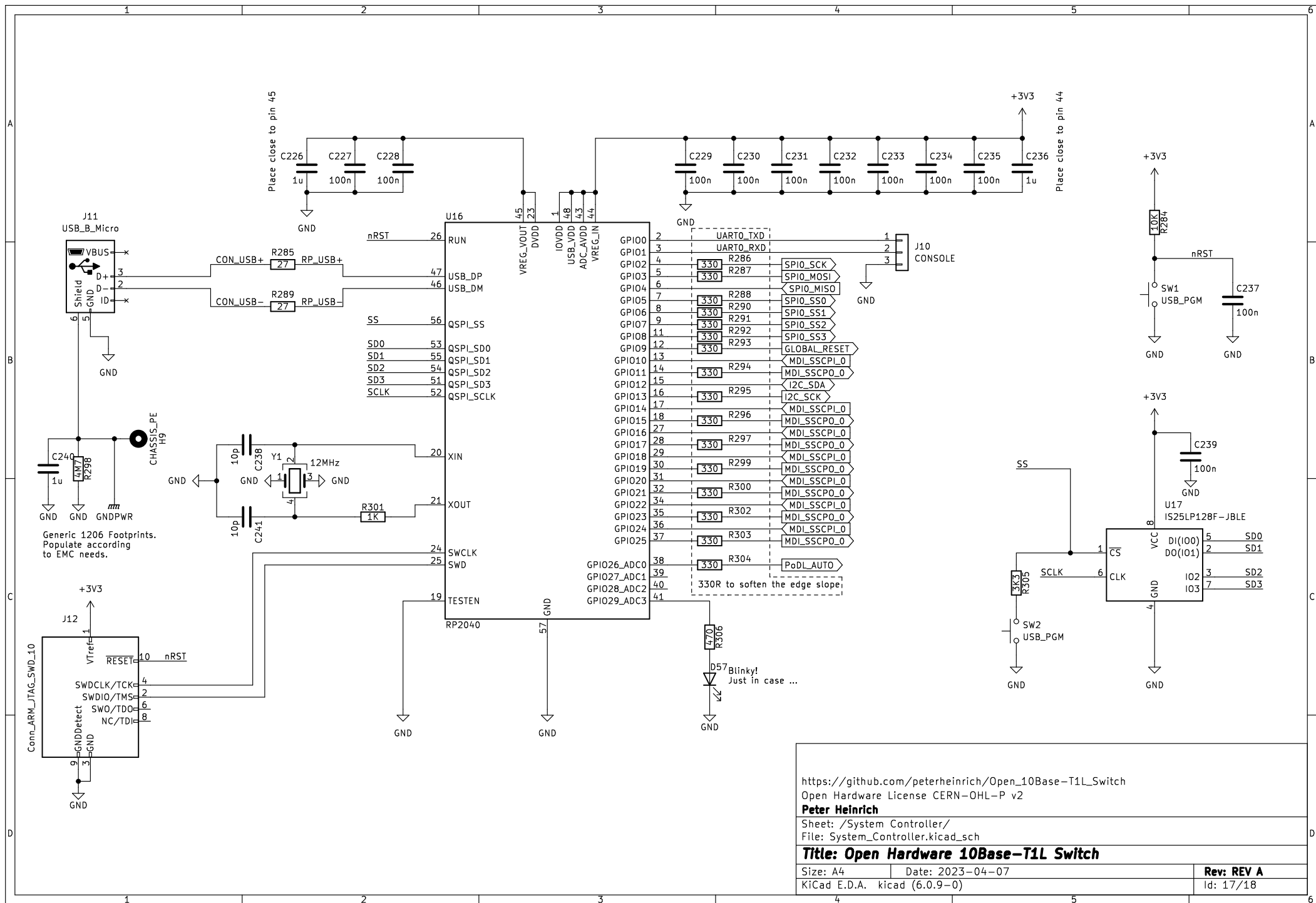
Size: A4 Date: 2023-04-07

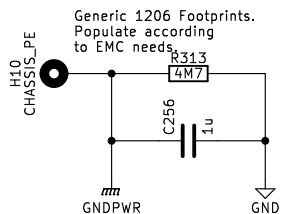
KiCad E.D.A. kicad (6.0.9-0)

Rev: REV A

Id: 15/18







Rev: REV A
Id: 18/18