System Controller

File: System_Controller.kicad_sch

RP2040
System Controller

8-Port 10MBit SPE Field Switch

7-Port 10Base-T1L/PoDL CLASS 12
10/100/1000MBit Uplink (RJ45)

STATUS: DESIGN ONLY!
!!! UNTESTED !!!

2x 5-Port Switch (SJA1105Q) Daisy Chained

SJA1105Q Switch

File: SJA1105Q_Switch.kicad_sch

SJA1105Q Power

File: SJA1105Q_Power.kicad_sch

10Base-T1L-PHY0

SCCPI — MDI_SCCPI_0
SCCPO — MDI_SCCPO_0
REG_LSNS — REG0_LSNS0

File: 10Base-T1L-PHY.kicad_sch

10Base-T1L-PHY1

SCCPI — MDI_SCCPI_1
SCCPO — MDI_SCCPO_1
REG_LSNS — REG0_LSNS12

File: 10Base-T1L-PHY.kicad_sch

10Base-T1L-PHY2

SCCPI — MDI_SCCPI_2
SCCPO — MDI_SCCPO_2
REG_LSNS — REG0_LSNS12

File: 10Base-T1L-PHY.kicad_sch

10Base-T1L-PHY3

SCCPI — MDI_SCCPI_3
SCCPO — MDI_SCCPO_3
REG_LSNS — REG0_LSNS34

File: 10Base-T1L-PHY.kicad_sch

10Base-T1L-PHY4

SCCPI — MDI_SCCPI_4
SCCPO — MDI_SCCPO_4
REG_LSNS — REG1_LSNS0

File: 10Base-T1L-PHY.kicad_sch

10Base-T1L-PHY5

SCCPI — MDI_SCCPI_5
SCCPO — MDI_SCCPO_5
REG_LSNS — REG1_LSNS12

File: 10Base-T1L-PHY.kicad_sch

10Base-T1L-PHY6

SCCPI — MDI_SCCPI_6
SCCPO — MDI_SCCPO_6
REG_LSNS — REG1_LSNS12

File: 10Base-T1L-PHY.kicad_sch

7 PHYs 10Base-T1L
ADIN1100 PHY
PoDL circuitry

100Base-TX-PHY7

File: 100Base-TX-PHY7.kicad_sch

1 PHY 100Base-TX
Uplink
KSZ9131RNX

PoDL_REG0

LSNS0 — REG0_LSNS0
LSNS12 — REG0_LSNS12
LSNS34 — REG0_LSNS34
SPI_SS — SPI0_SS2

File: PoDL_REG.kicad_sch

UnusedUnits

File: UnusedUnits.kicad_sch

PoDL_REG1

LSNS0 — REG1_LSNS0
LSNS12 — REG1_LSNS12
LSNS34
SPI_SS — SPI0_SS3

File: PoDL_REG.kicad_sch

7 Port PoDL CLASS 12
2x LTC4296-1 Controller

Power Supply

File: Power_Supply.kicad_sch

24V supply

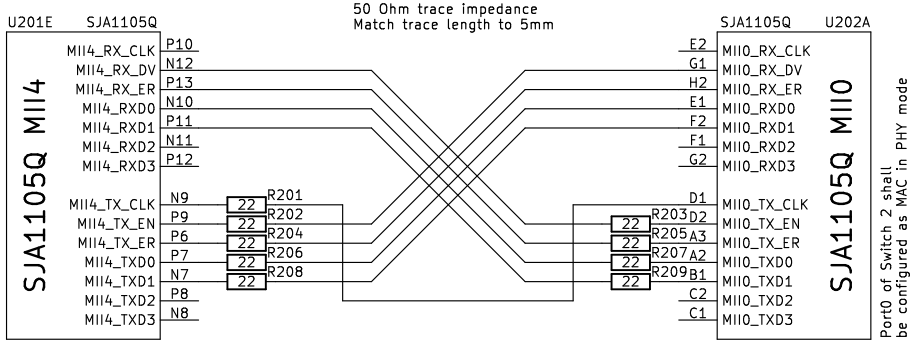
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich

Sheet: /
File: Open_10Base-T1L_Switch.kicad_sch

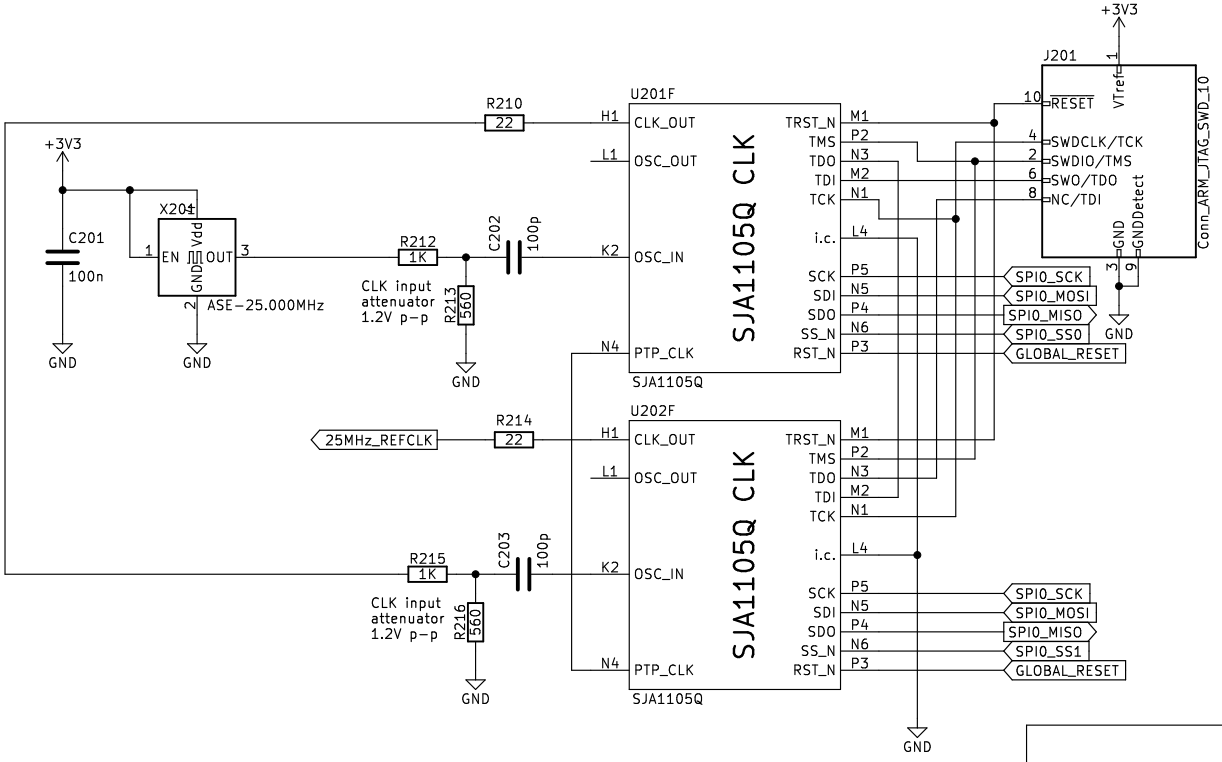
Title: Open Hardware 10Base-T1L Switch

Size: A4	Date: 2023-04-07	**Rev: REV A**
KiCad E.D.A. kicad (6.0.9-0)		Id: 1/16

Inter Switch Connection RMII<->RMII 100MBit



Switch Clock Generation / JTAG Debug



Keep clock lines less than 14 cm, according to
"1/3 rise time" rule.
https://www.altium.com/documentation/altium-designer/interactively-routing-controlled-impedance-pcb

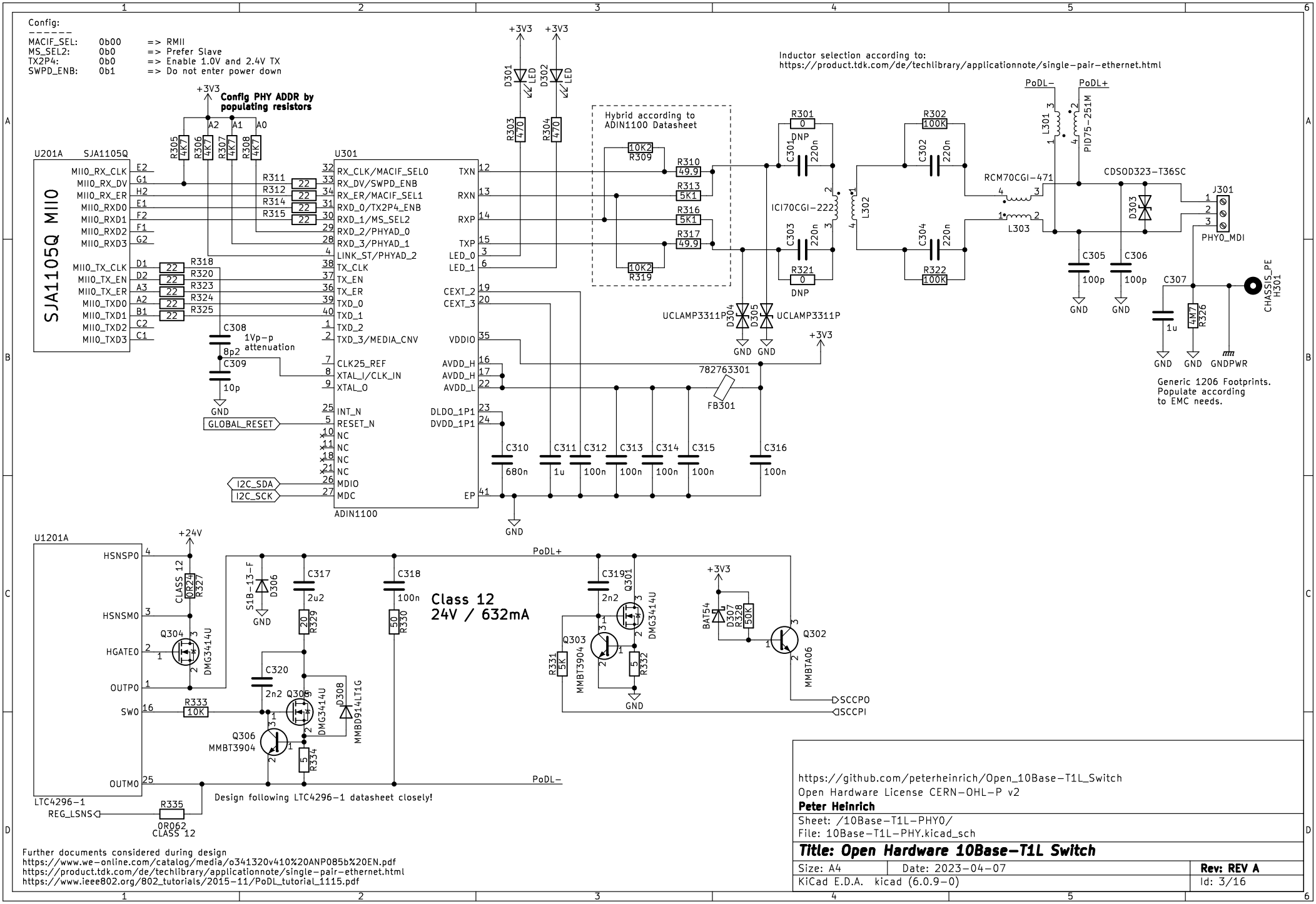
The ASE-25.000MHz has a 2.8ns rise time, hence 0.93ns trace delay, which equals to 14cm trace length on FR4.

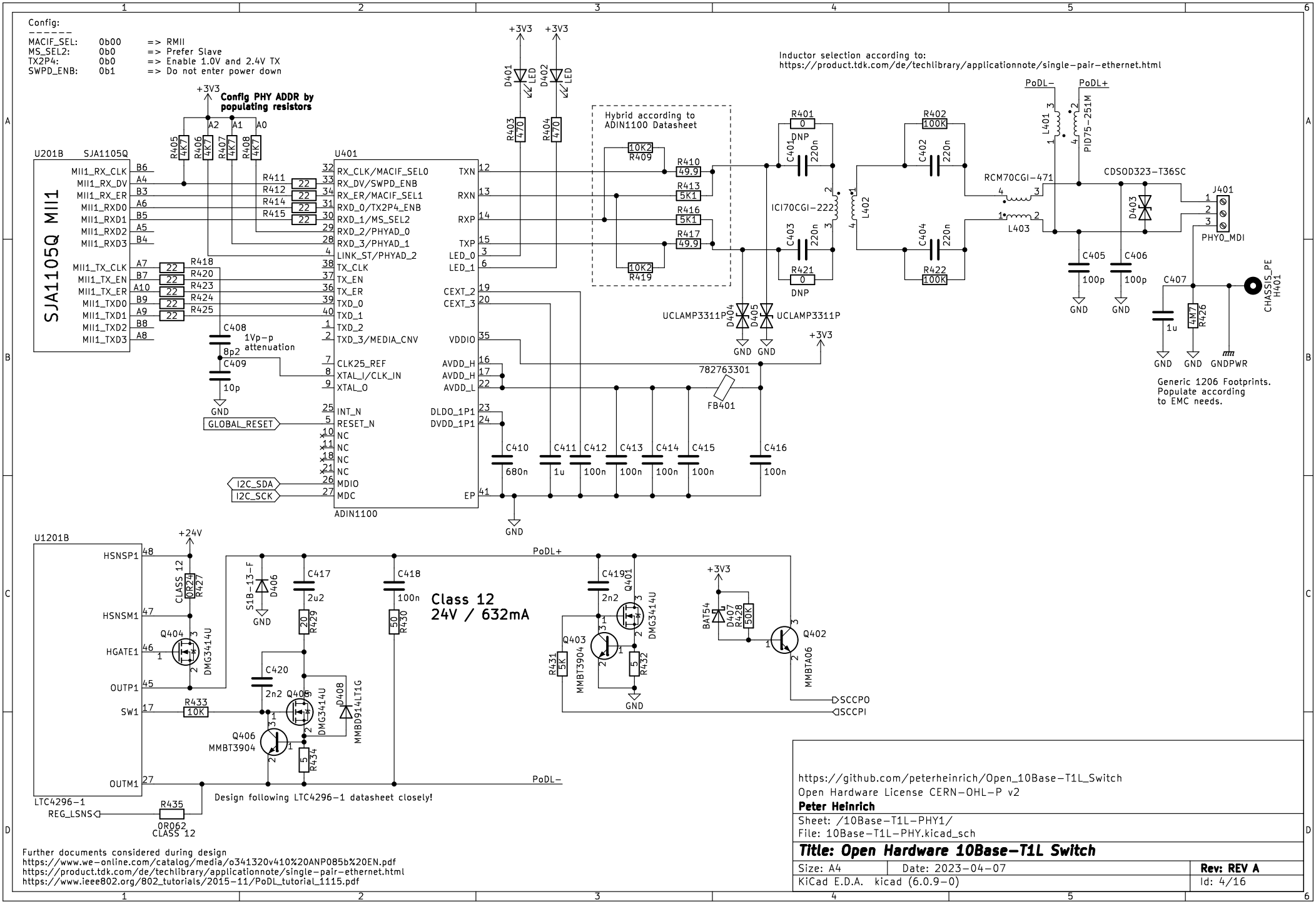
Peter Heinrich

Sheet: /SJA1105Q Switch/
File: SJA1105Q_Switch.kicad_sch

Title: Open Hardware 10Base-T1L Switch

Size: A4	Date: 2023-04-07	**Rev: REV A**
KiCad E.D.A. kicad (6.0.9-0)		Id: 2/16


Config:
MACIF_SEL: 0b00 => RMII
MS_SEL2: 0b0 => Prefer Slave
TX2P4: 0b0 => Enable 1.0V and 2.4V TX
SWPD_ENB: 0b1 => Do not enter power down
Config PHY ADDR by populating resistors
Inductor selection according to:
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
Hybrid according to ADIN1100 Datasheet
U201A SJA1105Q
SJA1105Q MII0
U301
ADIN1100
U1201A
LTC4296-1
Class 12
24V / 632mA
Design following LTC4296-1 datasheet closely!
Generic 1206 Footprints.
Populate according to EMC needs.
Further documents considered during design
https://www.we-online.com/catalog/media/o341320v410%20ANP085b%20EN.pdf
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
https://www.ieee802.org/802_tutorials/2015-11/PoDL_tutorial_1115.pdf
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich
Sheet: /10Base-T1L-PHY0/
File: 10Base-T1L-PHY.kicad_sch
Title: Open Hardware 10Base-T1L Switch
Size: A4
Date: 2023-04-07
Rev: REV A
KiCad E.D.A. kicad (6.0.9-0)
Id: 3/16


Config:
MACIF_SEL: 0b00 => RMII
MS_SEL2: 0b0 => Prefer Slave
TX2P4: 0b0 => Enable 1.0V and 2.4V TX
SWPD_ENB: 0b1 => Do not enter power down
Config PHY ADDR by populating resistors
Inductor selection according to:
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
Hybrid according to ADIN1100 Datasheet
U201B SJA1105Q
SJA1105Q MII1
U401
ADIN1100
ICI70CGI-222
RCM70CGI-471
CDSOD323-T36SC
PID75-251M
UCLAMP3311P
782763301
FB401
PHY0_MDI
CHASSIS_PE
GNDPWR
Generic 1206 Footprints.
Populate according to EMC needs.
GLOBAL_RESET
I2C_SDA
I2C_SCK
1Vp-p attenuation
U1201B
LTC4296-1
Class 12
24V / 632mA
Design following LTC4296-1 datasheet closely!
PoDL+
PoDL-
SCCPO
SCCPI
Further documents considered during design
https://www.we-online.com/catalog/media/o341320v410%20ANP085b%20EN.pdf
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
https://www.ieee802.org/802_tutorials/2015-11/PoDL_tutorial_1115.pdf
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
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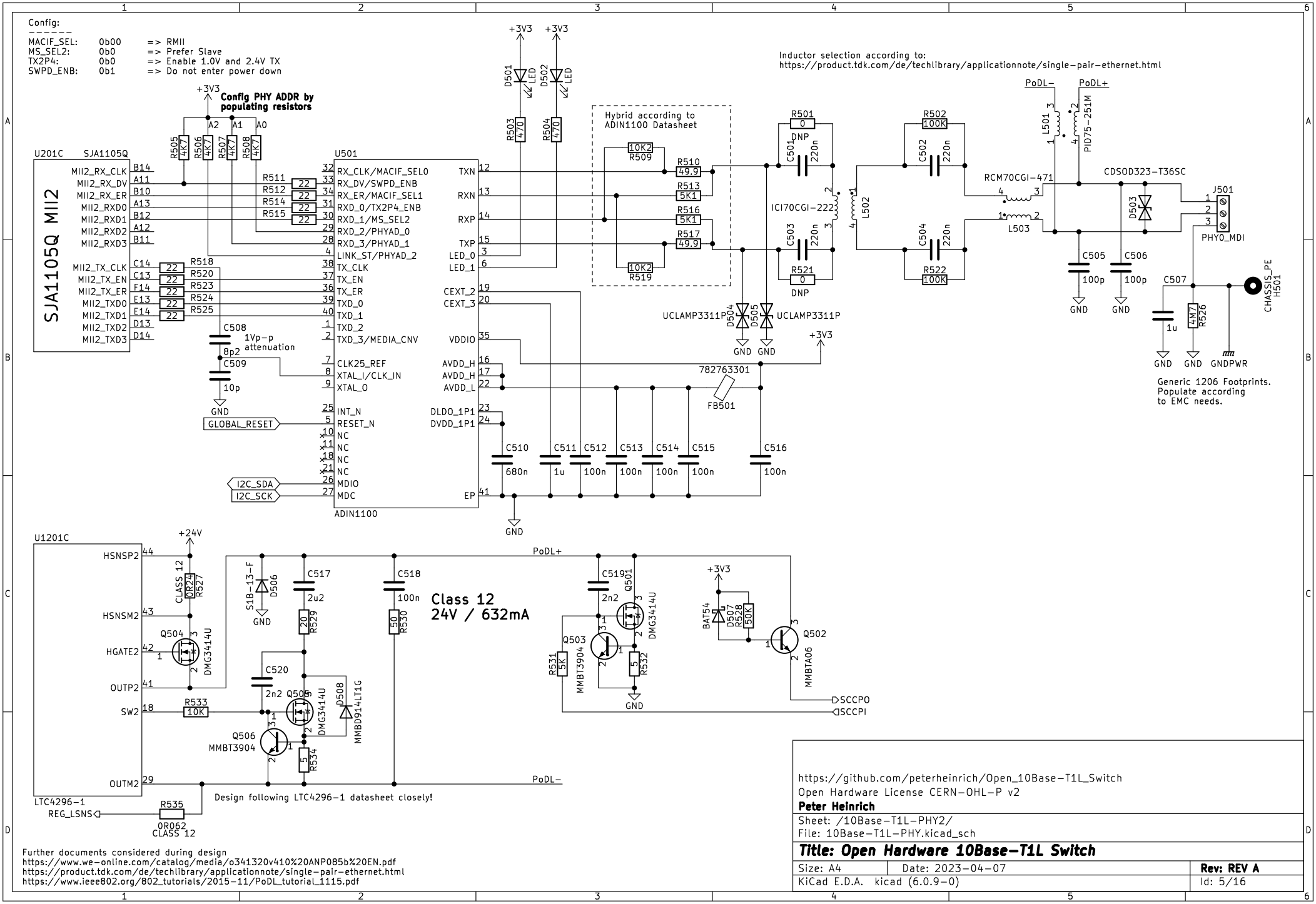
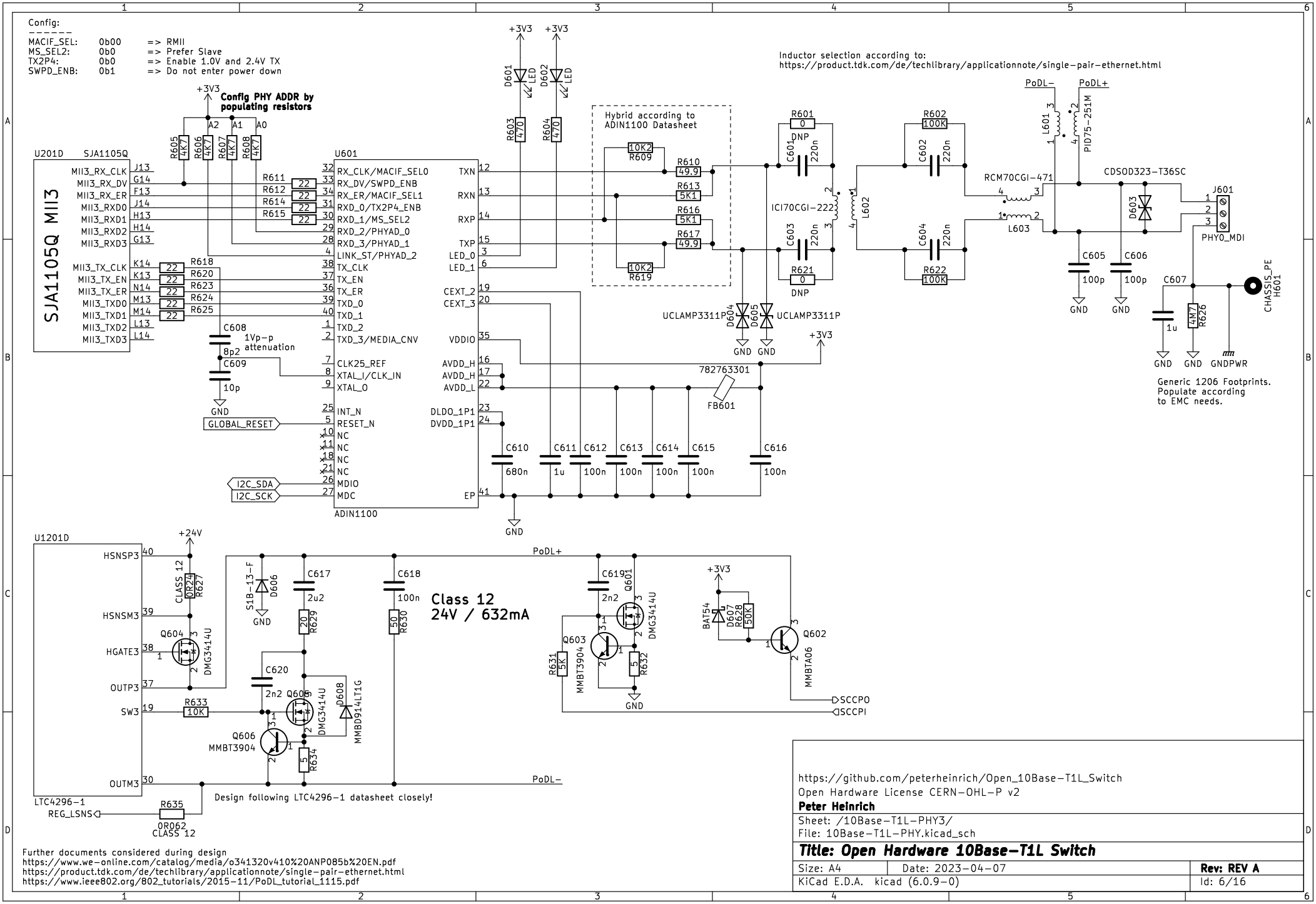
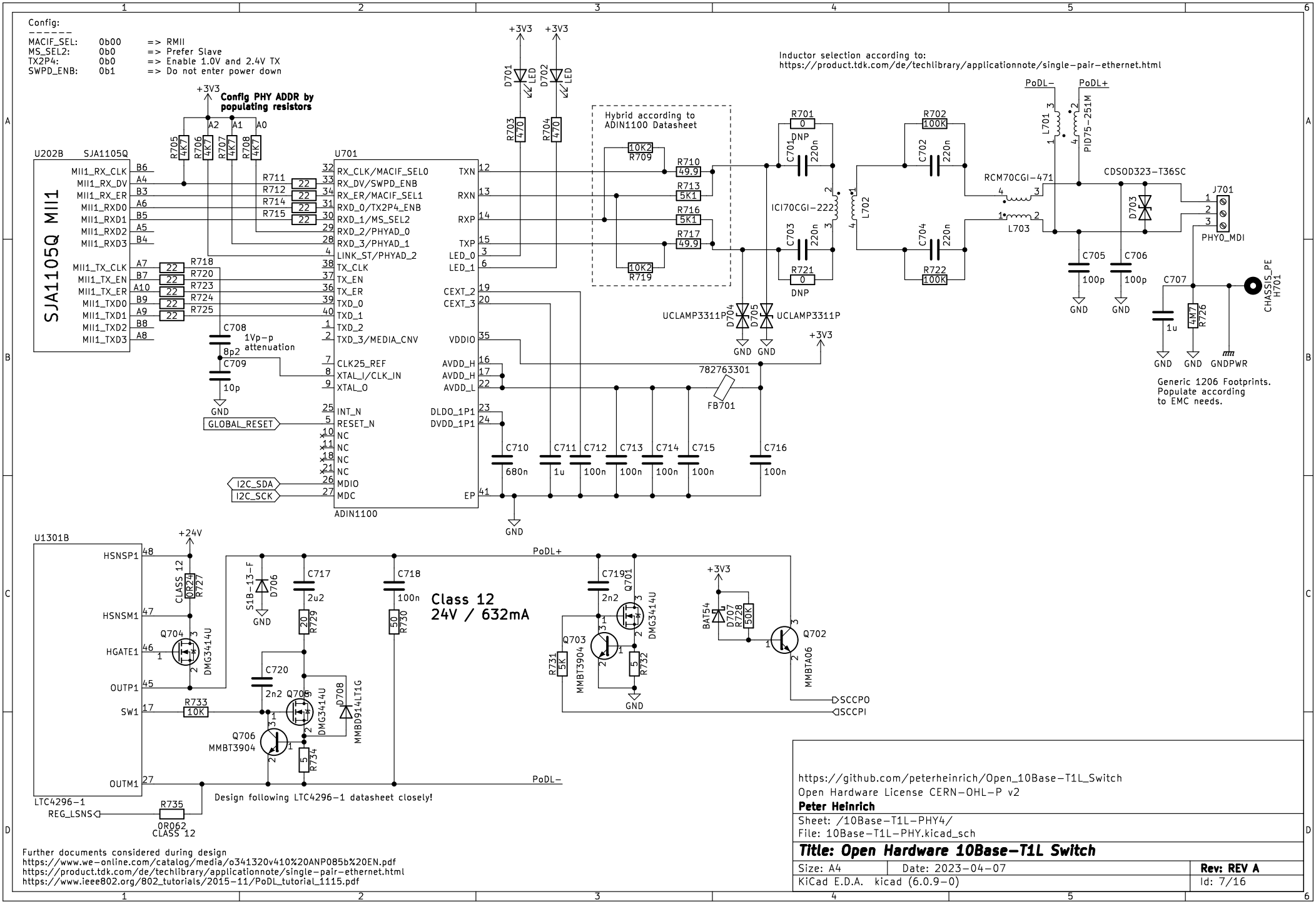
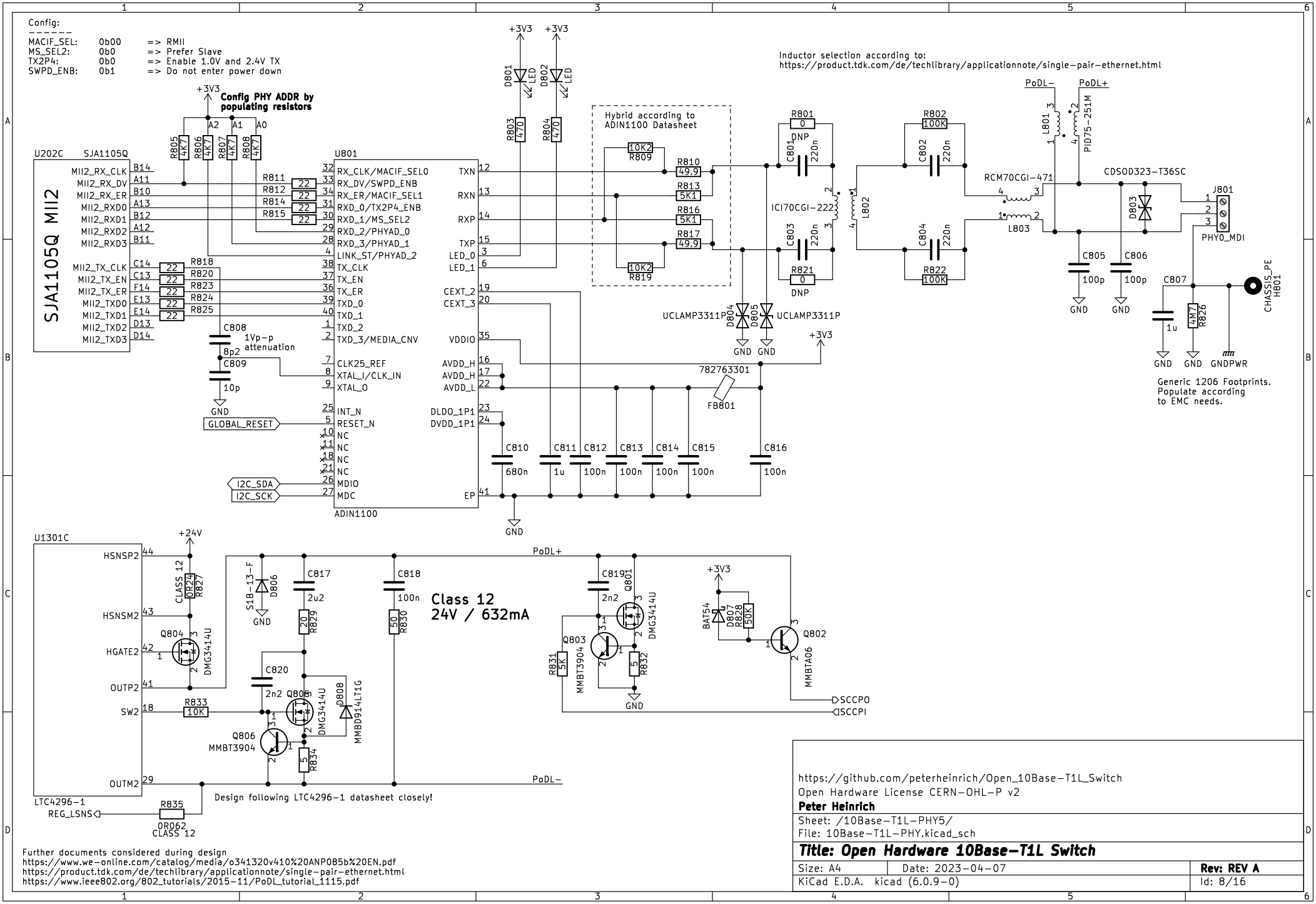
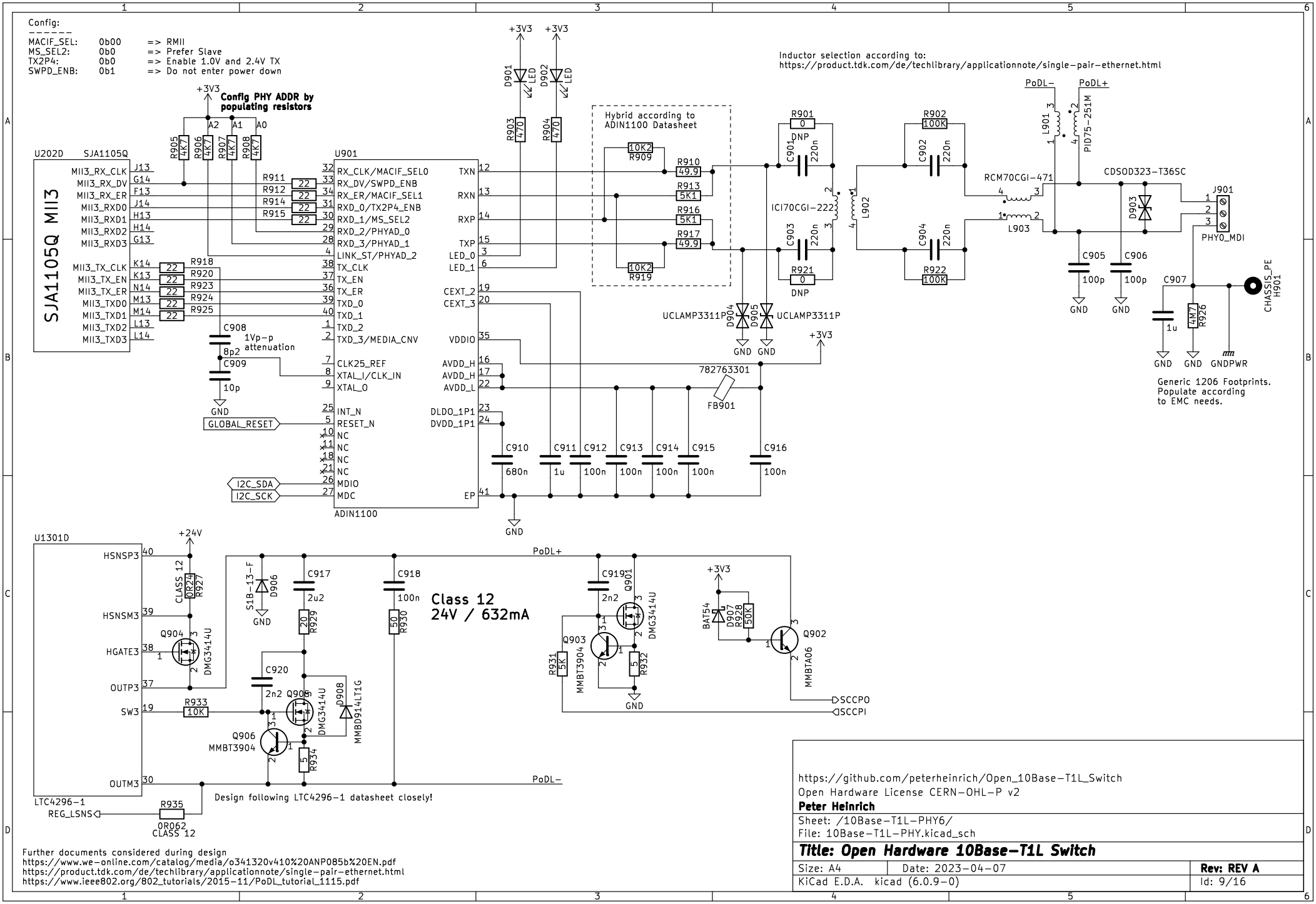
Sheet: /10Base-T1L-PHY1/
File: 10Base-T1L-PHY.kicad_sch
Title: Open Hardware 10Base-T1L Switch
Size: A4
Date: 2023-04-07
Rev: REV A
KiCad E.D.A. kicad (6.0.9-0)
Id: 4/16

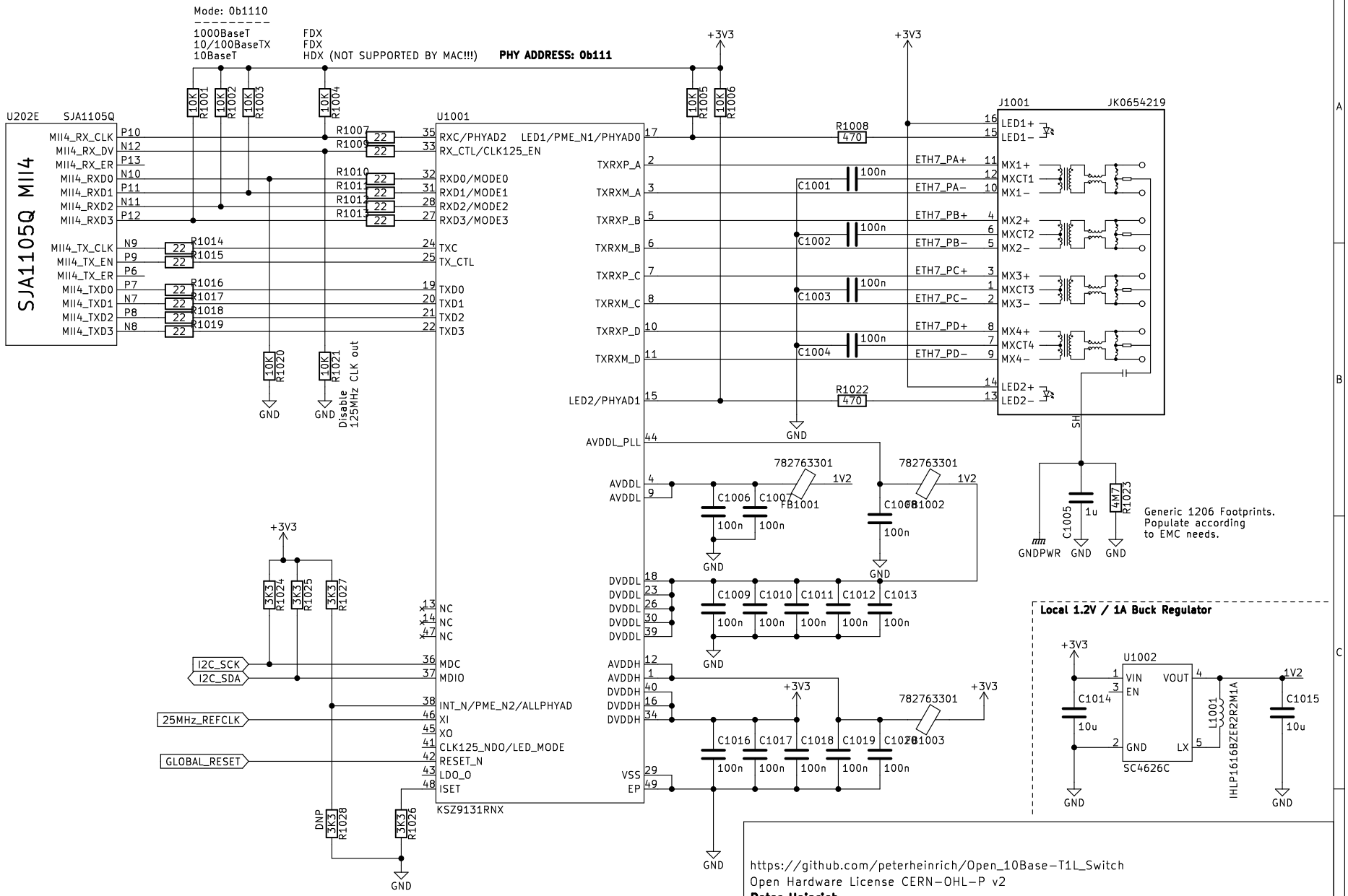

Config:
MACIF_SEL: 0b00 => RMII
MS_SEL2: 0b0 => Prefer Slave
TX2P4: 0b0 => Enable 1.0V and 2.4V TX
SWPD_ENB: 0b1 => Do not enter power down
Config PHY ADDR by populating resistors
Inductor selection according to:
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
Hybrid according to ADIN1100 Datasheet
SJA1105Q MII2
U201C SJA1105Q
U501
ADIN1100
1Vp-p attenuation
GLOBAL_RESET
I2C_SDA
I2C_SCK
UCLAMP3311P
782763301
FB501
RCM70CGI-471
CDSOD323-T36SC
PHY0_MDI
CHASSIS_PE
GNDPWR
Generic 1206 Footprints.
Populate according to EMC needs.
U1201C
LTC4296-1
Class 12
24V / 632mA
Design following LTC4296-1 datasheet closely!
PoDL+
PoDL-
SCCPO
SCCPI
REG_LSNS
CLASS 12
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich
Sheet: /10Base-T1L-PHY2/
File: 10Base-T1L-PHY.kicad_sch
Title: Open Hardware 10Base-T1L Switch
Size: A4
Date: 2023-04-07
Rev: REV A
KiCad E.D.A. kicad (6.0.9-0)
Id: 5/16
Further documents considered during design
https://www.we-online.com/catalog/media/o341320v410%20ANP085b%20EN.pdf
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
https://www.ieee802.org/802_tutorials/2015-11/PoDL_tutorial_1115.pdf

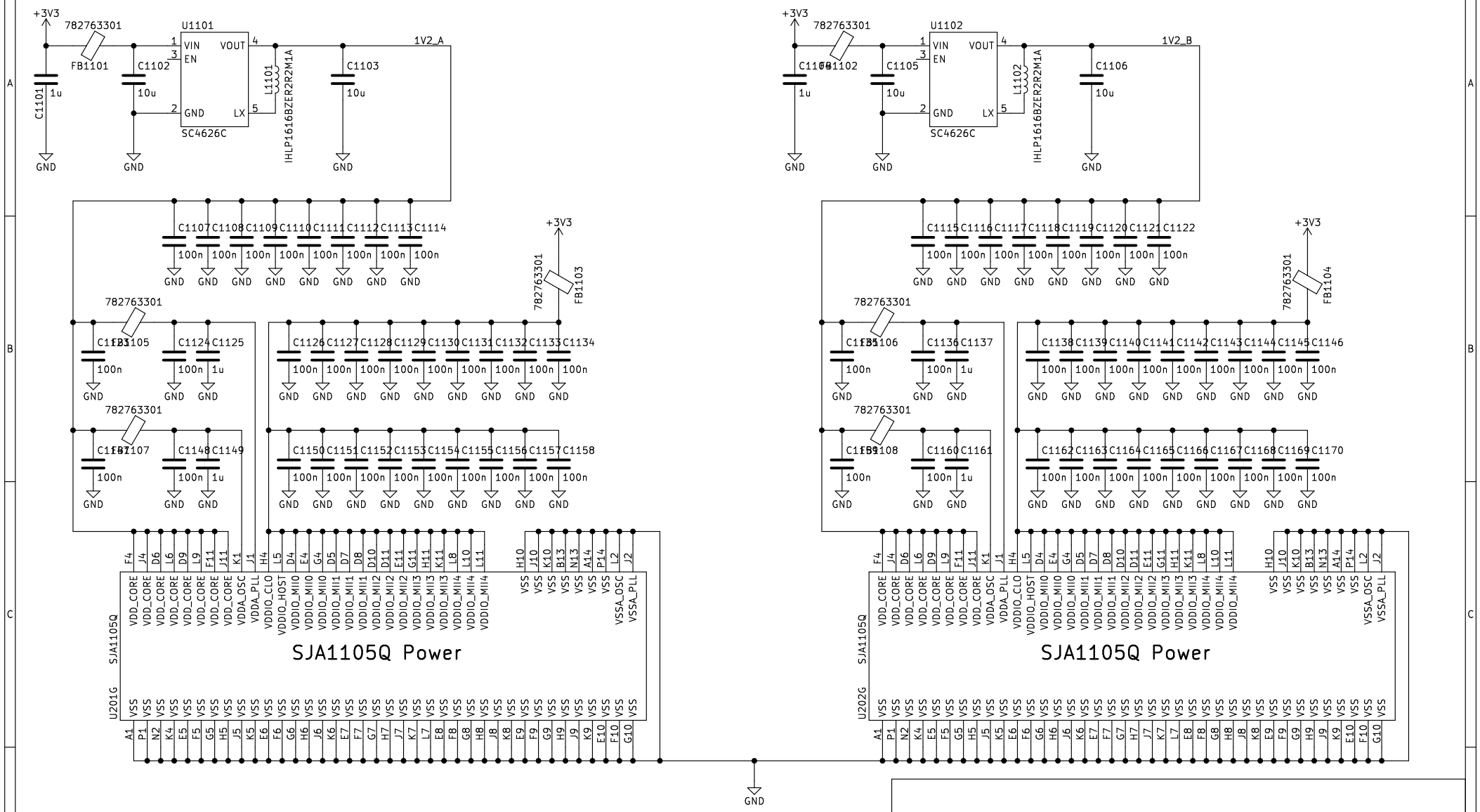

Config:
MACIF_SEL: 0b00 => RMII
MS_SEL2: 0b0 => Prefer Slave
TX2P4: 0b0 => Enable 1.0V and 2.4V TX
SWPD_ENB: 0b1 => Do not enter power down
Config PHY ADDR by populating resistors
Inductor selection according to:
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
Hybrid according to ADIN1100 Datasheet
U201D SJA1105Q
SJA1105Q MII3
U601
ADIN1100
1Vp-p attenuation
GLOBAL_RESET
I2C_SDA
I2C_SCK
UCLAMP3311P
782763301
FB601
RCM70CGI-471
ICI70CGI-222
CDSOD323-T36SC
PHY0_MDI
CHASSIS_PE
Generic 1206 Footprints.
Populate according to EMC needs.
U1201D
LTC4296-1
Class 12
24V / 632mA
Design following LTC4296-1 datasheet closely!
PoDL+
PoDL-
SCCPO
SCCPI
Further documents considered during design
https://www.we-online.com/catalog/media/o341320v410%20ANP085b%20EN.pdf
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
https://www.ieee802.org/802_tutorials/2015-11/PoDL_tutorial_1115.pdf
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich
Sheet: /10Base-T1L-PHY3/
File: 10Base-T1L-PHY.kicad_sch
Title: Open Hardware 10Base-T1L Switch
Size: A4
Date: 2023-04-07
Rev: REV A
KiCad E.D.A. kicad (6.0.9-0)
Id: 6/16


Config:
MACIF_SEL: 0b00 => RMII
MS_SEL2: 0b0 => Prefer Slave
TX2P4: 0b0 => Enable 1.0V and 2.4V TX
SWPD_ENB: 0b1 => Do not enter power down
Config PHY ADDR by populating resistors
Inductor selection according to:
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
Hybrid according to ADIN1100 Datasheet
U202B SJA1105Q
SJA1105Q MII1
U701
ADIN1100
ICI70CGI-222
RCM70CGI-471
CDSOD323-T36SC
PID75-251M
UCLAMP3311P
782763301
FB701
PHY0_MDI
CHASSIS_PE
GNDPWR
Generic 1206 Footprints.
Populate according to EMC needs.
GLOBAL_RESET
I2C_SDA
I2C_SCK
1Vp-p attenuation
U1301B
LTC4296-1
Class 12
24V / 632mA
Design following LTC4296-1 datasheet closely!
PoDL+
PoDL-
SCCPO
SCCPI
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich
Sheet: /10Base-T1L-PHY4/
File: 10Base-T1L-PHY.kicad_sch
Title: Open Hardware 10Base-T1L Switch
Size: A4
Date: 2023-04-07
Rev: REV A
KiCad E.D.A. kicad (6.0.9-0)
Id: 7/16
Further documents considered during design
https://www.we-online.com/catalog/media/o341320v410%20ANP085b%20EN.pdf
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
https://www.ieee802.org/802_tutorials/2015-11/PoDL_tutorial_1115.pdf


Config:
MACIF_SEL: 0b00 => RMII
MS_SEL2: 0b0 => Prefer Slave
TX2P4: 0b0 => Enable 1.0V and 2.4V TX
SWPD_ENB: 0b1 => Do not enter power down
Config PHY ADDR by populating resistors
Inductor selection according to:
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
Hybrid according to ADIN1100 Datasheet
U202C SJA1105Q
SJA1105Q MII2
U801
ADIN1100
ICI70CGI-222
RCM70CGI-471
CDSOD323-T36SC
PID75-251M
782763301
FB801
UCLAMP3311P
PHY0_MDI
CHASSIS_PE
GNDPWR
Generic 1206 Footprints.
Populate according to EMC needs.
GLOBAL_RESET
I2C_SDA
I2C_SCK
1Vp-p attenuation
U1301C
LTC4296-1
Class 12
24V / 632mA
Design following LTC4296-1 datasheet closely!
PoDL+
PoDL-
SCCPO
SCCPI
REG_LSNS
CLASS 12
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich
Sheet: /10Base-T1L-PHY5/
File: 10Base-T1L-PHY.kicad_sch
Title: Open Hardware 10Base-T1L Switch
Size: A4
Date: 2023-04-07
Rev: REV A
KiCad E.D.A. kicad (6.0.9-0)
Id: 8/16
Further documents considered during design
https://www.we-online.com/catalog/media/o341320v410%20ANP085b%20EN.pdf
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
https://www.ieee802.org/802_tutorials/2015-11/PoDL_tutorial_1115.pdf


Config:
MACIF_SEL: 0b00 => RMII
MS_SEL2: 0b0 => Prefer Slave
TX2P4: 0b0 => Enable 1.0V and 2.4V TX
SWPD_ENB: 0b1 => Do not enter power down
Config PHY ADDR by populating resistors
Inductor selection according to:
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
Hybrid according to ADIN1100 Datasheet
U202D SJA1105Q
SJA1105Q MII3
U901
ADIN1100
U1301D
LTC4296-1
Class 12
24V / 632mA
Design following LTC4296-1 datasheet closely!
Generic 1206 Footprints.
Populate according to EMC needs.
Further documents considered during design
https://www.we-online.com/catalog/media/o341320v410%20ANP085b%20EN.pdf
https://product.tdk.com/de/techlibrary/applicationnote/single-pair-ethernet.html
https://www.ieee802.org/802_tutorials/2015-11/PoDL_tutorial_1115.pdf
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich
Sheet: /10Base-T1L-PHY6/
File: 10Base-T1L-PHY.kicad_sch
Title: Open Hardware 10Base-T1L Switch
Size: A4
Date: 2023-04-07
Rev: REV A
KiCad E.D.A. kicad (6.0.9-0)
Id: 9/16


Mode: 0b1110
1000BaseT FDX
10/100BaseTX FDX
10BaseT HDX (NOT SUPPORTED BY MAC!!!)
PHY ADDRESS: 0b111
U202E SJA1105Q
SJA1105Q MII4
MII4_RX_CLK P10
MII4_RX_DV N12
MII4_RX_ER P13
MII4_RXD0 N10
MII4_RXD1 P11
MII4_RXD2 N11
MII4_RXD3 P12
MII4_TX_CLK N9
MII4_TX_EN P9
MII4_TX_ER P6
MII4_TXD0 P7
MII4_TXD1 N7
MII4_TXD2 P8
MII4_TXD3 N8
U1001
KSZ9131RNX
RXC/PHYAD2 LED1/PME_N1/PHYAD0
RX_CTL/CLK125_EN
RXD0/MODE0
RXD1/MODE1
RXD2/MODE2
RXD3/MODE3
TXC
TX_CTL
TXD0
TXD1
TXD2
TXD3
TXRXP_A
TXRXM_A
TXRXP_B
TXRXM_B
TXRXP_C
TXRXM_C
TXRXP_D
TXRXM_D
LED2/PHYAD1
AVDDL_PLL
AVDDL
DVDDL
AVDDH
DVDDH
VSS
EP
NC
MDC
MDIO
INT_N/PME_N2/ALLPHYAD
XI
XO
CLK125_NDO/LED_MODE
RESET_N
LDO_O
ISET
J1001 JK0654219
LED1+
LED1−
LED2+
LED2−
MX1+
MXCT1
MX1−
MX2+
MXCT2
MX2−
MX3+
MXCT3
MX3−
MX4+
MXCT4
MX4−
SH
ETH7_PA+
ETH7_PA−
ETH7_PB+
ETH7_PB−
ETH7_PC+
ETH7_PC−
ETH7_PD+
ETH7_PD−
+3V3
GND
GNDPWR
I2C_SCK
I2C_SDA
25MHz_REFCLK
GLOBAL_RESET
Disable 125MHz CLK out
DNP
782763301
1V2
FB1001
FB1002
FB1003
Generic 1206 Footprints.
Populate according
to EMC needs.
Local 1.2V / 1A Buck Regulator
U1002
SC4626C
VIN
VOUT
EN
GND
LX
IHLP1616BZER2R2M1A
https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich
Sheet: /100Base-TX-PHY7/
File: 100Base-TX-PHY7.kicad_sch
Title: Open Hardware 10Base-T1L Switch
Size: A4
Date: 2023-04-07
Rev: REV A
KiCad E.D.A. kicad (6.0.9-0)
Id: 10/16

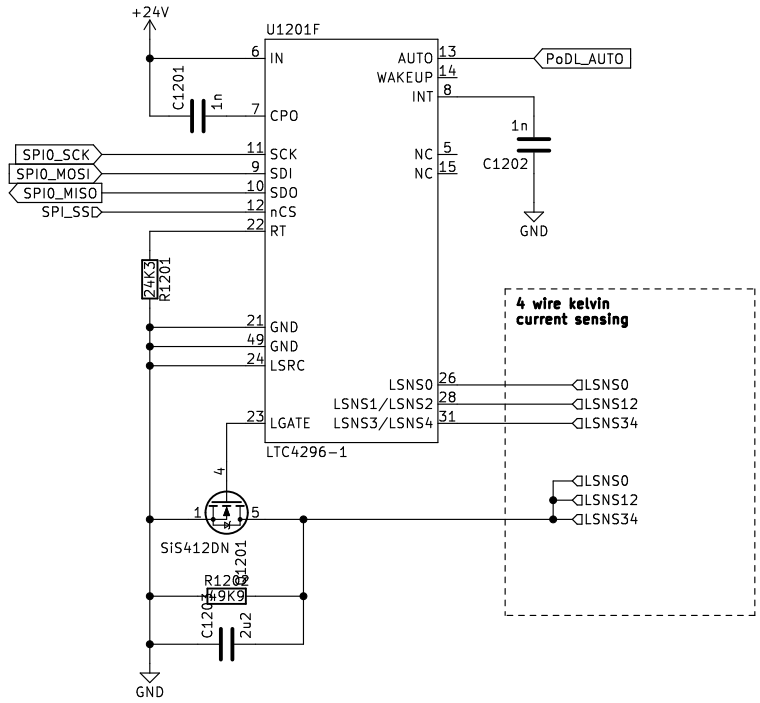


https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich

Sheet: /SJA1105Q Power/
File: SJA1105Q_Power.kicad_sch

Title: Open Hardware 10Base-T1L Switch

Size: A4	Date: 2023-04-07	**Rev: REV A**
KiCad E.D.A. kicad (6.0.9-0)		Id: 11/16

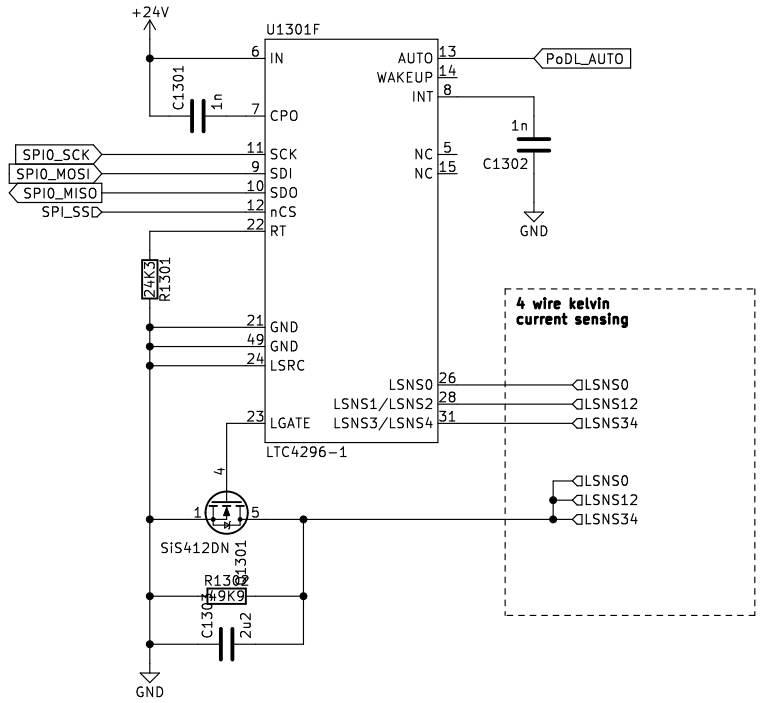


https://github.com/peterheinrich/Open_10Base-T1L_Switch
Open Hardware License CERN-OHL-P v2
Peter Heinrich

Sheet: /PoDL_REG0/
File: PoDL_REG.kicad_sch

Title: Open Hardware 10Base-T1L Switch

Size: A4	Date: 2023-04-07	**Rev: REV A**
KiCad E.D.A. kicad (6.0.9-0)		Id: 12/16



https://github.com/peterheinrich/Open_10Base-T1L_Switch
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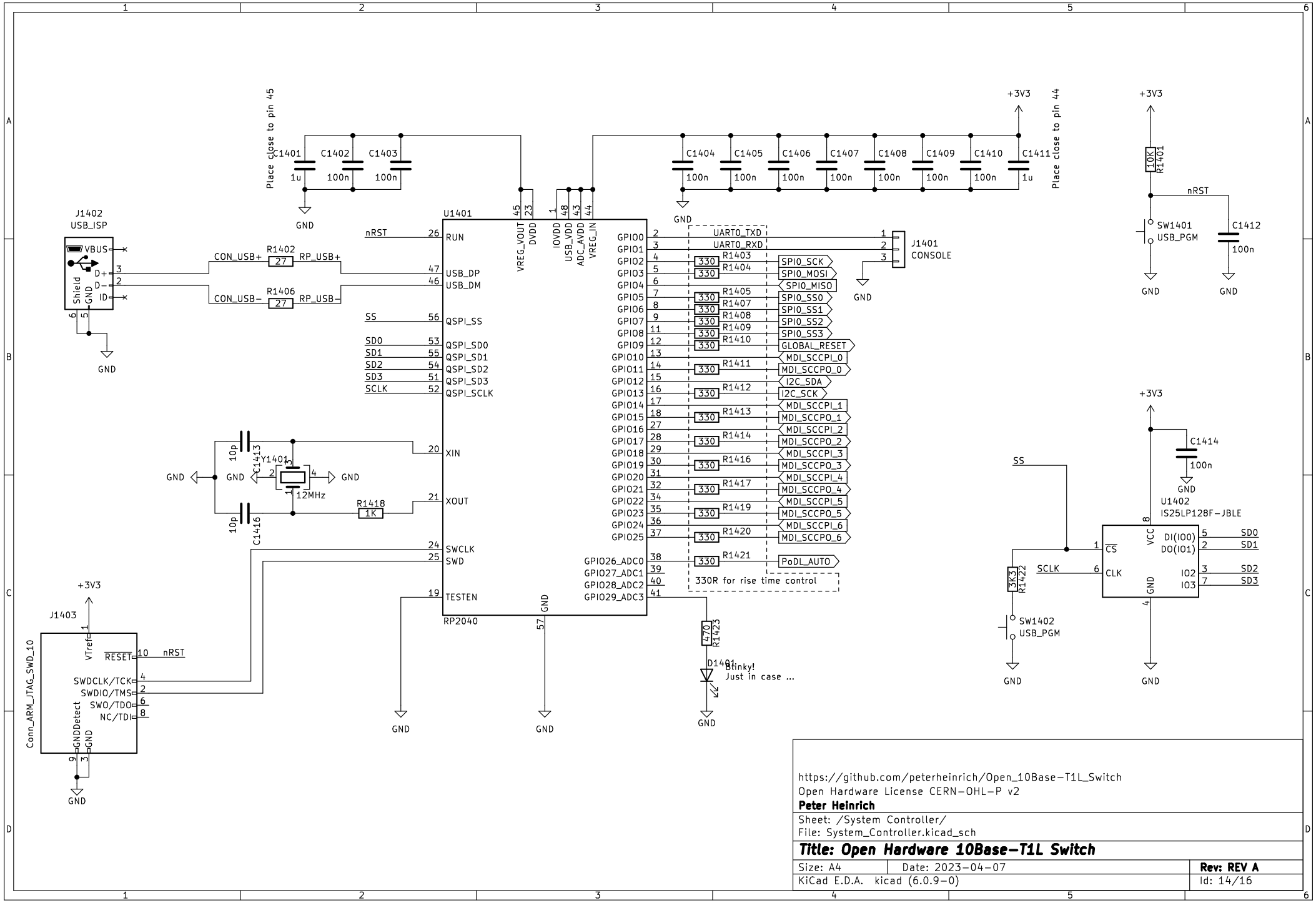
Sheet: /PoDL_REG1/
File: PoDL_REG.kicad_sch

Title: Open Hardware 10Base-T1L Switch

Size: A4	Date: 2023-04-07	**Rev: REV A**
KiCad E.D.A. kicad (6.0.9-0)		Id: 13/16



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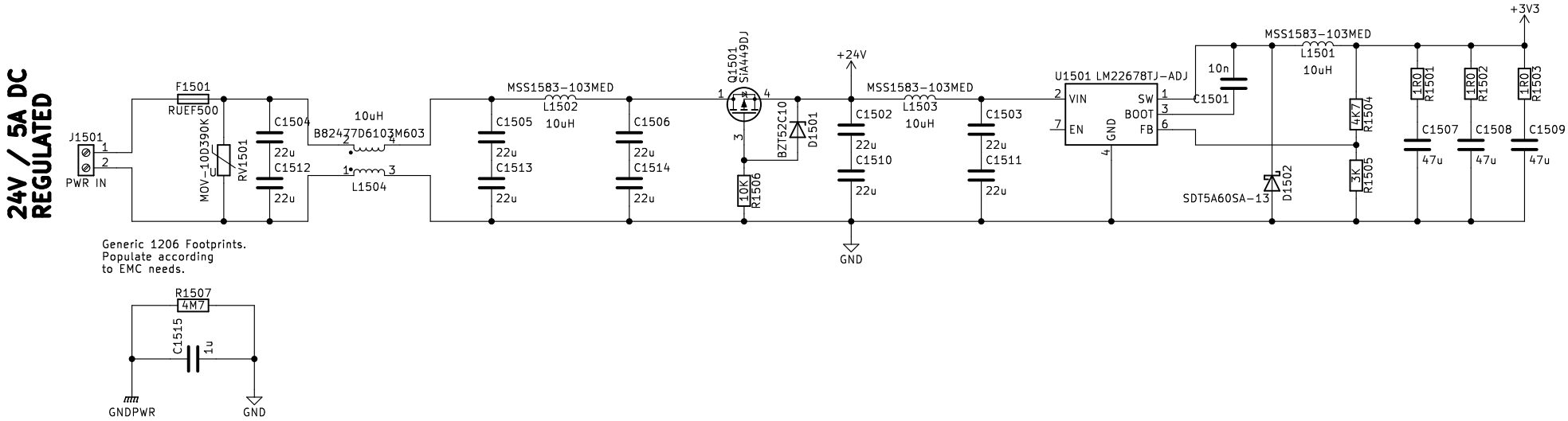
Sheet: /System Controller/
File: System_Controller.kicad_sch

Title: Open Hardware 10Base-T1L Switch

Size: A4	Date: 2023-04-07	**Rev: REV A**
KiCad E.D.A. kicad (6.0.9-0)		Id: 14/16



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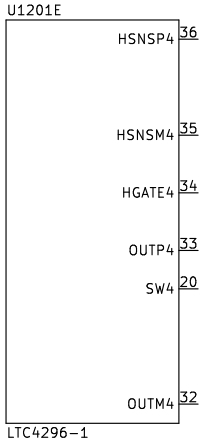
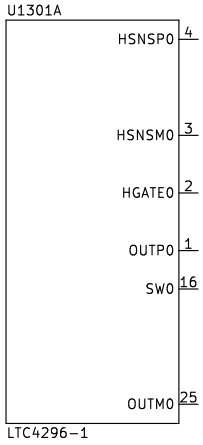
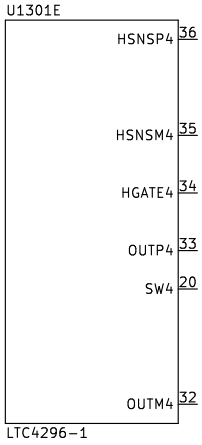
Sheet: /Power Supply/
File: Power_Supply.kicad_sch

Title: Open Hardware 10Base-T1L Switch

Size: A4	Date: 2023-04-07	**Rev: REV A**
KiCad E.D.A. kicad (6.0.9-0)		Id: 15/16







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Title:

Size: A4	Date:	**Rev:**
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