3.3V 4Gb SLC
NAND Flash Memory
Specification and Technical Notes

PSU4GA30AT-1bECC

PSU4GA30AT (X8)

Memory Cell: (2112 x 8bit)/page x 64 page/block x 4096 block/device
Or 2112 X 256K X 8bit

Register: 2112 X 8

Page Size: 2112 Byte

Block Size: (128K + 4K) Byte

Device: 4096 block

Document Title

4Gbit (512M x 8bit) NAND Flash Memory

Revision History

Rev.	Description	Date	Remark
0.1	Initial Draft	Aug. 2, 2013	Preliminary
0.2	1b-ECC Confirmation	Oct. 14, 2013	Preliminary
0.3	Revise Two-Plane Page Program Diagram	Apr. 8, 2014	Preliminary

4Gbit (512M x 8bit) NAND Flash Memory

1. Product List

Part Number	Vcc Range	Organization	Package
PSU4GA30AT	2.7V~3.6V	X8	48TSOP1

2. Features

- Voltage Supply: 3.3V (2.7 V ~ 3.6V)
- - Commercial Temperature: 0 ~ 70℃
  - Industrial Temperature: -40 ~ 85℃
- Organization
  X8:
  - Memory Cell Array: (512M + 16M) x 8bit
  - Data Register: (2K + 64) x 8bit
- Automatic Program and Erase
  X8:
  - Page Program: (2K + 64) Byte
  - Block Erase: (128K + 4K) Byte
- Page Read Operation
  - Page Size: (2K + 64) Byte (X8)
  - Random Read: 25us (Max.)
  - Serial Access: 25ns (Min.) (x8)
- Memory Cell: 1bit/Memory Cell
- Fast Write Cycle Time
  - Program time: 400us - typical
  - Block Erase time: 2ms - typical
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating Gate Technology
  - ECC Requirement: X8 - 1bit/512Byte,
  - Endurance: 100K Program/Erase cycles
  - Data Retention: 10 years
- Command Register Operation
- Automatic Page 0 Read at Power-Up Option
  - Boot from NAND support
  - Automatic Memory Download
- NOP: 4 cycles
- Cache Program Operation for High Performance Program
- Cache Read Operation
- Copy-Back Operation
- EDO mode
- OTP Operation
- Two-Plane Operation
- Bad-Block-Protect

3. Summary Description

The Powerchip PSU4GA30AT is a 512Mx8bit with spare 16Mx8bit capacity. The device is offered in 3.3V Vcc Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 4,096 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to write the 2,112-Byte page in typical 400us and an erase operation can be performed in typical 2ms on a 128K-Byte for X8 device block.

Data in the page mode can be read out at 25ns cycle time per Word. The I/O pins serve as the ports for address and command inputs as well as data input/output. The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array. This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This device includes extra feature: Automatic Read at Power Up.

4. Pin Configuration

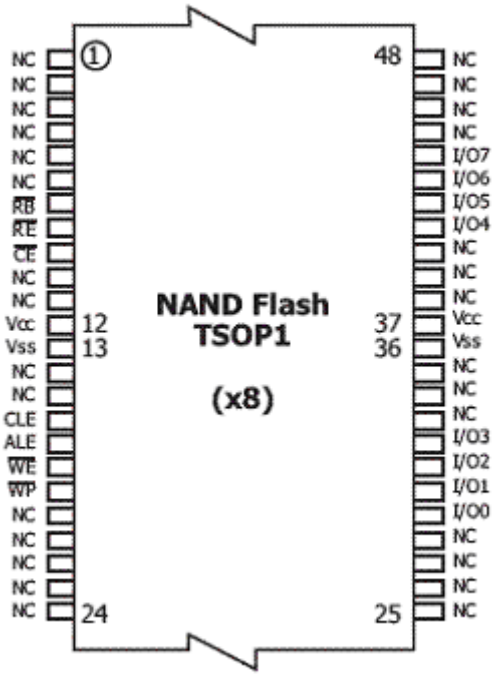
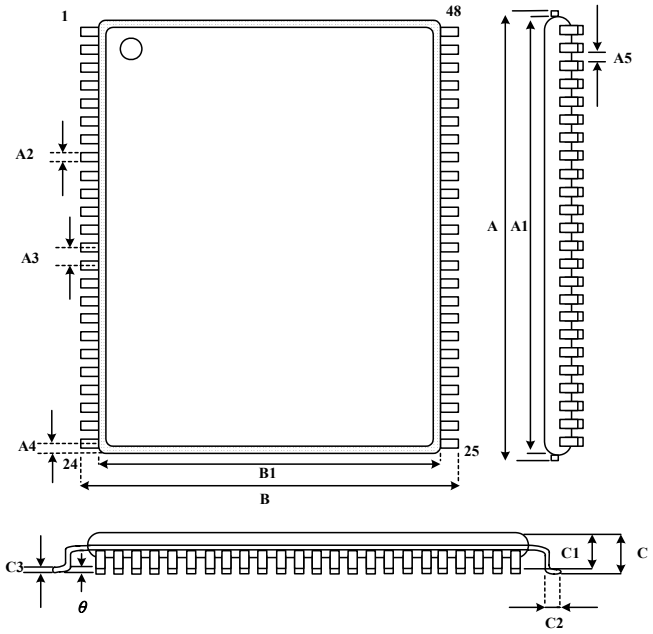


Figure Pin-Out Diagram of x8 Device



Unit:Millimeter (mm) ; θ : (˚)

ITEM	MIN	TYP	MAX
A	–	–	12.4
A1	11.9	–	12.1
A2	0.14	–	0.3
A3	–	0.5	–
A4	–	0.25	–
A5	–	0.1	–
B	19.8	–	20.2
B1	18.3	–	18.5
C	–	–	1.2
C1	0.9	–	1.1
C2	0.4	–	0.6
C3	0.09	–	0.2
θ (°)	0 (°)	–	10 (°)

Figure Diagram of 48-TSOP1

5. Pin Description

Pin Name	Pin Function
I/O0 ~ I/O7 (X8)	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the internal command registers. Commands are latched into the command register through the I/O ports on the rising edge of the WE# signal with CLE high.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high.
CE#	**CHIP ENABLE** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when it is active low, it drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WE#	**WRITE ENABLE** The WE# input controls writes to the I/O ports. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	**WRITE PROTECT** The WP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	**READY/BUSY OUTPUT** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**
N.C.	**NO CONNECTION** Lead is not internally connected.

NOTE : Connect all VCC and VSS pins of each device to common power supply outputs. Do not leave VCC or VSS disconnected.

6. Block Diagram

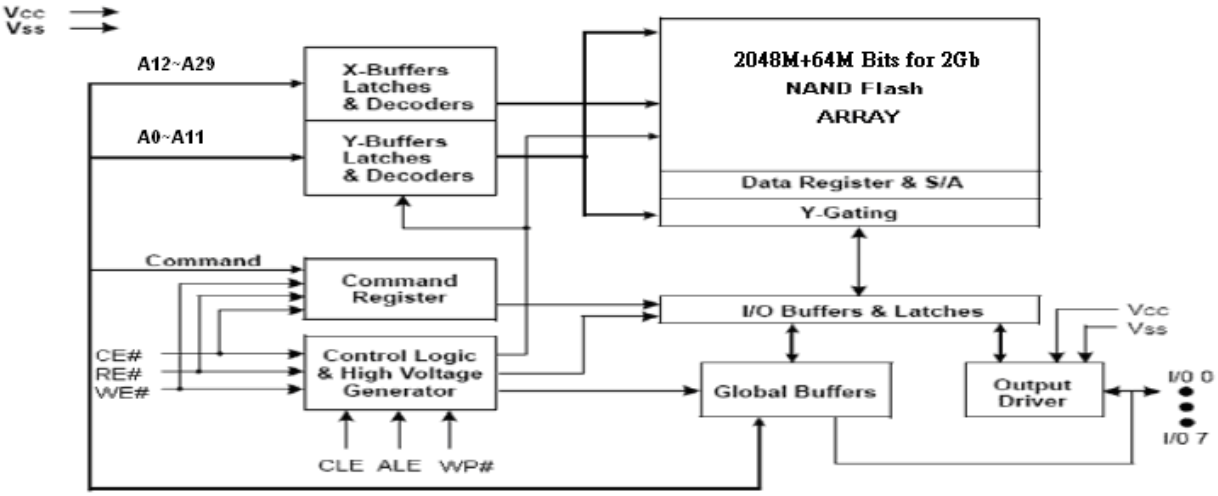


Figure Functional Block Diagram (x8)

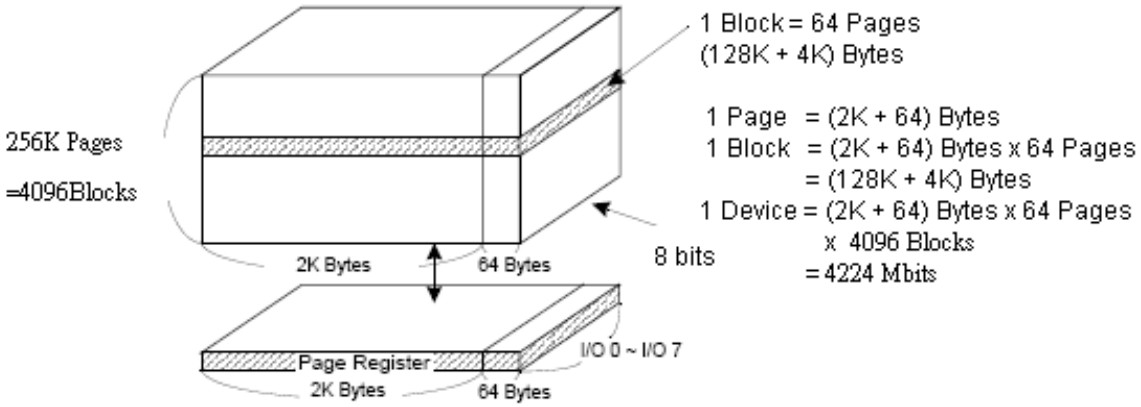


Figure Array Organization (x8)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	Address
1st cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_5	A_7	Column Address
2nd cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	Column Address
3rd cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	Row Address
4th cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	Row Address
5th cycle	A_{28}	A_{29}	*L	*L	*L	*L	*L	*L	Row Address

NOTE:

Column Address: Starting Address of the Register.
*L must be set to “Low”.
*The device ignores any additional input of address cycles than required.
A_{18} is for Plane Address setting.

Table Array Address (x8)

7. Product Introduction

The PSU4GA30AT is a 4,224Mbit memory organized as 256K rows (pages) by 2,112x8 columns. Spare 64x8 columns are located from column address of 2,048~2,111. A 2,112-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The program and read operations are executed on a page basis, while the erase operation is executed on a block basis. The memory array consists of 4,096 separately erasable 128K-byte blocks. It indicates that the bit-by-bit erase operation is prohibited on the PSU4GA30AT.

The PSU4GA30AT has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Those are latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input (1)	85h	-	
Random Data Output (1)	05h	E0h	
Read Status	70h	-	O
Read Status 2	F1h	-	O
Two-Plane Read(3)	60h-60h	30h	
Two-Plane Read for Copy-Back	60h-60h	35h	
Two-Plane Random Data Output(1) (3)	00h-05h	E0h	
Two-Plane Page Program(2)	80h-11h	81h-10h	
Two-Plane Copy-Back Program(2)	85h-11h	81h-10h	
Two-Plane Block Erase	60h-60h	D0h	
Cache Program	80h	15h	
Cache Read	31h	-	
Read Start For Last Page Cache Read	3Fh	-	
Two-Plane Cache Read(3)	60h-60h	33h	
Two-Plane Cache Program(2)	80h-11h	81h-15h	

NOTE :

1. Random Data Input/Output can be executed in a page.
2. Any command between 11h and 80h/81h/85h is prohibited except 70h/F1h and FFh.
3. Two-Plane Random Data Output must be used after Two-Plane Read operation or Two-Plane Cache Read operation.

Table Command Set

7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	Vcc	-0.6 to +4.6	V
	VIN	-0.6 to +4.6	
	VI/O	-0.6 to Vcc+0.3(<4.6V)	
Temperature Under Bias	TBIAS	-40 to +125	℃
Storage Temperature	TSTG	-65 to +150	℃
Short Circuit Current	IOS	5	mA

NOTE :
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

7.2 Recommended Operating Conditions

(Voltage reference to GND, TA=-40 to 85℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	2.7	3.3	3.6	V
Supply Voltage	Vss	0	0	0	V

7.3 DC and Operation Characteristics

(Recommended operating conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	ICC1	TBD tRC=25ns, CE#=VIL, IOUT=0mA	-	15	30	mA
	Program	ICC2	-	-	15		
	Erase	ICC3	-	-	15		
Stand-by Current (TTL)		ISB1	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)		ISB2	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc (max)	-	-	+/-10	
Output Leakage Current		ILO	VOUT=0 to Vcc (max)	-	-	+/-10	
Input High Voltage		VIH (1)		0.8xVCC	-	Vcc+0.3	V
Input Low Voltage, All inputs		VIL (1)		-0.3	-	0.2xVCC	
Output High Voltage Level		VOH	TBD IOH=-400 uA	2.4	-	-	
Output Low Voltage Level		VOL	TBD IOL=2.1mA	-	-	0.4	
Output Low Current (R/B#)		IOL (R/B#)	TBD VOL=0.4V	8	10	-	mA

NOTE :

1. VIL can undershoot to -0.4V and VIH can overshoot to VCC + 0.4V for durations of 20 ns or less.
2. Typical value are measured at Vcc=3.3V, TA=25℃. Not 100% tested.

7.4 Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
PSU4GA30AT	NVB	4,016	-	4,096	Block

NOTE :

1. The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits which cause status failure during program and erase operation. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

7.5 AC Test Condition

(Commercial: T_A=0 to 70℃, Industrial: T_A=-40 to 85℃, Vcc=2.7V ~ 3.6V)

Parameter	PSU4GA30AT
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load*	1 TTL GATE and CL=50pF

NOTE: Refer to 11.16 Ready/Busy#, R/B# output's Busy to Ready time is decided by the pull-up resistor (Rp) tied to the R/B# pin.

7.6 Capacitance

(T_A=25℃, V_{CC}=3.3V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	CI/O	VIL=0V	-	8	pF
Input Capacitance	CIN	VIN=0V	-	8	pF

NOTE: Capacitance is periodically sampled and not 100% tested.

7.7 Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input (5 clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input (5 clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X(1)	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}(2)	Stand-by	

NOTE :
1. X can be VIL or VIH.
2. WP# should be biased to CMOS high or CMOS low for standby.

7.8 Program / Erase Characteristics

(Commercial: T_A=0 to 70℃, Industrial: T_A=-40 to 85℃, Vcc=2.7V ~ 3.6V)

Parameter	Symbol	Min	Typ	Max	Unit
Average Program Time	tPROG	-	400	950	us
Dummy Busy Time for Cache Operation	tCBSY	-	3	950	us
Number of Partial Program Cycles in the Same Page	Nop	-	-	4	cycle
Block Erase Time	tBERS	-	2	10	ms
Dummy Busy Time for Two-Plane Page Program	tDBSY	-	0.5	1	us

NOTE :

1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V Vcc and 25℃ temperature.
2. **tPROG is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.**
3. tCBSY max. time depends on timing between internal program completion and data-in.

7.9 AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS(1)	12	-	ns
CLE Hold Time	tCLH	5	-	ns
CE# Setup Time	tCS(1)	20	-	ns
CE# Hold Time	tCH	5	-	ns
WE# Pulse Width	tWP	12	-	ns
ALE Setup Time	tALS(1)	12	-	ns
ALE Hold Time	tALH	5	-	ns
Data Setup Time	tDS(1)	12	-	ns
Data Hold Time	tDH	5	-	ns
Write Cycle Time	tWC	25	-	ns
WE# High Hold Time	tWH	10	-	ns
Address to Data Loading Time	tADL(2)	70(2)	-	ns

NOTE :

1. The transition of the corresponding control pins must occur only once while WE# is held low.
2. tADL is the time from the WE rising edge of final address cycle to the WE# rising edge of first data cycle.

7.10 AC Characteristics for Operation

Parameter		Symbol	Min	Max	Unit
Data Transfer from Cell to Register		tR	-	25	us
ALE to RE# Delay		tAR	10	-	ns
CLE to RE# Delay		tCLR	10	-	ns
Ready to RE# Low		tRR	20	-	ns
RE# Pulse Width		tRP	12	-	ns
WE# High to Busy		tWB	-	100	ns
WP# Low to WE# Low (disable mode)		tWW	100	-	ns
WP# High to WE# Low (enable mode)					
Read Cycle Time		tRC	25	-	ns
RE# Access Time		tREA	-	20	ns
CE# Access Time		tCEA	-	25	ns
RE# High to Output Hi-Z		tRHZ	-	100	ns
CE# High to Output Hi-Z		tCHZ	-	30	ns
CE# High to ALE or CLE Don't care		tCSD	0		ns
RE# High to Output Hold		tRHOH	15	-	ns
RE# Low to Output Hold		tRLOH	5		ns
CE# High to Output Hold		tCOH	15	-	ns
RE# High Hold Time		tREH	10	-	ns
Output Hi-Z to RE# Low		tIR	0	-	ns
RE# High to WE# Low		tRHW	100	-	ns
WE# High to RE# Low		tWHR	60	-	ns
Device Resetting Time during…	Read	tRST	-	5	us
	Program		-	10	us
	Erase		-	500	us
	Ready		-	5 (1)	us
Cache Busy in Read Cache (following 31h and 3Fh)		tDCBSYR	-	30	us

NOTE: If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

8. NAND Flash Technical Notes

8.1 Mask Out Initial Invalid Block(s)

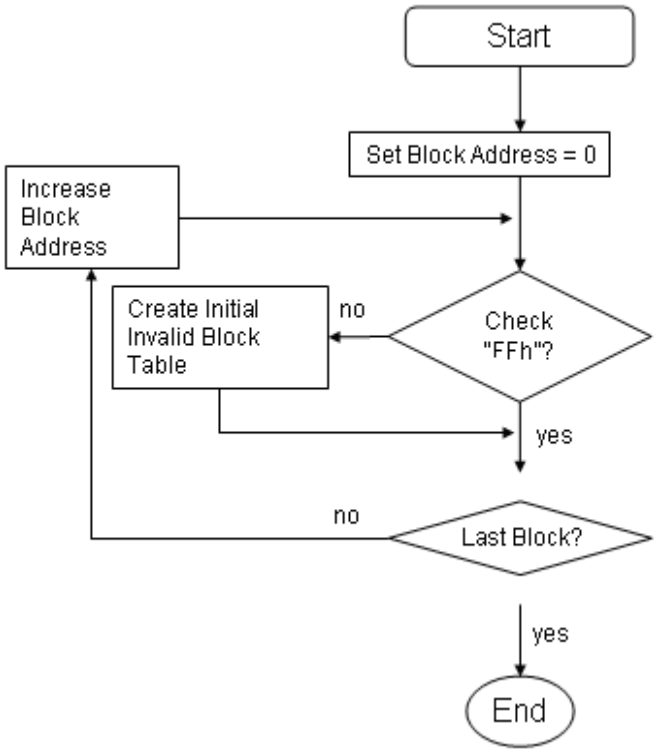
Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Powerchip. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/512Byte ECC.

8.2 Identifying Initial Invalid Block(s) and Block Replacement Management

Unpredictable behavior may result from programming or erasing the defective blocks. Figure below illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.

A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address of 2,048. If the read data is not FFh, the block is interpreted as an invalid block. Do not erase or program factory-marked bad blocks. The host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.



Check “FFh” at column address 2048 of the first page and the second page

```
For (i=0; i<Num_of_LUs; i++)
{
     For (j=0; j<Blocks_Per_LU; j++)
     {
          Defect_Block_Found=False;

          Read_Page(lu=i, block=j, page=0);
          If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

          Read_Page(lu=i, block=j, 1);
          If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

          If (Defect_Block_Found)   Mark_Block_as_Defective(lu=i, block=j);
     }

  }
```

Figure Algorithm for Bad Block Scanning

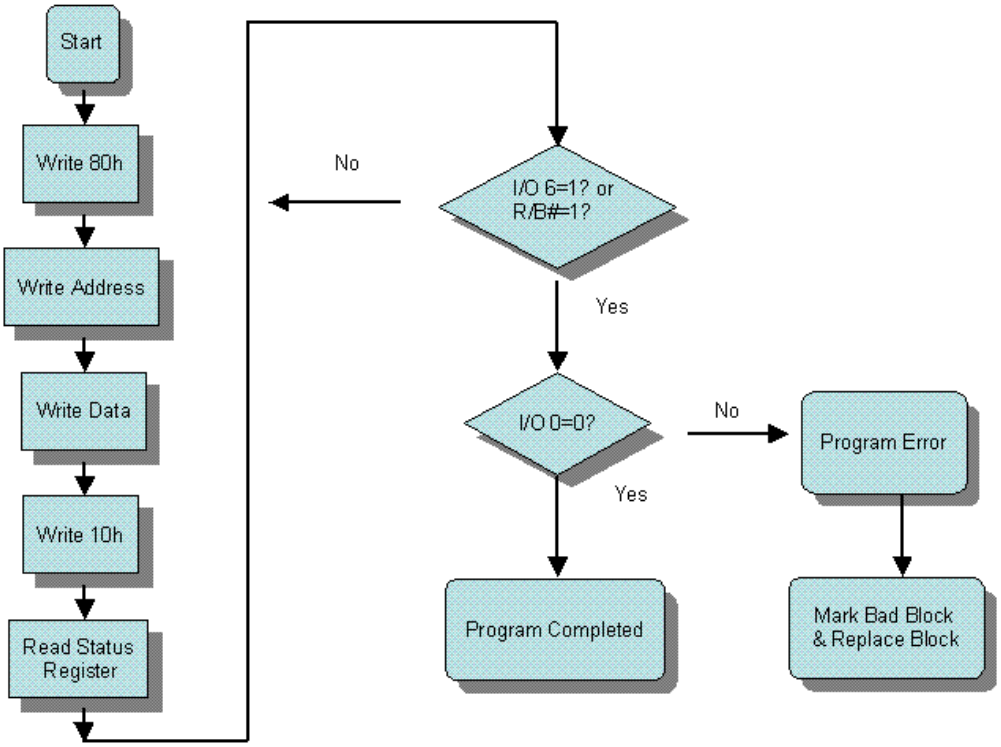
8.3 Error in Write or Read Operation

Within its lifetime, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

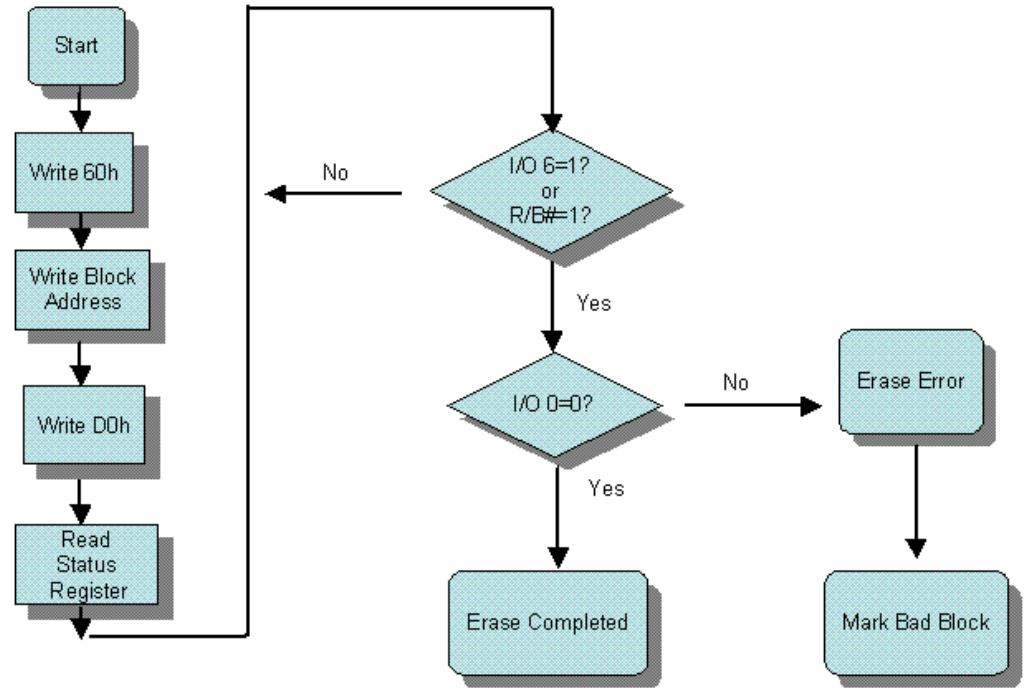
Failure Mode		Detection and Countermeasure Sequence
Write	Erase failure	Read Status after Erase → Block Replacement
	Program failure	Read Status after Program → Block Replacement
Read	Up to 4 bits failure	Verify ECC → ECC Correction

NOTE: Error Correcting Code → RS Code or BCH Code etc.
Example: 1bit correction / 512 Byte

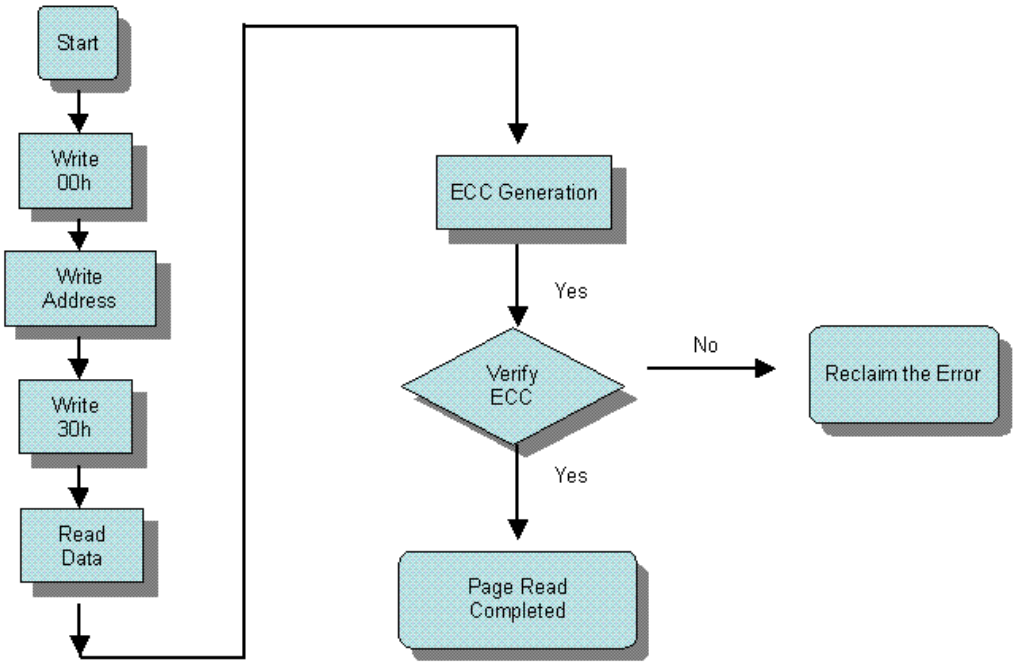
Program Flow Chart



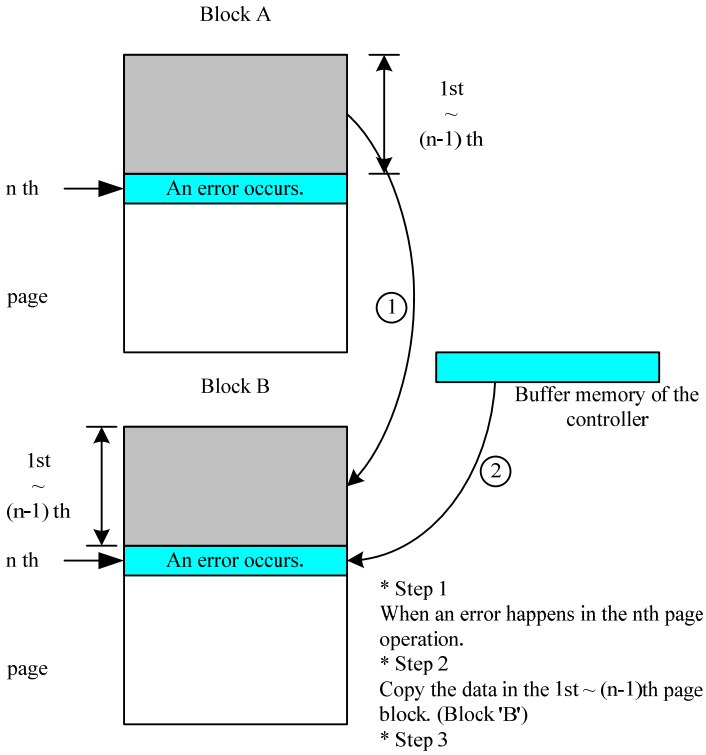
Erase Flow Chart



Read Flow Chart



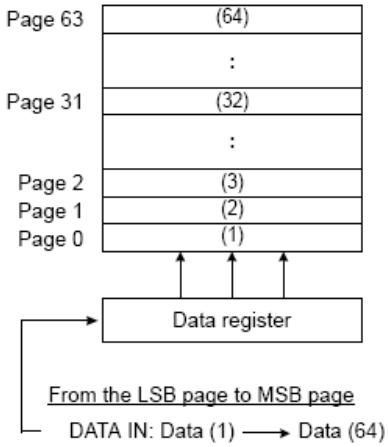
Block Replacement

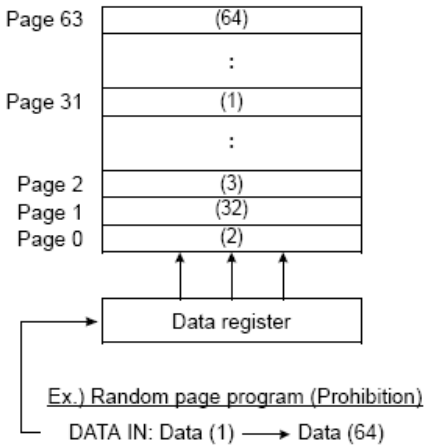


* Step 1
When an error happens in the nth page of the Block 'A' during erase or program operation.
* Step 2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
* Step 3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'
* Step 4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

8.4 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.





8.5 System Interface Using CE# Don't Care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications that use slow cycle time on the order of μ-seconds, de-activating CE# during the data-loading and serial access would provide significant savings in power consumption.

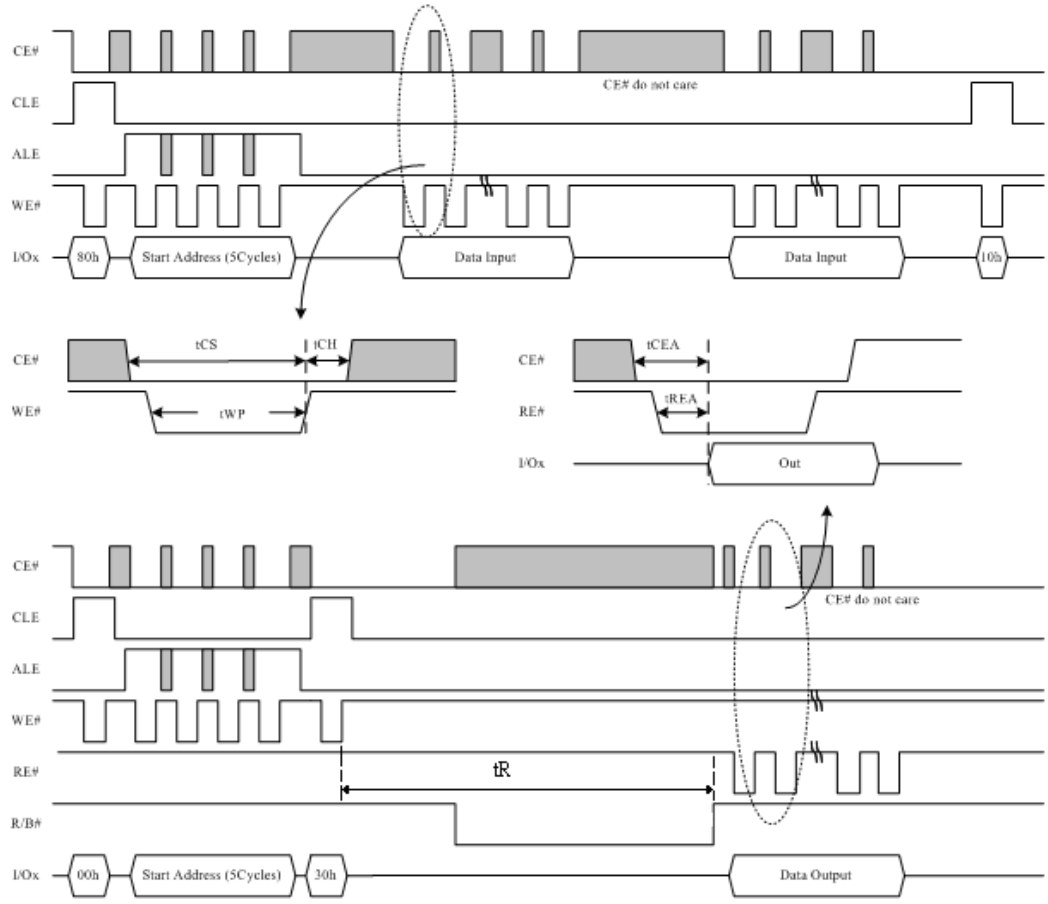


Figure Program/Read Operation with "CE# not-care"

Address Information

Device	Data	I/O	Address				
	Data In/Out	I/Ox	Col. Add1	Col. Add2	Row Add1	Row Add2	Row Add3
PSU4GA30AT (x8)	2,112Byte	I/O 0~I/O 7	A0 ~ A7	A8 ~ A11	A12 ~ A19	A20 ~ A27	A28 ~ A29

9. Timing Diagrams

9.1 Command Latch Cycle

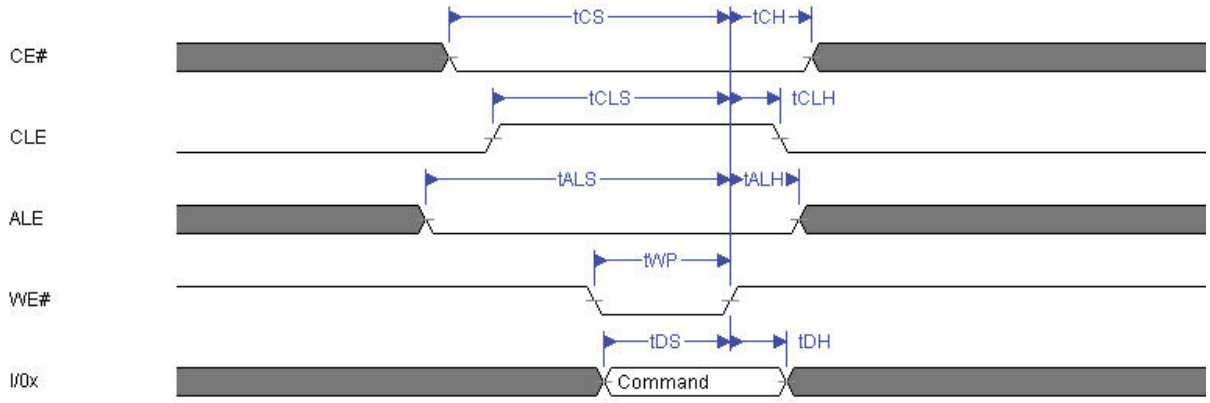


Figure Command Latch Cycle

9.2 Address Latch Cycle

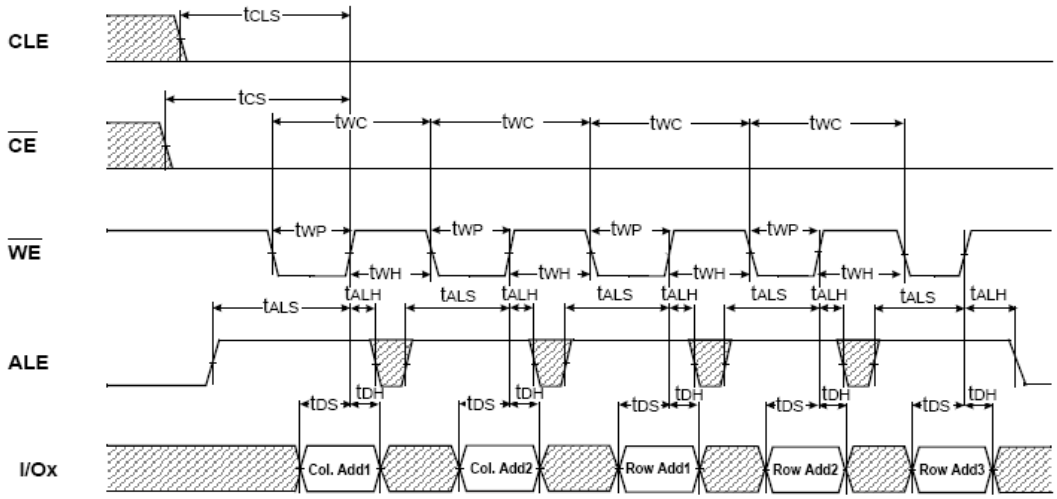


Figure Address Latch Cycle

9.3 Input Data Latch Cycle

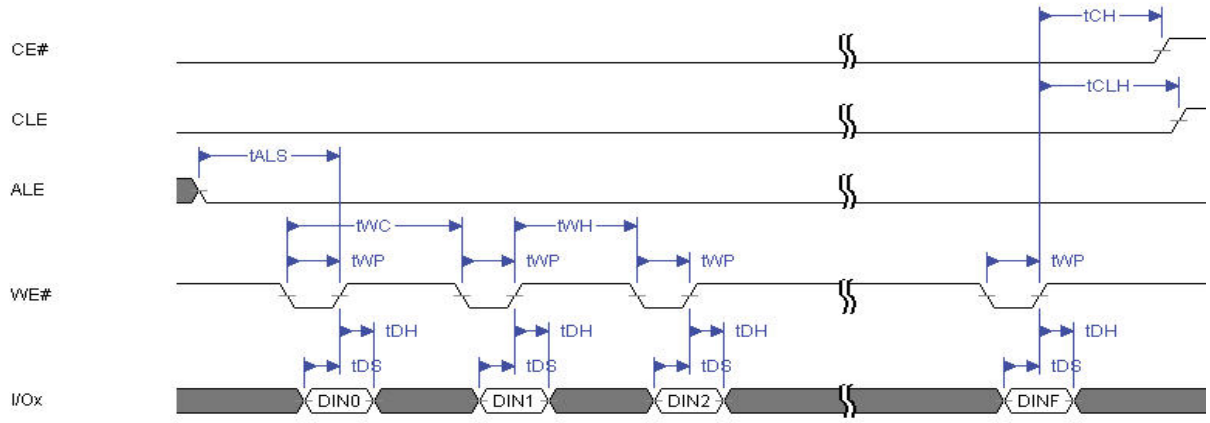
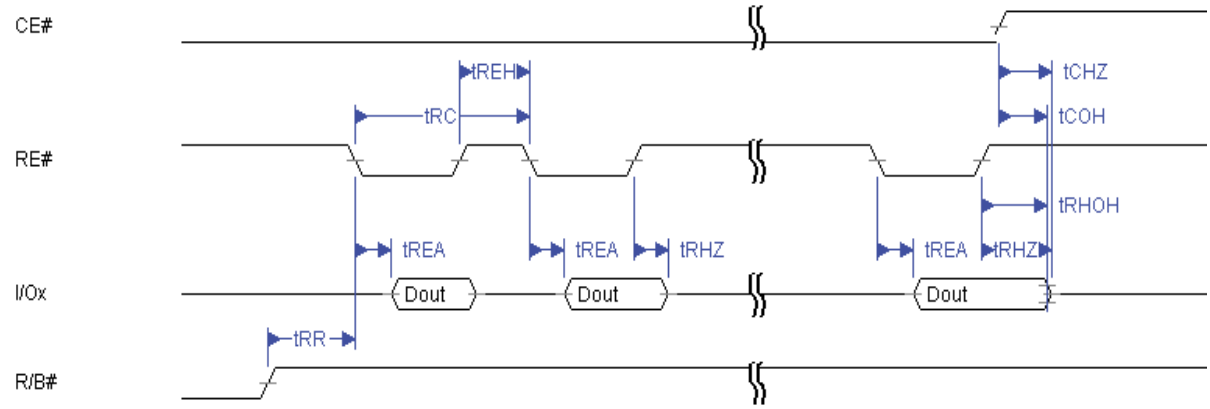


Figure Input Data Latch Cycle

9.4 Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)

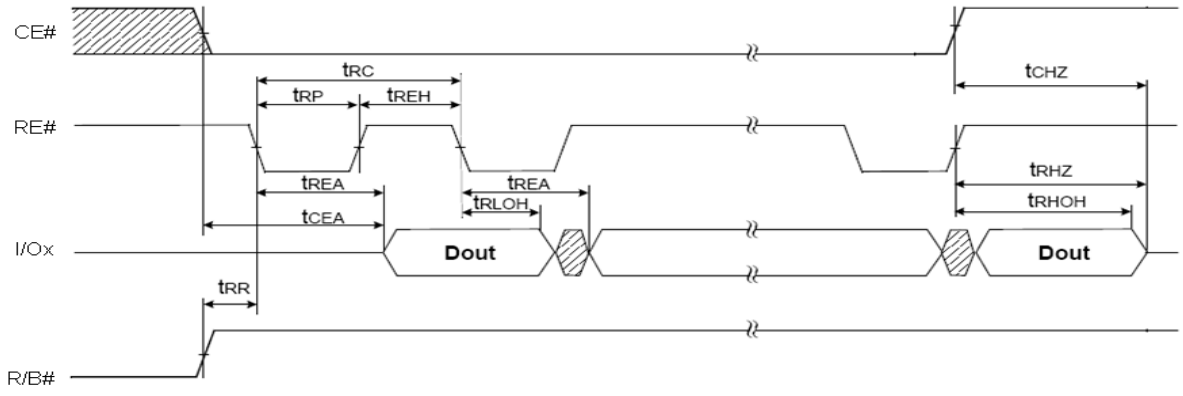


NOTE:

1. Dout transition is measured at ±200mV from steady state voltage at I/O with load.
2. t_{RHOH} starts to be valid when frequency is lower than 33MHz.

Figure Sequential Out Cycle after Read

9.5 Serial Access Cycle after Read (EDO Type CLE=L, WE#=H, ALE=L)



NOTE:
1. Transition is measured at +/-200mV from steady state voltage with load.
   This parameter is sample and not 100% tested. (tCHZ, tRHZ)
2. tRLOH is valid when frequency is higher than 33MHZ.
   tRHOH starts to be valid when frequency is lower than 33MHZ.

Figure Sequential Out Cycle after Read (EDO Type CLE=L, WE#=H, ALE=L)

9.6 Status Read Cycle

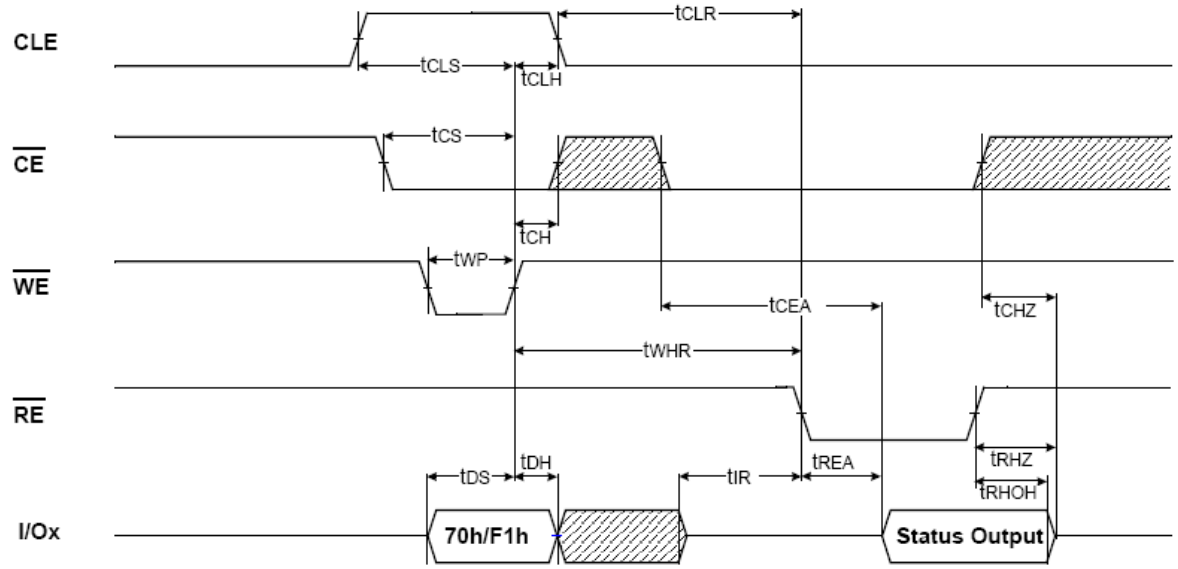


Figure Status Read Cycle

9.7 Read Operation

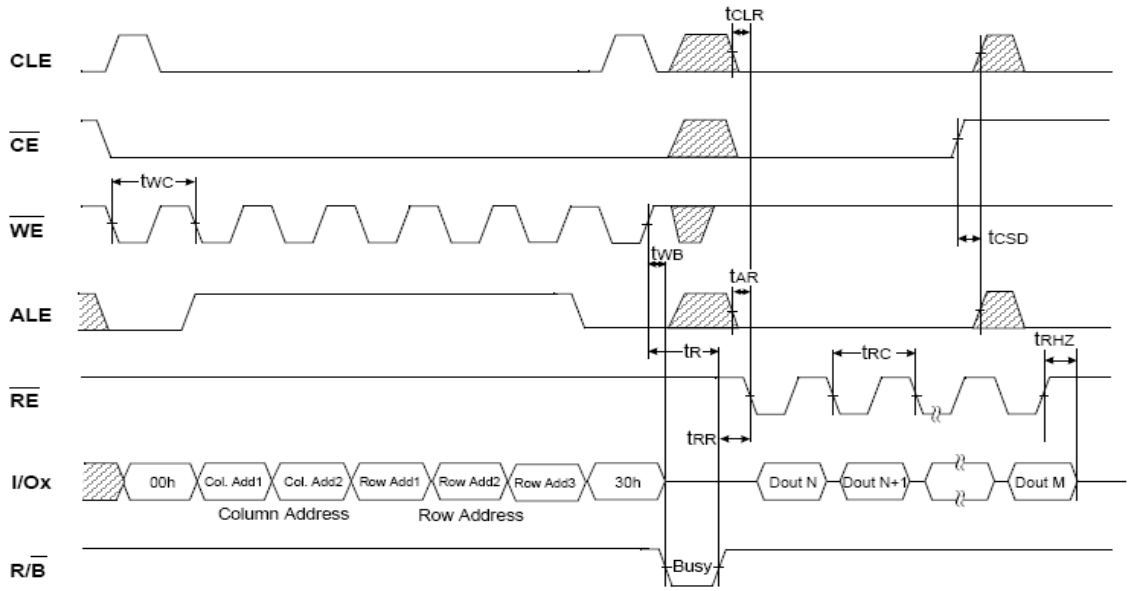


Figure Read Operation (Read One Page)

9.8 Read Operation (Intercepted by CE#)

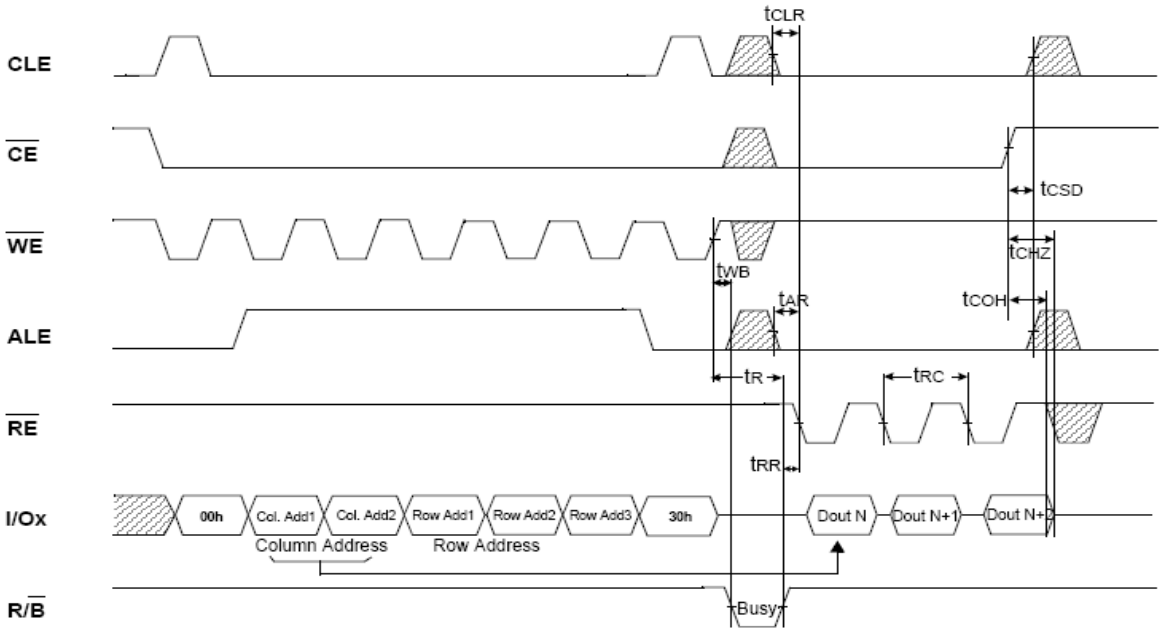


Figure Read Operation Intercepted by CE#

9.9 Random Data Output In a Page

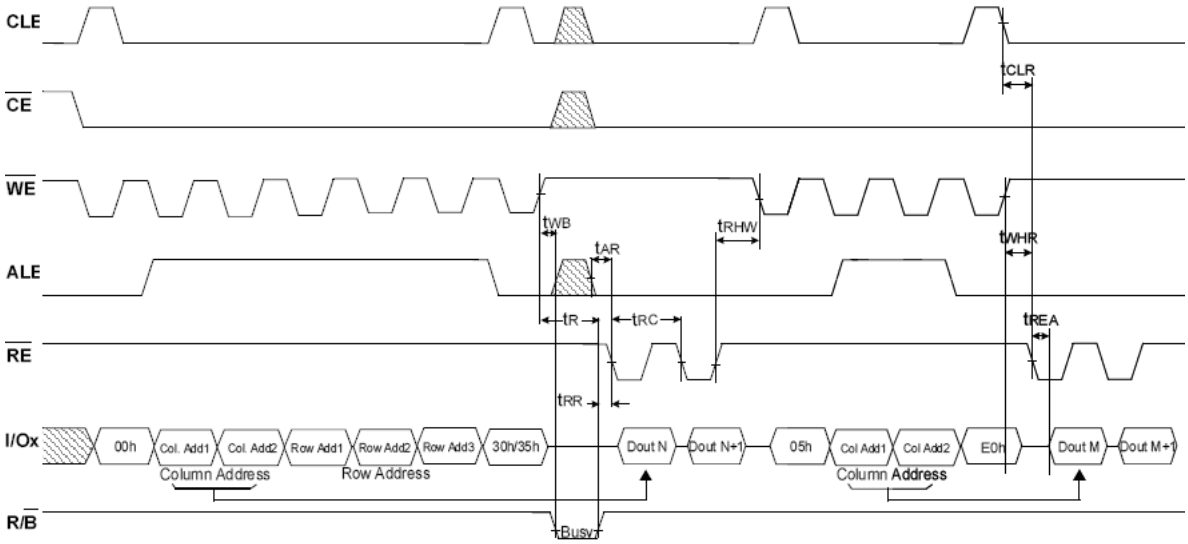


Figure Random Data Output

9.10 Page Program Operation

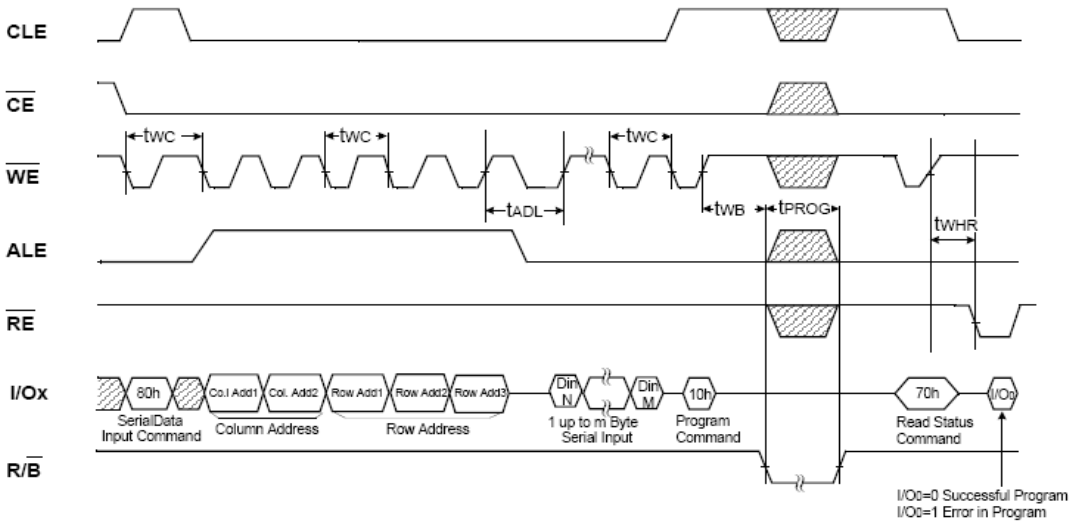
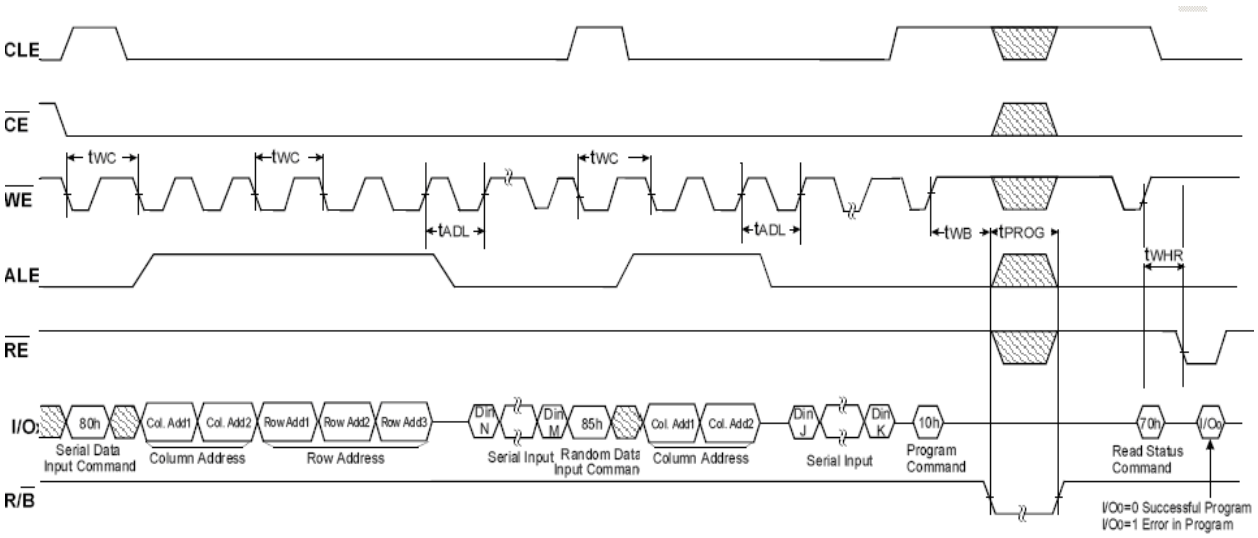


Figure Page Program Operation

9.11 Page Program Operation with Random Data Input



NOTE: t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of the first data cycle.

Figure Random Data Input

9.12 Copy-Back Operation with Random Data Input

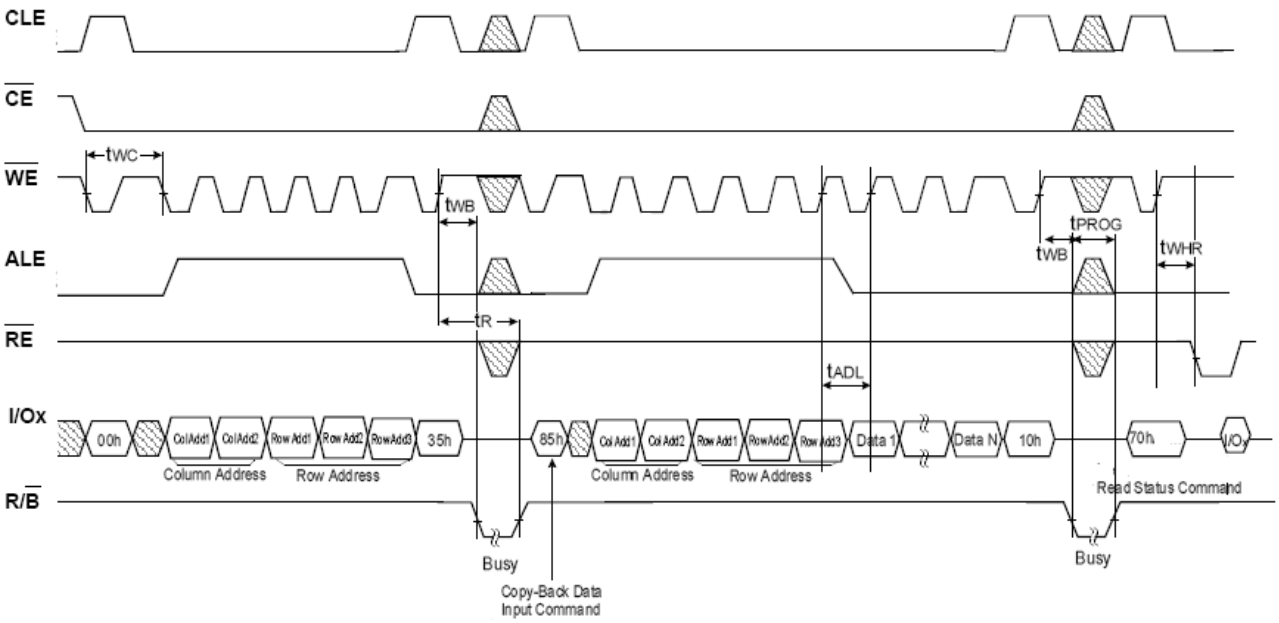


Figure Copy-Back Operation with Random Data Input

9.13 Cache Program Operation

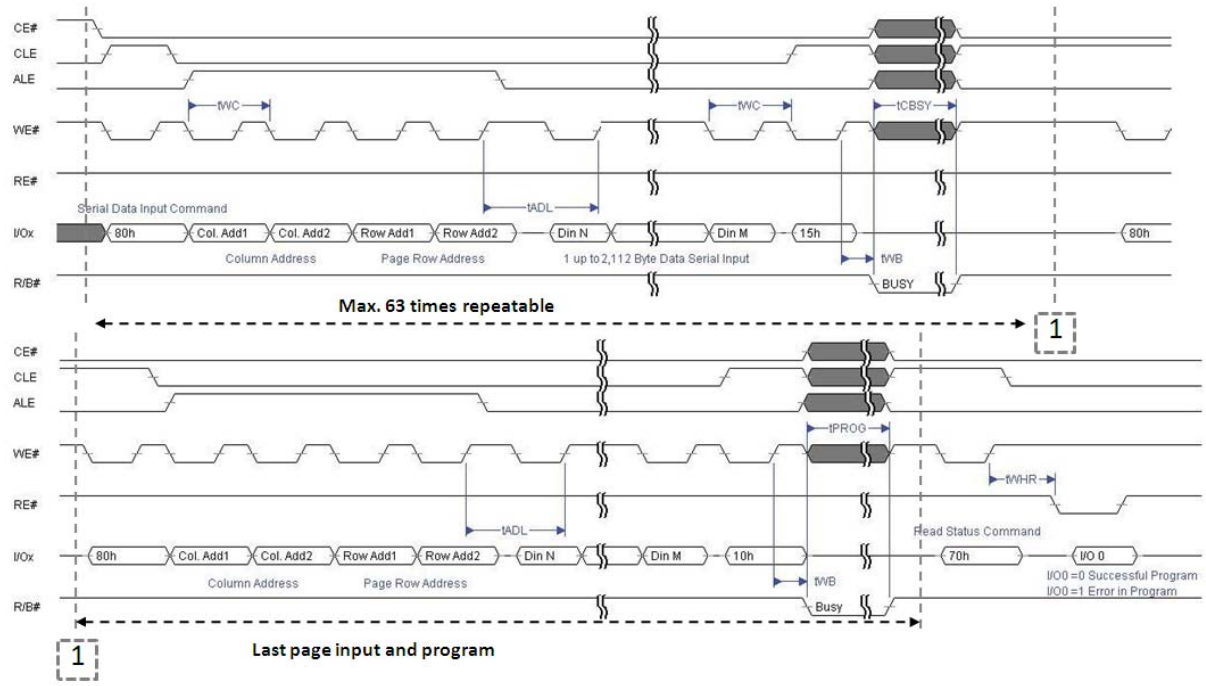


Figure Cache Program Operation

9.14 Cache Read Operation

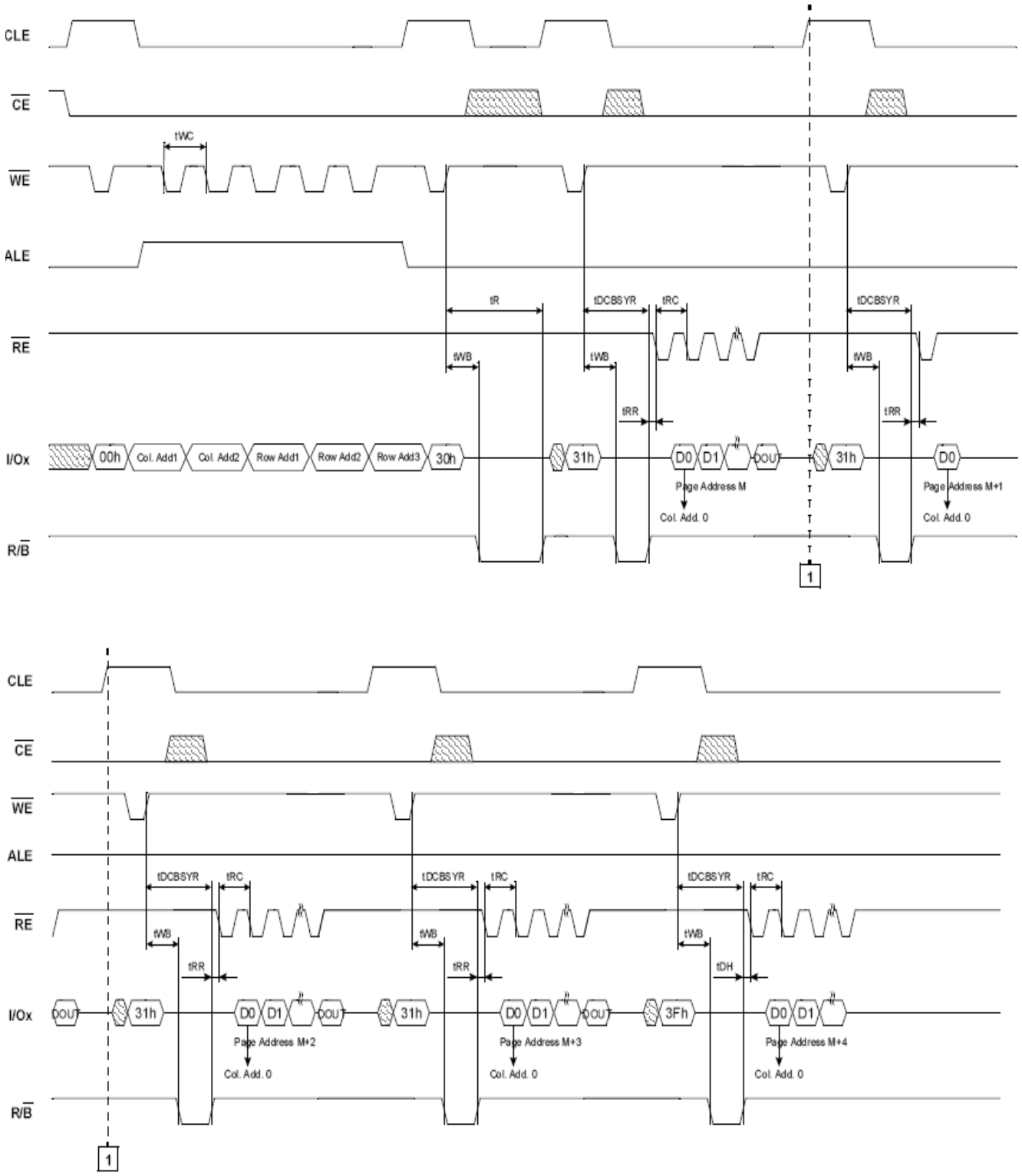


Figure Cache Read Operation

9.15 Block Erase Operation

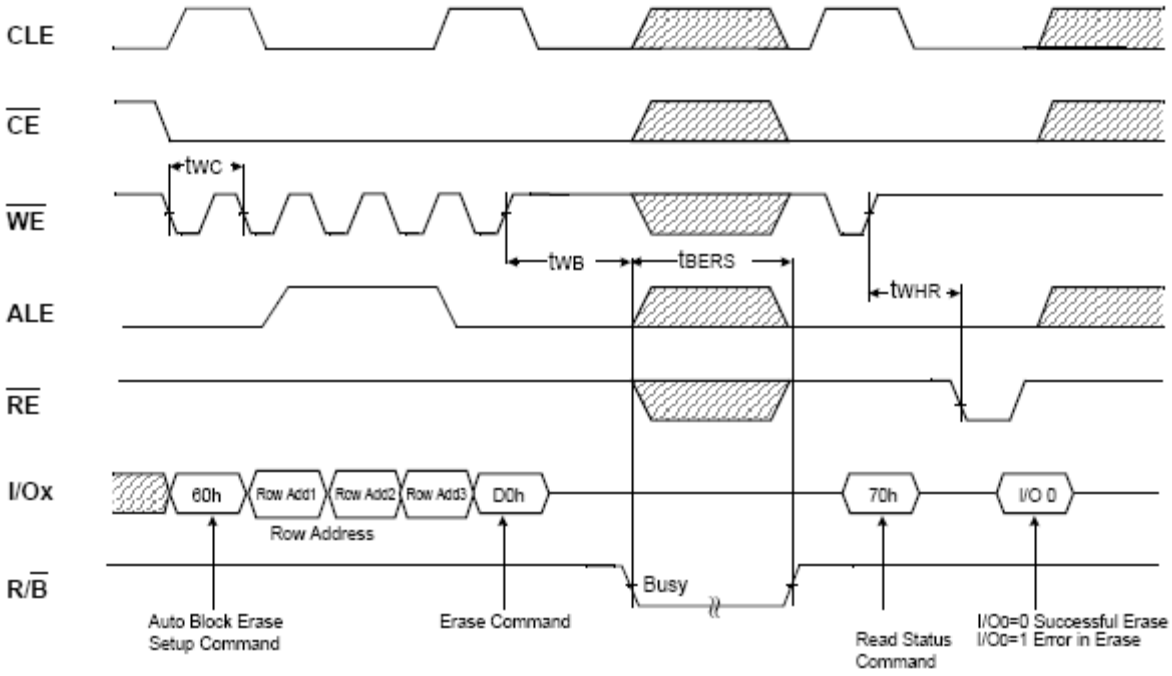


Figure Block Erase Operation

9.16 Read ID Operation

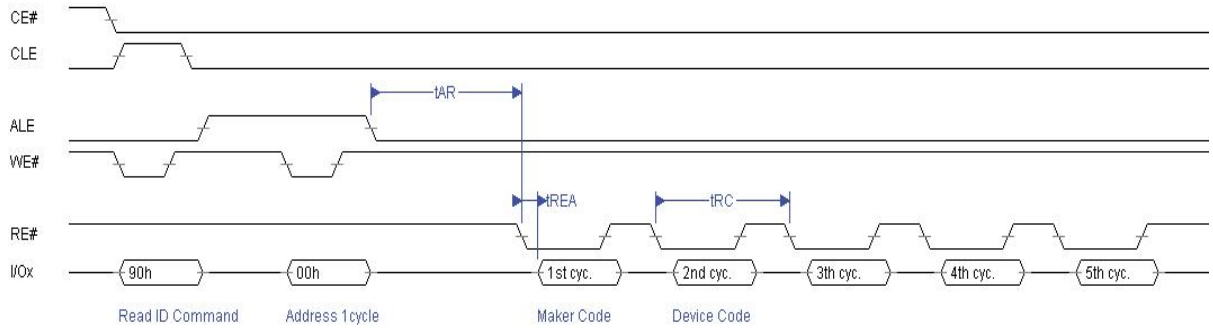


Figure Read ID Operation

9.17 Two-plane Page Read Operation with Two-plane Random Data Out

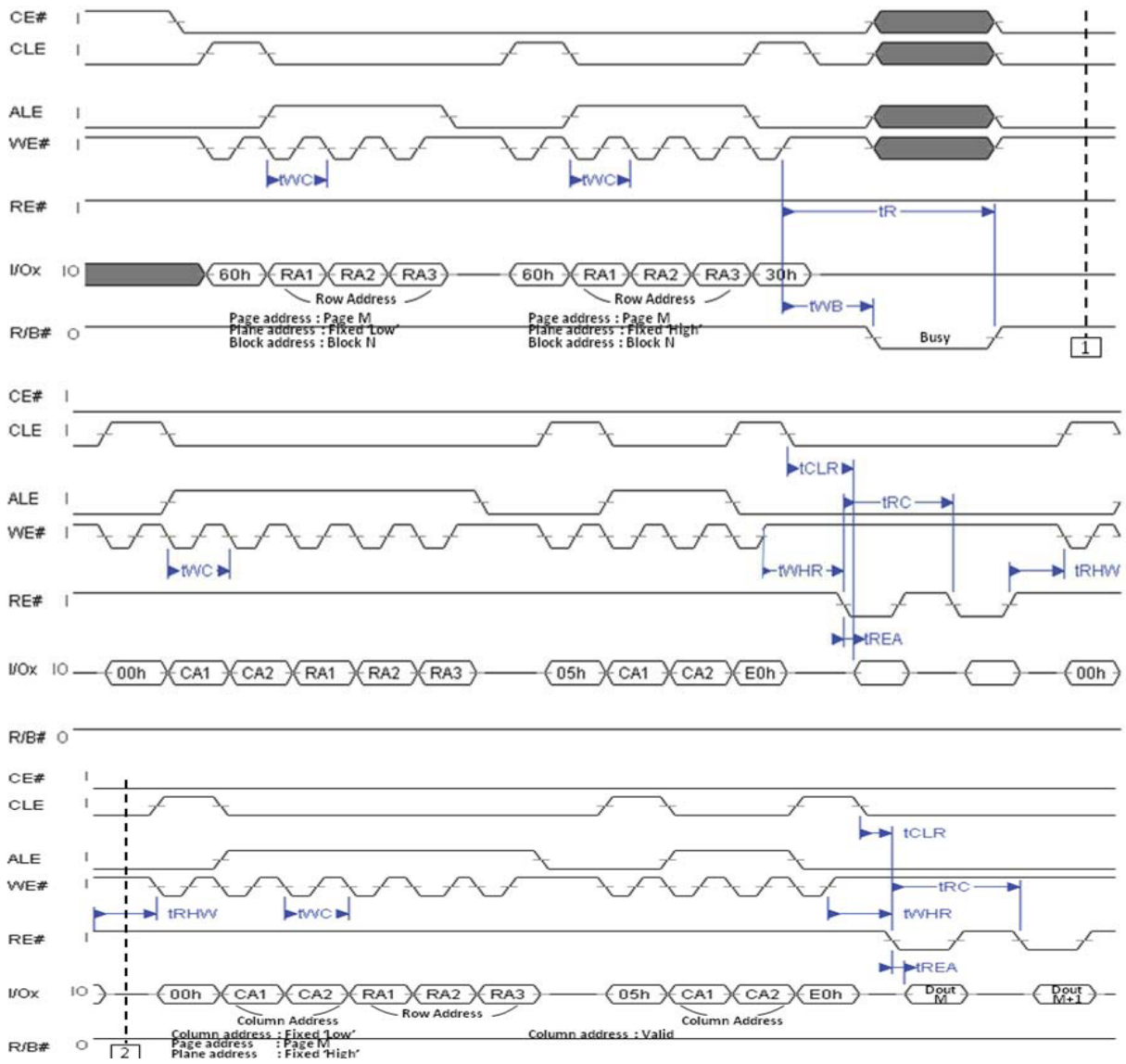
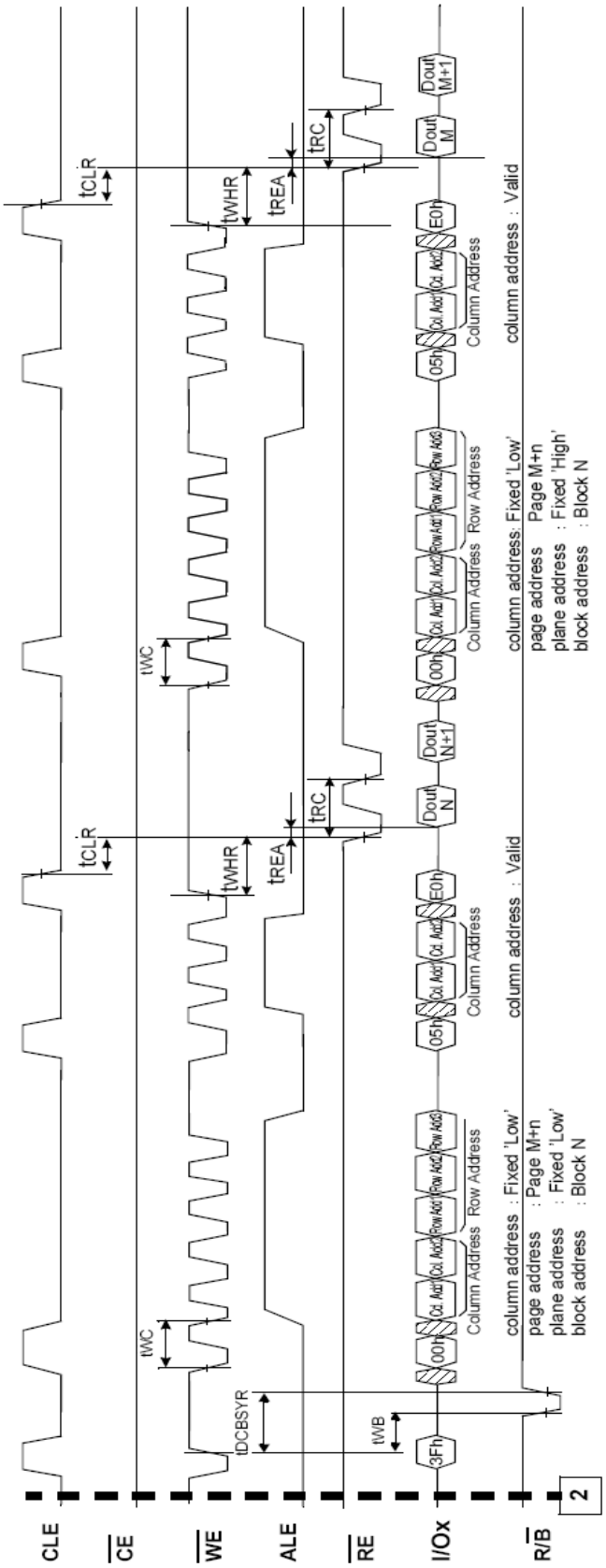


Figure Two-plane Page Read Operation with Two-plane Random Data Out

9.18 Two-plane Cache Read Operation



NOTE:
1. The column address will be reset to 0 by the 3Fh command input.
2. Cache Read operation is available only within a block.
3. Make sure to terminate the operation with 3Fh command. If the operation is terminated by 31h command, monitor I/O6 (Ready/Busy) by issuing Status Read Command (70h) and make sure the previous page read operation is completed. If the page read operation is completed, issue FFh reset before next operation.

Figure Two-plane Cache Read Operation

9.19 Two-plane Page Program Operation

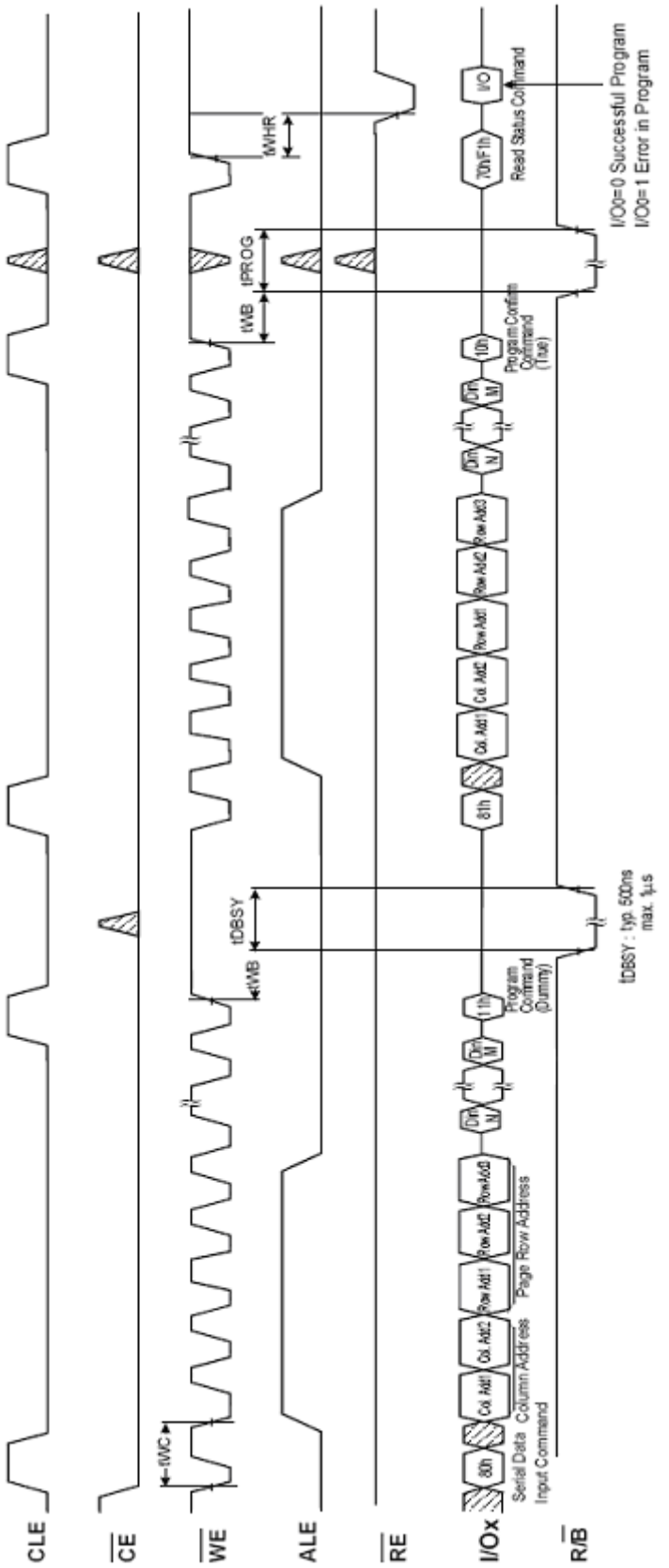


Figure Two-plane Page Program Operation

9.20 Two-plane Cache Program Operation

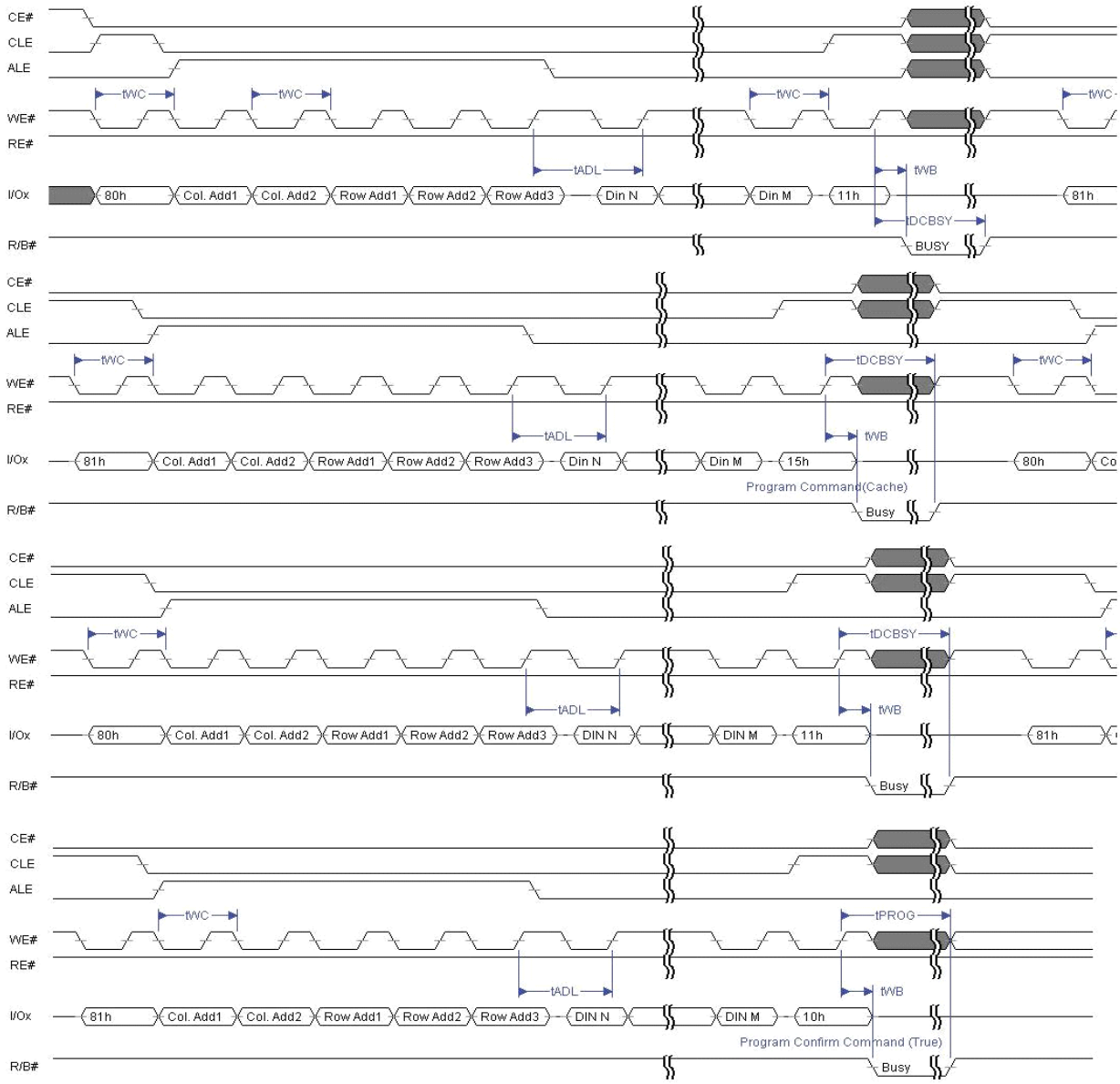


Figure Two-plane Cache Program Operation

9.21 Two-plane Block Erase Operation

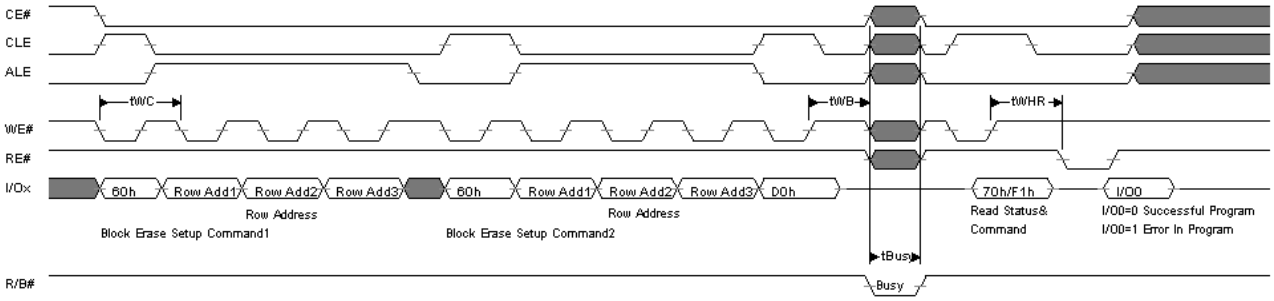


Figure Two-plane Block Erase Operation

10. ID Definition Table

90 ID : Access command = 90H

Part No.	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle	6th ~ 8th Cycle
PSU4GA30AT (X8)	C8h	DCh	90h	95h	56h	7Fh

	Description
1st Byte	Maker Code
2nd Byte	Device Code
3rd Byte	Internal Chip Number, Cell Type, etc
4th Byte	Page Size, Block Size, etc
5th Byte	Plane Number, Plane Size, ECC Level
6th Byte	JEDEC Maker Code Continuation Code, 7Fh
7th Byte	JEDEC Maker Code Continuation Code, 7Fh
8th Byte	JEDEC Maker Code Continuation Code, 7Fh

3rd ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1 2 4 8							0 0 1 1	0 1 0 1
Cell Type	2 Level Cell 4 Level Cell 8 Level Cell 16 Level Cell					0 0 1 1	0 1 0 1		
Number of Simultaneously Programmed Pages	1 2 4 8			0 0 1 1	0 1 0 1				
Interleave Program Between Multiple Chips	Not Support Support		0 1						
Cache Program	Not Support Support	0 1							

4th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB 2KB 4KB 8KB							0 0 1 1	0 1 0 1
Redundant Area Size (Byte/512Byte)	8 16						0 1		
Block Size (w/o redundant area)	64KB 128KB 256KB 512KB			0 0 1 1	0 1 0 1				
Organization	X8 X16		0 1						
Serial Access Time	45ns Reserved 25ns Reserved	0 0 1 1				0 1 0 1			

5th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	4bit/512B 2bit/512B 1bit/512B Reserved							0 0 1 1	0 1 0 1
Plane Number	1 2 4 8					0 0 1 1	0 1 0 1		
Plane Size(without Redundant Area)	64Kb 128Kb 256Kb 512Kb 1Gb 2Gb 4Gb 8Gb		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1				
Reserved	Reserved	0							

6th ~ 8th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
JEDEC Maker Code Continuation Code	7F	0	1	1	1	1	1	1	1

11. Device Operation

11.1 Page Read

Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h command, five-cycle address, and 30h command. After initial power up, the 00h command can be skipped because it has been latched in the command register. The 2,112Byte of data on a page are transferred to cache registers via data registers within 25us (tR). Host controller can detect the completion of this data transfer by checking the R/B# output. Once data in the selected page have been loaded into cache registers, each Byte can be read out in 25ns cycle time by continuously pulsing RE#. The repetitive high-to-low transitions of RE# clock signal make the device output data starting from the designated column address to the last column address.

The device can output data at a random column address instead of sequential column address by using the Random Data Output command. Random Data Output command can be executed multiple times in a page.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.

A page read sequence is illustrated in Figure below, where column address, page address are placed in between commands 00h and 30h. After tR read time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 30h. Host controller can toggle RE# to access data starting with the designated column address and their successive bytes.

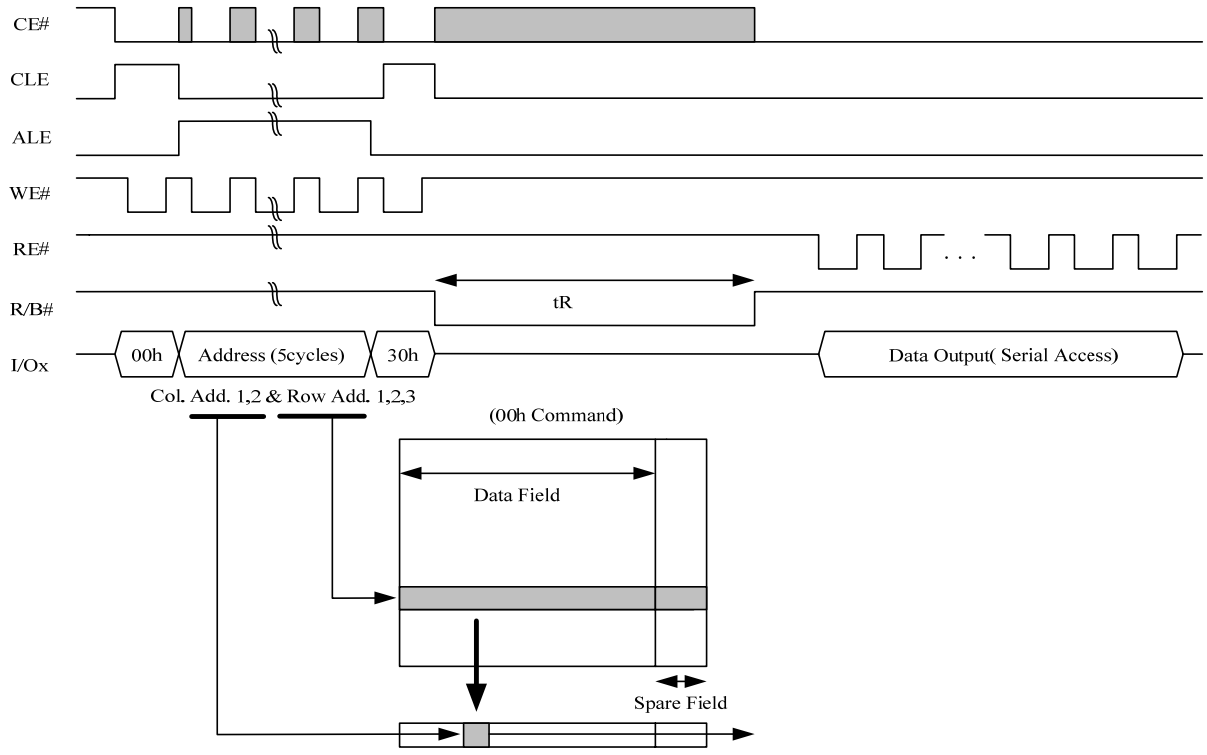


Figure Read Operation

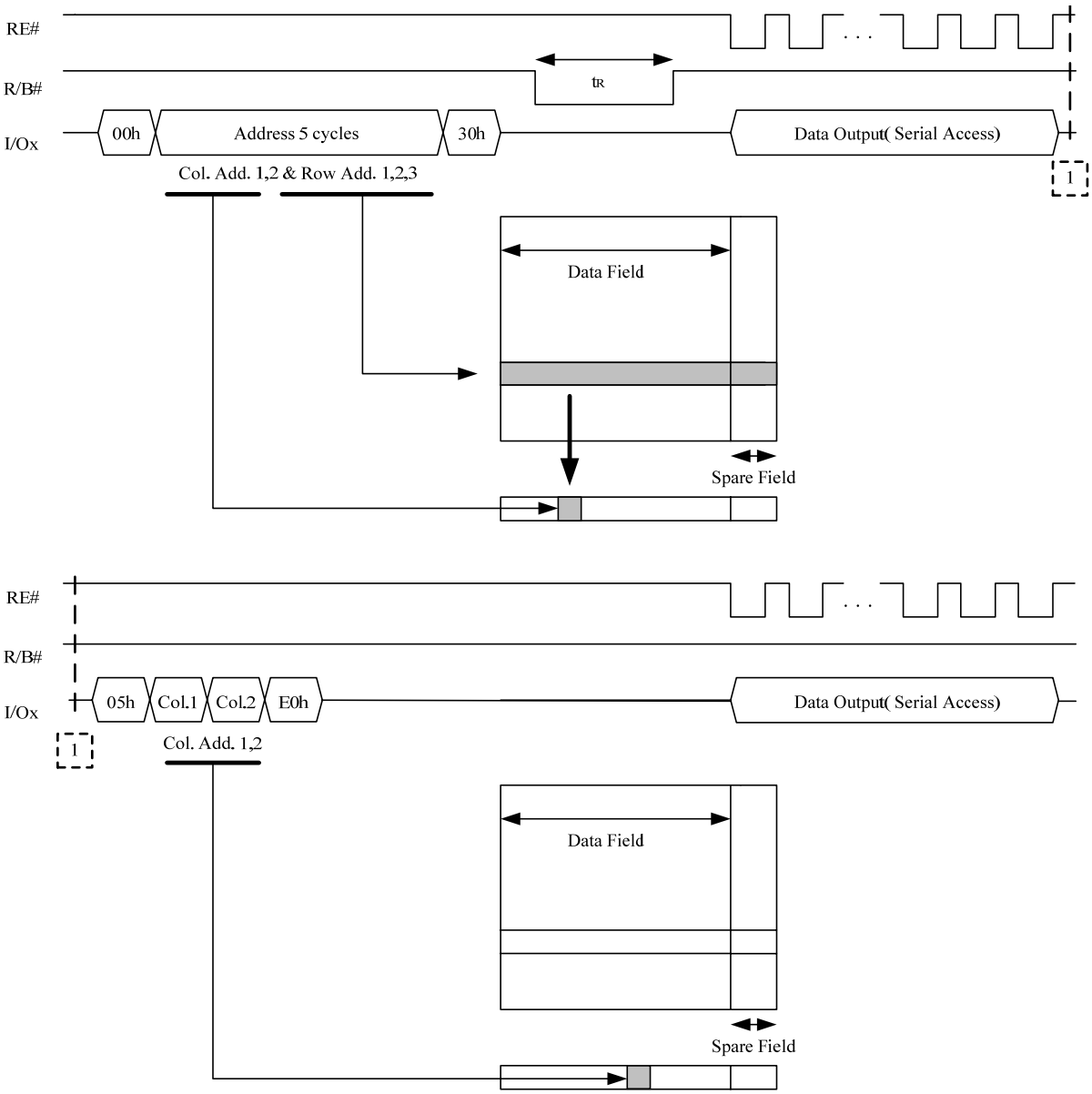


Figure Random Data Output In a Page

11.2 Page Program

The device is programmed based on the unit of a page, and consecutive partial page programming on one page without intervening erase operation is strictly prohibited. Addressing of page program operations within a block should be in sequential order. A complete page program cycle consists of a serial data input cycle in which up to 2,112byteof data can be loaded into data register via cache register, followed by a programming period during which the loaded data are programmed into the designated memory cells.

The serial data input cycle begins with the Serial Data Input command (80h), followed by a five-cycle address input and then serial data loading. The bytes not to be programmed on the page do not need to be loaded. The column address for the next data can be changed to the address follows Random Data Input command (85h). Random Data Input command may be repeated multiple times in a page. The Page Program Confirm command (10h) starts the programming process. Writing 10h alone without entering data will not initiate the programming process. The internal write engine automatically executes the corresponding algorithm and controls timing for programming and verification, thereby freeing the host controller for other tasks. Once the program process starts, the host controller can detect the completion of a program cycle by monitoring the R/B# output or reading the Status bit (I/O6) using the Read Status command. Only Read Status and Reset commands are valid during programming. When the Page Program operation is completed, the host controller can check the Status bit (I/O0) to see if the Page Program operation is successfully done. The command register remains the Read Status mode unless another valid command is written to it.

A page program sequence is illustrated in Figure below, where column address, page address, and data input are placed in between 80h and 10h. After tPROG program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.

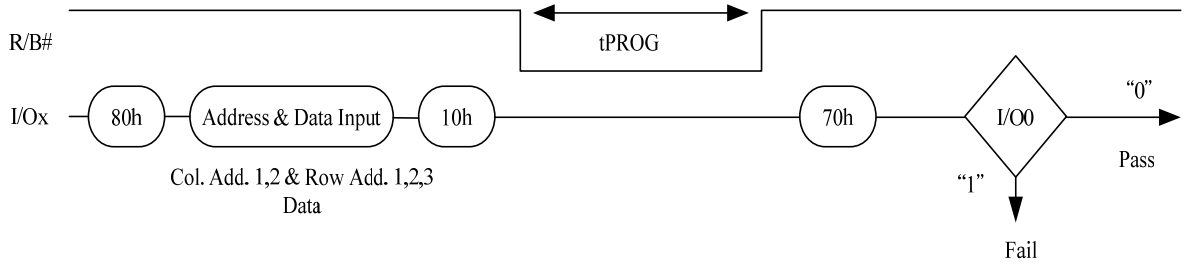


Figure Program & Read Status Operation

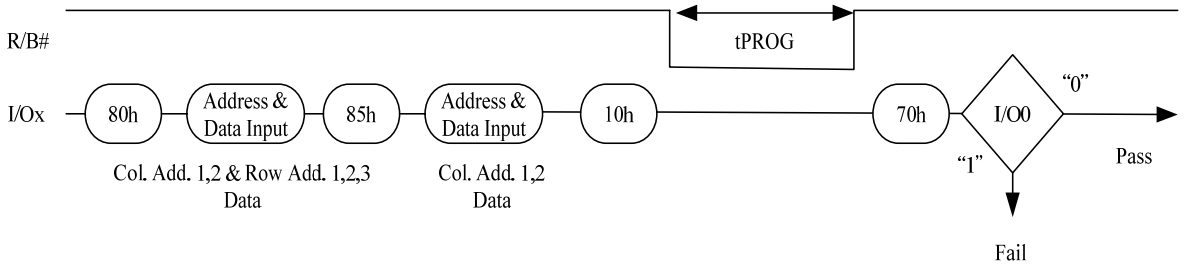


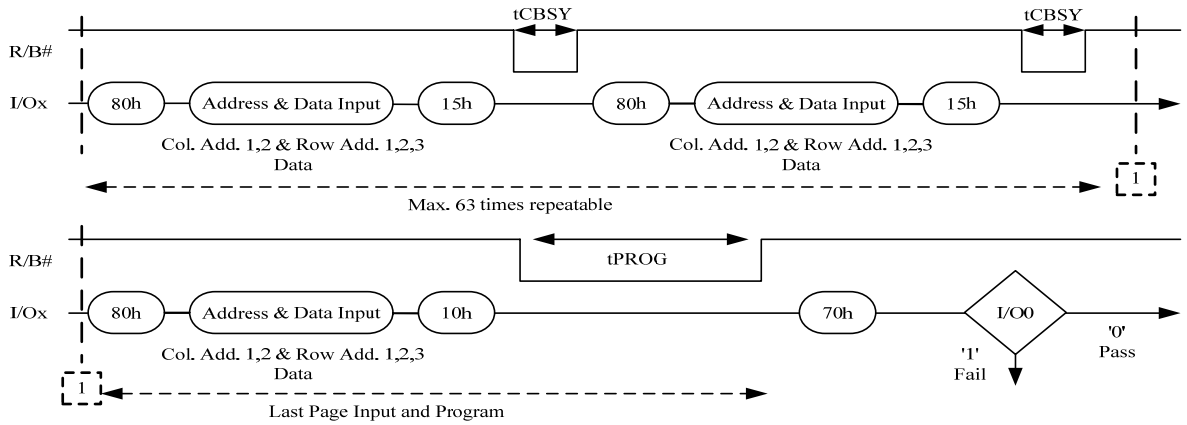
Figure Random Data Input In a Page

11.3 Cache Program

Cache Program is an extension of Page Program, which is executed with 2,112 byte(x8) data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2,112 bytes(x8) into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (t_{CBSY}) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, tCBSY is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identity the completion of internal programming. If the system monitors the progress of programming only with R/B#, the last page of the target programming sequence must be programmed with actual Page Program command (10h).

Cache Program (available only within a block)



NOTE:

1. Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.
2. t_{PROG} = Program time for the last page + Program time for the (last-1)th page – (Program command cycle time + Last page data loading time)

Figure Cache Program

11.4 Copy-Back Program

Copy-Back Program is designed to efficiently copy data stored in memory cells without time-consuming data reloading when there is no bit error detected in the stored data. The benefit is particularly obvious when a portion of a block is updated and the rest of the block needs to be copied to a newly assigned empty block. Copy-Back operation is a sequential execution of Read for Copy-Back and of Copy-Back Program with Destination address. A Read for Copy-Back operation with “35h” command and the Source address moves the whole 2,112byte data into the internal buffer. The host controller can detect bit errors by sequentially reading the data output. Copy-Back Program is initiated by issuing Page-Copy Data-Input command (85h) with Destination address. If data modification is necessary to correct bit errors and to avoid error propagation, data can be reloaded after the Destination address. Data modification can be repeated multiple times as shown in Figure below. Actual programming operation begins when Program Confirm command (10h) is issued. Once the program process starts, the Read Status command (70h) may be entered to read the status register. The host controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Copy-Back Program is complete, the Status Bit (I/O0) may be checked. The command register remains Read Status mode until another valid command is written to it.

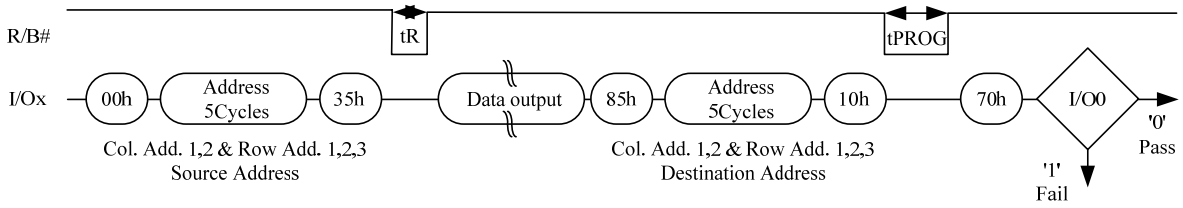


Figure Page Copy-Back Program Operation

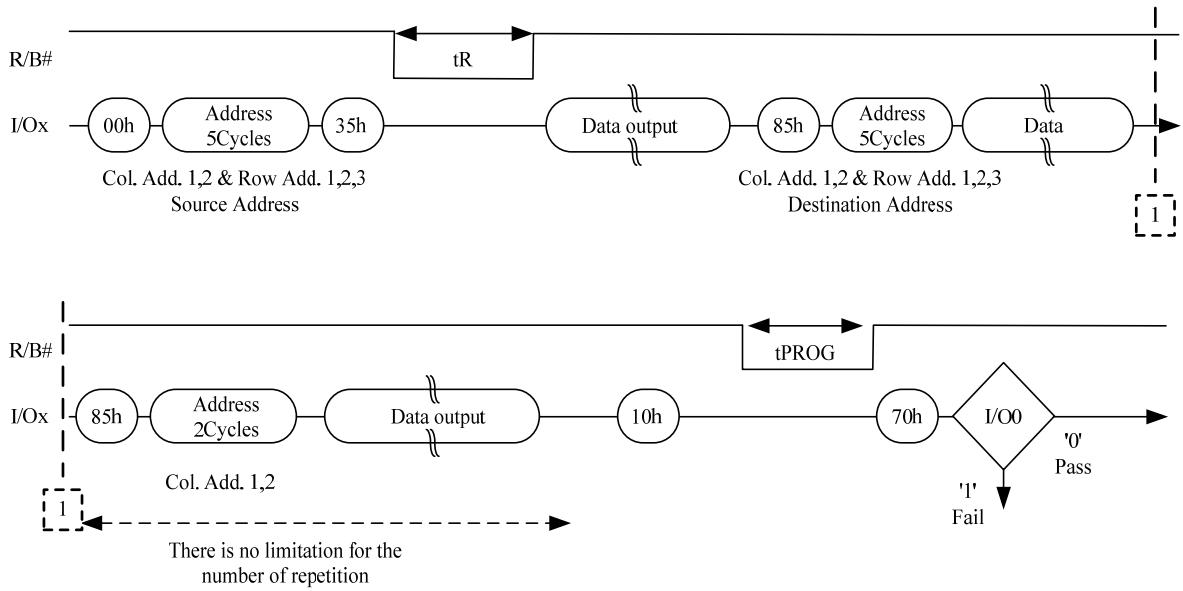


Figure Page Copy-Back Program Operation with Random Data Input

11.5 Block Erase

The block-based Erase operation is initiated by an Erase Setup command (60h), followed by a three-cycle row address, in which only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command (D0h) following the row address starts the internal erasing process. The two-step command sequence is designed to prevent memory content from being inadvertently changed by external noise.

At the rising edge of WE# after the Erase Confirm command input, the internal control logic handles erase and erase-verify. When the erase operation is completed, the host controller can check Status bit (I/O0) to see if the erase operation is successfully done. Figure below illustrates a block erase sequence, and the address input (the first page address of the selected block) is placed in between commands 60h and D0h. After tBERS erase time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after D0h to check the execution status of erase operation.

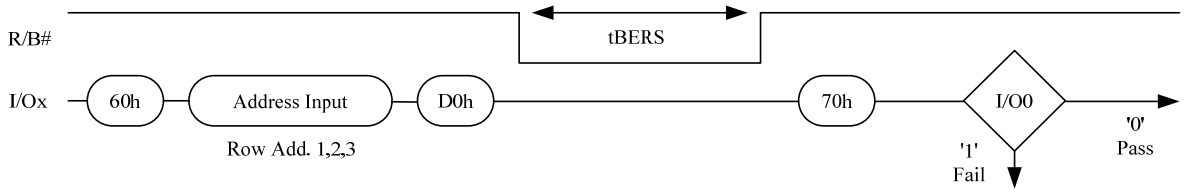


Figure Block Erase Operation

11.6 Read Status

A status register on the device is used to check whether program or erase operation is completed and whether the operation is completed successfully. After writing 70h/F1h command to the command register, a read cycle outputs the content of the status register to I/O pins on the falling edge of CE# or RE#, whichever occurs last. These two commands allow the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to toggle for status change.

The command register remains in Read Status mode unless other commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h) is needed to start read cycles.

I/O	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Pass/Fail(N)	NA	NA	Pass : 0 Fail : 1
I/O 1	NA	NA	Pass/Fail(N-1)	NA	NA	Don't cared
I/O 2	NA (Pass/Fail,OTP)	NA	NA	NA	NA	Don't cared
I/O 3	NA	NA	NA	NA	NA	Don't cared
I/O 4	NA	NA	NA	NA	NA	Don't cared
I/O 5	NA	NA	True Ready/Busy	NA	True Ready/Busy	Busy : 0 Ready : 1
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : 0 Ready : 1
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected :0 Not Protected : 1

Table Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O 0	Chip Pass/Fail	Chip Pass/Fail	Chip Pass/Fail(N)	NA	NA	Pass : 0 Fail : 1
I/O 1	Plane0 Pass/Fail	Plane0 Pass/Fail	Plane0 Pass/Fail(N)	NA	NA	Pass : 0 Fail : 1
I/O 2	Plane1 Pass/Fail	Plane1 Pass/Fail	Plane1 Pass/Fail(N)	NA	NA	Pass : 0 Fail : 1
I/O 3	NA	NA	Plane0 Pass/Fail(N-1)	NA	NA	Pass : 0 Fail : 1
I/O 4	NA	NA	Plane1 Pass/Fail(N-1)	NA	NA	Pass : 0 Fail : 1
I/O 5	NA	NA	True Ready/Busy	NA	True Ready/Busy	Busy : 0 Ready : 1
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Busy : 0 Ready : 1
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Protected :0 Not Protected : 1

Table Status Register Definition for F1h Command

NOTE :

1. I/Os defined NA are recommended to be masked out when Read Status is being executed.
2. n : current page, n-1 : previous page.

11.7 Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.

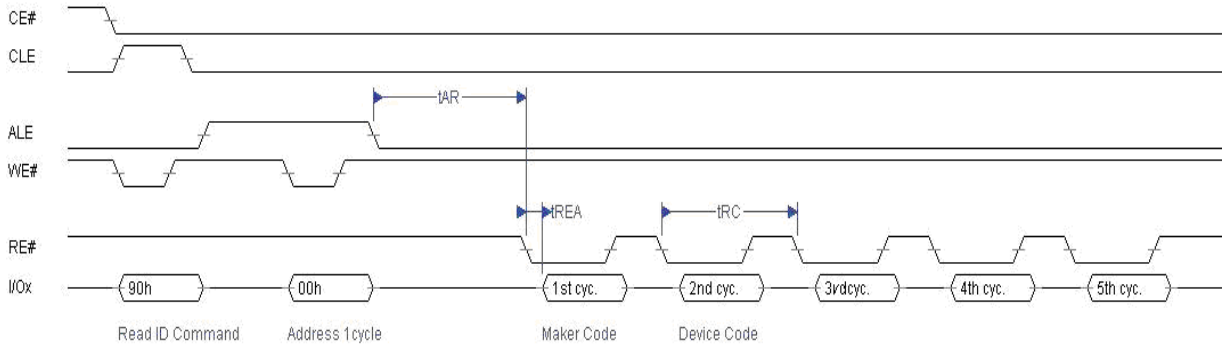


Figure Read ID Operation

Part No.	1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
PSU4GA30AT (X8)	C8h	DCh	90h	95h	56h

Table ID Definition Table

11.8 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP# is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin changes to low for tRST after the Reset command is written. Refer to Figure below.

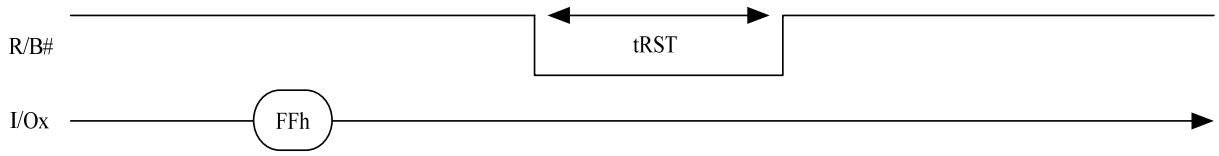


Figure Reset Operation

	After Power-up	After Reset
Operation Mode	00h Command is latched	Waiting for next command

Table Device Status

11.9 Cache Read

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of tDCBSYR, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.

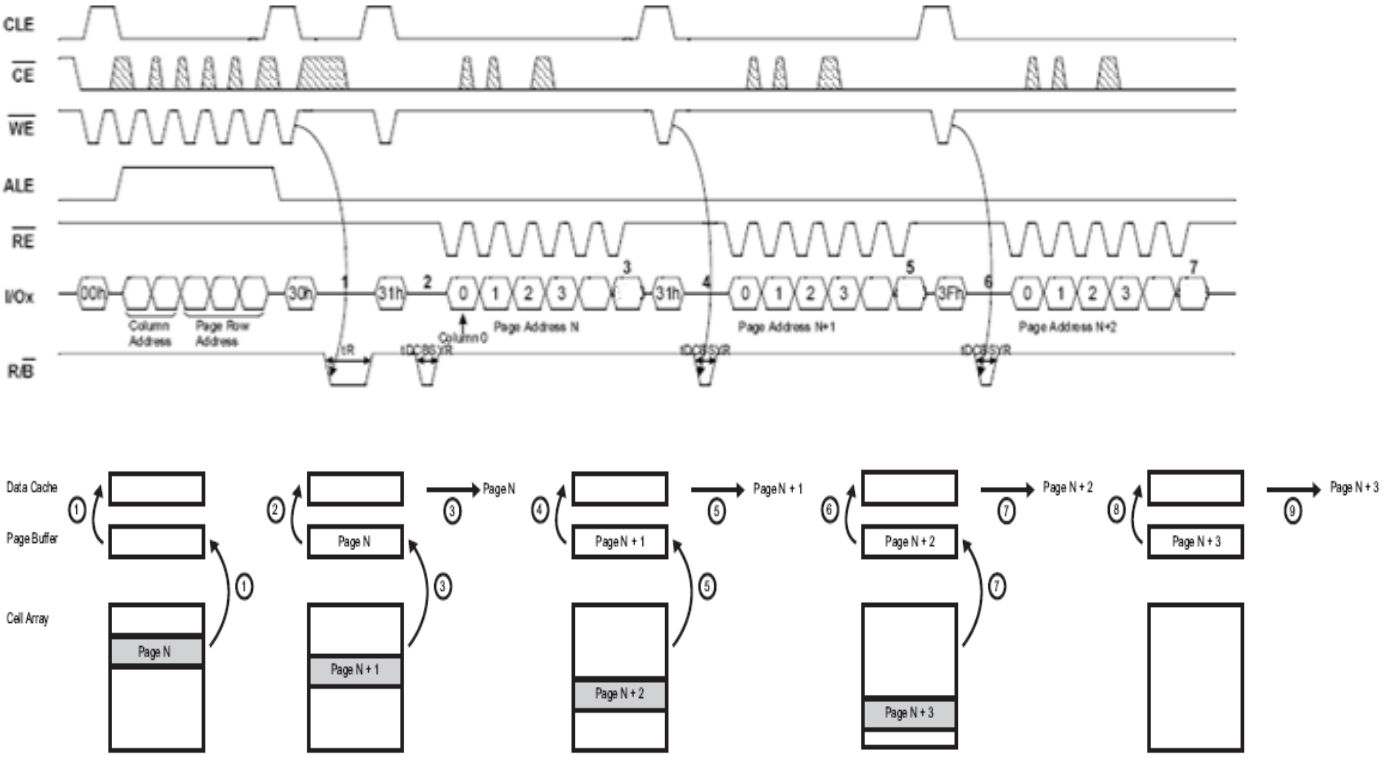


Figure Read Operation with Cache Read

11.10 Two-Plane Page Read

Two-Plane Page Read is an extension of Page Read, for a single plane with 2,112 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 2,112 byte data registers enables a random read of two pages. Two-Plane Page Read is initiated by repeating command 60h followed by three address cycles twice. In this case, only same page of same block can be selected from each plane.

After Read Confirm command(30h) the 4,224 bytes of data within the selected two page are transferred to the cache registers via data registers in less than 25us(tR). The system controller can detect the completion of data transfer (tR) by monitoring the output of R/B pin.

Once the data is loaded into the cache registers, the data output of first plane can be read out by issuing command 00h with five address cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences.

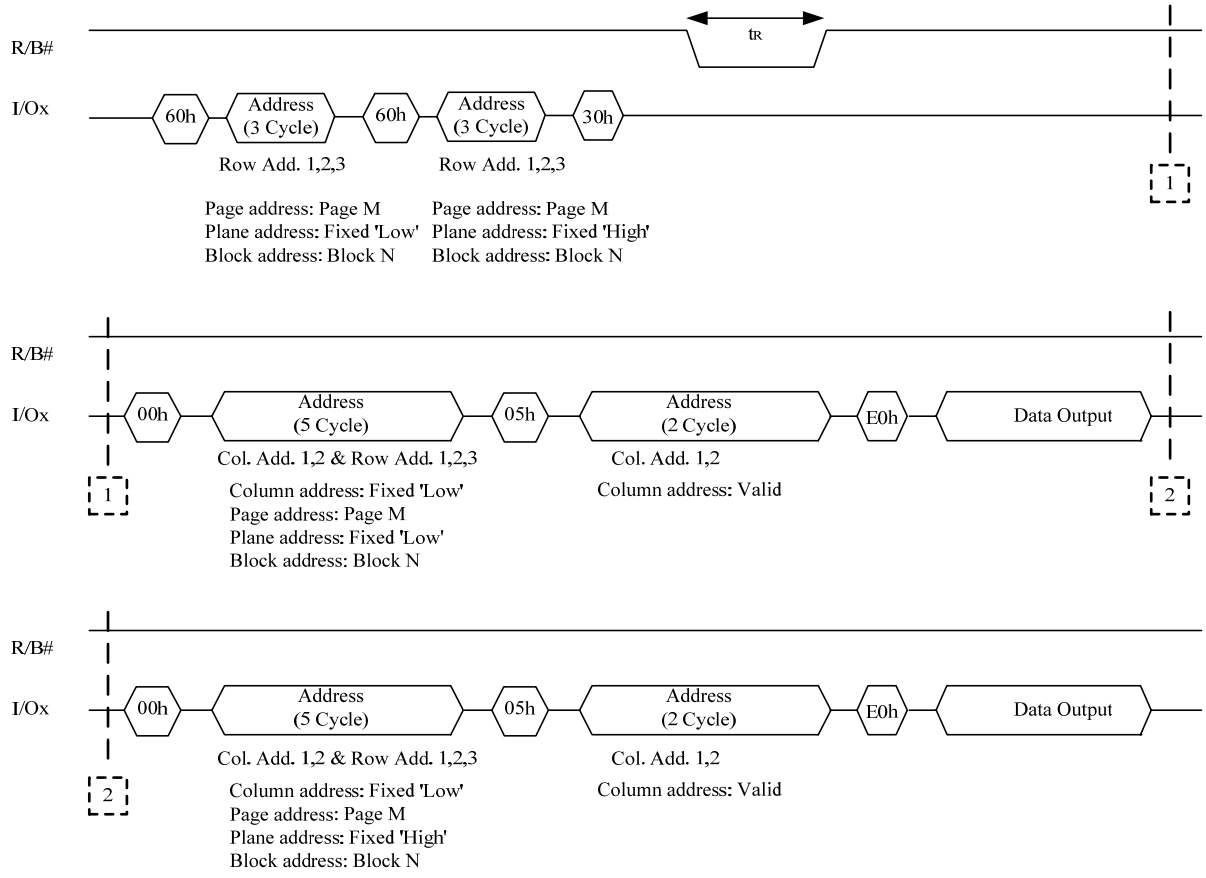


Figure Two-Plane Page Read

11.11 Two-Plane Cache Read

Two-Plane Cache Read is an extension of Cache Read, for a single plane with 2,112 byte data registers. Since the device is equipped with two memory planes, the two sets of 2,112 byte data registers enables a cache read of two pages. Two-Plane Cache Read is initiated by repeating command 60h followed by three address cycles twice. In this case only same page of same block can be selected from each plane.

After Read Confirm command(33h) the 4,224 bytes of data within the selected two page are transferred to the cache registers via data registers in less than 25us(tR). After issuing Cache Read command(31h), read data in the data registers is transferred to cache registers for a short period of time(tDBSY). Once the data is loaded into the cache registers from data registers, the data output of first plane can be read out by issuing command 00h with five address cycles, command 05h with two column address and finally E0h. The data output of second plane can be read out using the identical command sequences.

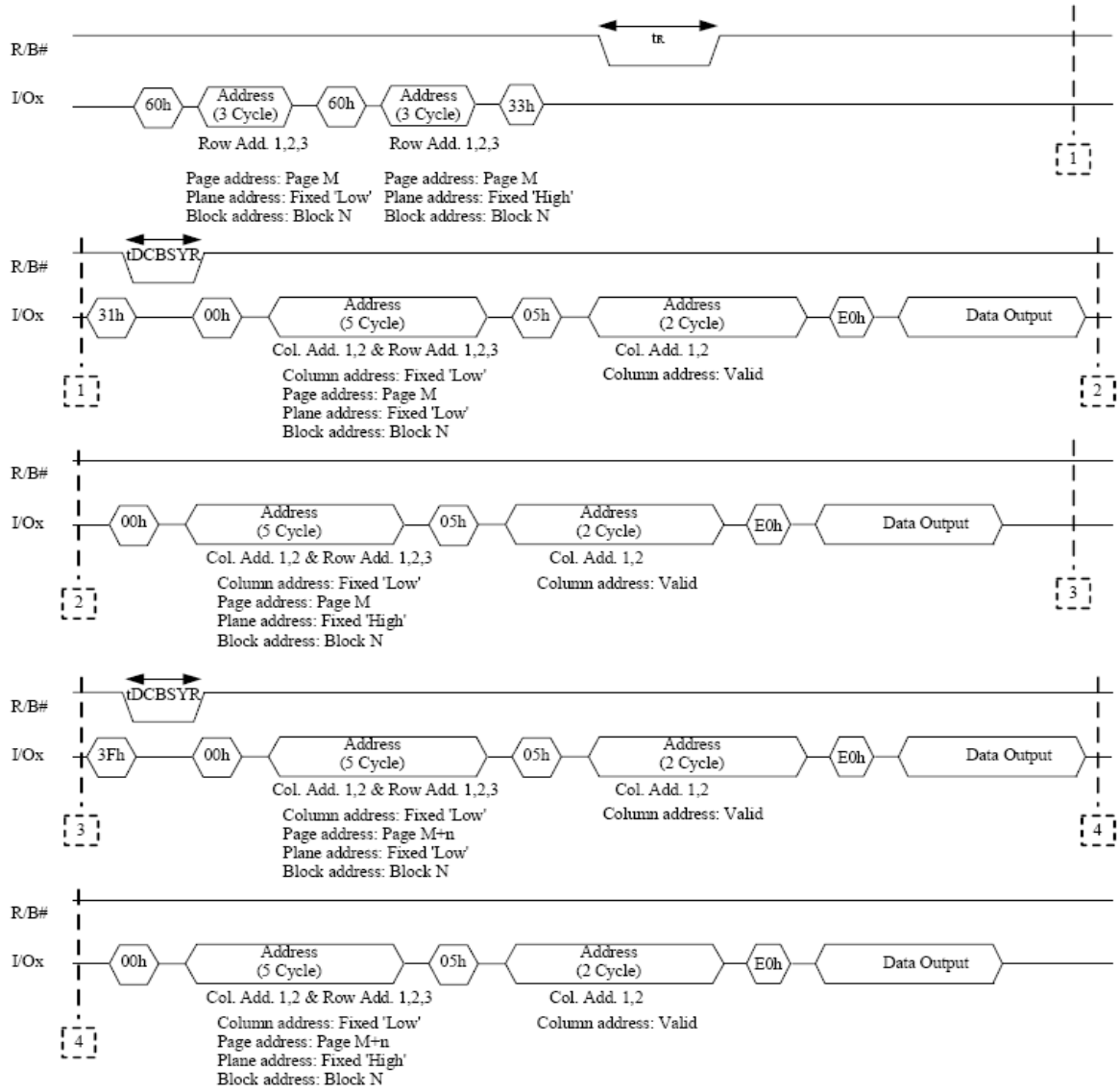


Figure Two-Plane Cache Read

11.12 Two-Plane Page Program

Two-Plane Page Program is an extension of Page Program, for a single plane with 2,112 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 2112 byte data registers enables a simultaneous programming of two pages.

After writing the first set of data up to 2,112 byte into the selected data registers via cache registers, Dummy Page Program command (11h) instead of actual Page Program command (10h) is inputted to finish data-loading of the first plane. Since no programming process is involved, R/B remains in busy state for a short period of time(tDBSY). Read Status command (70h) may be issued to find out when the device returns to ready state by polling the R/B status bit(I/O 6). Then the next set of data for the other plane is inputted after 81h command and address sequences. After inputting data for the last page, actual True Page Program(10h) instead of dummy Page Program command(11h) must be followed to start the programming process. The operation of R/B and Read Status is the same as that of Page Program. Although two planes are programmed simultaneously, pass/fail is not available for each page when the program operation completes. Status bit of I/O 0 is set to “1” when any of the pages fails.

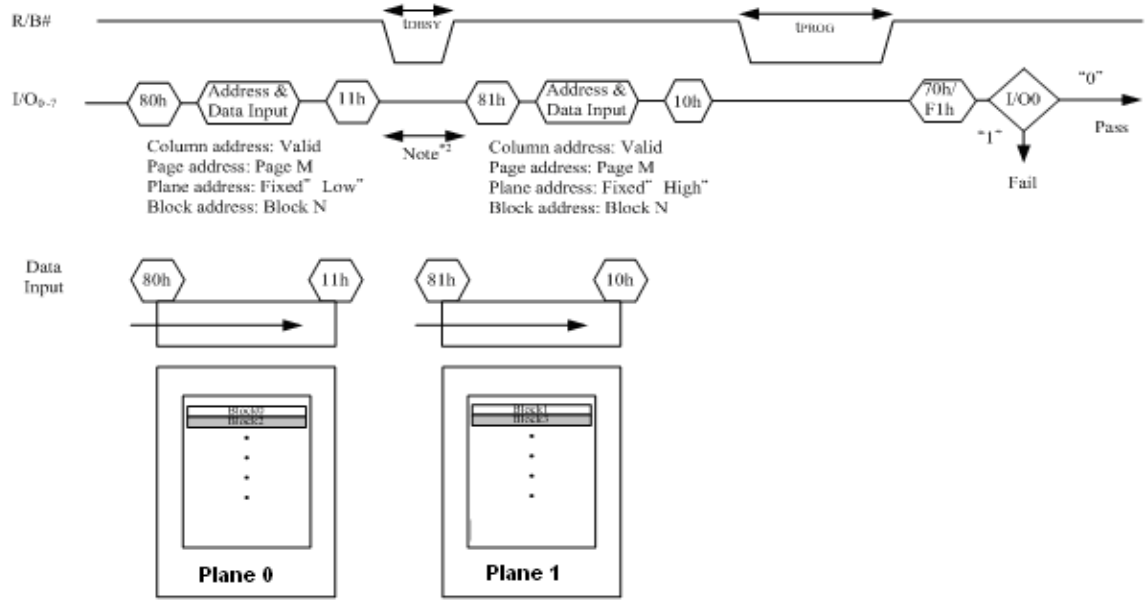


Figure Two-Plane Page Program

11.13 Two-Plane Copy-Back Program

Two-Plane Copy-Back Program is an extension of Copy-Back Program, for a single plane with 2,112 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 2,112 byte data registers enables a simultaneous programming of two pages.

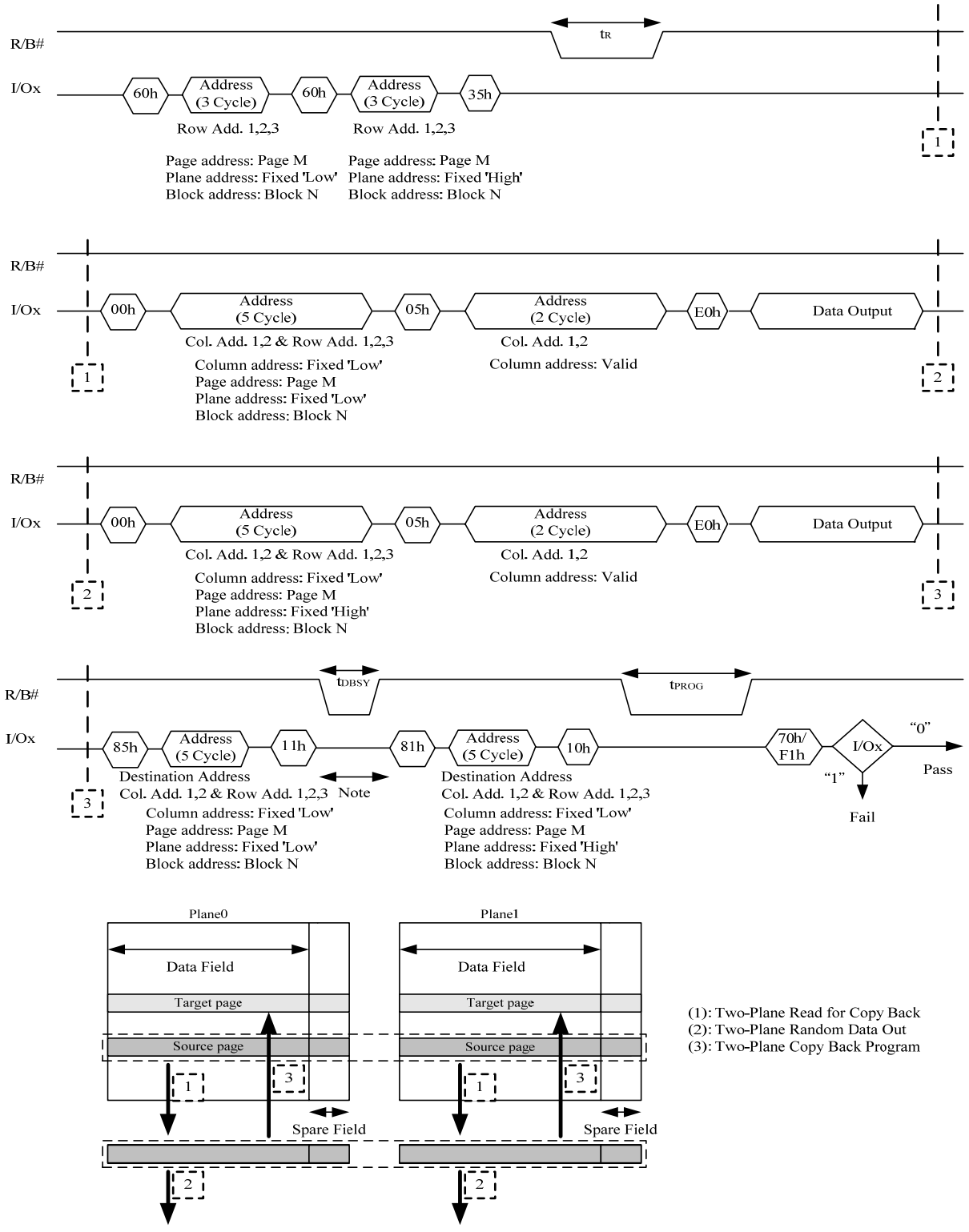


Figure Two-Plane Copy-Back Program

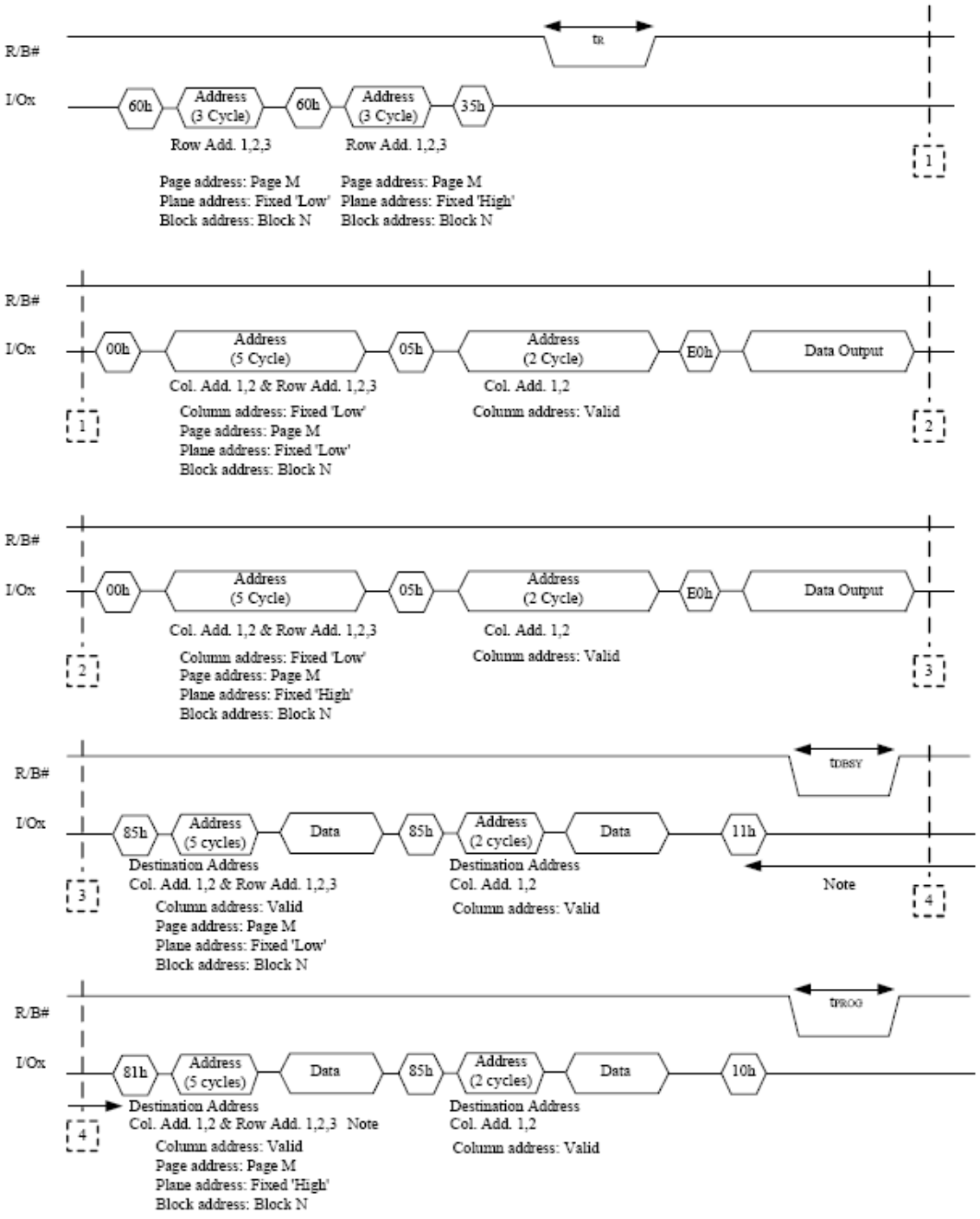


Figure Two-Plane Copy-Back Program with Random Data Input

11.14 Two-Plane Cache Program

Two-Plane Cache Program is an extension of Cache Program, for a single plane with 2,112 byte data registers. Since the device is equipped with two memory planes, activating the two sets of 2,112 byte data registers enables a simultaneous programming of two pages.

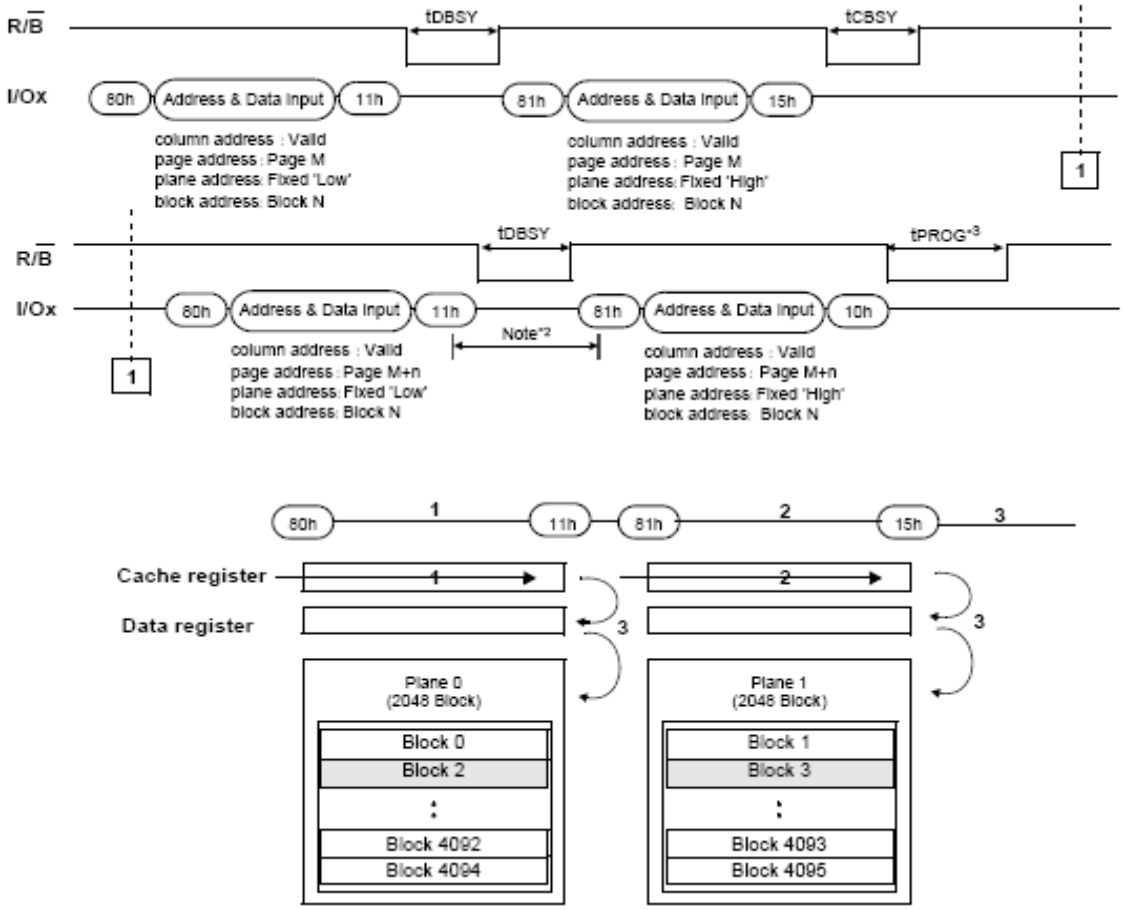


Figure Two-Plane Cache Program

11.15 Two-Plane Block Erase

Basic concept of Two-Plane Block Erase operation is identical to that of Two-Plane Page Program. Up to two blocks, one from each plane can be simultaneously erased. Standard Block Erase command sequences (Block Erase Setup command 60h followed by three address cycles) may be repeated up to twice for erasing up to two blocks. Only one block should be selected from each plane. The Erase Confirm command (D0h) initiates the actual erasing process. The completion is detected by monitoring R/B pin or Ready/Busy status bit (I/O 6).

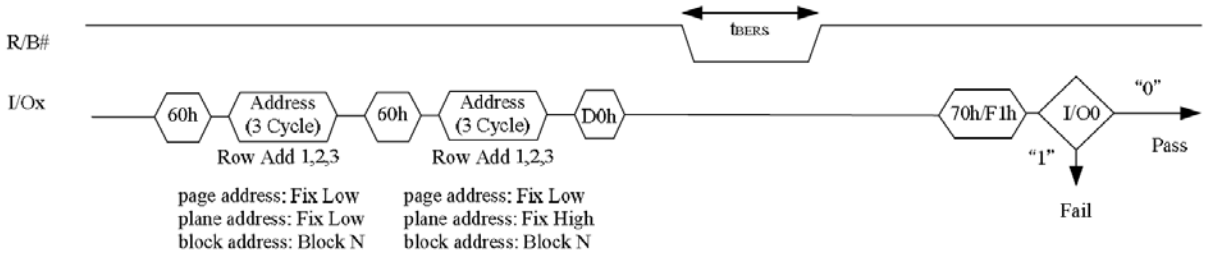
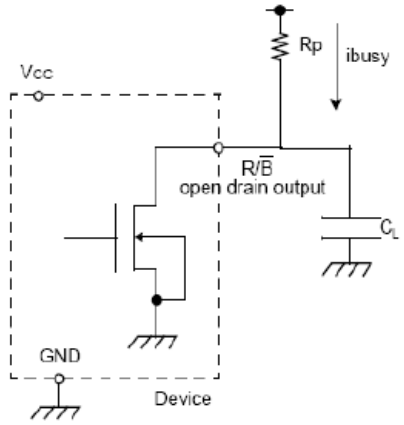
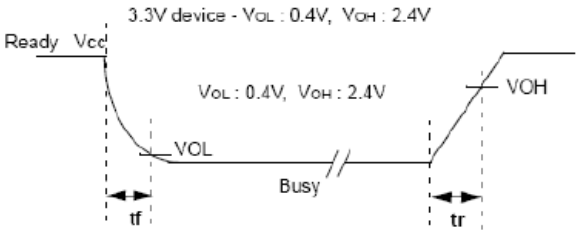


Figure Two-Plane Block Erase

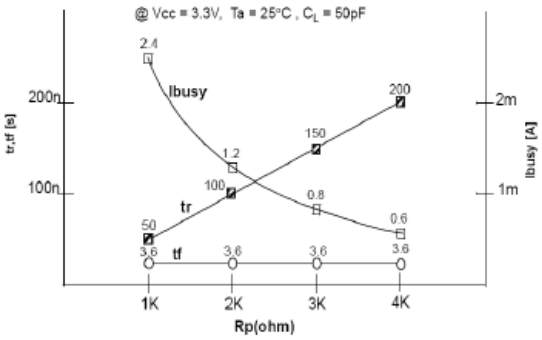
11.16 Ready/Busy#

The device has a R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transition to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B#) and current drain during busy (ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.





R_P vs t_{RHOH} vs C_L



R_P value guidance

$$Rp(min, 3.3V\ part) = \frac{V_{CC}(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the R/B# pin.
R_P (max) is determined by maximum permissible limit of tr

Figure Read/Busy# Pin Electrical Specifications

11.17 Data Protection & Power Up Sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device R/B# signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are 70h.

The WP# signal is useful for protecting against data corruption at power on/off.

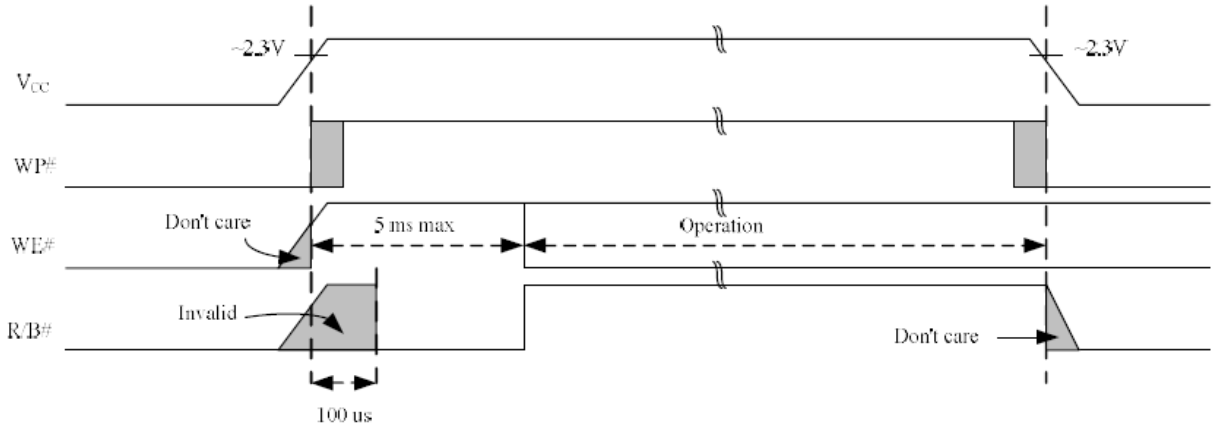
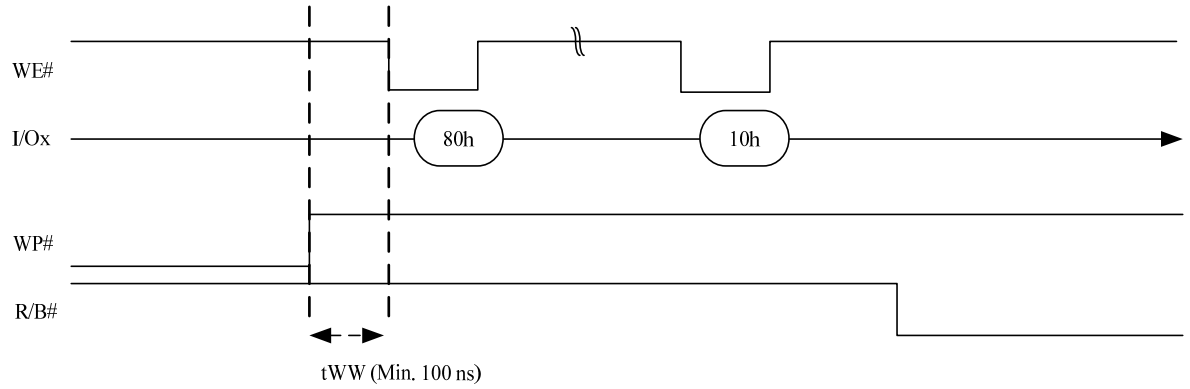


Figure AC Waveforms for Power Transition

11.18 Write Protect Operation

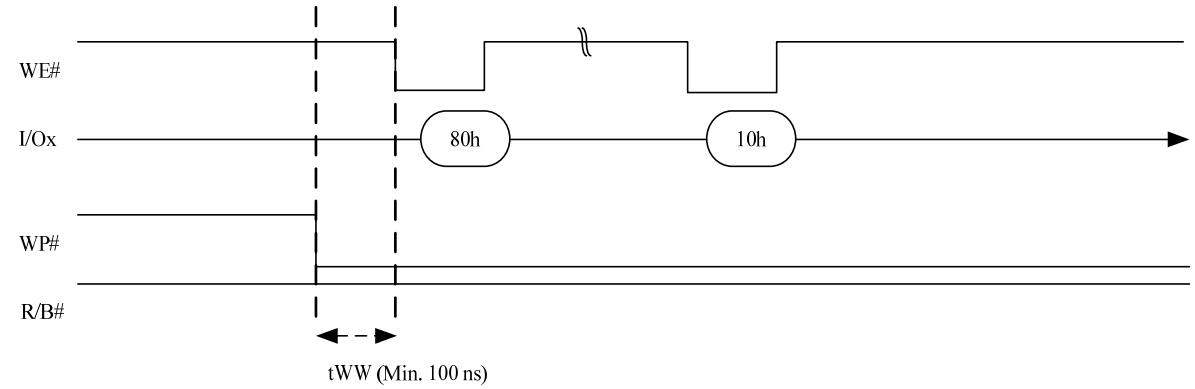
Enabling WP# during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Enable Programming

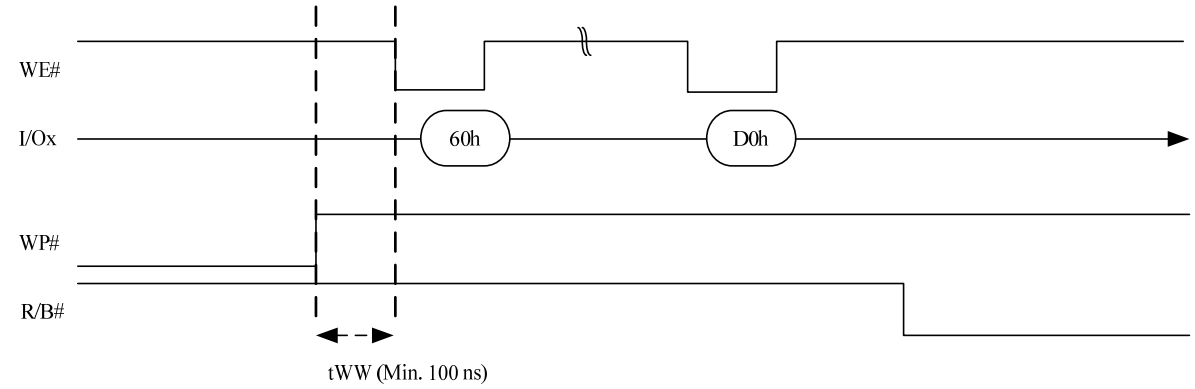


NOTE: WP# keeps “High” until programming finish

Disable Programming



Enable Erasing



NOTE: WP# keeps “High” until erasing finish

Disable Erasing

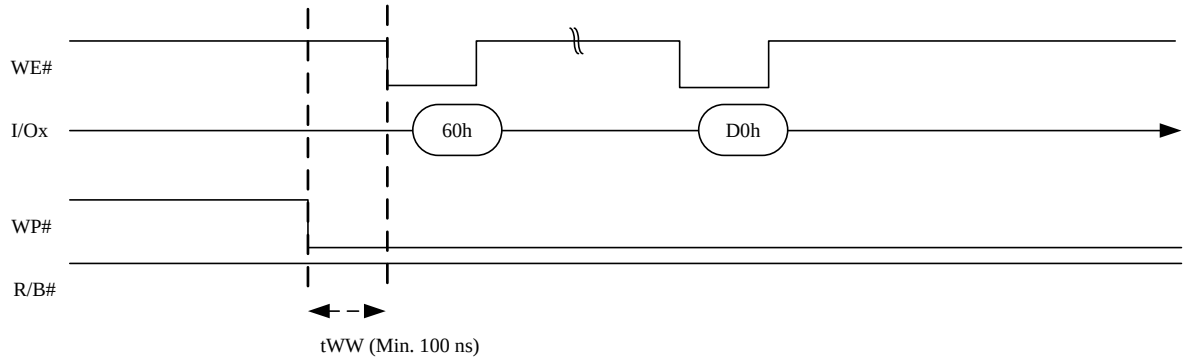


Figure Erase and Program Operations