MCP Specification

1Gb (128Mb x8) NAND Flash
+ 512Mb (32Mb x16) mobile DDR

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Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial draft	Aug. 2011	Preliminary
0.2	Modified TREF Characteristics of MDDR	Dec. 2011	Preliminary
0.3	Revise Timing diagram, failure mode, erratum	Dec. 2011	Preliminary
0.4	Revise unit of plane size in ID definition table	Dec. 2011	Preliminary

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FEATURES

[MCP]

- Operation Temperature - 30℃ ~ 85℃
- Package - 107-ball FBGA (10.5x13mm^2)

[NAND Flash]

- Supply Voltage - Vcc = 1.7 - 1.95 V
- Memory Cell Array - (2K + 64) bytes x 64 pages x 1024 blocks
- Memory Cell - 1bit/Memory Cell
- Page Size - (2K+ 64 spare) Bytes
- Block Size - (128K + 4K spare) Bytes
- Page Read / Program - Random access : 25us (max.)
  - Sequential access : 45ns (min.)
  - Page program time : 250us (typ.)
- FAST BLOCK ERASE - Block erase time: 2.0ms (typ.)
- ECC Requirement - 1bit/528Byte
- Command Register Operation
- DATA RETENTION - 100K Program/Erase cycles
  - 10 years Data Retention
- Cache Program Operation for High Performance Program
- COPY BACK Operation
- EDO mode
- OTP Operation
- Automatic Page 0 Read at Power-Up Option
  - Boot from NAND support
  - Automatic Memory Download

[mobile DDR SDRAM]

- Supply Voltage - VDD / VDDQ = 1.7 - 1.95 V
- Speed - Data rate : 400Mbps (max.)
- Organization - 8Mb x 4Bank x 16 I/O
  - 2KB page size
  - Row address : A0 to A12; Column address : A0 to A9
- Input Clock - Differential Clock Inputs (CK, /CK)
- /CAS latency - 3
- Burst Length - 2 / 4 / 8 / 16 with both sequential and interleave mode
- Refresh - auto-refresh, self-refresh, PASR(Partial Array Self-Refresh), ATCSR(Auto Temperature Compensated Self-Refresh)
  - cycles : 8192 cycles/64ms
  - average refresh period : 7.8uS
- Deep power-down mode
- Bidirectional data strobe (DQS)
- Input data mask signal (DQM)

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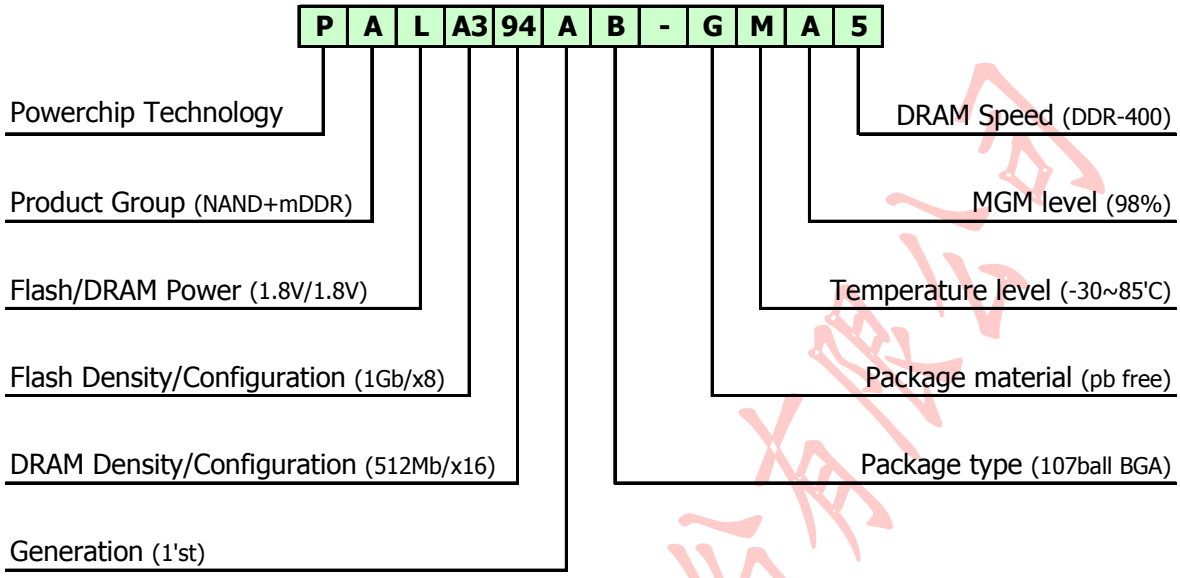
Ordering Information

Part Number	Memory combination	Operation Voltage	Density	Speed	Package
PALA394AB-GMA5	NAND Flash	1.8V	1Gb (128Mbx8)	45ns	107Balls FBGA
	Mobile DDR	1.8V	512Mb (32Mbx16)	DDR400	

Part Numbering Information



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MCP General Description

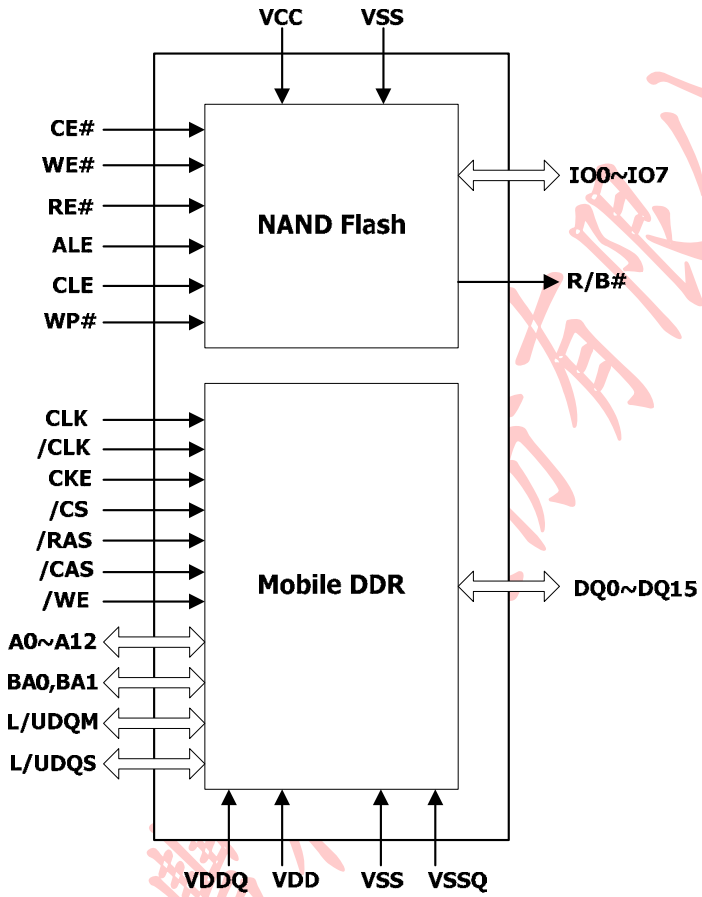
The Multi-Chip Package (MCP) products combine NAND Flash and Mobile DDR SDRAM devices in a single MCP. The products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements. The NAND Flash and Mobile DDR devices are also members of the discrete memory products portfolio.

The NAND Flash and Mobile DDR devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile DDR buses.

The NAND Flash and Mobile DDR devices have separate core power connections and share a common ground (that is, VSS is tied together on the two devices).

The bus architecture of this device also supports separate NAND Flash and Mobile DDR functionality without concern for device interaction. Operational characteristics for the NAND Flash and Mobile DDR devices are found in the standard Powerchip's data sheets for each of the discrete devices.

MCP Block Diagram



Pin Description

NAND Flash			mobile DDR SDRAM		
SYMBOL	Type	DESCRIPTION	SYMBOL	Type	DESCRIPTION
I/O0~I/O7	Input/output	Data Input / Output	CK, /CK	Input	Differential Clock Inputs
CLE	Input	Command Latch Enable	CKE	Input	Clock Enable
ALE	Input	Address Latch Enable	/CS	Input	Chip Select
CE#	Input	Chip Enable	/RAS, /CAS, /WE	Input	Command Inputs
WE#	Input	Write Enable	BA0, BA1	Input	Bank Address Inputs
RE#	Input	Read Enable	A0 ~ A12	Input	Address Input
WP#	Input	Write Protect	DQ0 ~ DQ15	Input/output	Data Input/Output
R/B#	Output	Ready / Busy Out	UDQM, LDQM	Input	Input Data Mask
VCC	Supply	Supply Voltage	UDQS, LDQS	Input	Data Strobe
VSS	Supply	Ground	VDD	Supply	Supply Voltage
Common			VSS	Supply	Ground
DNU	-	Do Not Use	VDDQ	Supply	I/O Power Supply
NC	-	No connection	VSSQ	Supply	I/O Ground

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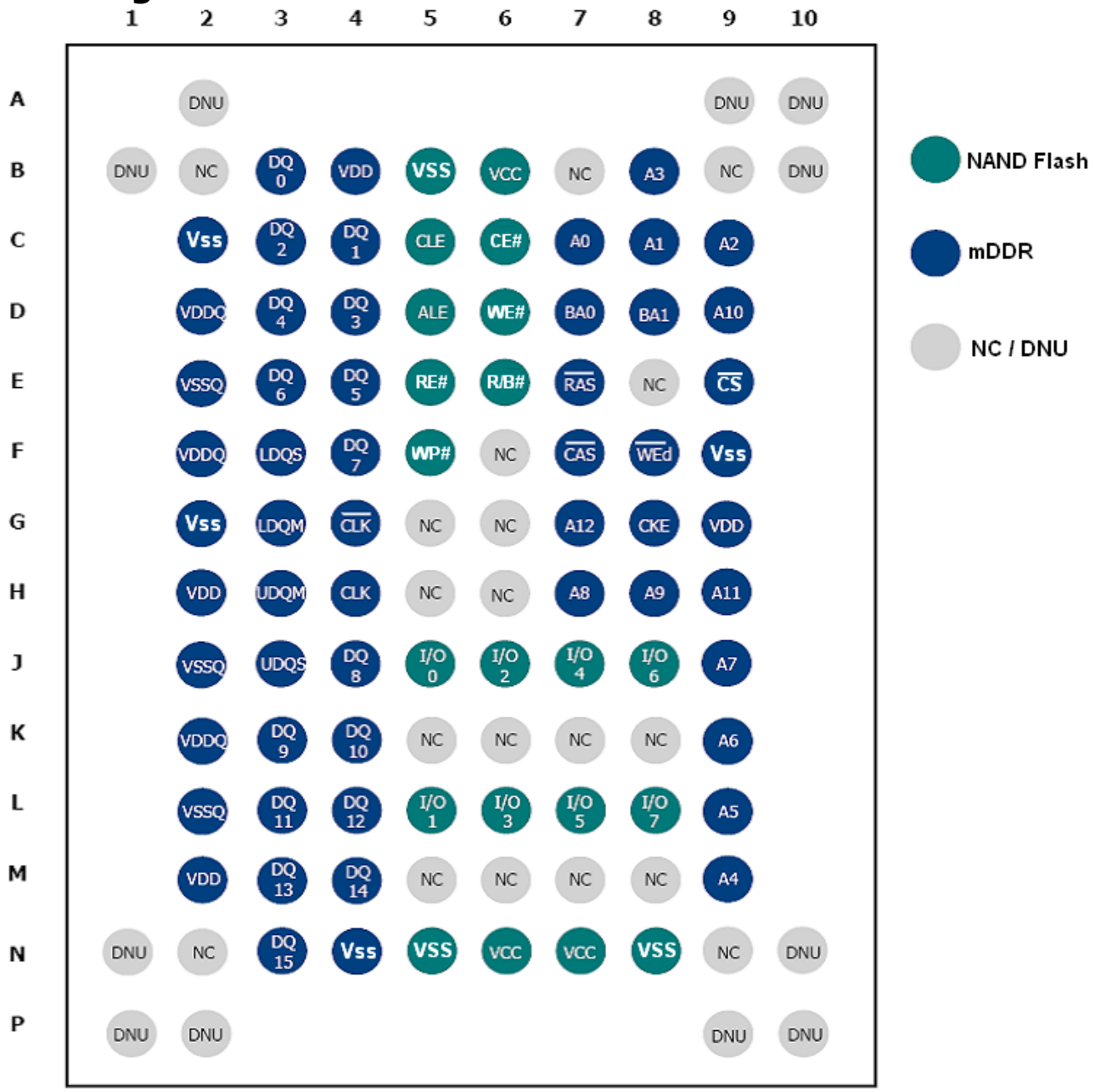
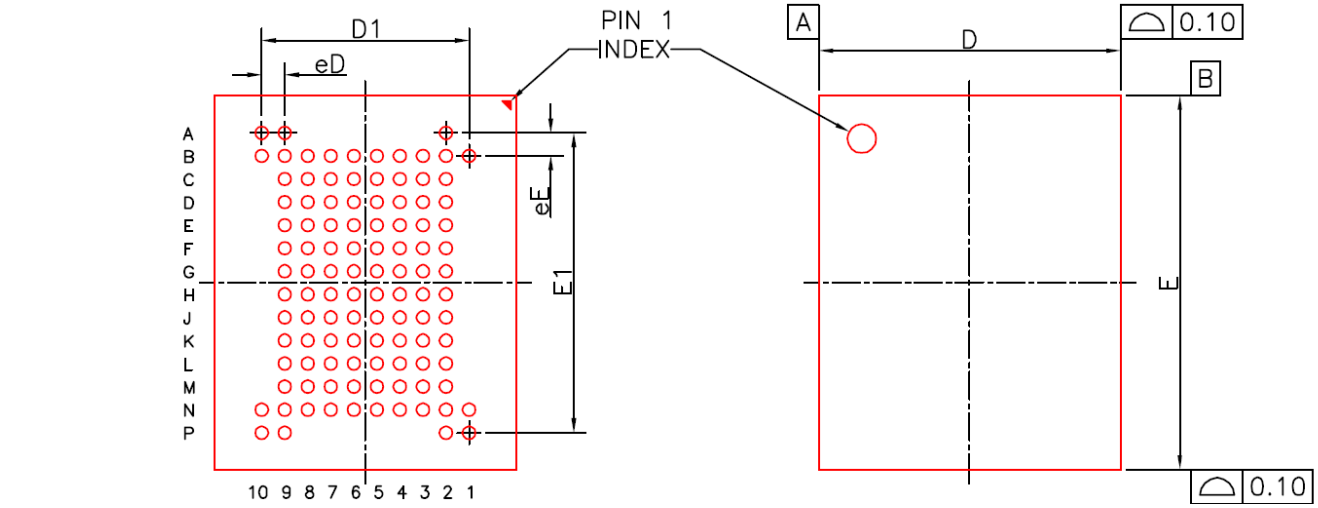
Pin Configuration

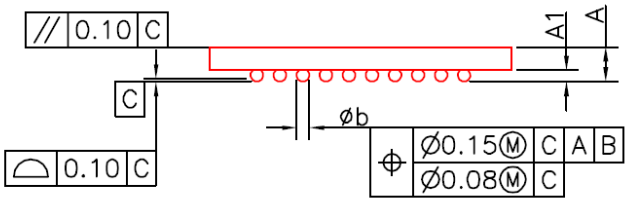


107 Balls FBGA Package (Top View)

Package Information

107 Ball 0.8mm pitch 10.5mm x 13.0mm FBGA





Symbol	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.20
A1	0.30	0.35	0.40
D	10.40	10.50	10.60
D1	7.20 BSC		
E	12.90	13.00	13.10
E1	10.40 BSC		
b	0.40	0.45	0.50
eD	0.80 BSC		
eE	0.80 BSC		

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1Gb (128Mb x8) NAND Flash

1 Product Description

The 1Gb NAND Flash is a 128Mx8bit with spare 4Mx8bit capacity. The device is offered in 1.8V Vcc Power Supply. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased.

The device contains 1024 blocks, composed by 64 pages consisting in two NAND structures of 32 series connected Flash cells. A program operation allows to writes the 2112-Byte page in typical 250us and an erase operation can be performed in typical 2ms on a 128K-byte for X8 device block.

Data in the page mode can be read out at 45ns cycle time per Word. The I/O pins serve as the ports for address and command inputs as well as data input/output. The copy back function allows the optimization of defective blocks management: when a page program operation fails the data can be directly programmed in another page inside the same array section without the time consuming serial data insertion phase. The cache program feature allows the data insertion in the cache register while the data register is copied into the Flash array. This pipelined program operation improves the program throughput when long files are written inside the memory. A cache read feature is also implemented. This feature allows to dramatically improving the read throughput when consecutive pages have to be streamed out. This device includes extra feature: Automatic Read at Power Up.

The 1Gb NAND Flash has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing WE# to low while CE# is low. Those are latched on the rising edge of WE#. Command Latch Enable (CLE) and Address Latch Enable (ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.

In addition to the enhanced architecture and interface, the device incorporates copy-back program feature from one page to another page without need for transporting the data to and from the external buffer memory.

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Pin Description

Pin Name	Pin Function
I/O0 ~ I/O7	**DATA INPUTS/OUTPUTS** The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** The CLE input controls the activating path for commands sent to the internal command registers. Commands are latched into the command register through the I/O ports on the rising edge of the WE# signal with CLE high.
ALE	**ADDRESS LATCH ENABLE** The ALE input controls the activating path for addresses sent to the internal address registers. Addresses are latched into the address register through the I/O ports on the rising edge of WE# with ALE high.
CE#	**CHIP ENABLE** The CE# input is the device selection control. When the device is in the Busy state, CE# high is ignored, and the device does not return to standby mode in program or erase operation. Regarding CE# control during read operation, refer to 'Page read' section of Device operation.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when it is active low, it drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address counter by one.
WE#	**WRITE ENABLE** The WE# input controls writes to the I/O ports. Commands, address and data are latched on the rising edge of the WE# pulse.
WP#	**WRITE PROTECT** The WP# pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the WP# pin is active low.
R/B#	**READY/BUSY OUTPUT** The R/B# output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in progress and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
VCC	**POWER** VCC is the power supply for device.
VSS	**GROUND**

Note : Connect all VCC and VSS pins of each device to common power supply outputs. Do not leave VCC or VSS disconnected.

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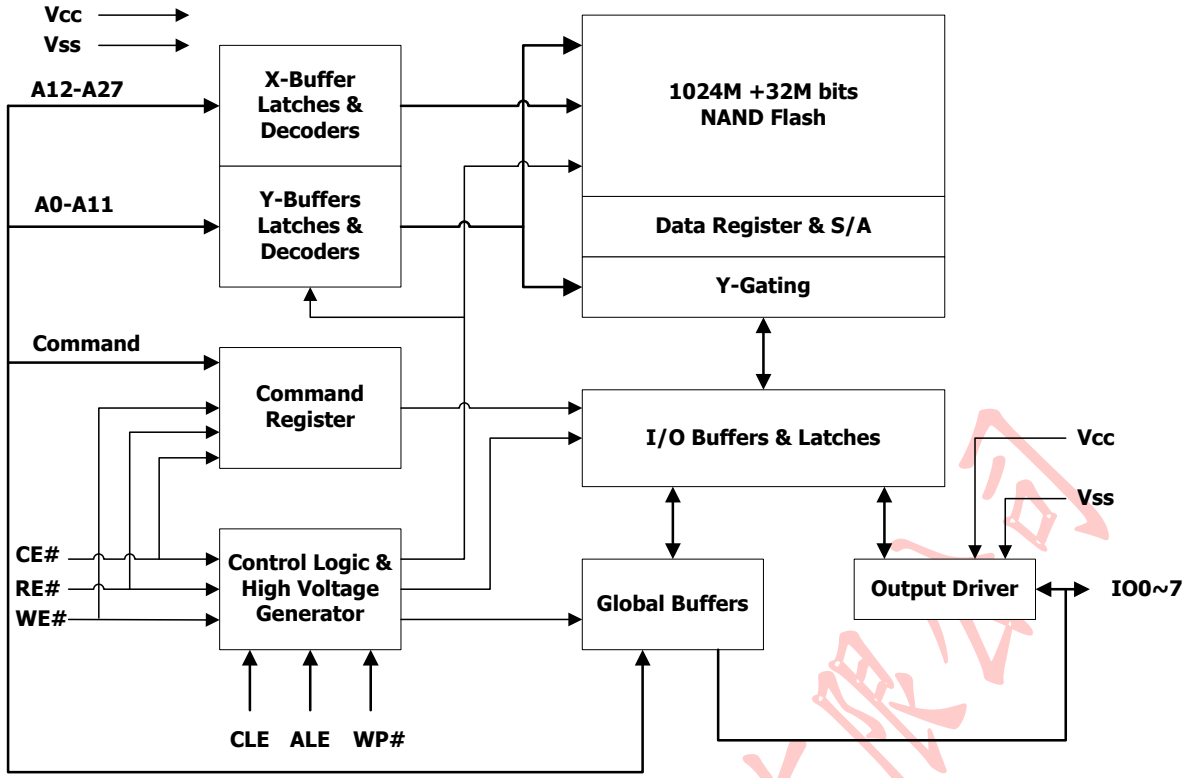
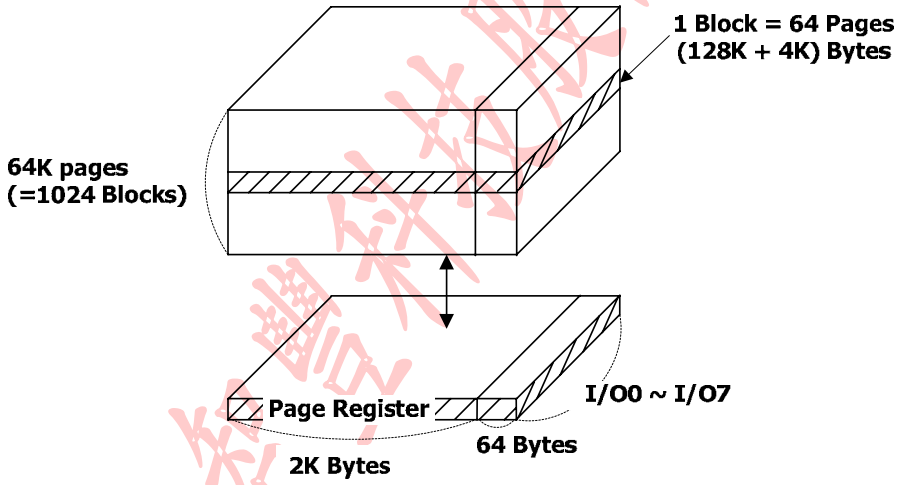
Block Diagram



1.3 Array Organization

1 Page = (2K + 64) Bytes
1 Block = (2K +64) Bytes x 64 Pages = (128K+4K) Bytes
1 Device = (2K +64) Bytes x 64 Pages x 1024 Blocks = 1056 Mbits



1.4 Address Cycle Map

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st cycle	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	**Column Address**
2nd cycle	A_8	A_9	A_{10}	A_{11}	*L	*L	*L	*L	**Column Address**
3rd cycle	A_{12}	A_{13}	A_{14}	A_{15}	A_{16}	A_{17}	A_{18}	A_{19}	**Row Address**
4th cycle	A_{20}	A_{21}	A_{22}	A_{23}	A_{24}	A_{25}	A_{26}	A_{27}	**Row Address**

Notes : Column Address : Starting Address of the Register.
* L must be set to "Low".
* The device ignores any additional input of address cycles than required.

1.5 Command Set

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy-Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input (1)	85h	-	
Random Data Output (1)	05h	E0h	
Read Status	70h	-	O
Cache Program	80h	15h	
Cache Read	31h		
Read Start for Last Page Cache Read	3Fh		

Notes : 1.Random Data Input/Output can be executed in a page.

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1.6 Mode Selection

CLE	ALE	CE#	WE#	RE#	WP#	Mode	
H	L	L	↑	H	X	Read Mode	Command Input
L	H	L	↑	H	X		Address Input (4 clock)
H	L	L	↑	H	H	Write Mode	Command Input
L	H	L	↑	H	H		Address Input (4 clock)
L	L	L	↑	H	H	Data Input	
L	L	L	H	↓	X	Data Output	
X	X	X	X	H	X	During Read (Busy)	
X	X	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X[1]	X	X	X	L	Write Protect	
X	X	H	X	X	0V/V_{CC}[2]	Stand-by	

Notes : 1.X can be VIL or VIH.
2.WP# should be biased to CMOS high or CMOS low for standby.

1.7 Condition / Parameter

1.7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to VSS	Vcc	-0.6 to +2.45	V
	VIN	-0.6 to +2.45	
	VI/O	-0.6 to Vcc+0.3(<2.45V)	
Temperature Under Bias	TBIAS	-40 to +125	°C
Storage Temperature	TSTG	-65 to +150	°C
Short Circuit Current	IOS	5	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1.7.2 Recommended Operating Conditions (Voltage reference to GND, TA=-30 to 85℃)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	1.7	1.8	1.95	V
Supply Voltage	Vss	0	0	0	V

1.7.3 Valid Block

Parameter	Symbol	Min	Typ.	Max	Unit
1Gb (128Mb x8)	NVB	1,004	-	1,024	Block

Notes :1. The device may include initial invalid blocks when first shipped. The number of valid blocks is presented as first shipped. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of initial invalid blocks.
2. The 1st block, which is placed on 00h block address, is guaranteed to be a valid block at the time of shipment and is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/528 Byte ECC.

1.7.4 AC Test Condition (T_A=-30 to 85℃, Vcc=1.7V ~ 1.95V)

Parameter	1Gb (128Mb x8)
Input Pulse Levels	0V to Vcc
Input Rise and Fall Times	5ns
Input and Output Timing Levels	Vcc/2
Output Load*	1 TTL GATE and CL=30pF

Note: Read/Busy#, R/B# output's Busy to Ready time is decided by the pull-up resistor (Rp) tied to the R/B# pin.

1.7.5 Capacitance (T_A=25℃, V_{CC}=1.8V, f=1.0MHz)

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	CI/O	VIL=0V	-	10	pF
Input Capacitance	CIN	VIN=0V	-	10	pF

Note: Capacitance is periodically sampled and not 100% tested.

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1.8 Characteristics

1.8.1 DC and Operation Characteristics (Recommended operation conditions otherwise noted)

Parameter		Symbol	Test Conditions	Min	Typ.	Max	Unit
Operating Current	Page Read with Serial Access	ICC1	tRC=45ns, CE#=VIL, IOUT=0mA	-	15	20	mA
	Program	ICC2	-	-	15		
	Erase	ICC3	-	-	15		
Stand-by Current (TTL)		ISB1	CE#=VIH, WP#=0V/VCC	-	-	1	
Stand-by Current (CMOS)		ISB2	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	uA
Input Leakage Current		ILI	VIN=0 to Vcc (max)		-	+/-10	
Output Leakage Current		ILO	VOUT=0 to Vcc (max)		-	+/-10	
Input High Voltage		VIH (1)		0.8 x Vcc	-	Vcc+0.3	V
Input Low Voltage, All inputs		VIL (1)		-0.3	-	0.2 x Vcc	
Output High Voltage Level		VOH	IOH=-100 uA	Vcc-0.1	-	-	
Output Low Voltage Level		VOL	IOL=+100 uA	-	-	0.1	
Output Low Current (R/B#)		IOL (R/B#)	VOL=0.1V	3	4	-	mA

Notes : 1. VIL can undershoot to -0.4V and VIH can overshoot to VCC + 0.4V for durations of 20 ns or less.
2. Typical value are measured at Vcc=1.8V, TA=25℃. Not 100% tested.

1.8.2 Program / Erase Characteristics (T_A=-30 to 85℃, Vcc=1.7V ~ 1.95V)

Parameter	Symbol	Min	Typ	Max	Unit
Average Program Time	tPROG	-	250	700	us
Dummy Busy Time for Cache Operation	tCBSY	-	3	700	us
Number of Partial Program Cycles in the Same Page	Nop	-	-	4	cycle
Block Erase Time	tBERS	-	2	10	ms

Notes :
1. Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 1.8V Vcc and 25℃ temperature.
2. tPROG is the average program time of all pages. Users should be noted that the program time variation from page to page is possible.
3. tCBSY max. time depends on timing between internal program completion and data-in.

1.8.3 AC Timing Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	tCLS(1)	25	-	ns
CLE Hold Time	tCLH	10	-	ns
CE# Setup Time	tCS(1)	35	-	ns
CE# Hold Time	tCH	10	-	ns
WE# Pulse Width	tWP	25	-	ns
ALE Setup Time	tALS(1)	25	-	ns
ALE Hold Time	tALH	10	-	ns
Data Setup Time	tDS(1)	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	45	-	ns
WE# High Hold Time	tWH	15	-	ns
Address to Data Loading Time	tADL(2)	100(2)	-	ns

Notes : 1.The transition of the corresponding control pins must occur only once while WE# is held low.
2.tADL is the time from the WE rising edge of final address cycle to the WE# rising edge of first data cycle.

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1.8.4 AC Characteristics for Operation

Parameter		Symbol	Min	Max	Unit
Data Transfer from Cell to Register		tR	-	25	us
ALE to RE# Delay		tAR	10	-	ns
CLE to RE# Delay		tCLR	10	-	ns
Ready to RE# Low		tRR	20	-	ns
RE# Pulse Width		tRP	25	-	ns
WE# High to Busy		tWB	-	100	ns
WP# Low to WE# Low (disable mode)		tWW	100	-	ns
WP# High to WE# Low (enable mode)					
Read Cycle Time		tRC	45	-	ns
RE# Access Time		tREA	-	30	ns
CE# Access Time		tCEA	-	45	ns
RE# High to Output Hi-Z		tRHZ	-	100	ns
CE# High to Output Hi-Z		tCHZ	-	30	ns
CE# High to ALE or CLE Don't care		tCSD	0		ns
RE# High to Output Hold		tRHOH	15	-	ns
RE# Low to Output Hold		tRLOH	5		ns
CE# High to Output Hold		tCOH	15	-	ns
RE# High Hold Time		tREH	15	-	ns
Output Hi-Z to RE# Low		tIR	0	-	ns
RE# High to WE# Low		tRHW	100	-	ns
WE# High to RE# Low		tWHR	60	-	ns
Device Resetting Time during…	Read	tRST	-	5	us
	Program		-	10	us
	Erase		-	500	us
	Ready		-	5 (1)	us
Cache Busy in Read Cache (following 31h and 3Fh)		tDCBSYR	-	30	ns

Note: 1. If reset command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

2 NAND Flash Technical Notes

2.1 Mask Out Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

The 1st block, which is placed on 00h block address, is guaranteed to be a valid block up to 1K program/erase cycles with 1bit/528Byte ECC.

2.2 Identifying Initial Invalid Block(s) and Block Replacement Management

Unpredictable behavior may result from programming or erasing the defective blocks. Figure below illustrates an algorithm for searching factory-mapped defects, and the algorithm needs to be executed prior to any erase or program operations.

A host controller has to scan blocks from block 0 to the last block using page read command and check the data at the column address of 0 or 2,047. If the read data is not FFh, the block is interpreted as an invalid block. The initial invalid block information is erasable, and which is impossible to be recovered once it has been erased. Therefore, the host controller must be able to recognize the initial invalid block information and to create a corresponding table to manage block replacement upon erase or program error when additional invalid blocks develop with Flash memory usage.

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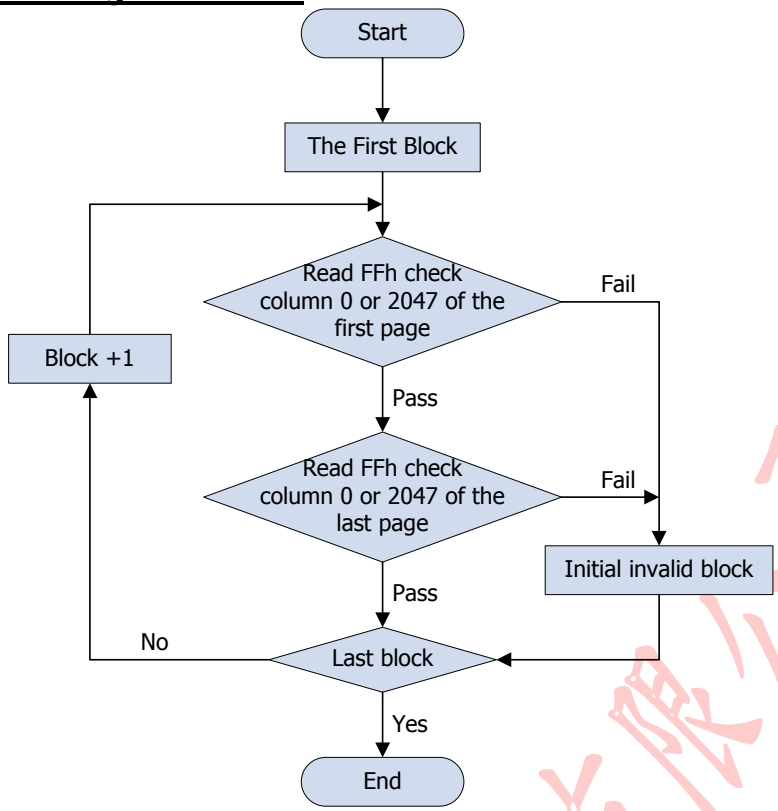
Bad Block scanning Flow Chart




```
For (i=0; i<Num_of_LUs; i++)  {
    For (j=0; j<Blocks_Per_LU; j++)  {
        Defect_Block_Found=False;

        Read_Page(lu=i, block=j, page=0);
        If (Data[coloumn=0]!=FFh)   Defect_Block_Found=True;
       If Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;

        Read_Page(lu=i, block=j, page=Page_Per_Block-1);
        If (Data[coloumn=0]!=FFh)   Defect_Block_Found=True;
         If (Data[coloumn=First_Byte_of_Spare_Area]!=FFh)   Defect_Block_Found=True;
        If (Defect_Block_Found)   Mark_Block_as_Defective(lu=i, block=j);
    }
}
```

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2.3 Error in Write or Read Operation

Within its lifetime, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The additional block failure rate does not include those reclaimed blocks.

Failure Mode		Detection and Countermeasure Sequence
Write	Erase failure	Read Status after Erase → Block Replacement
	Program failure	Read Status after Program → Block Replacement
Read	Single bit failure	Verify ECC → ECC Correction

Note: Error Correcting Code → Hamming Code etc.
Example: 1bit correction / 528 Byte

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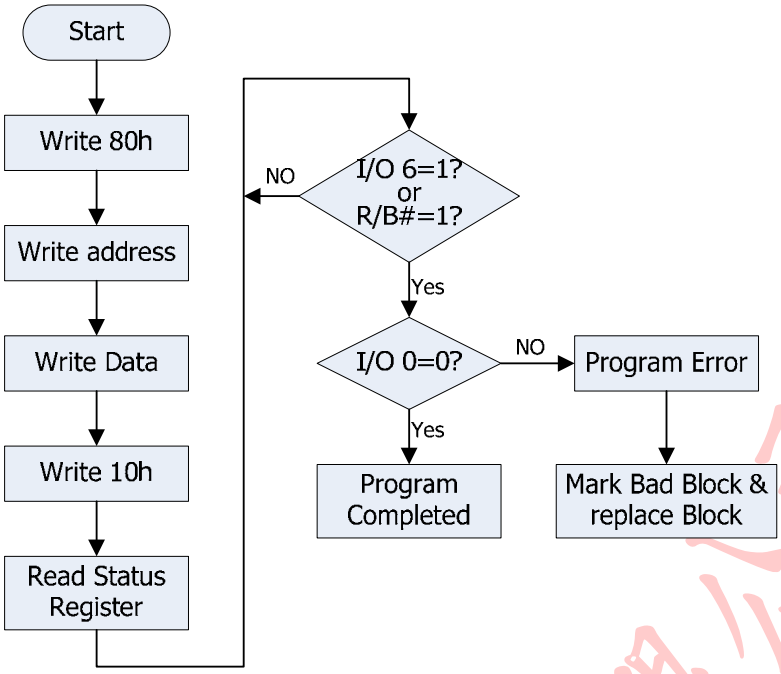
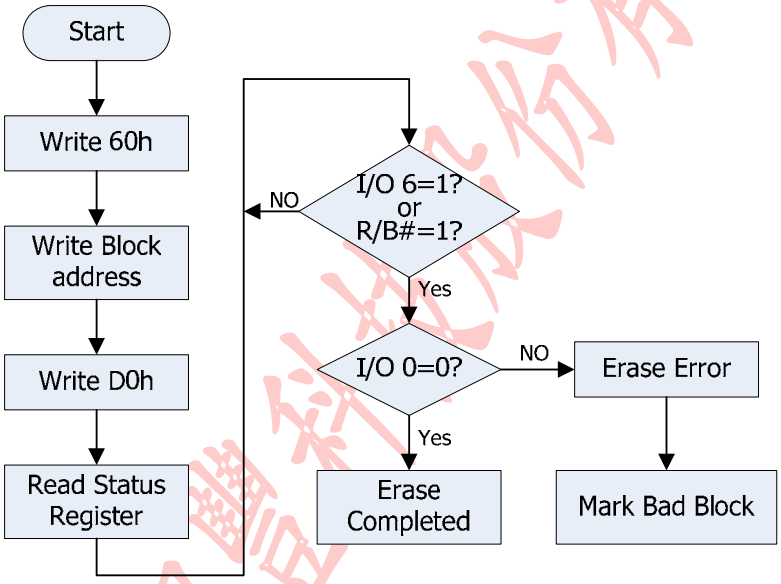
Program Flow Chart



Erase Flow Chart



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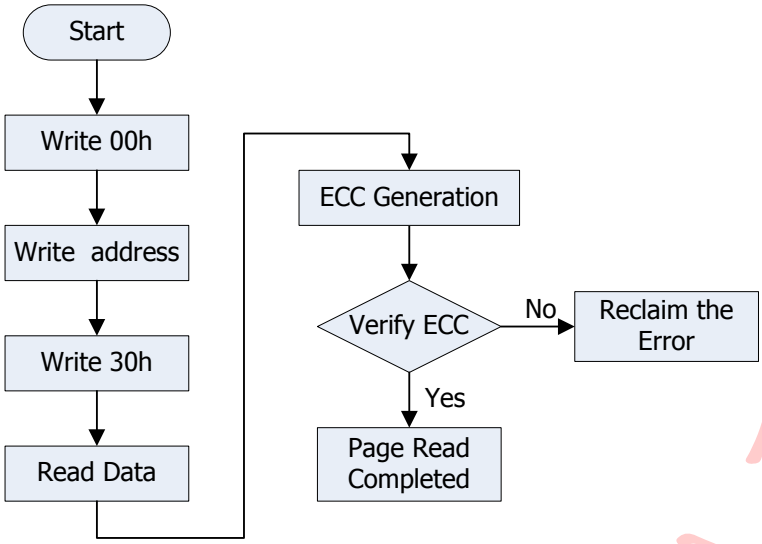
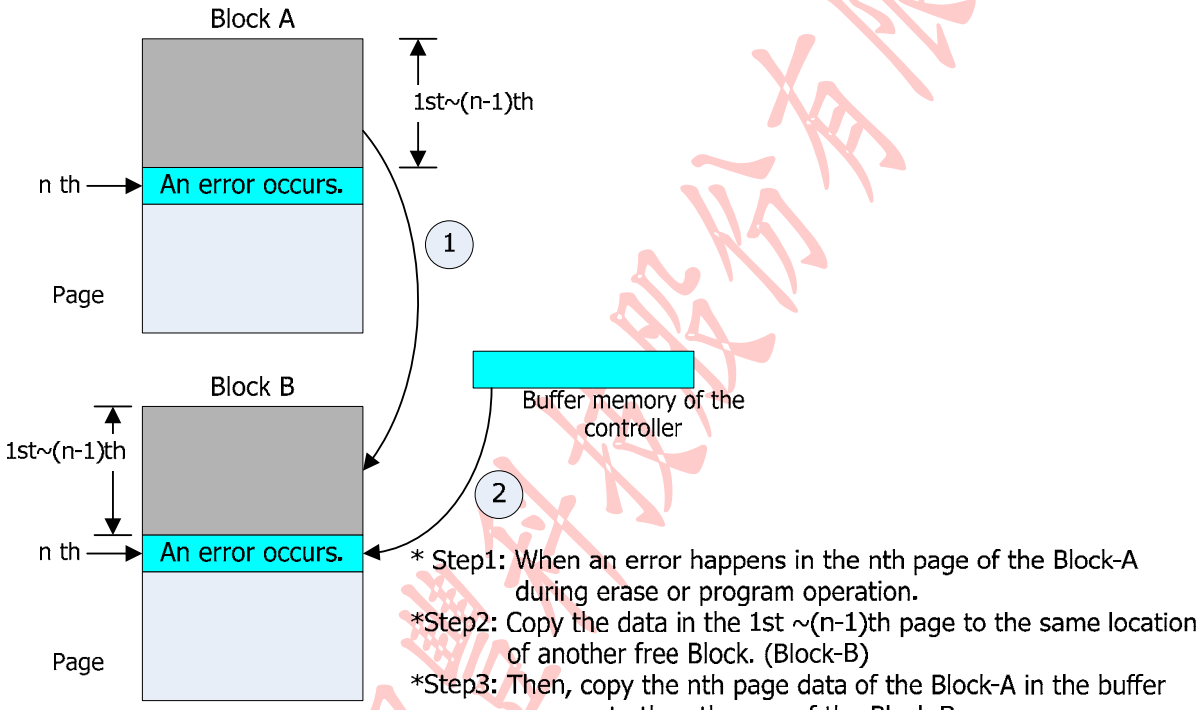
Read Flow Chart



Block Replacement



* Step1: When an error happens in the nth page of the Block-A during erase or program operation.
*Step2: Copy the data in the 1st ~(n-1)th page to the same location of another free Block. (Block-B)
*Step3: Then, copy the nth page data of the Block-A in the buffer memory to the nth page of the Block-B.
*Step4: Do not erase or program to Block-A by creating an 'invalid block' table or other appropriate scheme.

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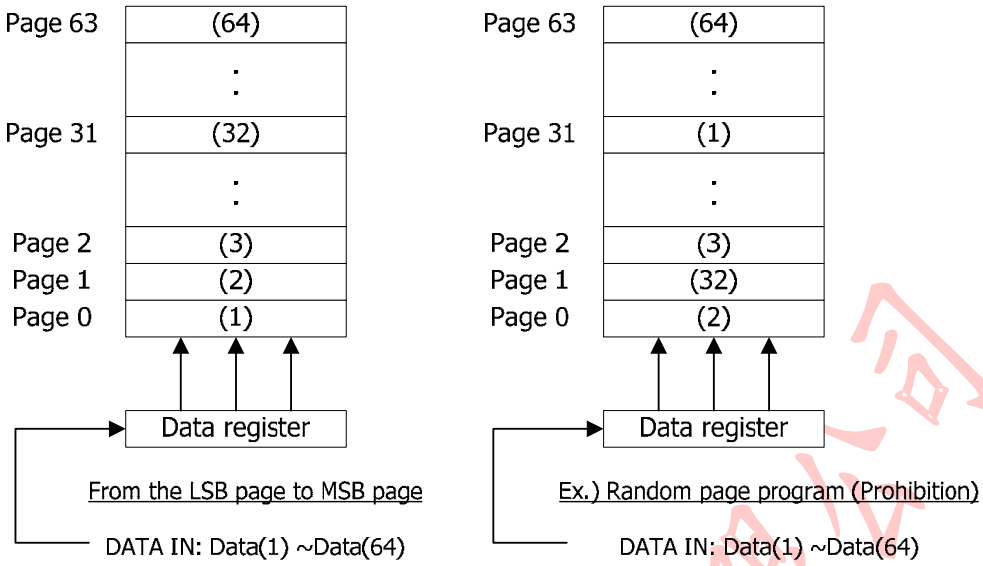
2.4 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB page doesn't need to be page 0.



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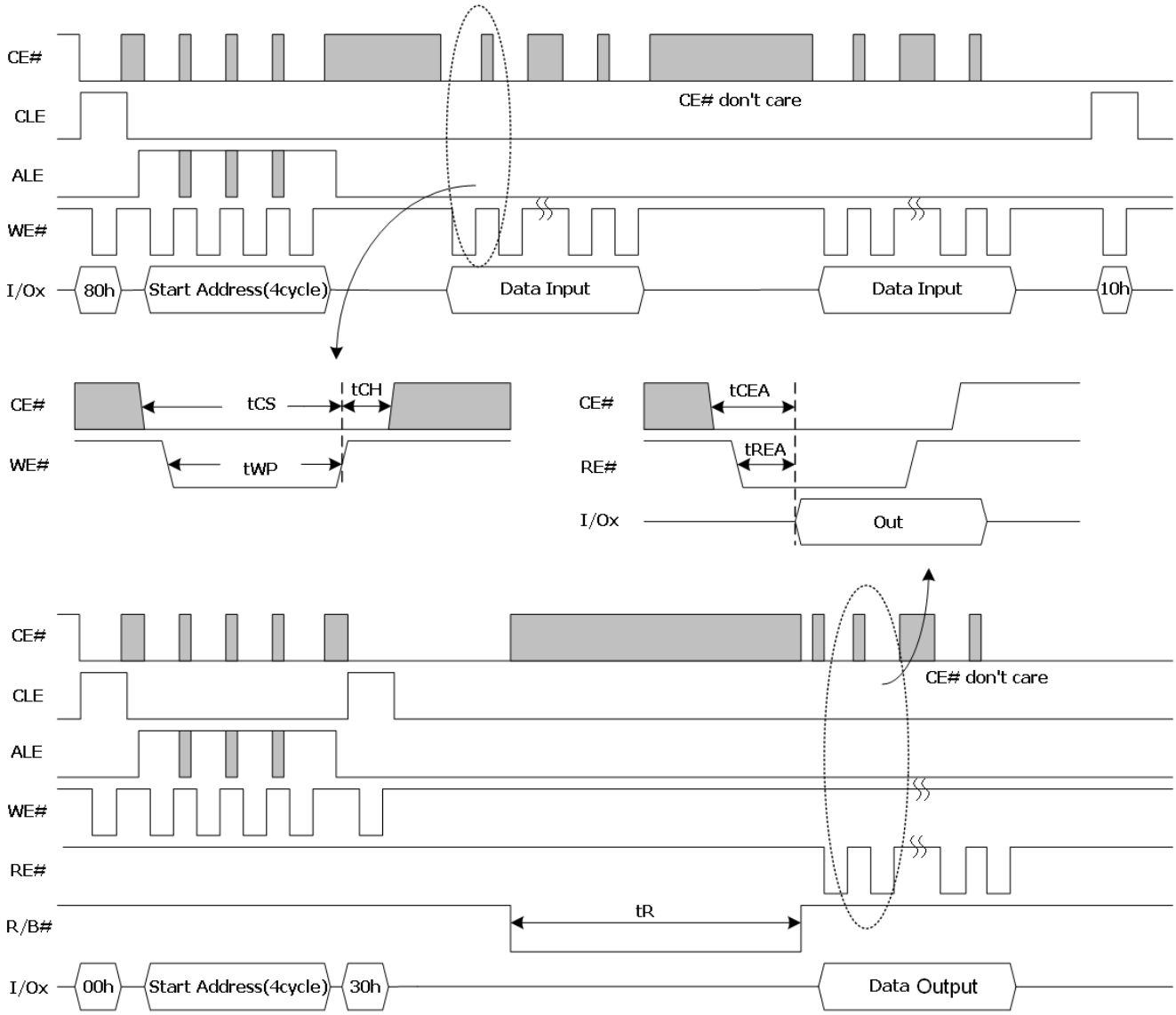
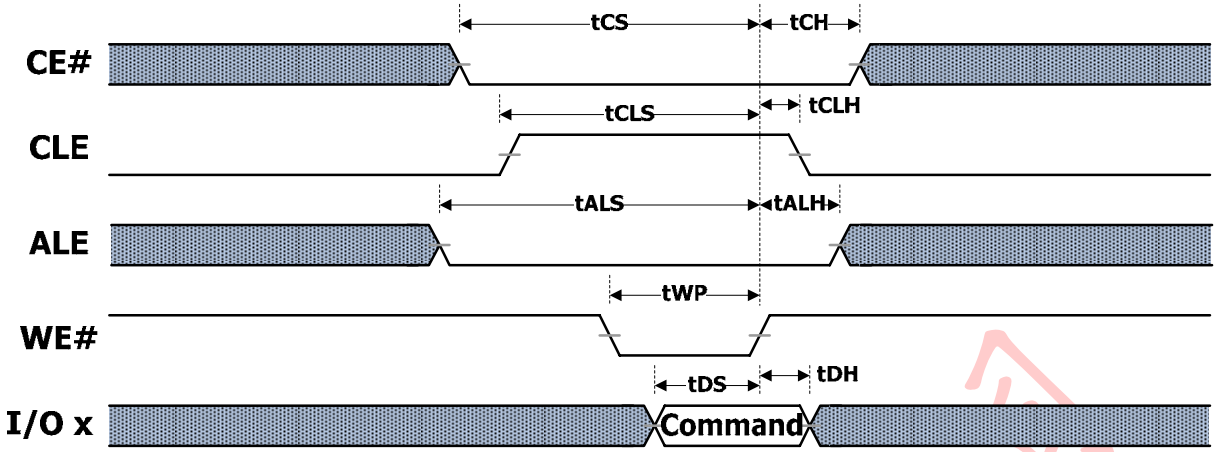
2.5 System Interface Using CE# Don't Care

For an easier system interface, CE# may be inactive during the data-loading or serial access as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications that use slow cycle time on the order of μ-seconds, de-activating CE# during the data-loading and serial access would provide significant savings in power consumption.

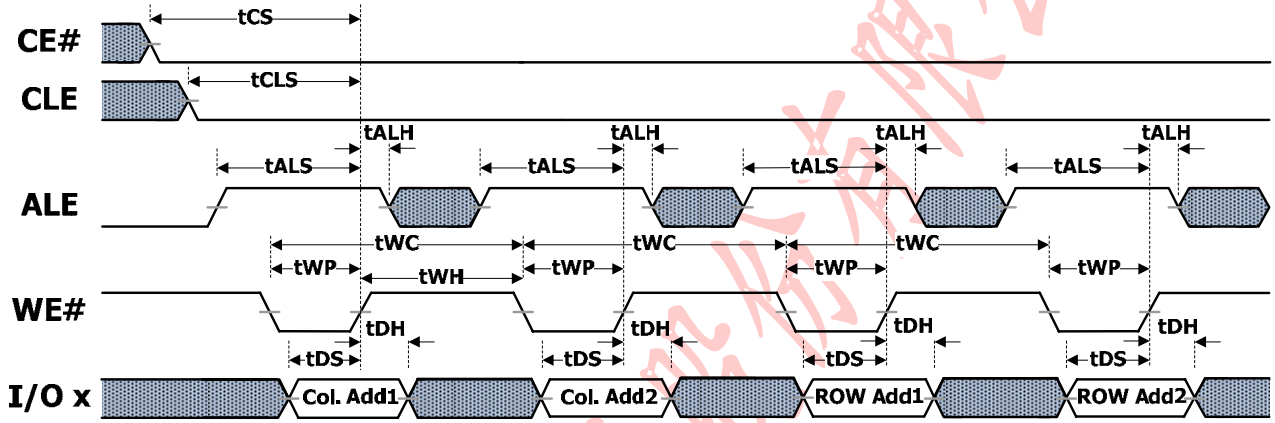


3 Timing Diagrams

3.1 Command latch Cycle



3.2 Address Latch Cycle



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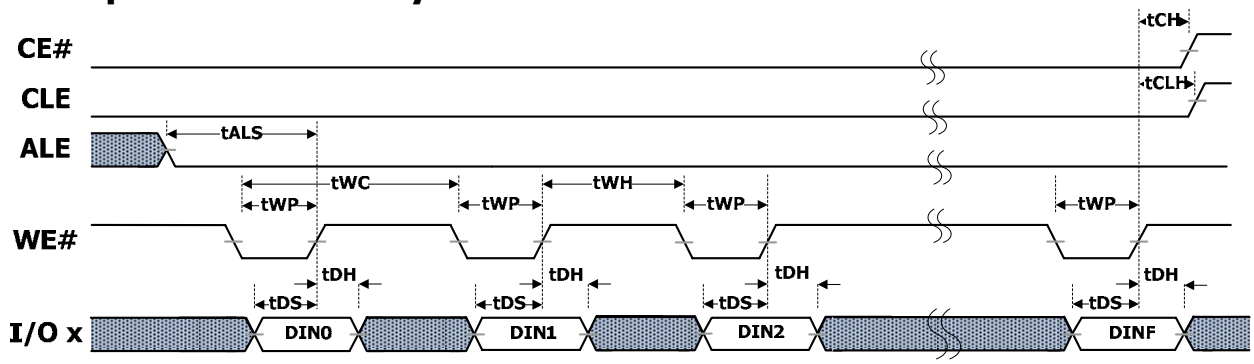
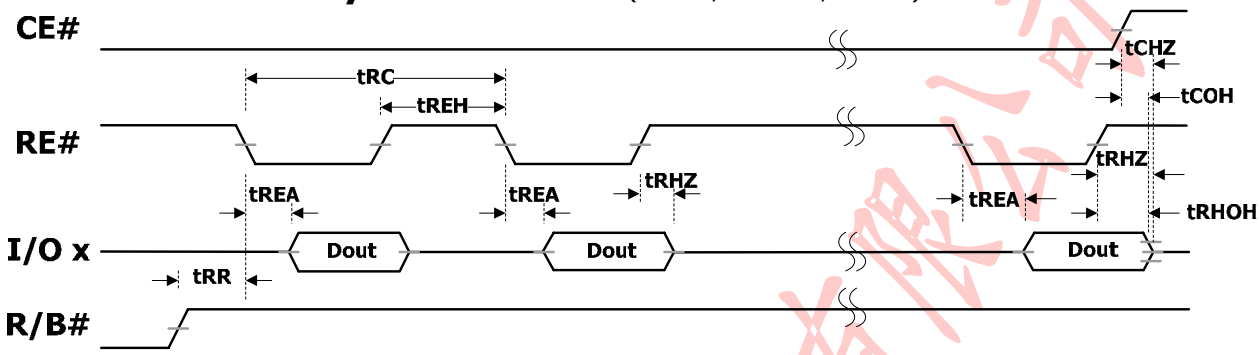
3.3 Input Data Latch Cycle



3.4 Serial Access Cycle after Read (CLE=L, WE#=H, ALE=L)



Notes: 1. Dout transition is measured at ±200mV from steady state voltage at I/O with load.
2. t_{RHOH} starts to be valid when frequency is lower than 20MHz.

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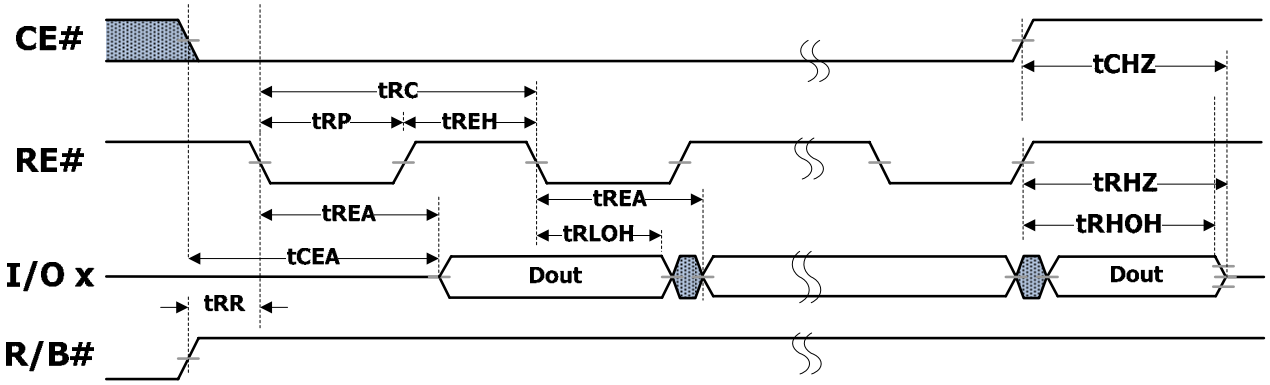
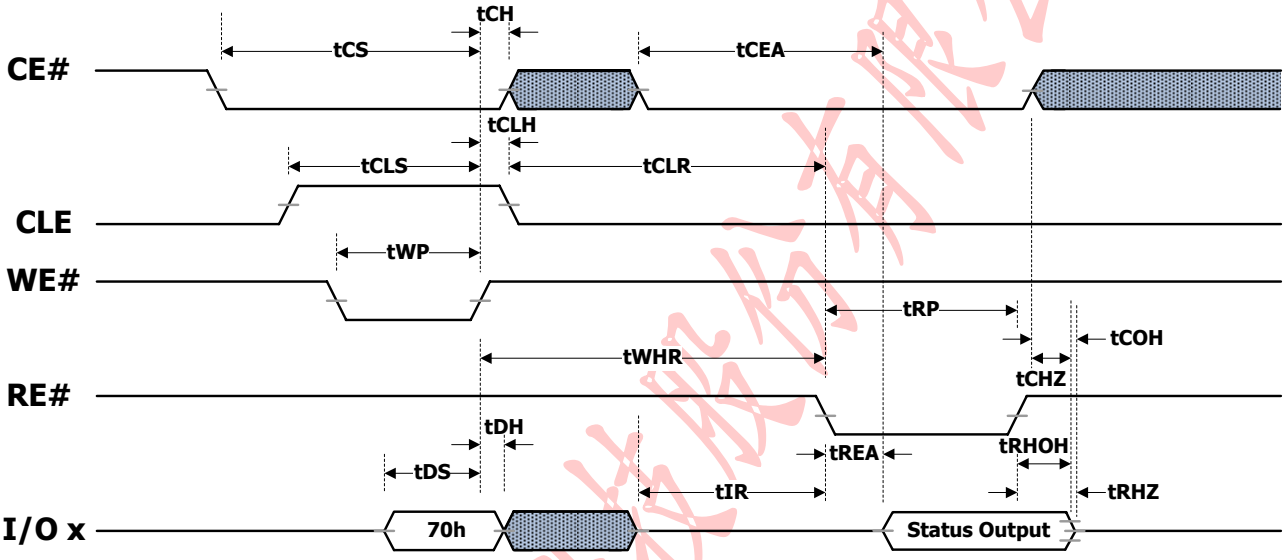
3.5 Serial Access Cycle after Read (EDO Type CLE=L, WE#=H, ALE=L)



Notes: 1. Transition is measured at +/-200mV from steady state voltage with load.
This parameter is sample and not 100% tested. (tCHZ, tRHZ)
2. tRLOH is valid when frequency is higher than 20MHZ.
tRHOH starts to be valid when frequency is lower than 20MHZ.

3.6 Status Read Cycle



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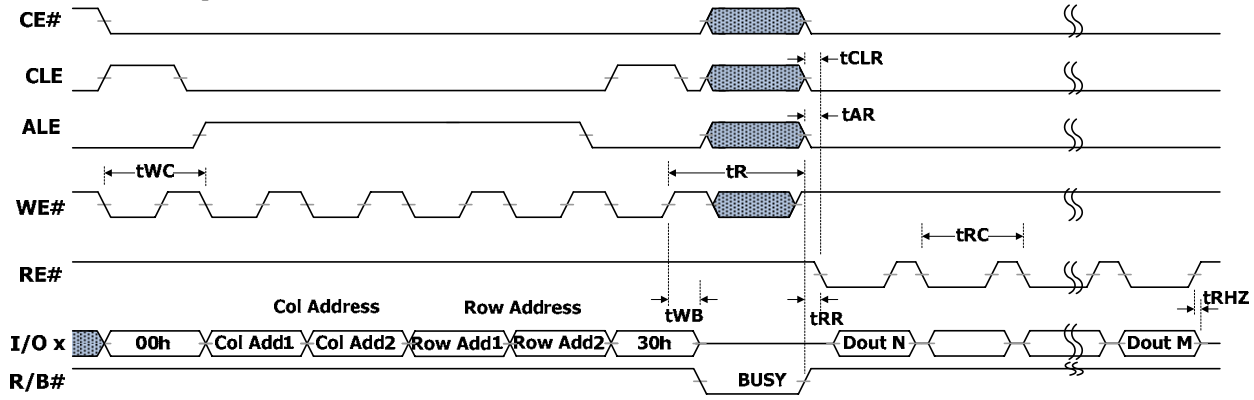
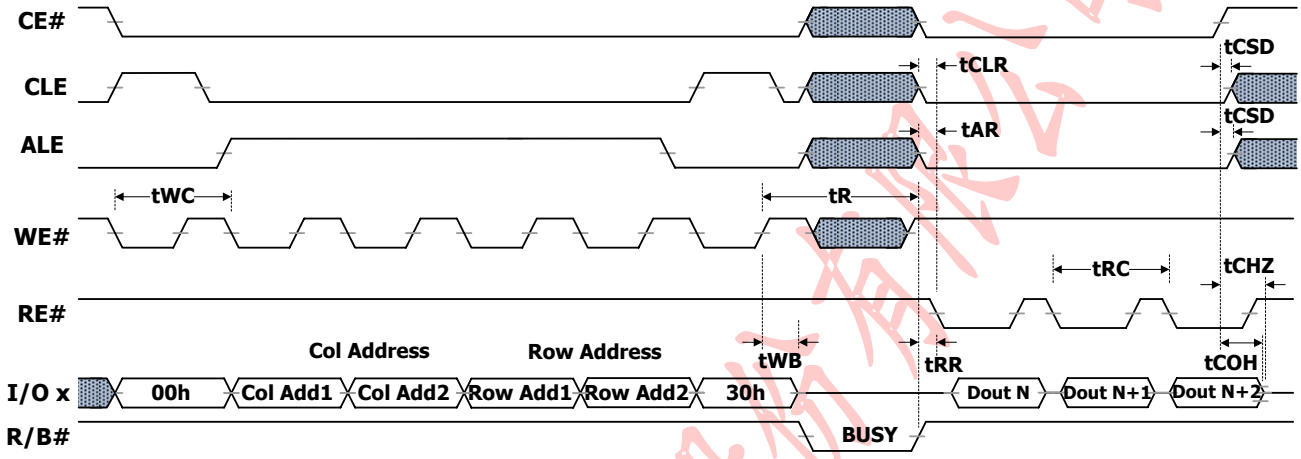
3.7 Read Operation (Read one Page)



3.8 Read Operation (Intercepted by CE#)



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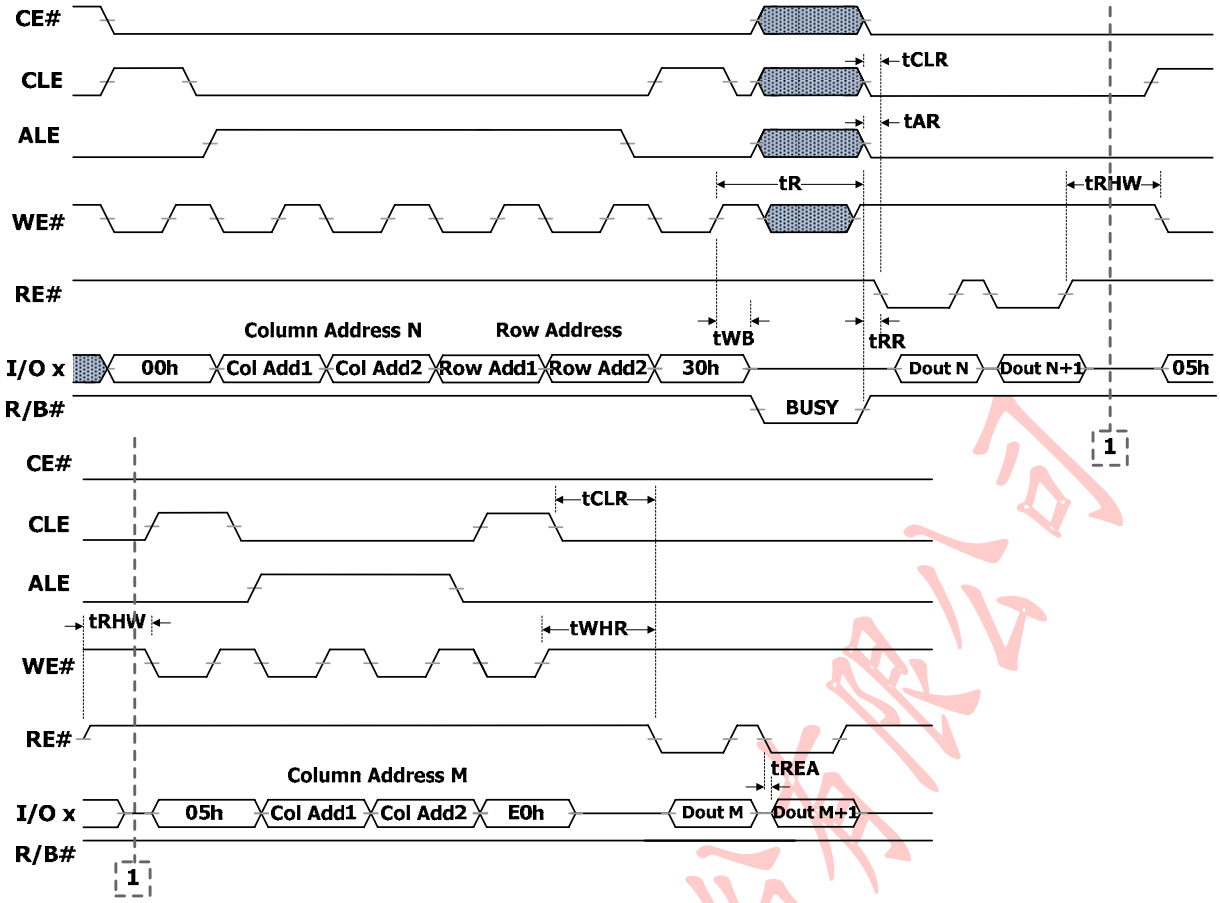
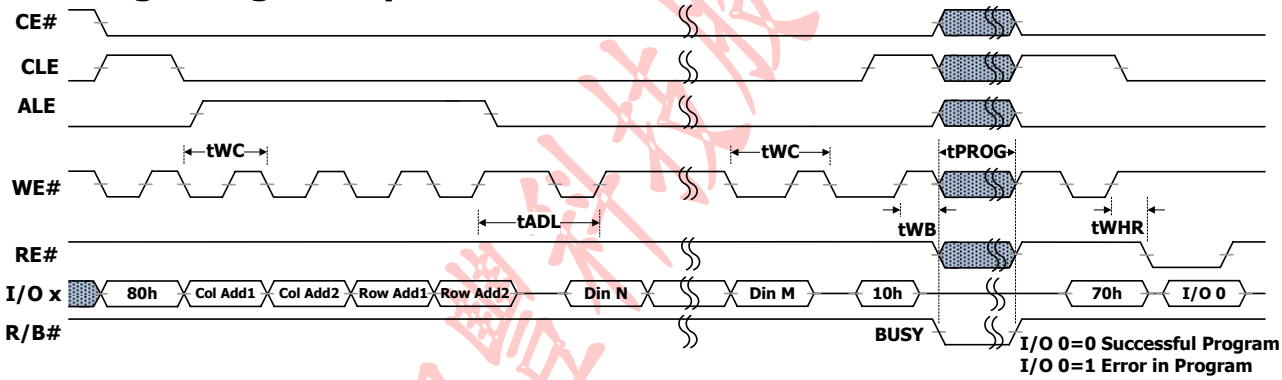
3.9 Random Data Output In a Page

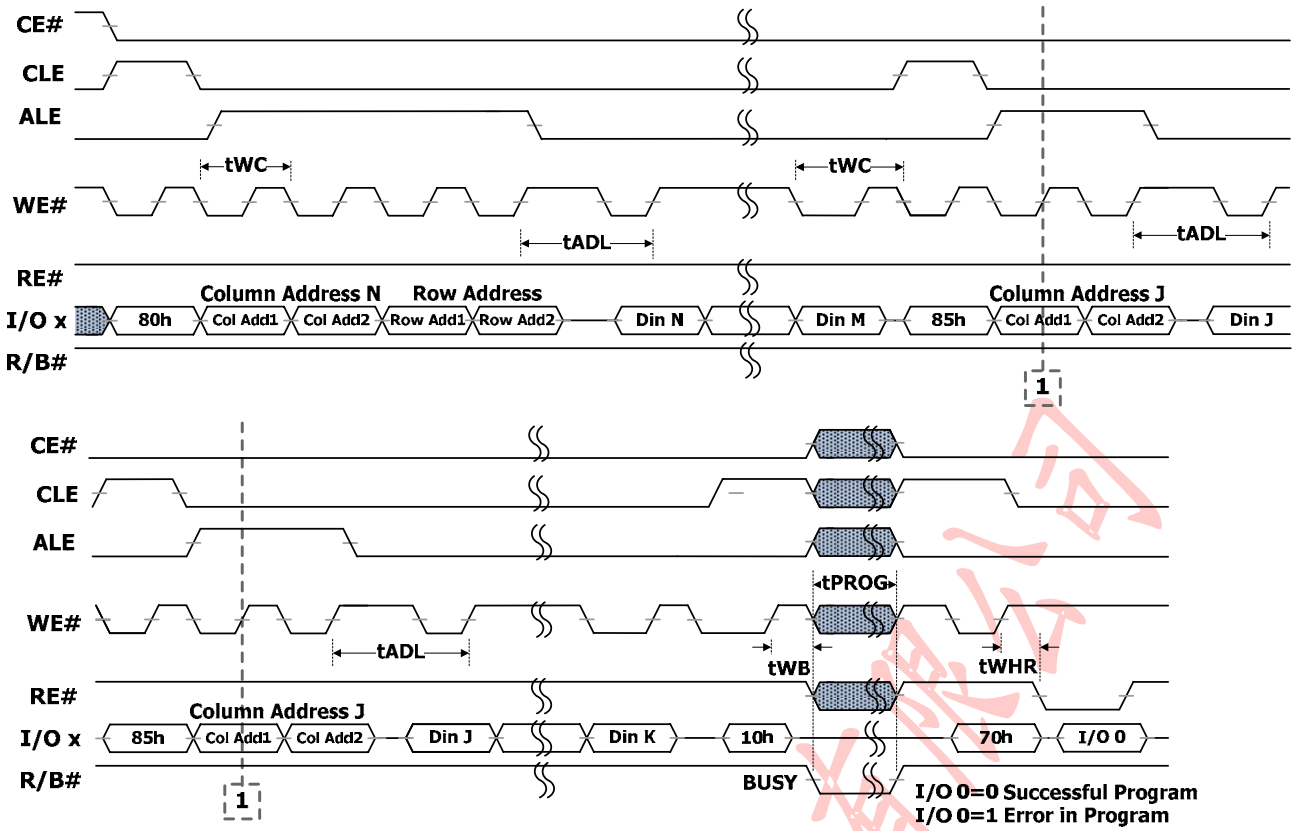


3.10 Page Program Operation



Note: t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of the first data cycle.

3.11 Page Program Operation with Random Data Input



Note: t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of the first data cycle.

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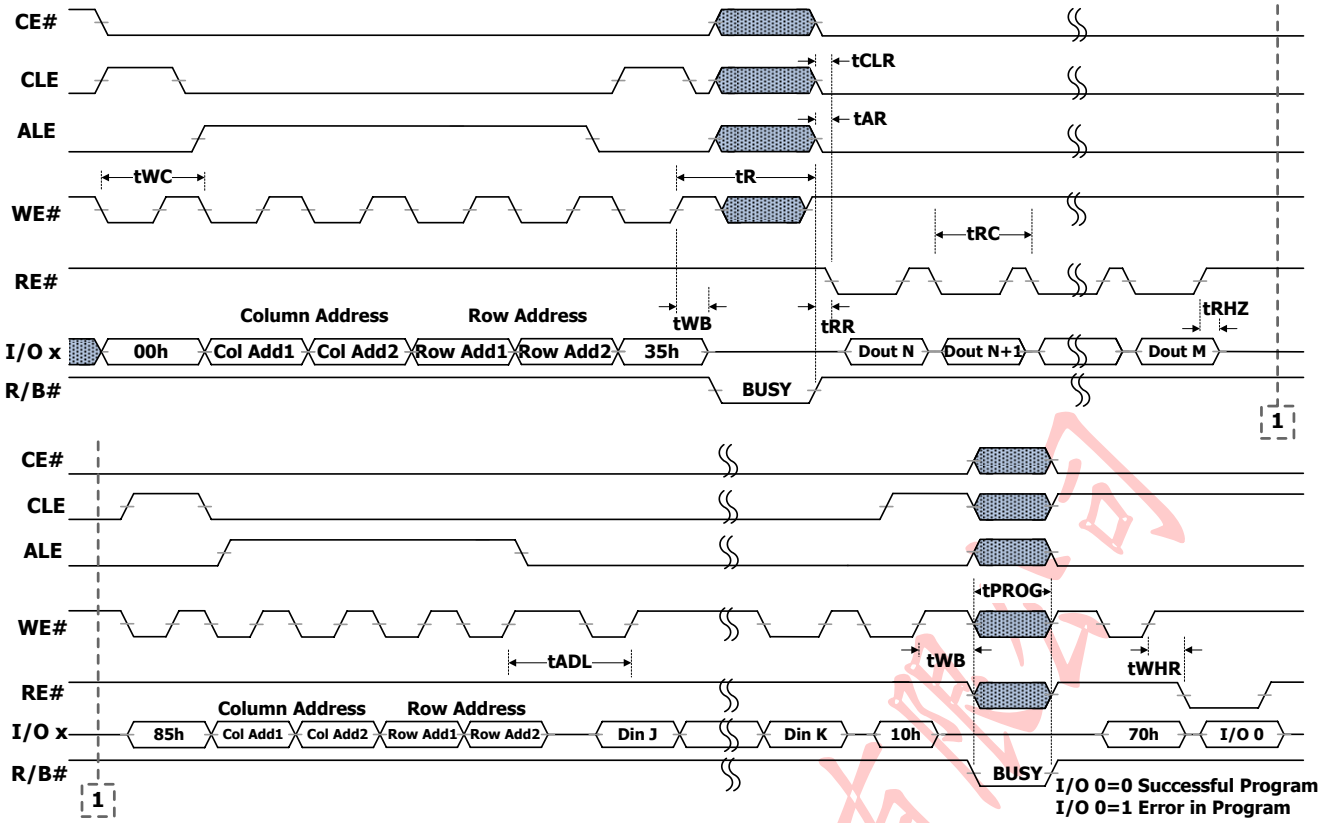
3.12 Copy-Back Operation with Random Data Input



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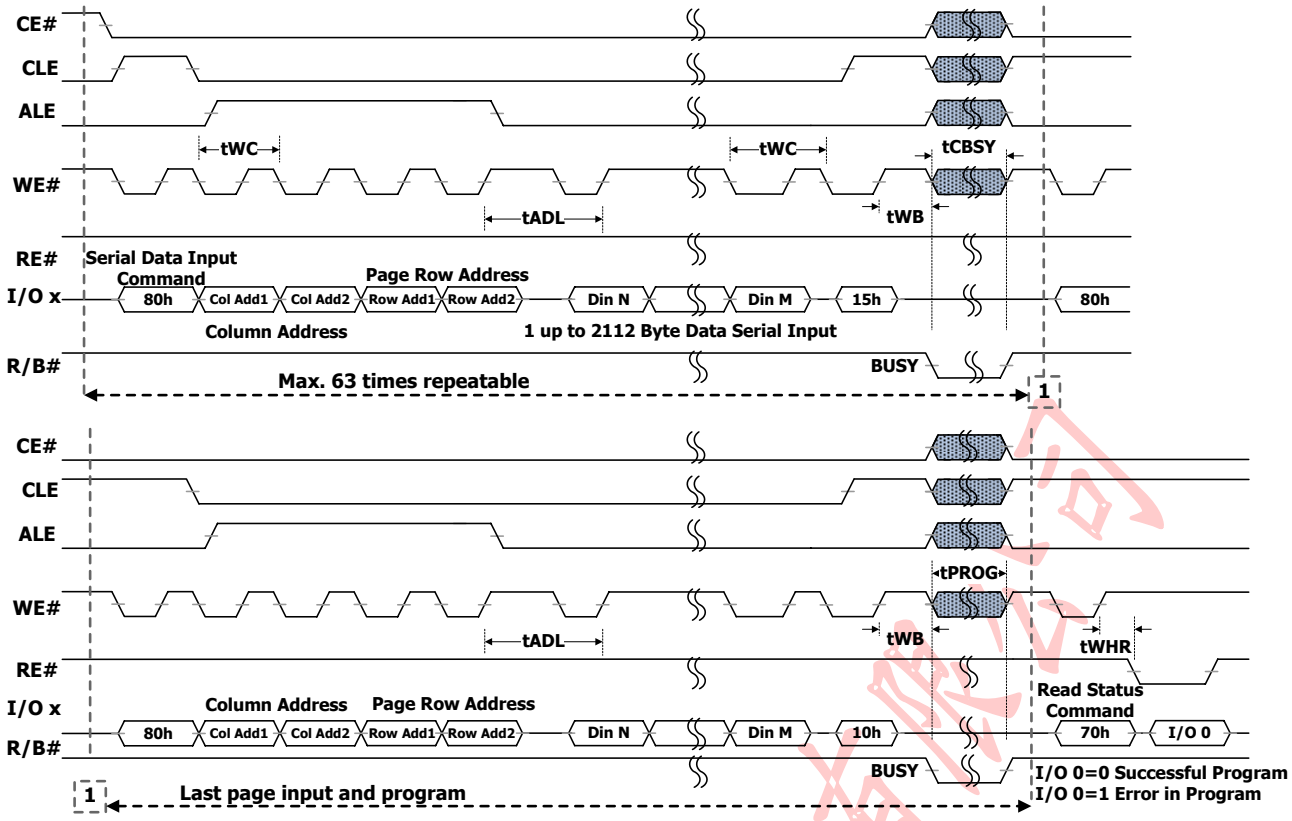
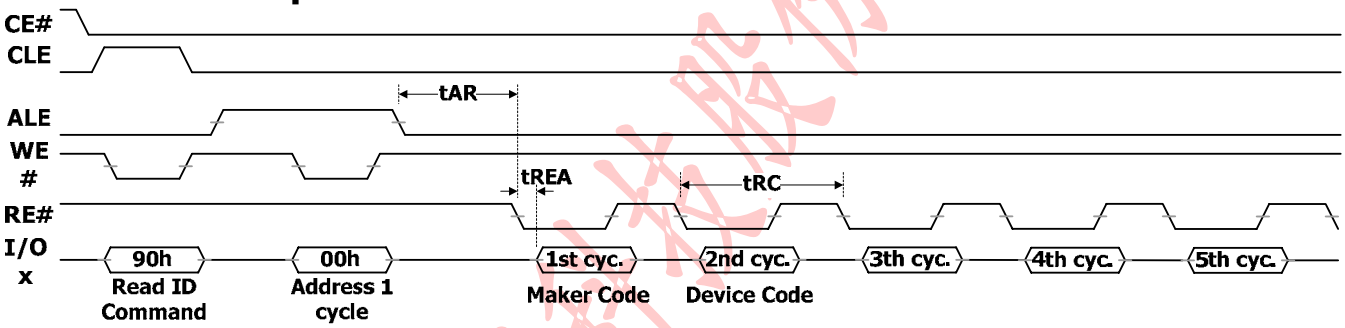
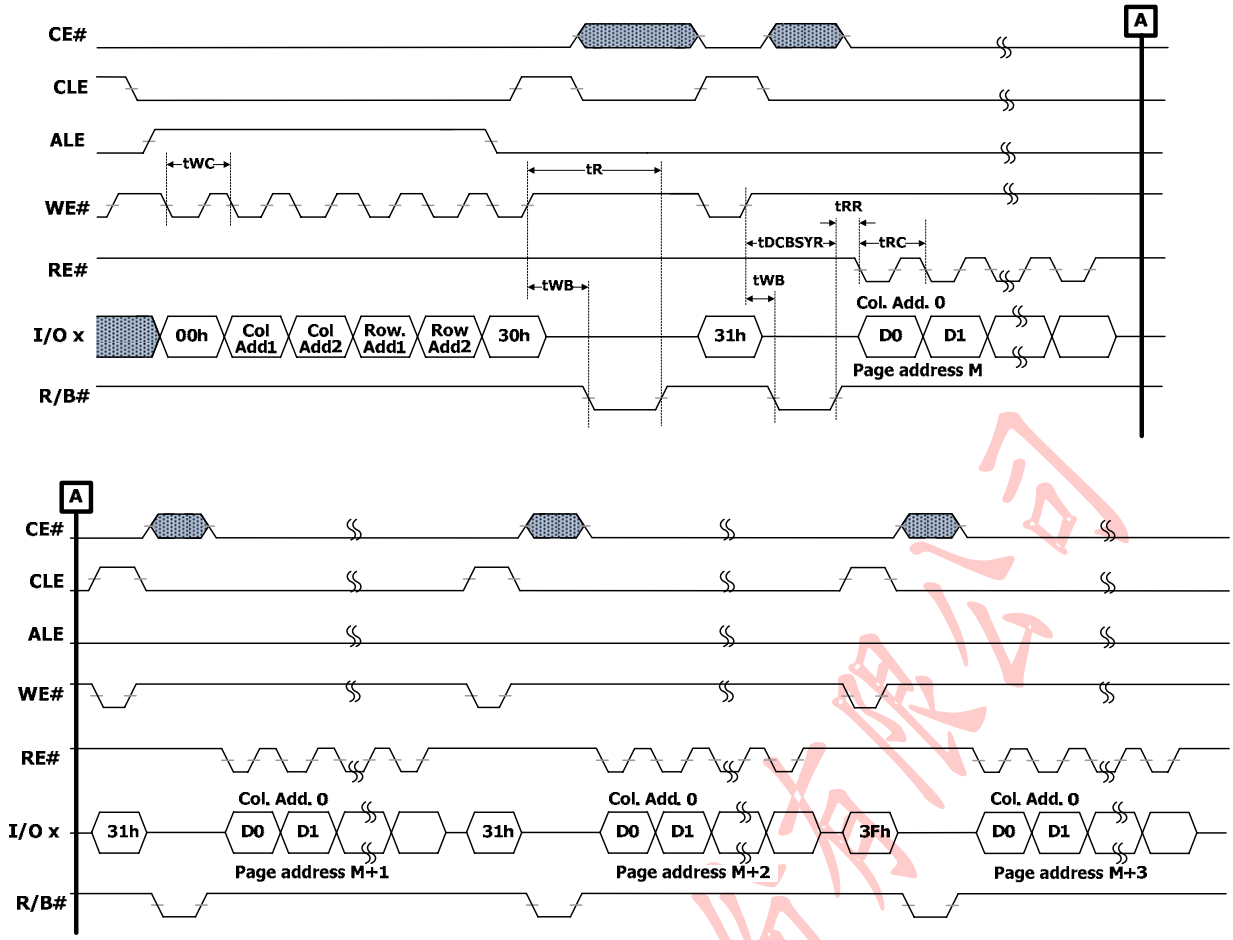
3.13 Cache Program Operation



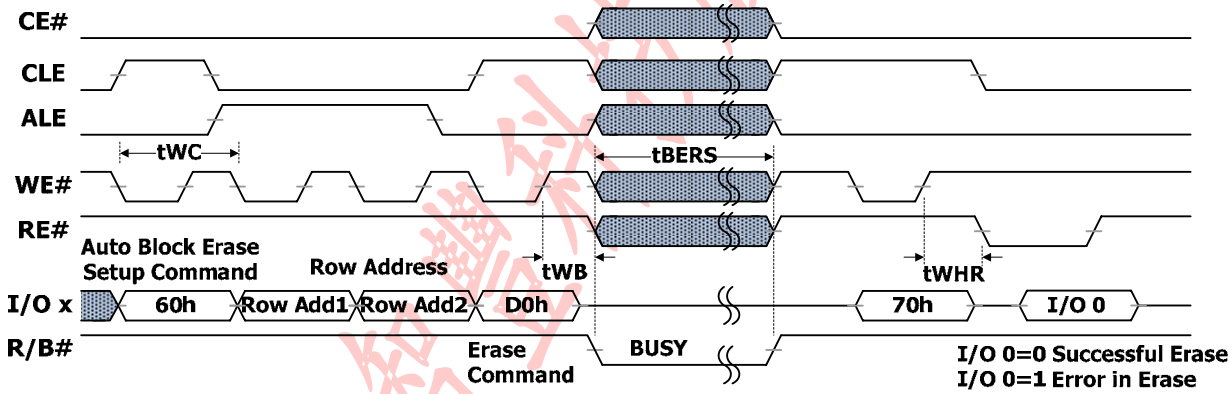
3.14 Read ID Operation



3.15 Cache Read Operation



3.16 Block Erase Operation



4 ID Definition Table

ID Access command : 90H

1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle	6th ~ 8th Cycle
C8h	A1h	80h	15h	40h	7Fh

Byte	Description
1st	Maker Code
2nd	Device Code
3rd	Internal Chip Number, Cell Type, etc
4th	Page Size, Block Size, etc
5th	Plane Number, Plane Size, ECC Level
6th	JEDEC Maker Code Continuation Code, 7Fh
7th	JEDEC Maker Code Continuation Code, 7Fh
8th	JEDEC Maker Code Continuation Code, 7Fh

3rd ID data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Program Between Multiple Chips	Not Support		0						
	Support		1						
Cache Program	Not Support	0							
	Support	1							

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4th ID data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Redundant Area Size (Byte/512Byte)	8						0		
	16						1		
Block Size (w/o redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Organization	X8		0						
	X16		1						
Serial Access Time	45ns	0				0			
	Reserved	0				1			
	Reserved	1				0			
	Reserved	1				1			

5th ID data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
ECC Level	1bit ECC/512Byte							0	0
	2bit ECC/512Byte							0	1
	4bit ECC/512Byte							1	0
	Reserved							1	1
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size (without Redundant Area)	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Reserved	Reserved	0							

6th ~ 8th ID data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
JEDEC Maker Code Continuation Code	7F	0	1	1	1	1	1	1	1

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5 Device Operation

5.1 Page Read

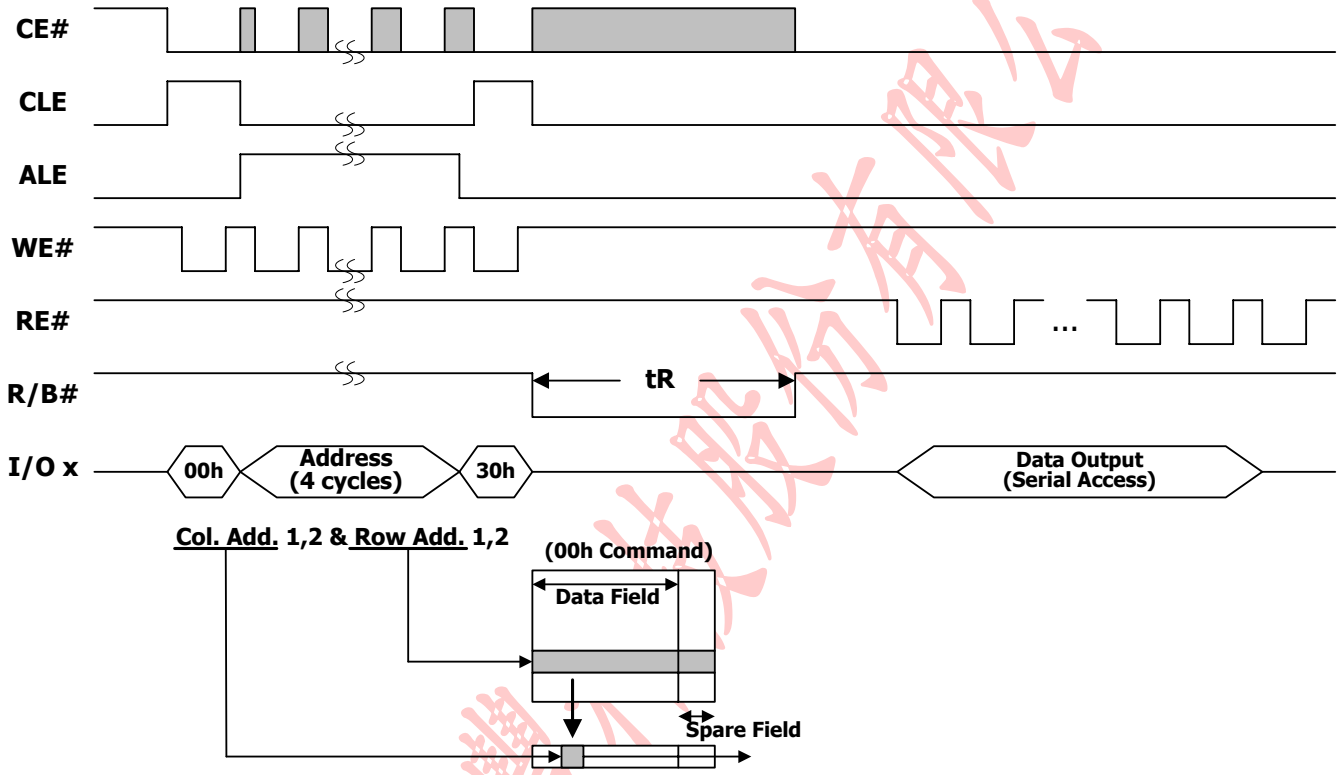
Upon initial device power up, the device defaults to Read mode. This operation is also initiated by writing 00h command, four-cycle address, and 30h command. After initial power up, the 00h command can be skipped because it has been latched in the command register. The 2,112byte of data on a page are transferred to cache registers via data registers within 25us (t_R). Host controller can detect the completion of this data transfer by checking the R/B# output. Once data in the selected page have been loaded into cache registers, each Byte can be read out in 45ns cycle time by continuously pulsing RE#. The repetitive high-to-low transitions of RE# clock signal make the device output data starting from the designated column address to the last column address.

The device can output data at a random column address instead of sequential column address by using the Random Data Output command. Random Data Output command can be executed multiple times in a page.

After power up, device is in read mode so 00h command cycle is not necessary to start a read operation.

A page read sequence is illustrated in figure below, where column address, page address are placed in between commands 00h and 30h. After t_R read time, the R/B# de-asserts to ready state. Host controller can toggle RE# to access data starting with the designated column address and their successive bytes.

Read Operation



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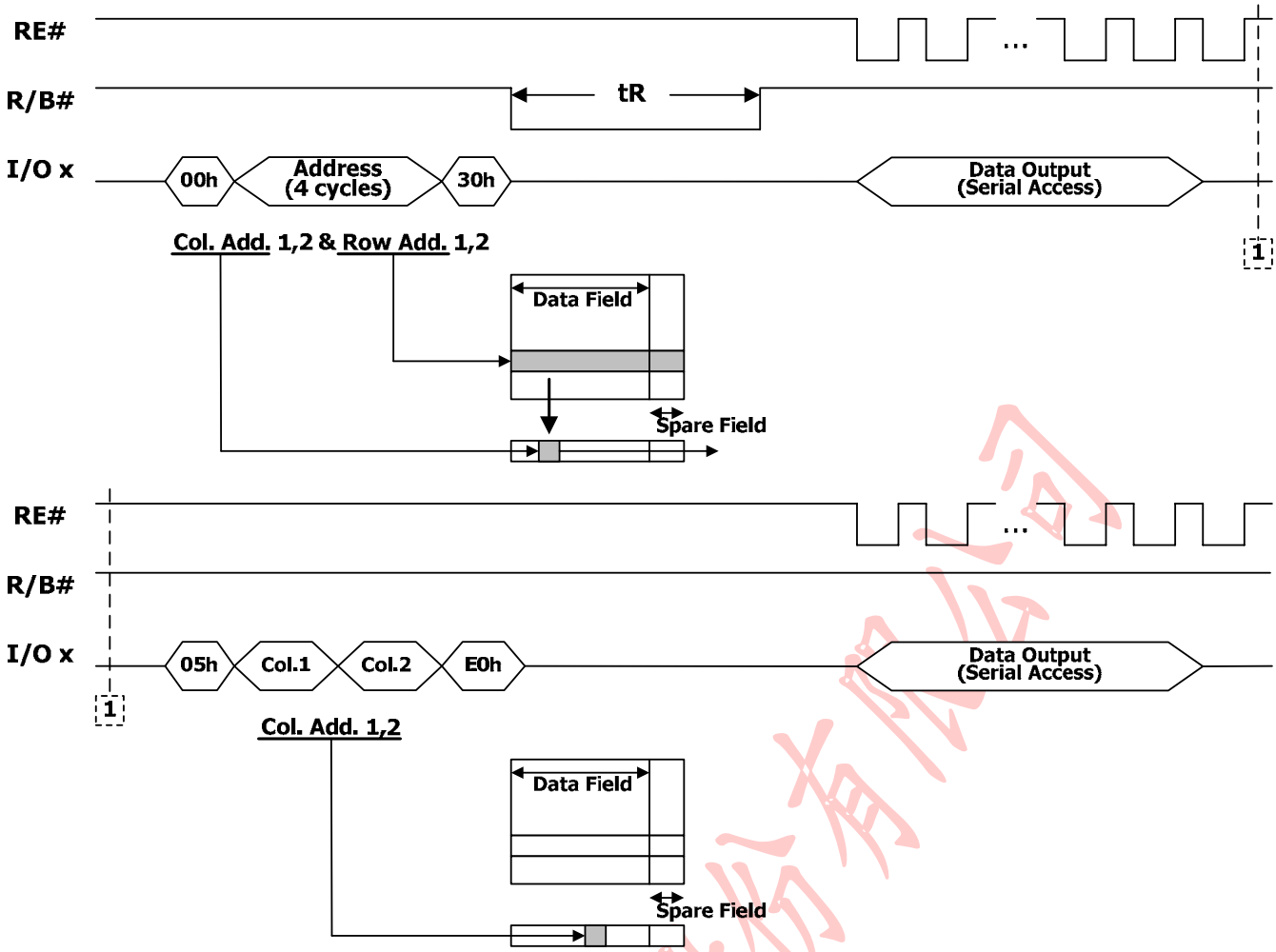
Random Data Output In a Page



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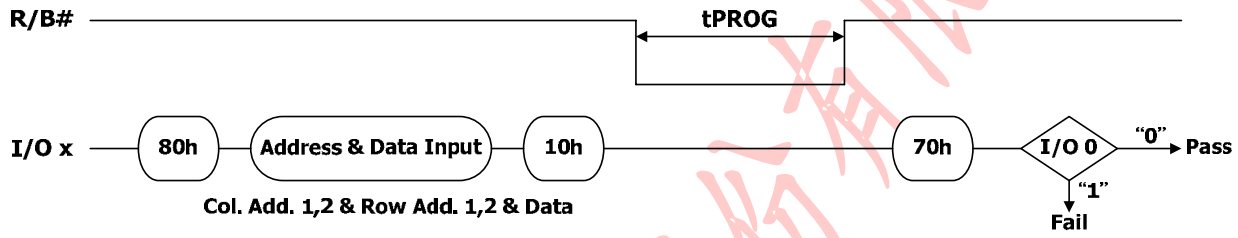
5.2 Page Program

The device is programmed basically on a page basis, but it does allow multiple partial page programming of a word or consecutive bytes up to 2,112 in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for a single page. Addressing of page program operations within a block should be in sequential order. A complete page program cycle consists of a serial data input cycle in which up to 2,112byte of data can be loaded into data register via cache register, followed by a programming period during which the loaded data are programmed into the designated memory cells.

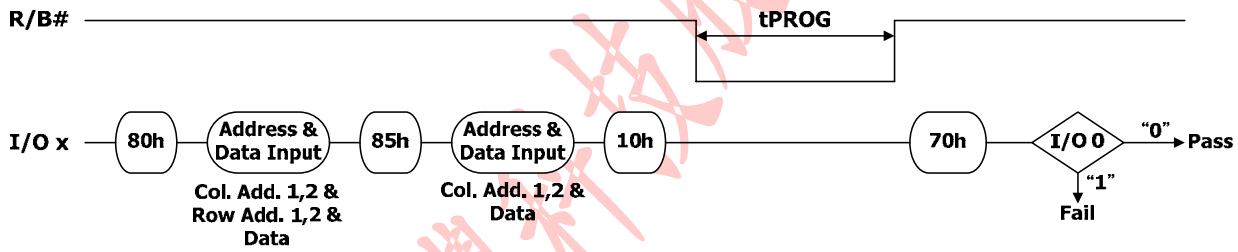
The serial data input cycle begins with the Serial Data Input command (80h), followed by a four-cycle address input and then serial data loading. The bytes not to be programmed on the page do not need to be loaded. The column address for the next data can be changed to the address follows Random Data Input command (85h). Random Data Input command may be repeated multiple times in a page. The Page Program Confirm command (10h) starts the programming process. Writing 10h alone without entering data will not initiate the programming process. The internal write engine automatically executes the corresponding algorithm and controls timing for programming and verification, thereby freeing the host controller for other tasks. Once the program process starts, the host controller can detect the completion of a program cycle by monitoring the R/B# output or reading the Status bit (I/O6) using the Read Status command. Only Read Status and Reset commands are valid during programming. When the Page Program operation is completed, the host controller can check the Status bit (I/O0) to see if the Page Program operation is successfully done. The command register remains the Read Status mode unless another valid command is written to it.

A page program sequence is illustrated in figure below, where column address, page address, and data input are placed in between 80h and 10h. After t_{PROG} program time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after 10h.

Program & Read Status Operation



Random Data Input In a Page



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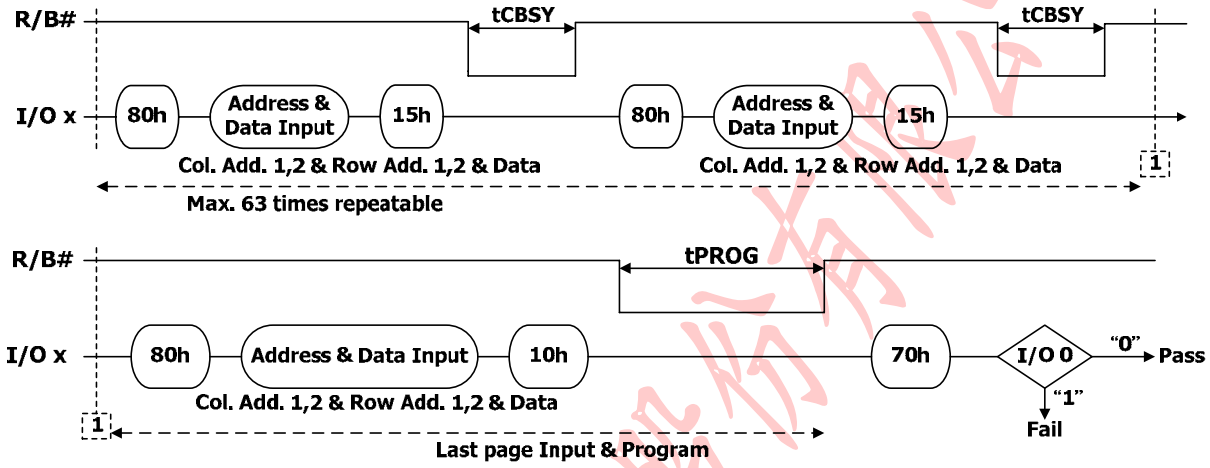
5.3 Cache Program

Cache Program is an extension of Page Program, which is executed with 2,112 bytes data registers, and is available only within a block. Since the device has 1 page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to 2,112 bytes into the selected cache registers, Cache Program command (15h) instead of actual Page Program (10h) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (t_{CBSY}) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70h) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is inputted with the Cache Program command, t_{CBSY} is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identity the completion of internal programming. If the system monitors the progress of programming only with R/B#, the last page of the target programming sequence must be programmed with actual Page Program command (10h).

Cache Program (available only within a block)



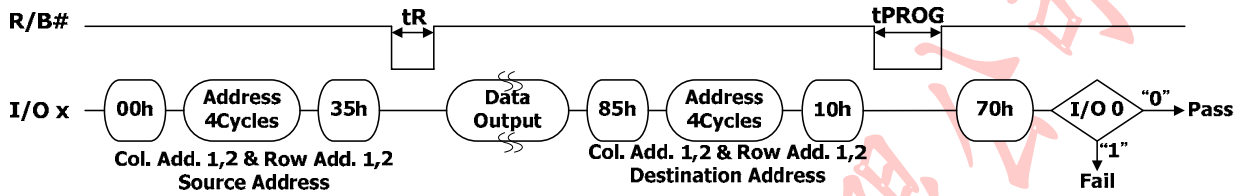
Note: Since programming the last page does not employ caching, the program time has to be that of Page Program. However, if the previous program cycle with the cache data has not finished, the actual program cycle of the last page is initiated only after completion of the previous cycle, which can be expressed as the following formula.

t_{PROG} = Program time for the last page + Program time for the (last-1)th page – (Program command cycle time + Last page data loading time)

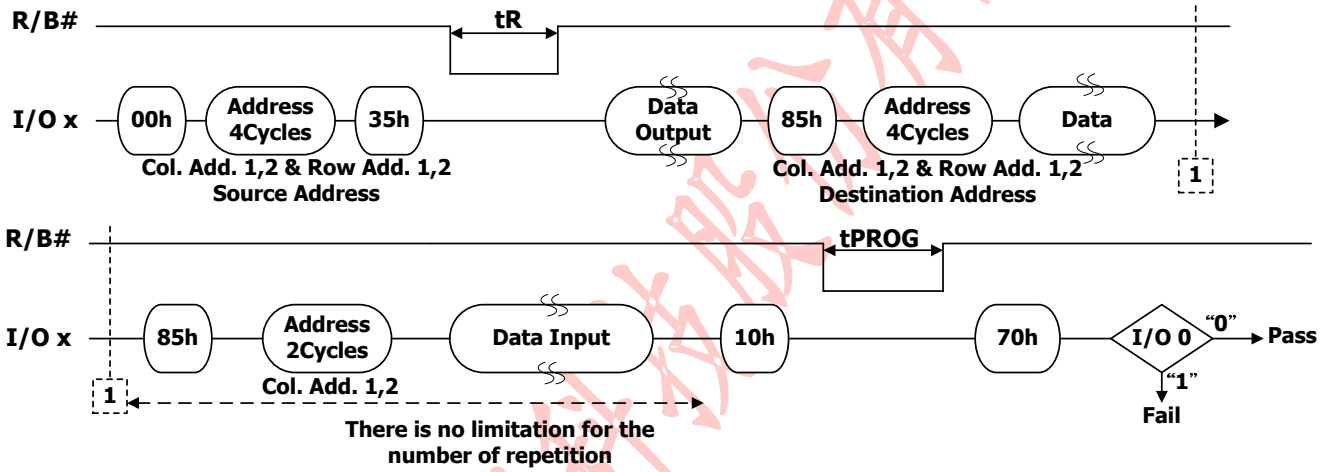
5.4 Copy-Back Program

Copy-Back Program is designed to efficiently copy data stored in memory cells without time-consuming data reloading when there is no bit error detected in the stored data. The benefit is particularly obvious when a portion of a block is updated and the rest of the block needs to be copied to a newly assigned empty block. Copy-Back operation is a sequential execution of Read for Copy-Back and of Copy-Back Program with Destination address. A Read for Copy-Back operation with "35h" command and the Source address moves the whole 2,112byte data into the internal buffer. The host controller can detect bit errors by sequentially reading the data output. Copy-Back Program is initiated by issuing Page-Copy Data-Input command (85h) with Destination address. If data modification is necessary to correct bit errors and to avoid error propagation, data can be reloaded after the Destination address. Data modification can be repeated multiple times as shown in figure below. Actual programming operation begins when Program Confirm command (10h) is issued. Once the program process starts, the Read Status command (70h) may be entered to read the status register. The host controller can detect the completion of a program cycle by monitoring the R/B# output, or the Status bit (I/O6) of the Status Register. When the Copy-Back Program is complete, the Status Bit (I/O0) may be checked. The command register remains Read Status mode until another valid command is written to it.

Page Copy-Back Program Operation



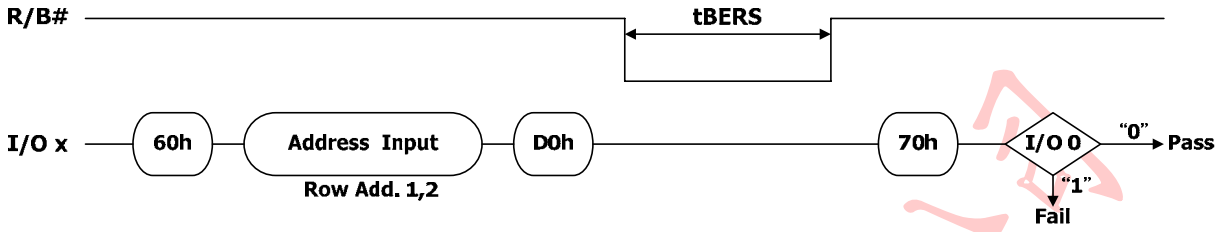
Page Copy-Back Program Operation with Random Data Input



5.5 Block Erase

The block-based Erase operation is initiated by an Erase Setup command (60h), followed by a two-cycle row address, in which only Plane address and Block address are valid while Page address is ignored. The Erase Confirm command (D0h) following the row address starts the internal erasing process. The two-step command sequence is designed to prevent memory content from being inadvertently changed by external noise.

At the rising edge of WE# after the Erase Confirm command input, the internal control logic handles erase and erase-verify. When the erase operation is completed, the host controller can check Status bit (I/O0) to see if the erase operation is successfully done. Figure below illustrates a block erase sequence, and the address input (the first page address of the selected block) is placed in between commands 60h and D0h. After t_{BERS} erase time, the R/B# de-asserts to ready state. Read Status command (70h) can be issued right after D0h to check the execution status of erase operation.



5.6 Read Status

A status register on the device is used to check whether program or erase operation is completed and whether the operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the status register to I/O pins on the falling edge of CE# or RE#, whichever occurs last. This command allow the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to toggle for status change.

The command register remains in Read Status mode unless other commands are issued to it. Therefore, if the status register is read during a random read cycle, a read command (00h) is needed to start read cycles.

I/O	Page Program	Block Erase	Read	Cache Read	Definition
I/O 0	Pass/Fail	Pass/Fail	NA	NA	Pass : 0 Fail : 1
I/O 1	NA	NA	NA	NA	Don't cared
I/O 2	NA	NA	NA	NA	Don't cared
I/O 3	NA	NA	NA	NA	Don't cared
I/O 4	NA	NA	NA	NA	Don't cared
I/O 5	NA	NA	NA	True Read/Busy	Busy : 0 Ready : 1
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Read/Busy	Busy : 0 Ready : 1
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Protected : 0 Not Protected : 1

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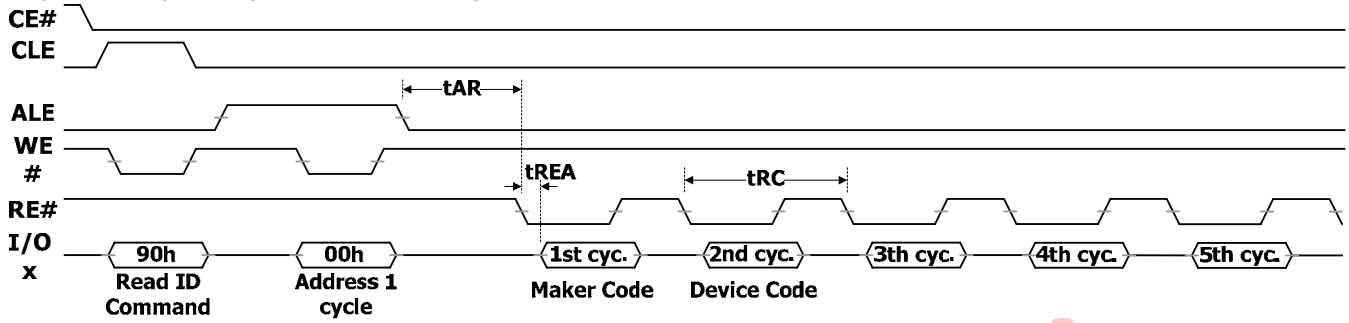
5.7 Read ID

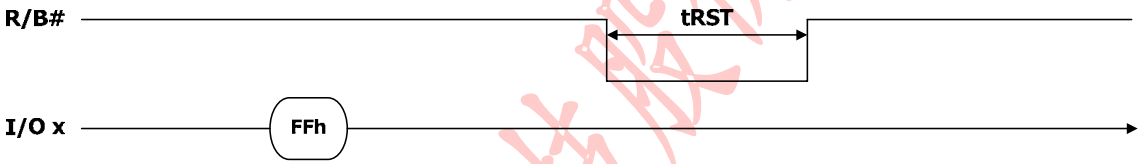
The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Four read cycles sequentially output the manufacturer code (C8h), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it.



1st Cycle (Maker Code)	2nd Cycle (Device Code)	3rd Cycle	4th Cycle	5th Cycle
C8h	A1h	80h	15h	40h

5.8 Reset

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when WP# is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin changes to low for t_{RST} after the Reset command is written. Refer to figure below.

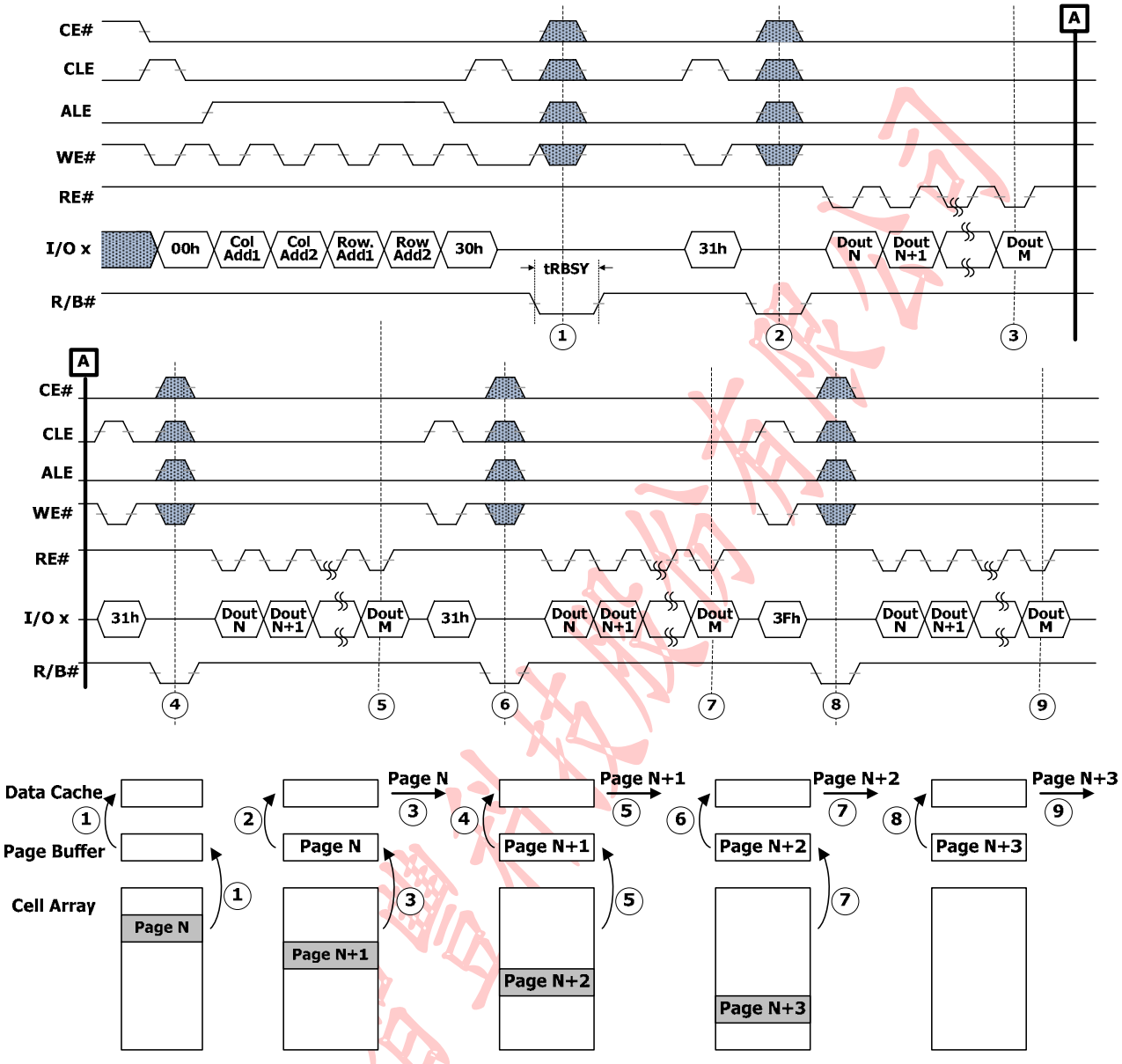


	After Power-up	After Reset
Operation Mode	00h Command is latched	Waiting for next command

5.9 Cache Read

Cache Read is an extension of Page Read, and is available only within a block. The normal Page Read command (00h-30h) is always issued before invoking Cache Read. After issuing the Cache Read command (31h), read data of the designated page (page N) are transferred from data registers to cache registers in a short time period of t_{DCBSYR}, and then data of the next page (page N+1) is transferred to data registers while the data in the cache registers are being read out. Host controller can retrieve continuous data and achieve fast read performance by iterating Cache Read operation. The Read Start for Last Page Cache Read command (3Fh) is used to complete data transfer from memory cells to data registers.

Read Operation with Cache Read



5.10 Read/Busy#

The device has a R/B# output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B# pin is normally high but transition to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B#) and current drain during busy (ibusy) , an appropriate value can be obtained with the following reference chart. Its value can be determined by the following guidance.

Read/Busy# Pin Electrical Specification

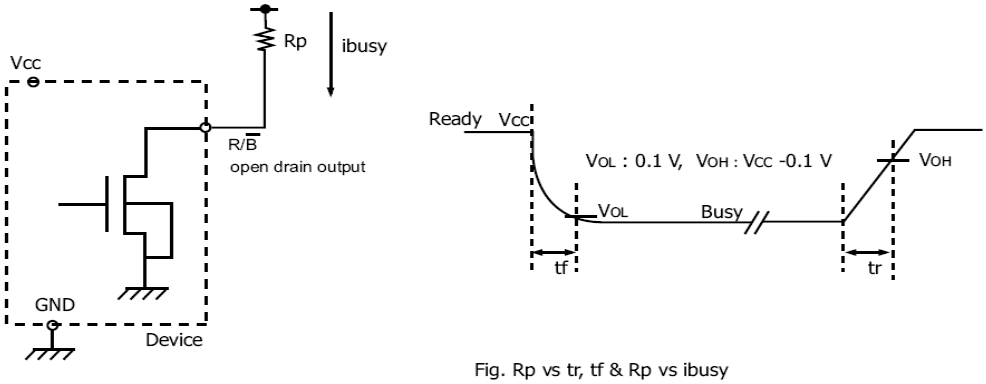
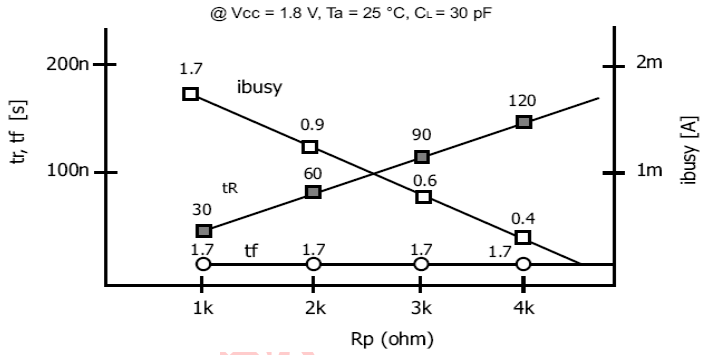


Fig. Rp vs tr, tf & Rp vs ibusy



Rp value guidence

$$Rp\ (min) = \frac{Vcc\ (Max.) - V_{OL}\ (Max.)}{I_{OL} + \sum I_L} = \frac{1.85\ V}{3\ mA + \sum I_L}$$

where IL is the sum of the iput currents of all devices tied to the R/B# pin.
Rp(max) is determined by maximum permissible limit of tr

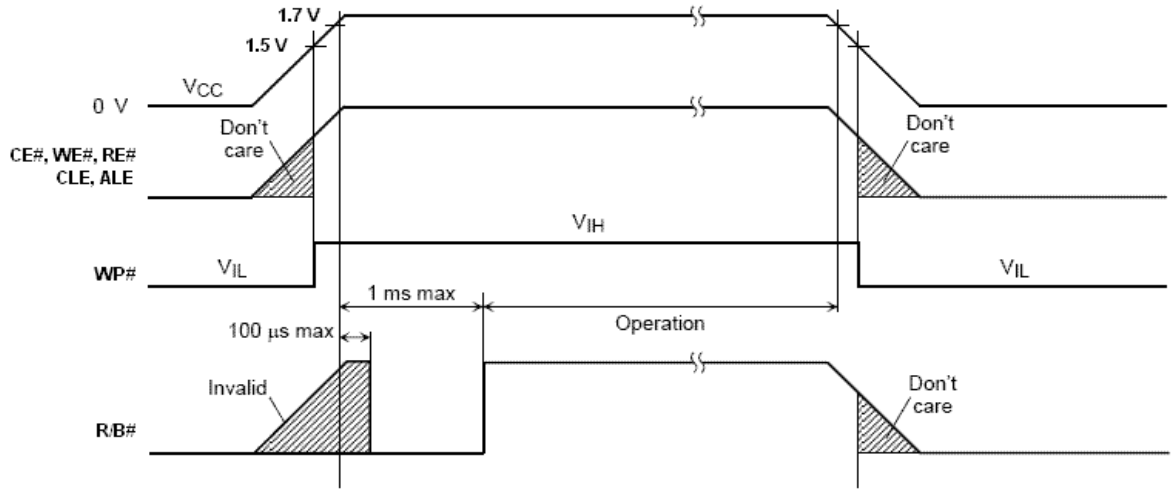
5.11 Data Protection & Power Up Sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence. During the initialization the device R/B# signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are 70h.

The WP# signal is useful for protecting against data corruption at power on/off.

AC Waveform for Power Transition



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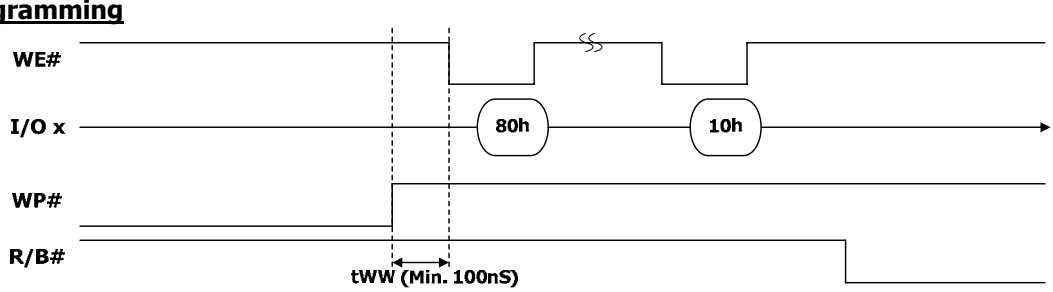
5.12 Write Protect Operation

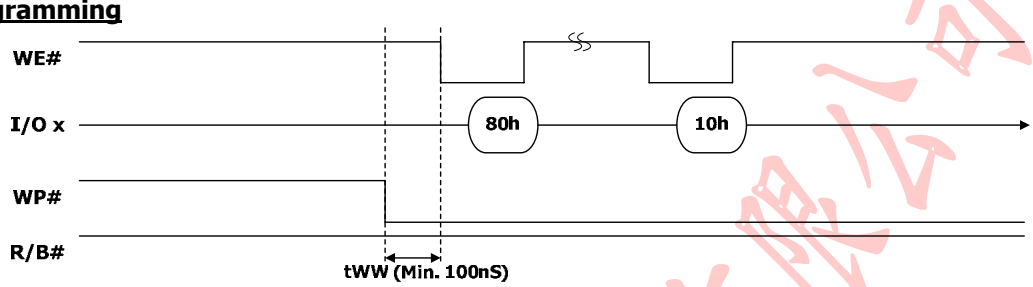
Enabling WP# during erase and program busy is prohibited. The erase and program operations are enabled and disabled as follows:

Enable Programming

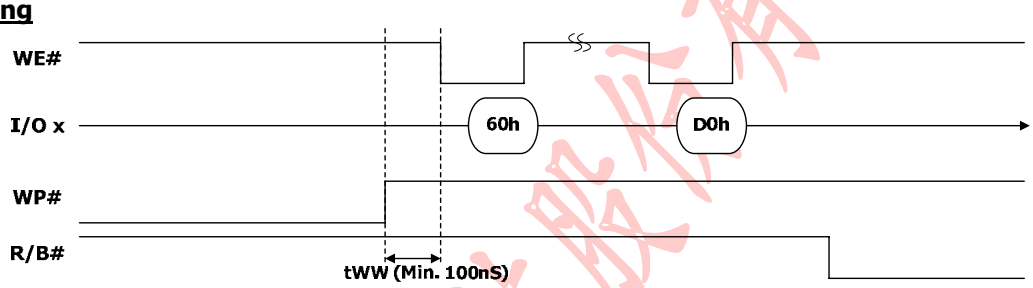


Note: WP# keeps "High" until programming finish

Disable Programming

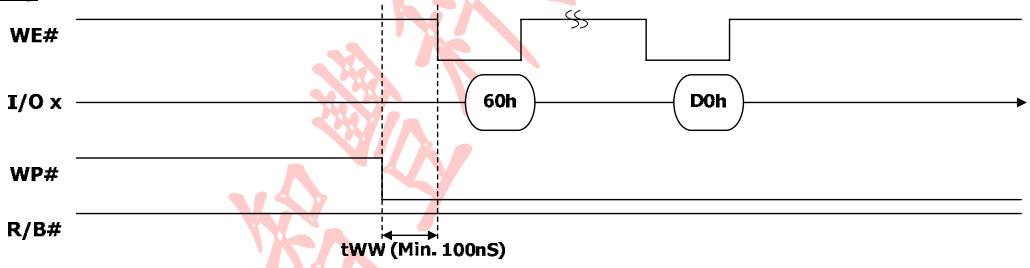


Enable Erasing



Note: WP# keeps "High" until erasing finish

Disable Erasing



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5.13 One-Time Programmable (OTP) Operations

This flash device offers one-time programmable memory area. Thirty full pages of OTP data are available on the device, and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands.

The OTP area leaves the factory in an unwritten state. The OTP area cannot be erased, whether it is protected or not. Protecting the OTP area prevents further programming of that area.

The OTP area is only accessible while in OTP operation mode. To set the device to OTP operation mode, issue the Set Feature (EFh-90h-01h) command. When the device is in OTP operation mode, subsequent Read and/or Page Program are applied to the OTP area. When you want to come back to normal operation, you need to use EFh-90h-00h for OTP mode release. Otherwise, device will stay in OTP mode.

To program an OTP page, issue the Serial Data Input (80h) command followed by 4 address cycles. The first two address cycles are column address. For the third cycle, select a page in the range of 01h through 1Eh. The fourth cycle is fixed at 00h. Next, up to 2112 bytes of data can be loaded into data register. The bytes other than those to be programmed do not need to be loaded. This device supports Random Data Input (85h) command, which can be operated multiple times in a page. The column address for the next data to be entered may be changed to the address follows the Random Data Input command. The Page Program confirm (10h) command initiates the programming process. The internal control logic automatically executes the programming algorithm, timing and verification. Please note that no partial-page program is allowed in the OTP area. In addition, the OTP pages must be programmed in the ascending order. A programmed OTP page will be automatically protected.

Similarly, to read data from an OTP page, set the device to OTP operation mode and then issue the Read (00h-30h) command. The device may output random data (not in sequential order) in a page by writing Random Data Output (05h-E0h) command, which can be operated multiple times in a page. The column address for the next data to be output may be changed to the address follows the Random Data Output command.

All pages in the OTP area will be protected simultaneously by issuing the Set Feature (EFh-90h-03h) command to set the device to OTP protection mode. After the OTP area is protected, no page in the area is programmable and the whole area cannot be unprotected.

The Read Status (70h) command is the only valid command for reading status in OTP operation mode.

OPT Modes and Commands		Set feature	Command
OTP Operation mode	Read	EFh-90h-01h	00h-30h
	Page Program	EFh-90h-01h	80h-10h
OTP Protection mode	Program Protect	EFh-90h-03h	80h-10h
OTP Release mode	Leave OTP mode	EFh-90h-00h	

Description (OTP Area Details)	Value
Number of OTP pages	30
OTP page address	01h – 1Eh
Number of partial page programs for each page in the OTP area	1

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512Mb (32Mb x16) Mobile DDR

1 Product Description

The Mobile DRAM SDRAM (mDDR) is 512M-bit CMOS Low Power Double Data Rate Synchronous DRAM (LPDDR), ideally suited for mobile applications which use the battery such as PDAs, 2.5G and 3G cellular phones with internet access and multimedia capabilities, mini-notebook, hand-held PCs. It is organized as 4banks of 8Mb x16. The mDDR uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n prefetch architecture with an interface designed to transfer two data per clock cycle at the I/O pins. DW.

The mDDR(LPDDR) offers fully synchronous operations referenced to both rising and falling edges of the clock. While all address and control inputs are latched on the rising edges of the CK (mDDR operates from a differential clock: the crossing of CK going HIGH and CK going LOW is referred to as the positive edge of CK), data, data strobe and data mask inputs are sampled on both rising and falling edges of it (Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK). The data paths are internally pipelined and 2-bit prefetched to achieve high bandwidth. All input voltage levels are compatible with LVCMOS.

Read and write accesses to the mDDR(LPDDR) are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and the row to be accessed. The address bits registered coincident with the READ or WRITE command are used to select the bank and the starting column location for the burst access.

The mDDR(LPDDR) provides for programmable read or write bursts of 2, 4 or 8 locations. An AUTO PRECHARGE function may be enabled to provide a self-timed row pre-charge that is initiated at the end of the burst access.

As with standard SDRAM, the pipelined and multi-bank architecture of mDDR(LPDDR) allows for concurrent operation, thereby providing high effective bandwidth by hiding row pre-charge and activation times.

The mDDR(LPDDR) also provides for special programmable Self Refresh options which are Partial Array Self Refresh (full, half, quarter and 1/8 and 1/16 array) and Temperature Compensated Self Refresh.

A burst of Read or Write cycles in progress can be interrupted and replaced by a new burst Read or Write command on any cycle (this pipelined design is not restricted by a 2N rule). Only Read bursts in progress with auto pre-charge disabled can be terminated by a burst terminate command. Burst Terminate command is undefined and should not be used for Read with Auto-pre-charge enabled and for Write bursts.

The mDDR(LPDDR) has the special Low Power function of Auto Temperature Compensated Self Refresh(ATCSR) to reduce self refresh current consumption. Since an internal temperature sensor is implemented, it enables to automatically adjust refresh rate according to temperature without external EMRS command.

All inputs are LVCMOS compatible. Devices will have a VDD and VDDQ supply of 1.8V (nominal).

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Pin Descriptions

CK, /CK (input pins)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the /CK falling edge. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DMs and DQs are referred to the cross point of the DQS and the VDDQ/2 level. DQSs for write operation are referred to the cross point of the CK and the /CK. The other input signals are referred at CK rising edge.

/CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See "Command operation".

A0 to A12 (input pins)

Row address (AX0 to AX12) is determined by the A0 to the A12 level at the cross point of the CK rising edge and the /CK falling edge in a bank active command cycle. Column address (AY0 to AY9) is loaded at the cross point of the CK rising edge and the /CK falling edge in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin)

A10 defines the pre-charge mode when a pre-charge command, a read command or a write command is issued. If A10 = high when a pre-charge command is issued, all banks are pre-charged. If A10 = low when a pre-charge command is issued, only the bank that is selected by BA1/BA0 is pre-charged. If A10 = high when read or write command, auto pre-charge function is enabled.

BA0 and BA1 (input pins)

BA0 and BA1 are bank select signals (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. (See Bank Select Signal Table)

[Bank Select Signal Table] (H:VIH ; L:VIL)

	BA0	BA1
Bank 0	L	L
Bank 1	H	L
Bank 2	L	H
Bank 3	H	H

CKE (input pin)

CKE controls power-down mode, self-refresh function and deep power-down function with other command inputs. The CKE level must be kept for 2 clocks at least, that is, if CKE changes at the cross point of the CK rising edge and the /CK falling edge with proper setup time tIS, by the next CK rising edge CKE level must be kept with proper hold time tIH.

DQ0 to DQ15 (input/output pins)

Data are input to and output from these pins.

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UDQS and LDQS (input and output pin)

DQS provides the read data strobes (as output) and the write data strobes (as input). Each DQS pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

UDM and LDM (input pin)

DM is the reference signals of the data input mask function. DM is sampled at the cross point of DQS and VDDQ/2. When DM = high, the data input at the same timing are masked while the internal burst counter will be counting up. Each DM pin corresponds to eight DQ pins, respectively (See DQS and DM Correspondence Table).

[DQS and DM Correspondence Table]

DQS	Data mask	DQs
LDQS	LDM	DQ0 to DQ7
UDQS	UDM	DQ8 to DQ15

VDD, VSS, VDDQ, VSSQ (Power supply)

VDD and VSS are power supply pins for internal circuits. VDDQ and VSSQ are power supply pins for the output buffers. VDD must be equal to VDDQ.

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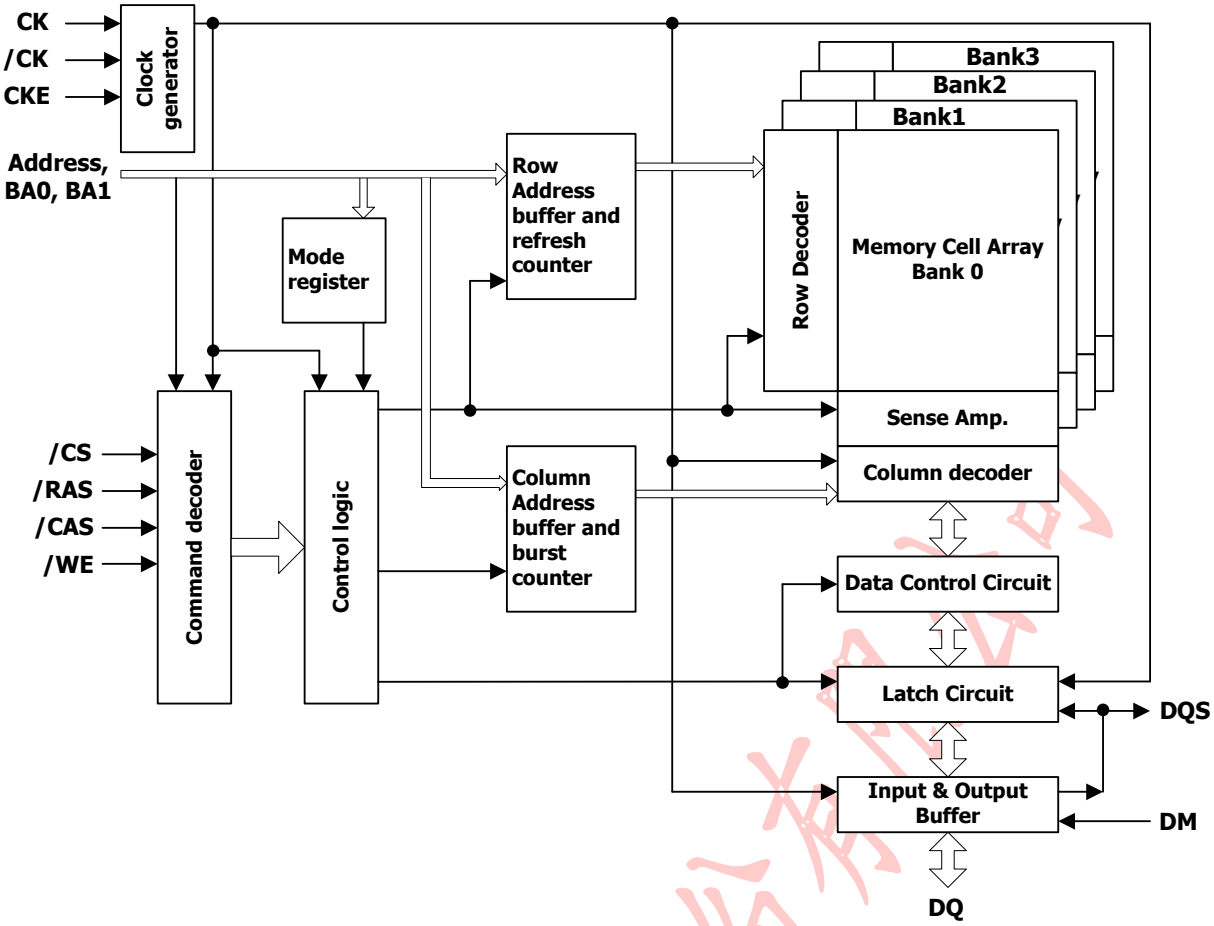
Block Diagram



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2 Electrical Specifications and Characteristics

- All voltages are referenced to VSS (GND).
- After power-up, wait more than 200 µs and then, execute power on sequence and CBR (Auto) refresh before proper device operation is achieved.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Note
Voltage on any pin relative to VSS	VT	–0.5 to +2.3	V	
Supply voltage relative to VSS	VDD	–0.5 to +2.3	V	
Short circuit output current	IOS	50	mA	
Power dissipation	PD	1	W	
Operating junction temperature	TJ	–30 to +85	°C	
Storage temperature	Tstg	–55 to +125	°C	

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (TJ=-30℃ to +85℃)

Parameter	Pins	Symbol	min.	typ.	max.	Unit	Note
Supply voltage		VDD,	1.7	1.8	1.95	V	1
		VDDQ					
		VSS,					
		VSSQ	0	0	0	V	
Input high voltage	All other input pins	VIH	0.8 × VDDQ	-	VDDQ + 0.3	V	
Input low voltage		VIL	-0.3	-	0.2 x VDDQ	V	
DC input voltage level	CK, /CK	VIN (DC)	-0.3	-	VDDQ + 0.3	V	
AC Input differential cross point voltage		VIX	0.4 × VDDQ	0.5 × VDDQ	0.6 × VDDQ	V	6
DC input differential voltage		VID (DC)	0.4 × VDDQ	-	VDDQ + 0.6	V	5
AC input differential voltage		VID (AC)	0.6 × VDDQ	-	VDDQ + 0.6	V	5
DC input high voltage	DQ, DM, DQS	VIHD (DC)	0.7× VDDQ	-	VDDQ + 0.3	V	
DC input low voltage		VILD (DC)	-0.3	-	0.3 × VDDQ	V	
AC input high voltage		VIHD (AC)	0.8× VDDQ	-	VDDQ + 0.3	V	
AC input low voltage		VILD (AC)	-0.3	-	0.2 × VDDQ	V	

Notes:

1. VDDQ must be equal to VDD.
2. VIH (max.) = 2.3V (pulse width ≦5ns).
3. VIL (min.) = –0.5V (pulse width ≦5ns).
4. All voltage referred to VSS and VSSQ must be same potential.
5. VID (DC) and VID (AC) are the magnitude of the difference between the input level on CK and the input level on /CK.
6. The value of VIX is expected to be 0.5 x VDDQ and must track variations in the DC level of the same.

DC Characteristics (TJ=-30℃ to +80℃, VDD and VDDQ=1.7V to 1.95V, VSS and VSSQ=0V)

Parameter	Symbol	max.	Unit	Test Condition	Note
Operating current (ACT-PRE)	IDD0	85	mA	One bank active-precharge, CKE = H, /CS = H between valid commands, tCK = tCK (min.), tRC = tRC (min.), Address bus inputs are SWITCHING; Data bus inputs are STABLE	
Standby current in power-down	IDD2P	0.8	mA	All banks idle, CKE = L, /CS = H, tCK = tCK (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Standby current in power-down with clock stop	IDD2PS	0.6	mA	All banks idle, CKE = L, /CS = H, CK = L, /CK = H, Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Standby current in non power-down	IDD2N	7.0	mA	All banks idle, CKE = H, /CS = H, tCK = tCK (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Standby current in non power-down with clock stop	IDD2NS	2.0	mA	All banks idle, CKE = H, /CS = H, CK = L, /CK = H, Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Active standby current in power-down	IDD3P	3.0	mA	One bank active, CKE = L, /CS = H, tCK = tCK (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Active standby current in power-down with clock stop	IDD3PS	2.0	mA	One bank active, CKE = L, /CS = H, CK = L, /CK = H; Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Active standby current in non power-down	IDD3N	10	mA	One bank active, CKE = H, /CS = H, tCK = tCK (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Active standby current in non power-down with clock stop	IDD3NS	7.0	mA	One bank active, CKE = H, /CS = H, CK = L, /CK = H, Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Burst operating current	IDD4	135	mA	One bank active, Continuous burst reads or writes; tCK = tCK (min.), CL = 3, BL = 4, IOUT = 0mA, Address inputs are SWITCHING, 50% data change each burst transfer	
Auto-refresh current	IDD5	80	mA	CKE = H, tCK = tCK (min.), tRFC = tRFC (min.), Address and control inputs are SWITCHING; Data bus inputs are STABLE	
Deep power-down current	IDD8	10	µA	Address and control inputs are STABLE; Data bus inputs are STABLE	

Advanced Data Retention Current

(TJ=-30℃ to +80℃, VDD and VDDQ=1.7V to 1.95V, VSS and VSSQ=0V)

Parameter	Symbol	typ.	max.	Unit	Condition	Note
Advanced data retention current (Self-refresh current) PASR="000" (Full)	IDD6	-	250	μA	-30°C ≤ TJ ≤ +40°C CKE = L	
PASR="001" (2BK)		-	220	μA		
PASR="010" (1BK)		-	200	μA		
PASR="000" (Full)	IDD6	-	480	μA	+40°C ≤ TJ ≤ +70°C CKE = L	
PASR="001" (2BK)		-	350	μA		
PASR="010" (1BK)		-	280	μA		
PASR="000" (Full)	IDD6	-	600	μA	+70°C ≤ TJ ≤ +85°C CKE = L	
PASR="001" (2BK)		-	400	μA		
PASR="010" (1BK)		-	300	μA		

Notes: 1. IDD specifications are tested after the device is properly initialized.
2. Input slew rate is specified by Test Conditions.
3. Definitions for IDD:
L is defined as VIN ≤ 0.1 × VDDQ;
H is defined as VIN ≥ 0.9 × VDDQ;
STABLE is defined as inputs stable at an H or L level;
SWITCHING is defined as:
Address and command: inputs changing between H and L once per two clock cycles;
Data bus inputs: DQ changing between H and L once per clock cycle; DM and DQS are STABLE.

DC Characteristics 2 (TJ=-30℃ to +80℃, VDD and VDDQ=1.7V to 1.95V, VSS and VSSQ=0V)

Parameter	Symbol	min.	max.	Unit	Condition	Note
Input leakage current	ILI	-2.0	2.0	μA	0 ≤ VIN ≤ VDDQ	
Output leakage current	ILO	-1.5	1.5	μA	0 ≤ VOUT ≤ VDDQ, DQ = disable	
Output high voltage	VOH	0.9 x VDDQ	-	V	IOH = − 0.1mA	
Output low voltage	VOL	-	0.1 x VDDQ	V	IOL = 0.1 mA	

Pin Capacitance (TA=+25℃, VDD and VDDQ=1.7V to 1.95V)

Parameter	Symbol	Pins	min.	typ.	max.	Unit	Note
Input capacitance	CI1	CK, /CK	1.5	-	3.5	pF	1
	CI2	All other input-only pins	1.5	-	3.0	pF	1
Delta input capacitance	Cdi1	CK, /CK	-	-	0.25	pF	1
	Cdi2	All other input-only pins	-	-	0.5	pF	1
Data input/output capacitance	CI/O	DQ, DM, DQS	2.0	-	4.5	pF	1,2
Delta input/output capacitance	Cdio	DQ, DM, DQS	-	-	0.5	pF	1

Notes: 1. These parameters are measured on conditions: f = 100MHz, VOUT = VDDQ/2, ΔVOUT = 0.2V, TA = +25°C.
2. DOUT circuits are disabled.

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AC Characteristics (TJ=-30℃ to +80℃, VDD and VDDQ=1.7V to 1.95V, VSS and VSSQ=0V)

		200MHz			
Parameter	Symbol	min.	max.	Unit	Note
Clock cycle time	tCK	5.0	-	ns	
CK high-level width	tCH	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	tCK	
CK half period	tHP	min. (tCH, tCL)	-	tCK	
DQ output access time from CK, /CK	tAC	2.0	5.0	ns	2,8
DQS-in cycle time	tDSC	0.9	1.1	tCK	
DQS output access time from CK, /CK	tDQSCK	2.0	5.0	ns	2,8
DQ-out high-impedance time from CK, /CK	tHZ	-	5.0	ns	5,8
DQ-out low-impedance time from CK, /CK	tLZ	1.0	-	ns	6,8
DQS to DQ skew	tDQSQ	-	0.4	ns	3
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	-	ns	4
Data hold skew factor	tQHS	-	0.5	ns	
DQ and DM input setup time	tDS	0.5	-	ns	3
DQ and DM input hold time	tDH	0.5	-	ns	3
DQ and DM input pulse width	tDIPW	1.6	-	ns	
Read preamble	tRPRE	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	tCK	
Write preamble setup time	tWPRES	0	-	ns	
Write preamble	tWPRE	0.25	-	tCK	
Write postamble	tWPST	0.4	0.6	tCK	7
Write command to first DQS latching transition	tDQSS	0.75	1.25	tCK	
DQS falling edge to CK setup time	tDSS	0.2	-	tCK	
DQS falling edge hold time from CK	tDSH	0.2	-	tCK	
DQS input high pulse width	tDQSH	0.4	-	tCK	
DQS input low pulse width	tDQSL	0.4	-	tCK	
Address and control input setup time	tIS	0.9	-	ns	3
Address and control input hold time	tIH	0.9	-	ns	3
Address and control input pulse width	tIPW	2.3	-	ns	3
Mode register set command cycle time	tMRD	2	-	tCK	
Active to Pre-charge command period	tRAS	40	120000	ns	
Active to Active/Auto-refresh command period	tRC	55	-	ns	
Auto-refresh to Active/Auto-refresh command period	tRFC	96	-	ns	
Active to Read/Write delay	tRCD	15	-	ns	
Pre-charge to active command period	tRP	15	-	ns	
Column address to column address delay	tCCD	1	-	tCK	

		200MHz			
Parameter	Symbol	min.	max.	Unit	Note
Active to active command period	tRRD	10	-	ns	
Write recovery time	tWR	15	-	ns	
Autoprecharge write recovery and precharge time	tDAL	-	-		9
Self-Refresh Exit Period	tSREX	120	-	ns	
Power-down entry	tPDEN	2	-	tCK	
Power-down exit to command input	tPDEX	1	-	tCK	
Internal Write to Read command delay	tWTR	2	-	tCK	
Refresh period	tREF	-	64	ms	
Average periodic refresh interval	tREFI	-	7.8	us	
CKE minimum pulse width	tCKE	2	-	tCK	
Write to pre-charge command delay (same bank)	tWPD	4 + BL/2	-	tCK	
Read to pre-charge command delay (same bank)	tRPD	BL/2	-	tCK	
Write to read command delay (to input all data)	tWRD	3 + BL/2	-	tCK	
Burst stop command to write command delay (CL = 3)	tBSTW	3	-	tCK	
Burst stop command to DQ high-Z (CL = 3)	tBSTZ	3	-	tCK	
Read command to write command delay (to output all data) (CL = 3)	tRWD	3 + BL/2	-	tCK	
Pre-charge command to high-Z (CL = 3)	tHZP	3	-	tCK	
Mode register set command cycle time	tMRD	2	-	tCK	

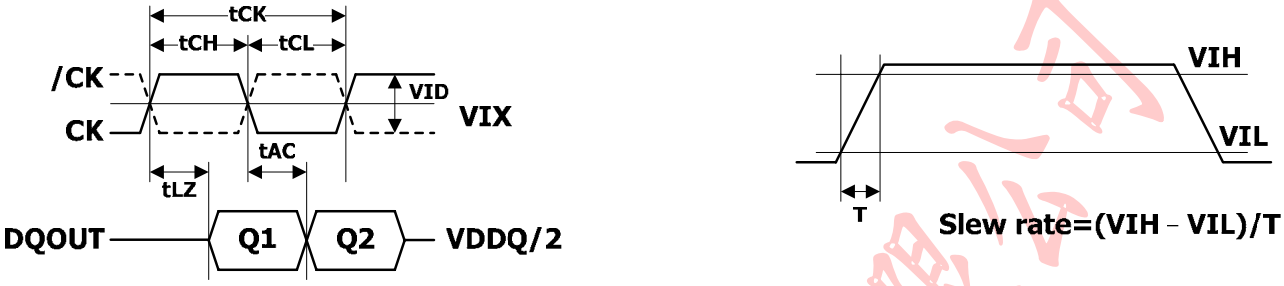
Notes:

1. On all AC measurements, we assume the test conditions shown in "Test conditions" and full driver strength is assumed for the output load, that is both A6 and A5 of EMRS is set to be "L".
2. This parameter defines the signal transition delay from the cross point of CK and /CK. The signal transition is defined to occur when the signal level crossing VDDQ/2.
3. The timing reference level is VDDQ/2.
4. Output valid window is defined to be the period between two successive transition of data out signals. The signal transition is defined to occur when the signal level crossing VDDQ/2.
5. tHZ is defined as DOUT transition delay from low-Z to high-Z at the end of read burst operation. The timing reference is cross point of CK and /CK. This parameter is not referred to a specific DOUT voltage level, but specify when the device output stops driving.
6. tLZ is defined as DOUT transition delay from high-Z to low-Z at the beginning of read operation. This parameter is not referred to a specific DOUT voltage level, but specify when the device output begins driving.
7. The transition from low-Z to high-Z is defined to occur when the device output stops driving. A specific reference voltage to judge this transition is not given.
8. tAC, tDQSCK, tHZ and tLZ are specified with 15pF bus loading condition.
9. Minimum 3 clocks of tDAL (= tWR + tRP) is required because it need minimum 2 clocks for tWR and minimum 1 clock for tRP. tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms above, if not already an integer, round to the next higher integer.

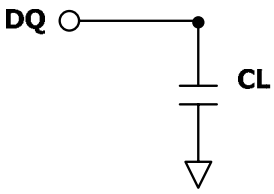
Test Conditions

Parameter	Symbol	Value	Unit	Note
Input high voltage	VIH (AC)	0.8 × VDDQ	V	1
Input low voltage	VIL (AC)	0.2 × VDDQ	V	1
Input differential voltage, CK and /CK inputs	VID (AC)	1.4	V	1
Input differential cross point voltage, CK and /CK inputs	VIX (AC)	VDDQ/2 with VDD=VDDQ	V	
Input signal slew rate	SLEW	1	V/ns	1
Output load	CL	15	pF	

Note: 1. VDD = VDDQ



Test condition (Wave form and Timing Reference)



Output Load

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3 Truth Table

Command Truth table

The DDR Mobile RAM recognizes the following commands specified by the /CS, /RAS, /CAS, /WE and address pins.

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA1	BA0	AP	Address
		n-1	n								
Ignore command	DESL	H	H	H	×	×	×	×	×	×	×
No operation	NOP	H	H	L	H	H	H	×	×	×	×
Burst stop command	BST	H	H	L	H	H	L	×	×	×	×
Column address and read command	READ	H	H	L	H	L	H	V	V	L	V
Read with auto precharge	READA	H	H	L	H	L	H	V	V	H	V
Column address and write command	WRIT	H	H	L	H	L	L	V	V	L	V
Write with auto precharge	WRITA	H	H	L	H	L	L	V	V	H	V
Row address strobe and bank active	ACT	H	H	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	H	L	L	H	L	V	V	L	×
Precharge all bank	PALL	H	H	L	L	H	L	×	×	H	×
Refresh	REF	H	H	L	L	L	H	×	×	×	×
	SELF	H	L	L	L	L	H	×	×	×	×
Mode register set	MRS	H	H	L	L	L	L	L	L	L	V
	EMRS	H	H	L	L	L	L	H	L	L	V

Remark: H: VIH. L: VIL. ×: Don't care V: Valid address input
Note: The CKE level must be kept for 1 CK cycle at least.

Ignore command [DESL]

When /CS is high at the cross point of the CK rising edge and the /CK falling edge, all input signals are neglected and internal state is held.

No operation [NOP]

As long as this command is input at the cross point of the CK rising edge and the /CK falling edge, address and data input are neglected and internal state is held.

Burst stop command [BST]

This command stops a current burst operation.

Column address strobe and read command [READ]

This command starts a read operation. The start address of the burst read is determined by the column address (AY0 to AY9) and the bank select address. After the completion of the read operation, all output buffers become high-Z.

Read with auto precharge [READA]

This command starts a read operation. After completion of the read operation, precharge is automatically executed.

Column address strobe and write command [WRIT]

This command starts a write operation. The start address of the burst write is determined by the column address (AY0 to AY9) and the bank select address.

Write with auto precharge [WRITA]

This command starts a write operation. After completion of the write operation, precharge is automatically executed.

Row address strobe and bank activate [ACT]

This command activates the bank that is selected by BA0 and BA1 (See Bank Select Signal Table) and determines the row address (AX0 to AX12).

Precharge selected bank [PRE]

This command starts precharge operation for the bank selected by BA0 and BA1. (See Bank Select Signal Table)

Precharge all banks [PALL]

This command starts a precharge operation for all banks.

Refresh [REF/SELF]

This command starts a refresh operation. There are two types of refresh operation, one is auto-refresh, and another is self-refresh. For details, refer to the CKE truth table section.

Mode register set/Extended mode register set [MRS/EMRS]

The DDR Mobile RAM has the two mode registers, the mode register and the extended mode register, to defines how it works. The both mode registers are set through the address pins in the mode register set cycle. For details, refer to "Mode register and extended mode register set".

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Function Truth Table

The following tables show the operations that are performed when each command is issued in each state of the DDR Mobile RAM.

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation
Precharging*1	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL*11
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11
	L	L	H	H	BA, RA	ACT	ILLEGAL*11
	L	L	H	L	BA,A10	PRE, PALL	NOP
	L	L	L	×	×		ILLEGAL
Idle*2	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11
	L	L	H	H	BA, RA	ACT	Activating
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	Refresh/Self-refresh*12
	L	L	L	L	MODE	MRS	Mode register set*12
Refresh (auto-refresh)*3	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	H	H	H	L	×	BST	ILLEGAL
	L	H	L	×	×		ILLEGAL
	L	L	×	×	×		ILLEGAL
Activating*4	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL*11
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL*11
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*11
	L	L	H	H	BA, RA	ACT	ILLEGAL*11
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*11
	L	L	L	×	×		ILLEGAL
Active*5	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting write operation
	L	L	H	H	BA, RA	ACT	ILLEGAL*11
	L	L	H	L	BA, A10	PRE, PALL	Pre-charge
	L	L	L	×	×		ILLEGAL

Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation
Read*6	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	Burst stop
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst read operation to start new read
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL*13
	L	L	H	H	BA, RA	ACT	ILLEGAL*11
	L	L	H	L	BA, A10	PRE, PALL	Interrupting burst read operation to start precharge
	L	L	L	×	×		ILLEGAL
Read with auto-precharge*7	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL*11
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*11
	L	L	L	×	×		ILLEGAL
Write*8	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	Burst Stop
	L	H	L	H	BA, CA, A10	READ/READA	Interrupting burst write operation to start read operation.
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Interrupting burst write operation to start new write operation.
	L	L	H	H	BA, RA	ACT	ILLEGAL*11
	L	L	H	L	BA, A10	PRE, PALL	Interrupting write operation to start pre-charge.
	L	L	L	×	×		ILLEGAL

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Current state	/CS	/RAS	/CAS	/WE	Address	Command	Operation
Write recovering*9	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	Starting read operation.
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Starting new write operation.
	L	L	H	H	BA, RA	ACT	ILLEGAL*11
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL*11
	L	L	L	×	×		ILLEGAL
Write with auto-pre-charge*10	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL*11
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*11
	L	L	L	×	×		ILLEGAL

Remark: H: VIH. L: VIL. ×: Don't care

Notes:
1. The DDR Mobile RAM is in "Pre-charging" state for tRP after pre-charge command is issued.
2. The DDR Mobile RAM reaches "IDLE" state tRP after pre-charge command is issued.
3. The DDR Mobile RAM is in "Refresh" state for tRFC after auto-refresh command is issued.
4. The DDR Mobile RAM is in "Activating" state for tRCD after ACT command is issued.
5. The DDR Mobile RAM is in "Active" state after "Activating" is completed.
6. The DDR Mobile RAM is in "READ" state until burst data have been output and DQ output circuits are turned off.
7. The DDR Mobile RAM is in "READ with auto pre-charge" from READA command until burst data has been output and DQ output circuits are turned off.
8. The DDR Mobile RAM is in "WRITE" state from WRIT command to the last burst data are input.
9. The DDR Mobile RAM is in "Write recovering" for tWR after the last data are input.
10. The DDR Mobile RAM is in "Write with auto pre-charge" until tWR after the last data has been input.
11. This command may be issued for other banks, depending on the state of the banks.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. Before executing a write command to stop the preceding burst read operation, BST command must be issued.

CKE Truth Table

Current state	Command	CKE		/CS	/RAS	/CAS	/WE	Address	Notes
		n – 1	n						
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	×	2
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	×	2
Active/Idle	Power-down entry (PDEN)	H	L	L	H	H	H	×	
		H	L	H	×	×	×	×	
Idle	Deep power-down entry (DPDEN)	H	L	L	H	H	L	×	2
Self-refresh	Self-refresh exit (SELFX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	
Power-down	Power-down exit (PDEX)	L	H	L	H	H	H	×	
		L	H	H	×	×	×	×	
Deep power-down	Power-down exit (DPDEX)	L	H	×	×	×	×	×	

Notes: 1. H: VIH . L: VIL × : Don't care.
2. All the banks must be in IDLE and no bursts in progress before executing this command.
3. The CKE level must be kept for 1 clock cycle at least.

Auto-refresh command [REF]

This command executes auto-refresh. The bank and the ROW addresses to be refreshed are internally determined by the internal refresh controller. The output buffer becomes high-Z after auto-refresh start. Pre-charge has been completed automatically after the auto-refresh. The ACT or MRS command can be issued tRFC after the last auto-refresh command.

The average refresh interval is 7.8μs. To allow for improved efficiency in scheduling, some flexibility in the absolute refresh interval is provided. A maximum of eight auto-refresh commands can be posted to the DDR Mobile RAM or the maximum absolute interval between any auto-refresh command and the next auto-refresh command is 8 × tREFI.

Self-refresh entry [SELF]

This command starts self-refresh. The self-refresh operation continues as long as CKE is held low. During the self-refresh operation, all ROW addresses are repeated refreshing by the internal refresh controller. A self-refresh is terminated by a self-refresh exit command.

Power-down mode entry [PDEN]

tPDEN (= 2 clocks) after the cycle when [PDEN] is issued, the DDR Mobile RAM enters into power-down mode. In power-down mode, power consumption is suppressed by deactivating the input initial circuit. Power-down mode continues while CKE is held low. No internal refresh operation occurs during the power-down mode.

Deep power-down entry [DPDEN]

After the command execution, deep power-down mode continues while CKE remains low. Before executing deep power-down, all banks must be pre-charged or in idle state.

Self-refresh exit [SELFX]

This command is executed to exit from self-refresh mode. tSREX after [SELFX], the device will be into idle state.

Power-down exit [PDEX]

The DDR Mobile RAM can exit from power-down mode tPDEX (1 cycle min.) after the cycle when [PDEX] is issued.

Deep power-down exit [DPDEX]

As CKE goes high in the deep power-down mode, the DDR Mobile RAM exit from the deep power-down mode through deep power-down exiting sequence.

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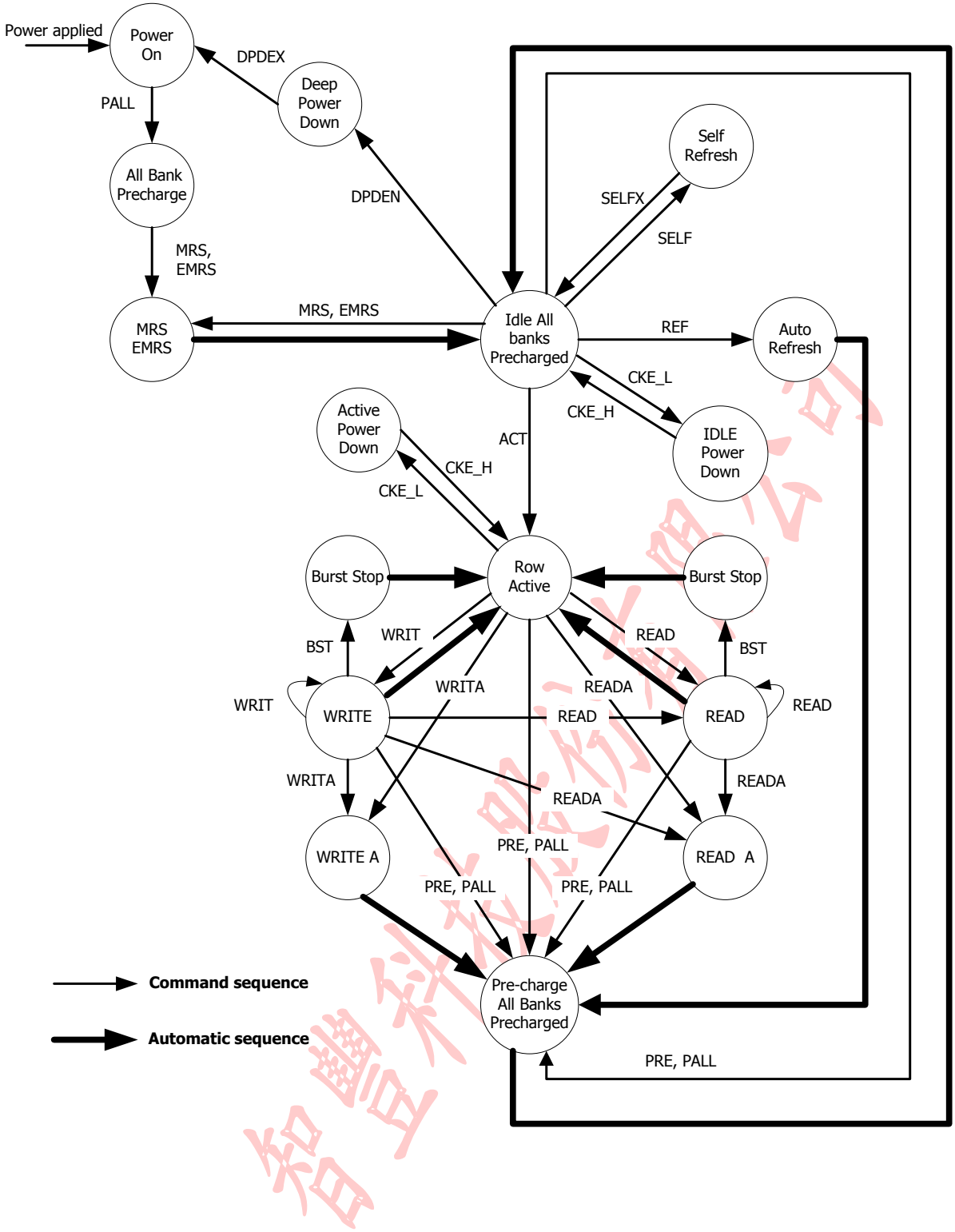
4 Simplified State Diagram



5 Function Description

Initialization

The DDR Mobile RAM is initialized in the power-on sequence according to the following.

1. Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also assert and hold Clock Enable (CKE) to a LV-CMOS logic high level.
2. Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.
3. There must be at least 200μs of valid clocks before any command may be given to the DRAM. During this time NOP or deselect (DESL) commands must be issued on the command bus.
4. Issue a pre-charge all command.
5. Provide NOPs or DESL commands for at least tRP time.
6. Issue an auto-refresh command followed by NOPs or DESL command for at least tRFC time. Issue the second auto-refresh command followed by NOPs or DESL command for at least tRFC time. Note as part of the initialization sequence there must be two auto-refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.
7. Using the MRS command, load the base mode register. Set the desired operating modes.
8. Provide NOPs or DESL commands for at least tMRD time.
9. Using the MRS command, program the extended mode register for the desired operating modes.
10. Provide NOP or DESL commands for at least tMRD time.
11. The DRAM has been properly initialized and is ready for any valid command.

Mode Register and Extended Register Set

There are two mode registers, the mode register and the extended mode register so as to define the operating mode. Parameters are set to both through the A0 to the A12 and BA0 and BA1 pins by the mode register set command [MRS] or the extended mode register set command [EMRS]. The mode register and the extended mode register are set by inputting signal via the A0 to the A12 and BA0 and BA1 pins during mode register set cycles.

BA0 and BA1 determine which one of the mode register or the extended mode register are set. Prior to a read or a write operation, the mode register must be set.

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5.2.1 Mode Register Definition

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	0	LTMODE			WT	BL		

Mode Register Set

Latency Mode	Bit6~4	/CAS latency
	000	R
	001	R
	010	R
	011	3
	100	R
	101	R
	110	R
	111	R

Burst Length	Bit2~0	WT=0	WT=1
	000	R	R
	001	2	2
	010	4	4
	011	8	8
	100	16	16
	101	R	R
	110	R	R
	111	R	R

Wrap type		
	0	Sequential
	1	Interleave

Remark: R:Reserved

Following mode register programming, no command can be issued before at least 2 clocks have elapsed.

/CAS Latency

/CAS latency must be set to 3.

Burst Latency

Burst Length is the number of words that will be output or input in a read or write cycle. After a read burst is completed, the output bus will become high-Z. The burst length is programmable as 2, 4, 8 and 16.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. This order is programmable as either "Sequential" or "Interleave". "Burst Operation" shows the addressing sequence for each burst length for each wrap type.

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5.2.2 Extended Mode Register Definition

BA1	BA0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1	0	0	0	0	0	0	0	DS		0	0	PARS		

Extended Mode Register Set

	Bit6~5	Strength
Driver Strength	00	Normal
	01	1/2 Strength
	10	1/4 Strength
	11	1/8 Strength

	Bit2~0	Refersh Array
Partial Array Self Refresh	000	All banks
	001	BankA & BankB (BA1=0)
	010	BankA (BA0=BA1=0)
	011	R
	100	R
	101	R
	110	R
	111	R

Remark: R:Reserved

Following extended mode register programming, no command can be issued before at least 2 clocks have elapsed.

Driver Strength

By setting specific parameter on A6 and A5, driving capability of data output drivers is selected.

Partial Array Self-Refresh

Memory array size to be refreshed during self-refresh operation is programmable in order to reduce power. Data outside the defined area will not be retained during self-refresh.

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5.2.3 Burst Operation

The burst type (BT) and the first three bits of the column address determine the order of a data out.

Burst Length	Starting column Address				Addressing (decimal)	
	A3	A2	A1	A0	Sequence	Interleaved
2				0	0 , 1	0 , 1
				1	1 , 0	1 , 0
4			0	0	0 , 1 , 2 , 3	0 , 1 , 2 , 3
			0	1	1 , 2 , 3 , 0	1 , 0 , 3 , 2
			1	0	2 , 3 , 0 , 1	2 , 3 , 0 , 1
			1	1	3 , 0 , 1 , 2	3 , 2 , 1 , 0
8		0	0	0	0 , 1 , 2 , 3 , 4 , 5 , 6 , 7	0 , 1 , 2 , 3 , 4 , 5 , 6 , 7
		0	0	1	1 , 2 , 3 , 4 , 5 , 6 , 7 , 0	1 , 0 , 3 , 2 , 5 , 4 , 7 , 6
		0	1	0	2 , 3 , 4 , 5 , 6 , 7 , 0 , 1	2 , 3 , 0 , 1 , 6 , 7 , 4 , 5
		0	1	1	3 , 4 , 5 , 6 , 7 , 0 , 1 , 2	3 , 2 , 1 , 0 , 7 , 6 , 5 , 4
		1	0	0	4 , 5 , 6 , 7 , 0 , 1 , 2 , 3	4 , 5 , 6 , 7 , 0 , 1 , 2 , 3
		1	0	1	5 , 6 , 7 , 0 , 1 , 2 , 3 , 4	5 , 4 , 7 , 6 , 1 , 0 , 3 , 2
		1	1	0	6 , 7 , 0 , 1 , 2 , 3 , 4 , 5	6 , 7 , 4 , 5 , 2 , 3 , 0 , 1
		1	1	1	7 , 0 , 1 , 2 , 3 , 4 , 5 , 6	7 , 6 , 5 , 4 , 3 , 2 , 1 , 0
16	0	0	0	0	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F
	0	0	0	1	1,2,3,4,5,6,7,8,9,A,B,C,D,E,F,0	1,0,3,2,5,4,7,6,9,8,B,A,D,C,F,E
	0	0	1	0	2,3,4,5,6,7,8,9,A,B,C,D,E,F,0,1	2,3,0,1,6,7,4,5,A,B,8,9,E,F,C,D
	0	0	1	1	3,4,5,6,7,8,9,A,B,C,D,E,F,0,1,2	3,2,1,0,7,6,5,4,B,A,9,8,F,E,D,C
	0	1	0	0	4,5,6,7,8,9,A,B,C,D,E,F,0,1,2,3	4,5,6,7,0,1,2,3,C,D,E,F,8,9,A,B
	0	1	0	1	5,6,7,8,9,A,B,C,D,E,F,0,1,2,3,4	5,4,7,6,1,0,3,2,D,C,F,E,9,8,B,A
	0	1	1	0	6,7,8,9,A,B,C,D,E,F,0,1,2,3,4,5	6,7,4,5,2,3,0,1,E,F,C,D,A,B,8,9
	0	1	1	1	7,8,9,A,B,C,D,E,F,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0,F,E,D,C,B,A,9,8
	1	0	0	0	8,9,A,B,C,D,E,F,0,1,2,3,4,5,6,7	8,9,A,B,C,D,E,F,0,1,2,3,4,5,6,7
	1	0	0	1	9,A,B,C,D,E,F,0,1,2,3,4,5,6,7,8	9,8,B,A,D,C,F,E,1,0,3,2,5,4,7,6
	1	0	1	0	A,B,C,D,E,F,0,1,2,3,4,5,6,7,8,9	A,B,8,9,E,F,C,D,2,3,0,1,6,7,4,5
	1	0	1	1	B,C,D,E,F,0,1,2,3,4,5,6,7,8,9,A	B,A,9,8,F,E,D,C,3,2,1,0,7,6,5,4
	1	1	0	0	C,D,E,F,0,1,2,3,4,5,6,7,8,9,A,B	C,D,E,F,8,9,A,B,4,5,6,7,0,1,2,3
	1	1	0	1	D,E,F,0,1,2,3,4,5,6,7,8,9,A,B,C	D,C,F,E,9,8,B,A,5,4,7,6,1,0,3,2
	1	1	1	0	E,F,0,1,2,3,4,5,6,7,8,9,A,B,C,D	E,F,C,D,A,B,8,9,6,7,4,5,2,3,0,1
	1	1	1	1	F,0,1,2,3,4,5,6,7,8,9,A,B,C,D,E	F,E,D,C,B,A,9,8,7,6,5,4,3,2,1,0

5.3 Auto Temperature Compensated Self-Refresh (ATCSR)

The DDR Mobile RAM automatically changes the self-refresh cycle by on die temperature sensor. No extended mode register program is required. Manual TCSR (Temperature Compensated Self-Refresh) is not implemented.

5.4 Deep Power-Down Exit Sequence

In order to exit from the deep power-down mode and enter into the idle mode, the following sequence is needed, which is similar to the power-on sequence.

(1) A 200μs or longer pause must precede any command other than ignore command (DESL).
(2) After the pause, all banks must be pre-charged using the pre-charge command (the pre-charge all banks command is convenient).
(3) Once the pre-charge is completed and the minimum tRP is satisfied, two or more Auto-refresh must be performed.
(4) Both the mode register and the extended mode register must be programmed. After the mode register set cycle or the extended mode register set cycle, tMRD (2 clocks minimum) pause must be satisfied.

Remarks: 1 The sequence of Auto-refresh, mode register programming and extended mode register programming above may be transposed.
2 CKE must be held high.

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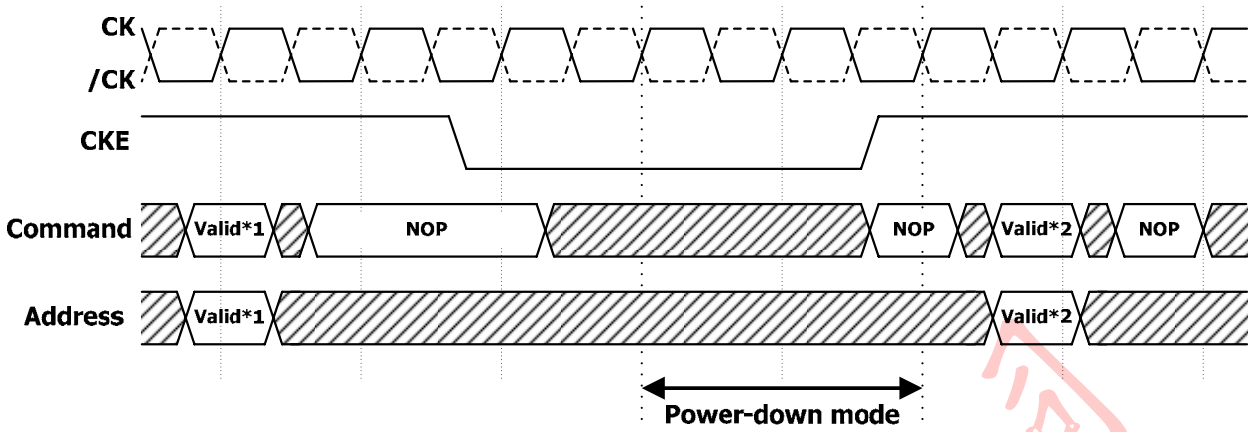
5.5 Power-Down Mode and CKE Control

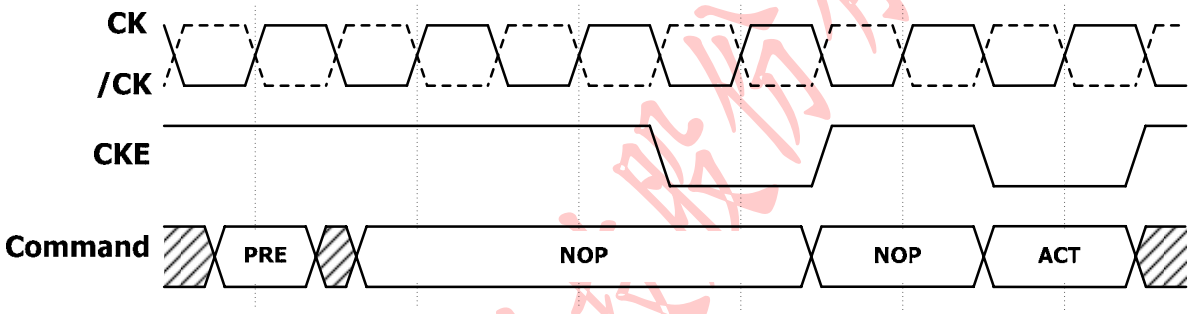
DDR Mobile RAM will be into power-down mode at the second CK rising edge after CKE to be low level with NOP or DESL command at first CK rising edge after CKE signal to be low.



Notes: 1. Valid*1 can be either Activate command or Pre-charge command, When Valid*1 is Activate command, power-down mode will be active power-down mode, while it will be pre-charge power down mode, if Valid*1 will be Pre-charge command.
2. Valid*2 can be any command as long as all of specified AC parameters are satisfied.

Power-Down Entry and Exit

However, if the CKE has one clock cycle high and on clock cycle low just as below, even DDR Mobile RAM will not enter power-down mode, this command flow does not hurt any data and can be done.



Note: Assume PRE and ACT command is closing and activating same bank.

CKE Control

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5.6 Read/Write Operation

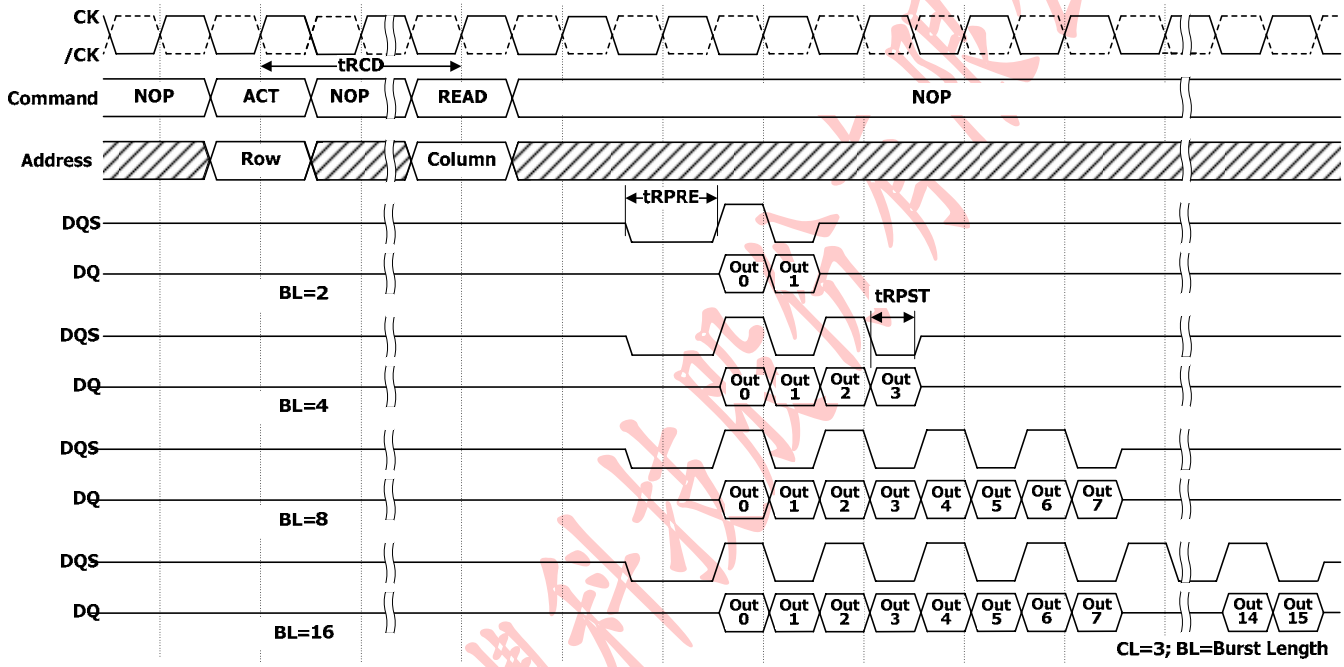
5.6.1 Bank Active

A read or a write operation begins with the bank active command [ACT]. The bank active command determines a bank address and a row address. For the bank and the row, a read or a write command can be issued tRCD after the ACT is issued.

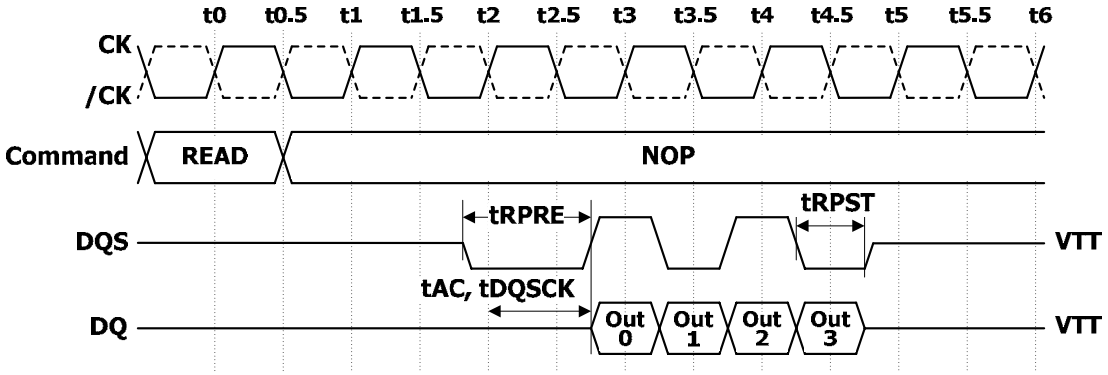
5.6.2 Read Operation

The burst length (BL), the /CAS latency (CL) and the burst type (BT) of the mode register are referred when a read command is issued. The burst length (BL) determines the length of a sequential output data by the read command that can be set to 2, 4, 8 or 16. The starting address of the burst read is defined by the column address, the bank select address (See "Pin Function") in the cycle when the read command is issued. The data output timing is characterized by CL and tAC. The read burst start (CL-1) × tCK + tAC (ns) after the clock rising edge where the read command is latched. The DDR Mobile RAM outputs the data strobe through DQS pins simultaneously with data.

tRPRE prior to the first rising edge of the data strobe, the DQS pins are driven low from high-Z state. This low period of DQS is referred as read preamble. The burst data are output coincidentally at both the rising and falling edge of the data strobe. The DQ pins become high-Z in the next cycle after the burst read operation completed. tRPST from the last falling edge of the data strobe, the DQS pins become high-Z. This low period of DQS is referred as read postamble.



Read Operation (Burst Length)

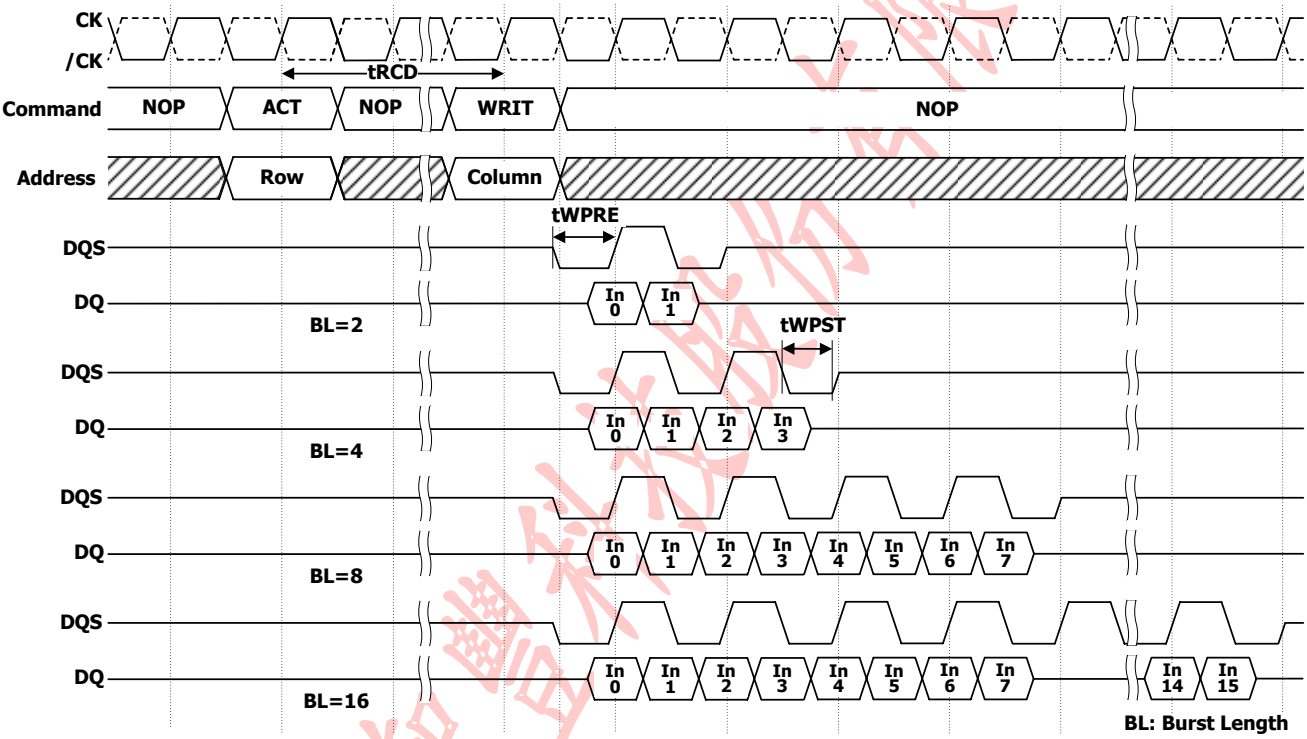


Read Operation (/CAS Latency)

5.6.3 Write Operation

The burst length (BL) and the burst type (BT) of the mode register are referred when a write command is issued.

The burst length (BL) determines the length of a sequential data input by the write command that can be set to 2, 4, 8 or 16. The latency from write command to data input is fixed to 1. The starting address of the burst write is defined by the column address, the bank select address (See "Pin Function") in the cycle when the write command is issued. DQS should be input as the strobe for the input-data and DM as well during burst operation. tWPRE prior to the first rising edge of DQS, DQS must be set to low. tWPST after the last falling edge of DQS, the DQS pins can be changed to high-Z. The leading low period of DQS is referred as write preamble. The last low period of DQS is referred as write postamble.



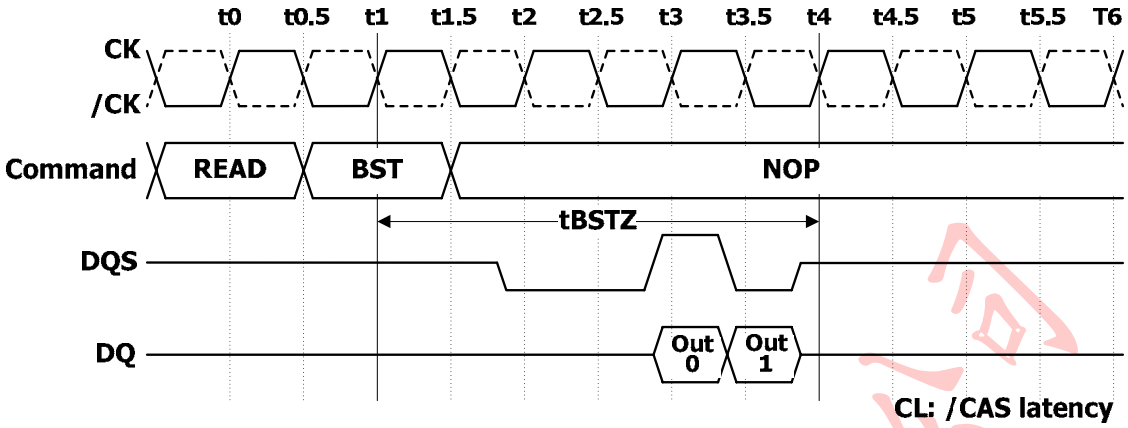
Write Operation

5.7 Burst stop

Burst stop command during burst operation

The burst stop (BST) command stops the burst read and sets all output buffers to high-Z. tBSTZ (= CL) cycles after a BST command issued, all DQ and DQS pins become high-Z.

The BST command is also supported for the burst write operation. No data will be written in subsequent cycles. Note that bank address is not referred when this command is executed.



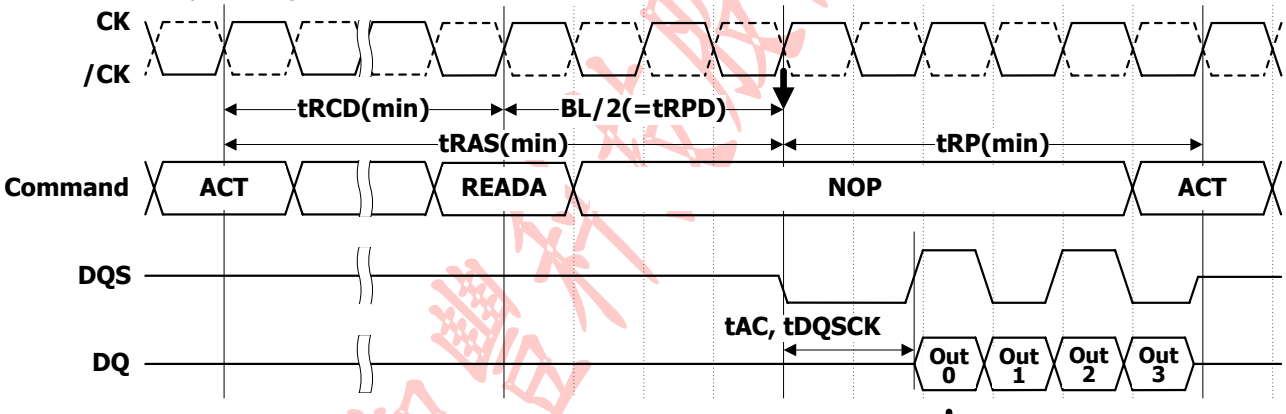
Burst Stop during a Read Operation

5.8 Auto Pre-charge

5.8.1 Read with auto pre-charge

The pre-charge is automatically performed after completing a read operation. The pre-charge starts BL/2 (= tRPD) clocks after READA command input. tRAS lock out mechanism for READA allows a read command with auto pre-charge to be issued to a bank that has been activated (opened) but has not yet satisfied the tRAS (min) specification. A column command to the other active bank can be issued the next cycle after the last data output.

Read with auto pre-charge command does not limit row commands execution for other bank.



Note: Internal auto-precharge starts at the timing indicated by " ↓ ".

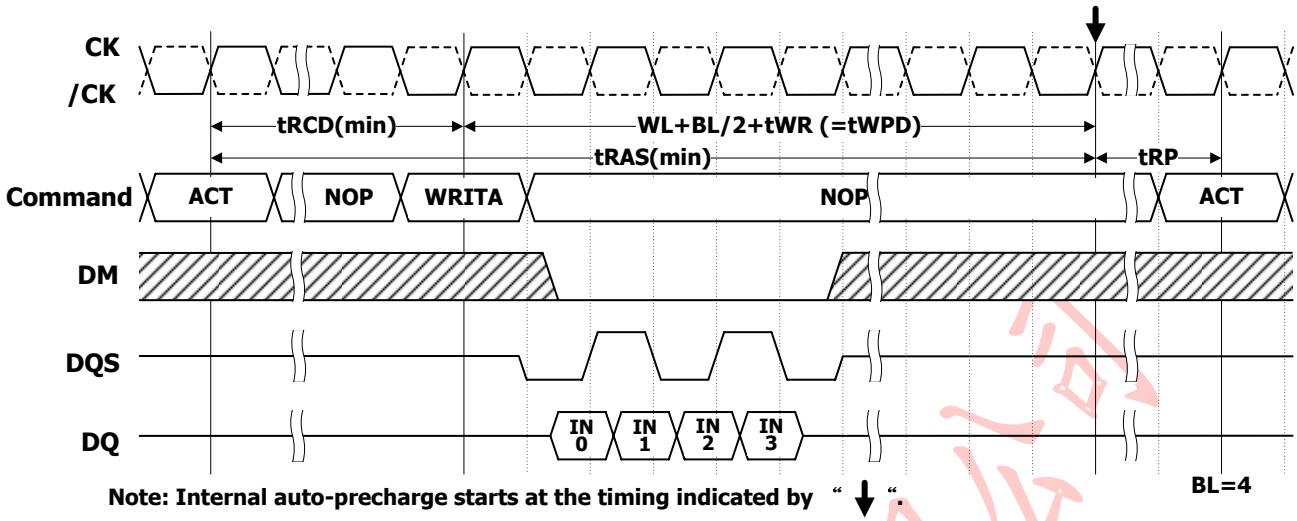
Read with auto pre-charge

5.8.2 Write with auto pre-charge

The pre-charge is automatically performed after completing a burst write operation. The pre-charge operation is started Write latency (WL) + BL/2 + tWR (= tWPD) clocks after WRITA command issued.

A column command to the other banks can be issued the next cycle after the internal pre-charge command issued.

Write with auto pre-charge command does not limit row commands execution for other bank.



Burst Write (BL=4)

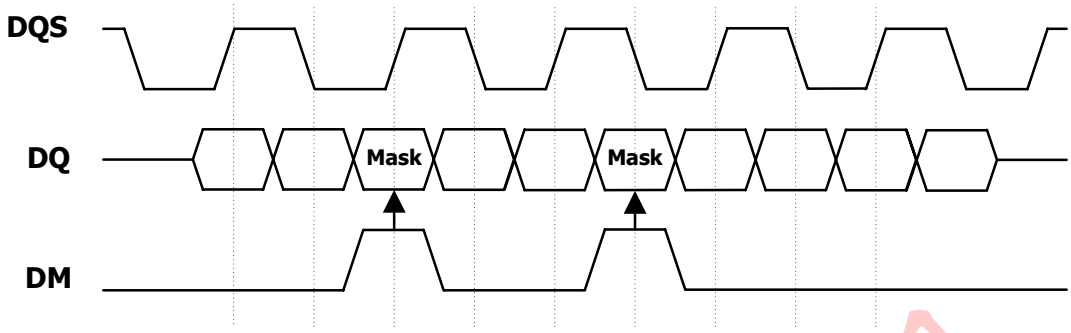
5.8.3 The Concurrent Auto Pre-charge

The DDR Mobile RAM supports the concurrent auto pre-charge feature, a read with auto pre-charge or a write with auto pre-charge, can be followed by any command to the other banks, as long as that command does not interrupt the read or write data transfer, and all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided.) The minimum delay from a read or write command with auto pre-charge, to a command to a different bank, is summarized below.

From command	To command (different bank, non-interrupting command)	Minimum delay (Concurrent AP supported)	Units
Read w/AP	Read or Read w/AP	BL/2	tCK
	Write or Write w/AP	CL (rounded up)+ (BL/2)	tCK
	Precharge or Activate	1	tCK
Write w/AP	Read or Read w/AP	1 + (BL/2) + tWTR	tCK
	Write or Write w/AP	BL/2	tCK
	Precharge or Activate	1	tCK

5.9 DM Control

DM can mask input data. By setting DM to low, data can be written. UDM and LDM can mask the upper and lower byte of input data, respectively. When DM is set to high, the corresponding data is not written, and the previous data is held. The latency between DM input and enabling/disabling mask function is 0.



Write mask latency = 0

DM Control

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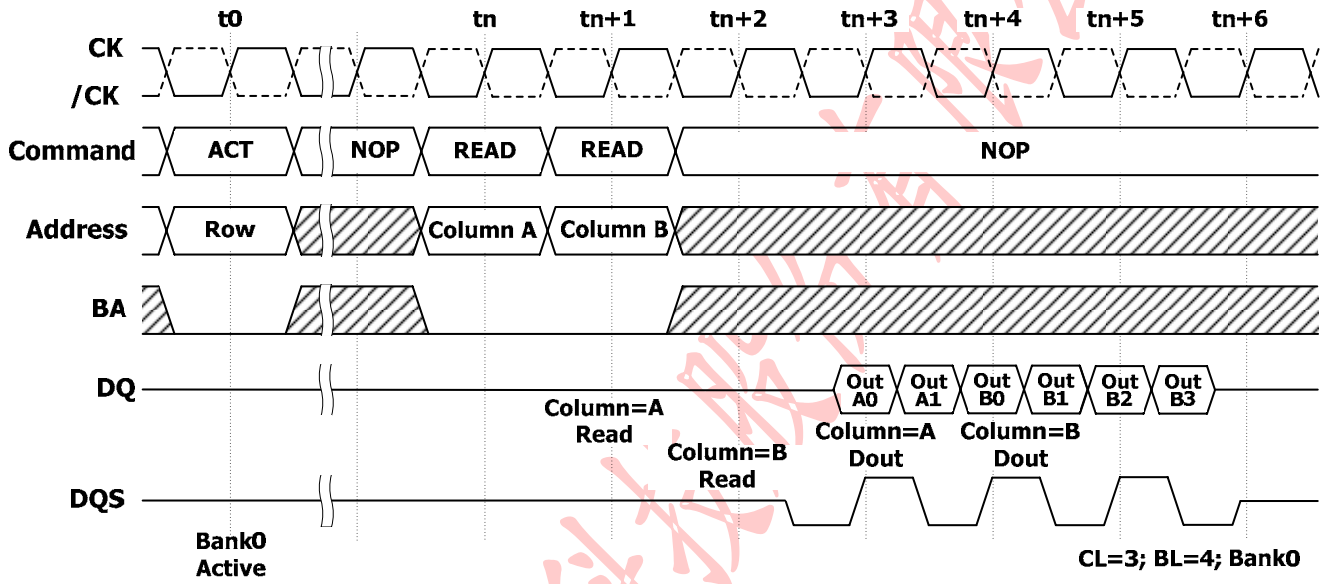
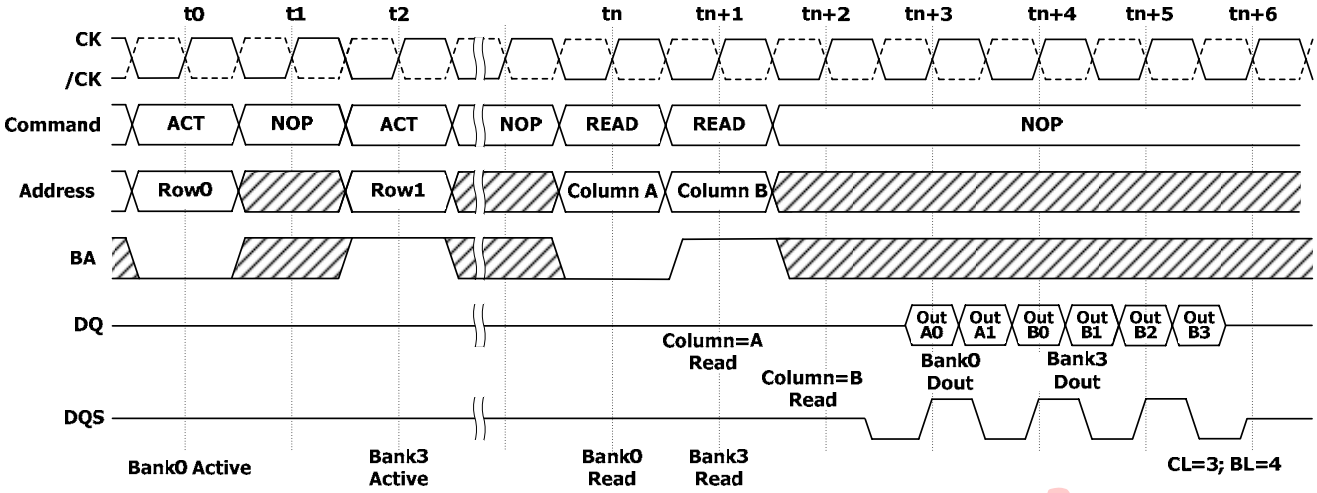
6 Command Intervals

6.1 A Read command to the consecutive Read command Interval

	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1	Same	Same	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
2	Same	Different	-	Precharge the bank to interrupt the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3	Different	Any	ACTIVE	The consecutive read can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
			IDLE	Precharge the bank without interrupting the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued.



READ to READ Command Interval (same ROW address in the same bank)



READ to READ command interval (different bank)

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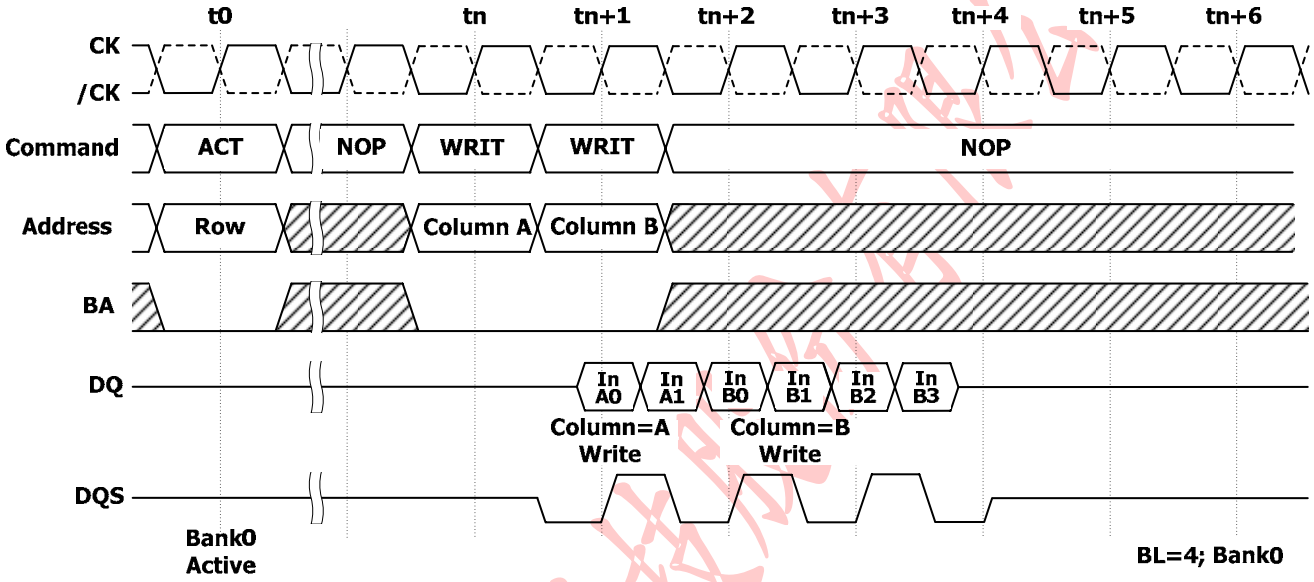
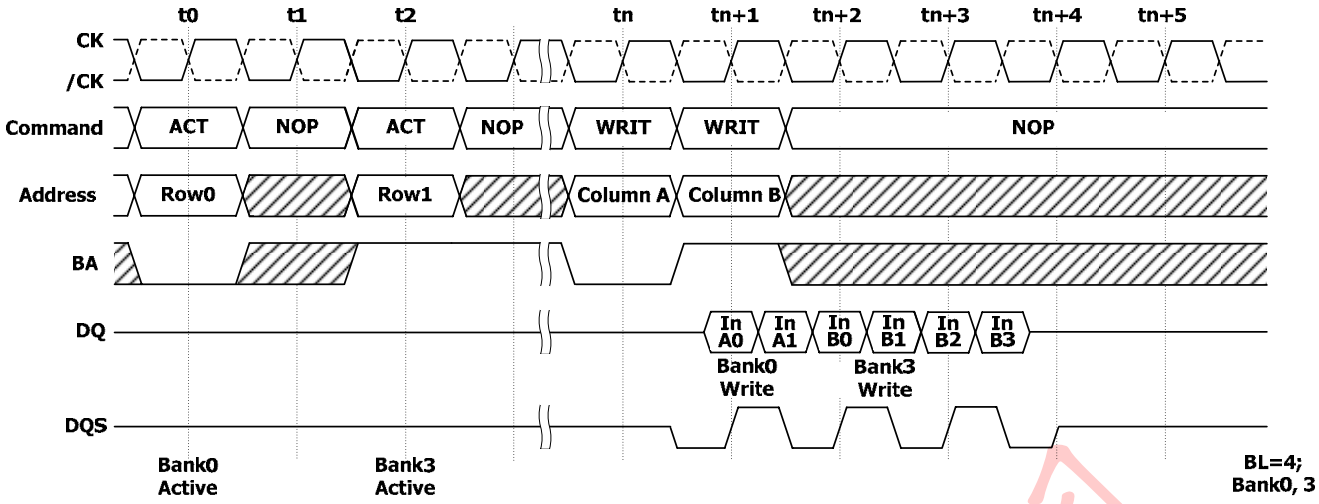
6.2 A Write command to the consecutive Write command Interval

	Destination row of the consecutive write command			
	Bank address	Row address	State	Operation
1	Same	Same	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding write operation.
2	Same	Different	-	Precharge the bank to interrupt the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued. See 'A write command to the consecutive precharge interval' section.
3	Different	Any	ACTIVE	The consecutive write can be performed after an interval of no less than 1 cycle to interrupt the preceding read operation.
			IDLE	Precharge the bank without interrupting the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued.



WRITE to WRITE command interval (same Row address in the same bank)



WRITE to WRITE command interval (different bank)

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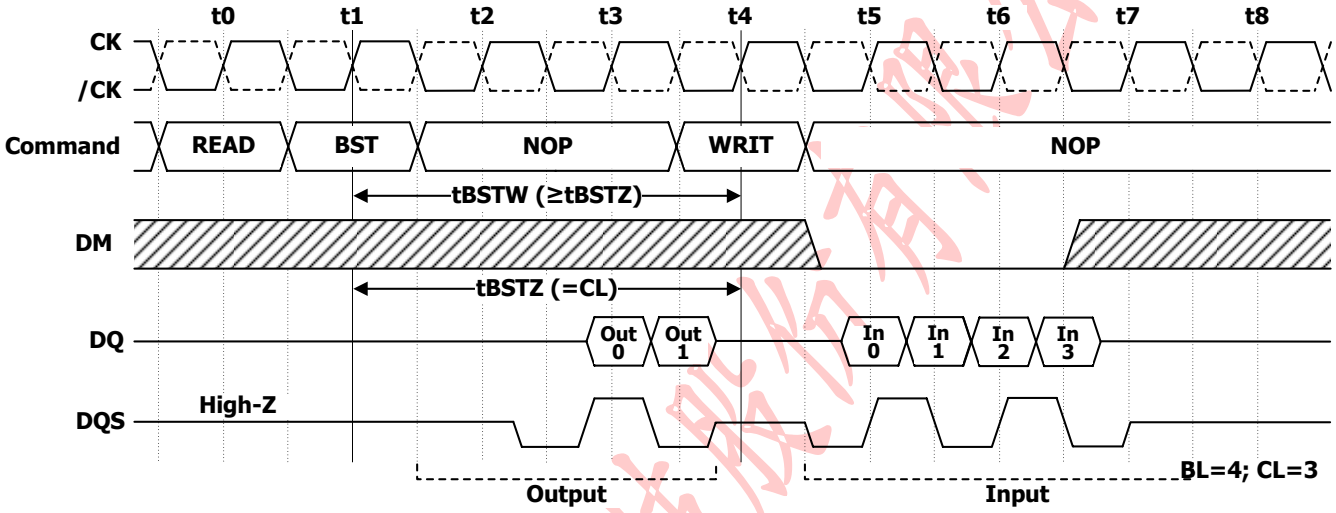
6.3 A Read command to the consecutive Write command Interval with the BST command

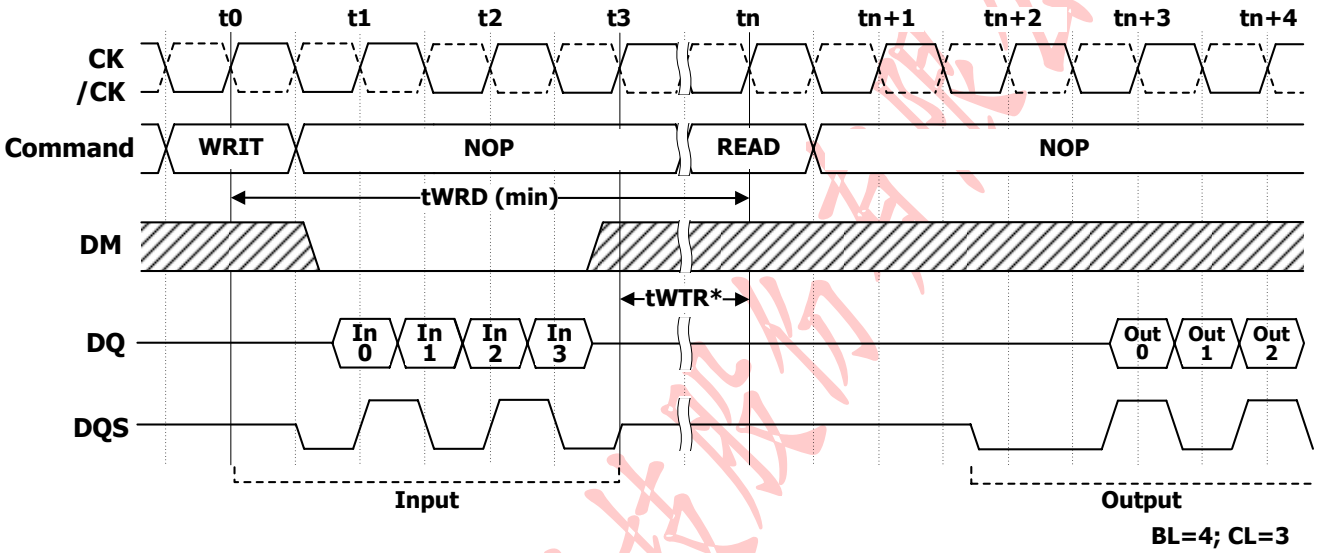
	Destination row of the consecutive write command			
	Bank address	Row address	State	Operation
1	Same	Same	ACTIVE	Issue the BST command. tBSTW (≥ tBSTZ) after the BST command, the consecutive write command can be issued.
2	Same	Different	-	Precharge the bank to interrupt the preceding read operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive write command can be issued. See 'A read command to the consecutive precharge interval' section.
3	Different	Any	ACTIVE	Issue the BST command. tBSTW (≥ tBSTZ) after the BST command, the consecutive write command can be sued.
			IDLE	Precharge the bank independently of the preceding read operation. tRP after the precharge command, issue the CT command. tRCD after the ACT command, the consecutive write command can be issued.



READ to WRITE Command Interval

6.4 A Write command to the consecutive Read command interval: To complete the burst operation

	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1	Same	Same	ACTIVE	To complete the burst operation, the consecutive read command should be performed tWRD after the write command.
2	Same	Different	-	Precharge the bank tWPD after the preceding write command. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued. See 'A read command to the consecutive precharge interval' section.
3	Different	Any	ACTIVE	To complete a burst operation, the consecutive read command should be performed tWRD after the write command.
			IDLE	Precharge the bank independently of the preceding write operation. tRP after the precharge command, issue the ACT command. tRCD after the ACT command, the consecutive read command can be issued.



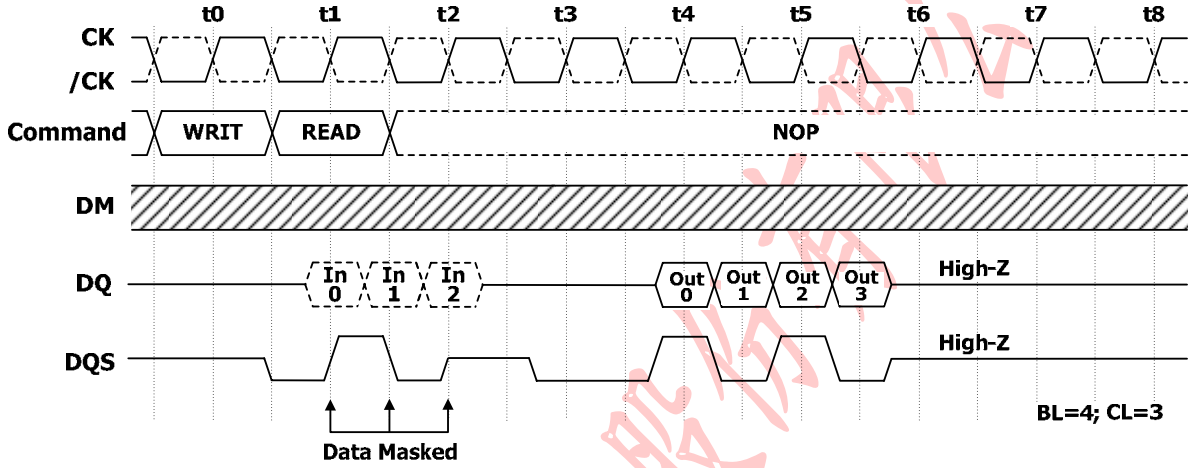
WRITE to READ Command Interval

6.5 A Write command to the consecutive Read command Interval: To interrupt the Write operation

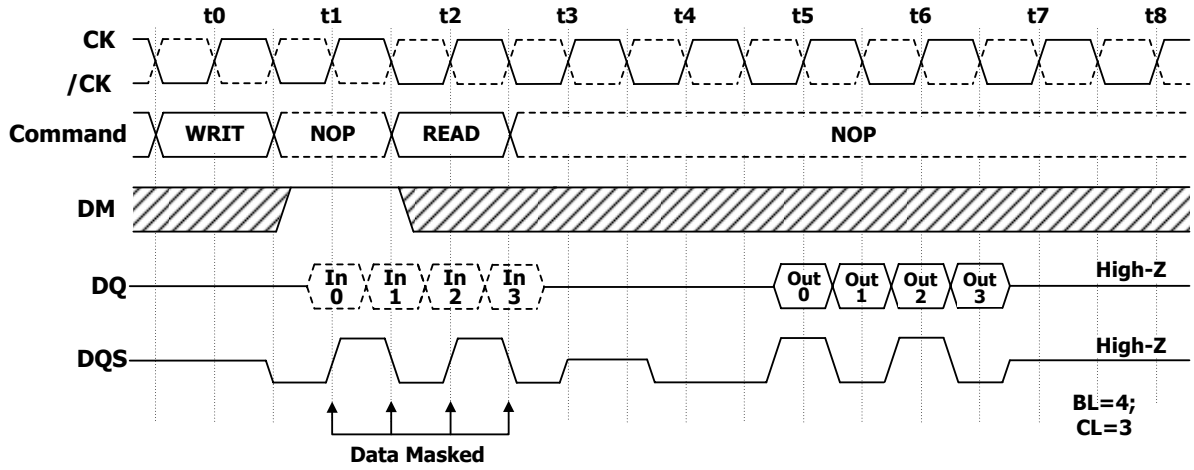
	Destination row of the consecutive read command			
	Bank address	Row address	State	Operation
1	Same	Same	ACTIVE	DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary.
2	Same	Different	-	—*1
3	Different	Any	ACTIVE	DM must be input 1 cycle prior to the read command input to prevent from being written invalid data. In case, the read command is input in the next cycle of the write command, DM is not necessary.
			IDLE	—*1

Note: 1. Precharge must be preceded to read command. Therefore read command can not interrupt the write operation in this case.

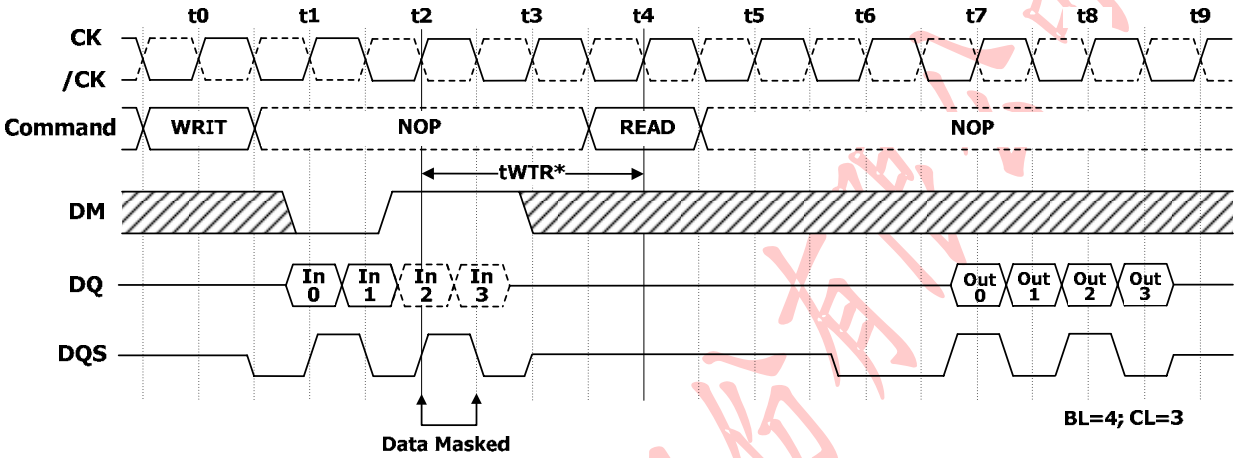
WRITE to READ Command Interval (Same bank, same ROW address)



WRITE to READ delay=1 clock cycle



WRITE to READ delay=2 clock cycle



WRITE to READ delay=4 clock cycle

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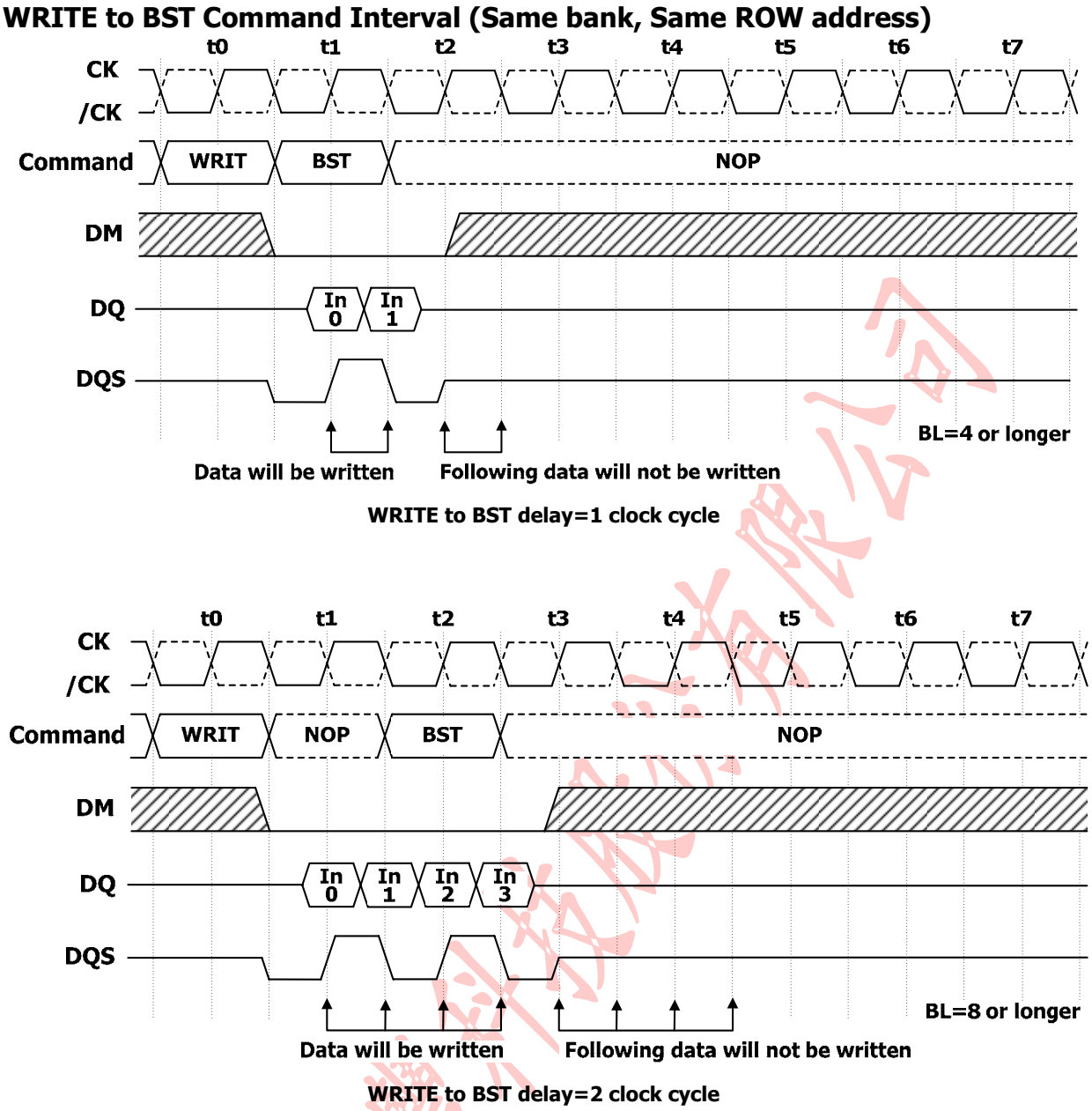
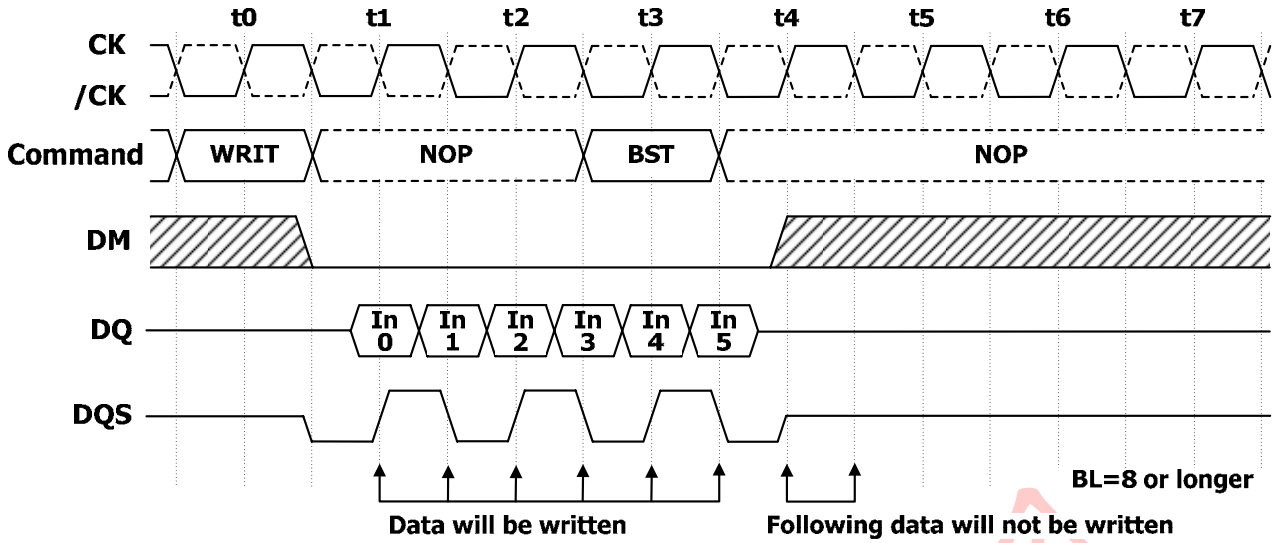
6.6 A Write command to the Bust stop command Interval: To interrupt the Write Operation





WRITE to BST delay=3 clock cycle

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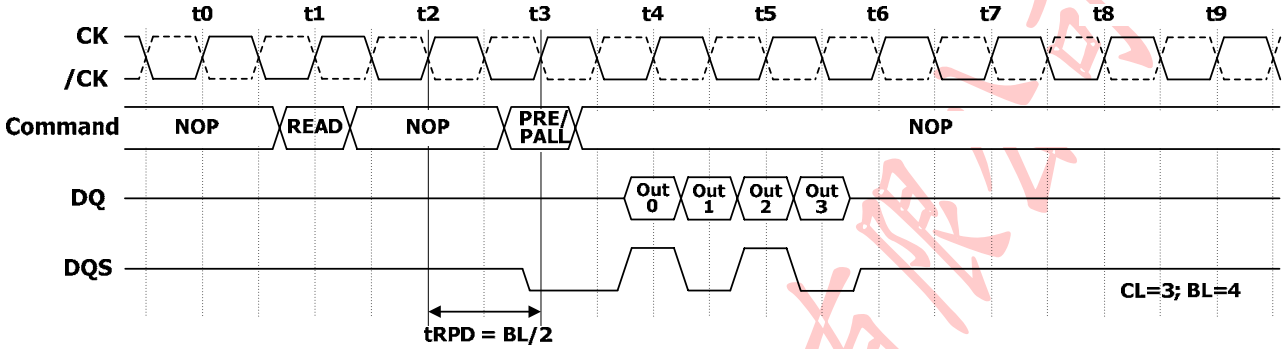
6.7 A Read command to the consecutive Pre-charge command Interval

Operation by each case of destination bank of the consecutive Pre-charge command.

	Bank address	Operation
1	Same	The PRE and PALL command can interrupt a read operation. To complete a burst read operation, tRPD is required between the read and the precharge command. Please refer to the following timing chart.
2	Different	The PRE command does not interrupt a read command. No interval timing is required between the read and the precharge command.

READ to PRECHARGE Command Interval (same bank) : To output all data

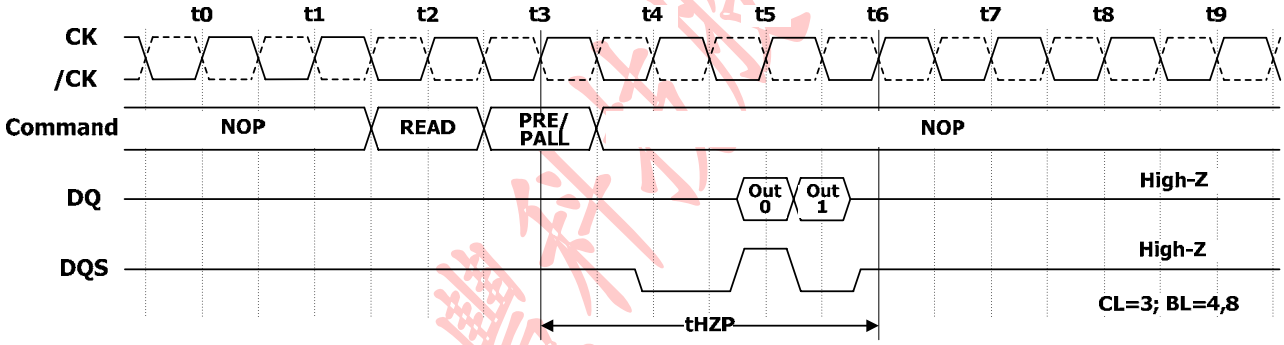
To complete a burst read operation and get a burst length of data, the consecutive precharge command must be issued tRPD (= BL/ 2 cycles) after the read command is issued.



READ to PRECHARGE Command Interval (same bank): To output all data (CL = 3, BL = 4)

READ to PRECHARGE Command Interval (same bank): To stop output data

A burst data output can be interrupted with a pre-charge command. All DQ pins and DQS pins become high-Z tHZP(= CL) after the pre-charge command.



READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 3, BL = 4, 8)

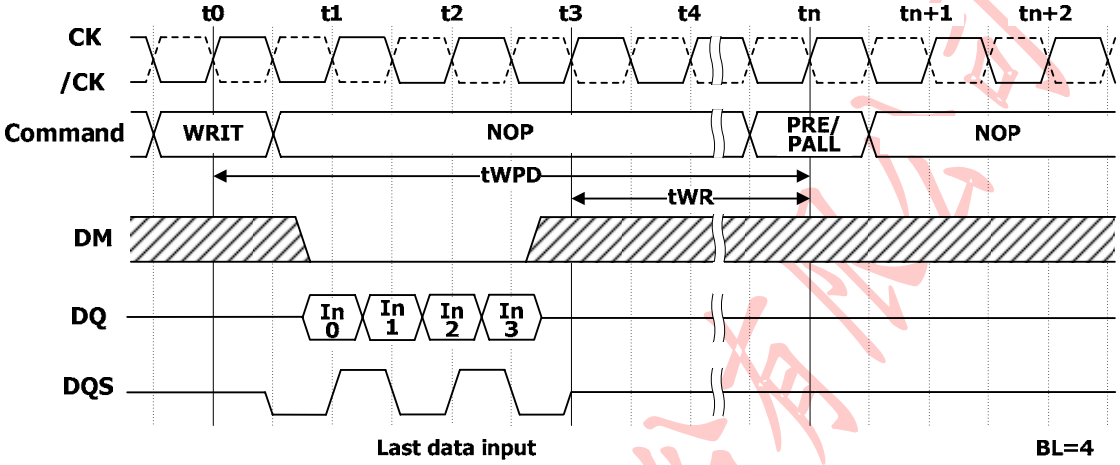
6.8 A Write command to the consecutive Pre-charge command interval (Same bank)

Operation by each case of destination bank of the consecutive Pre-charge command.

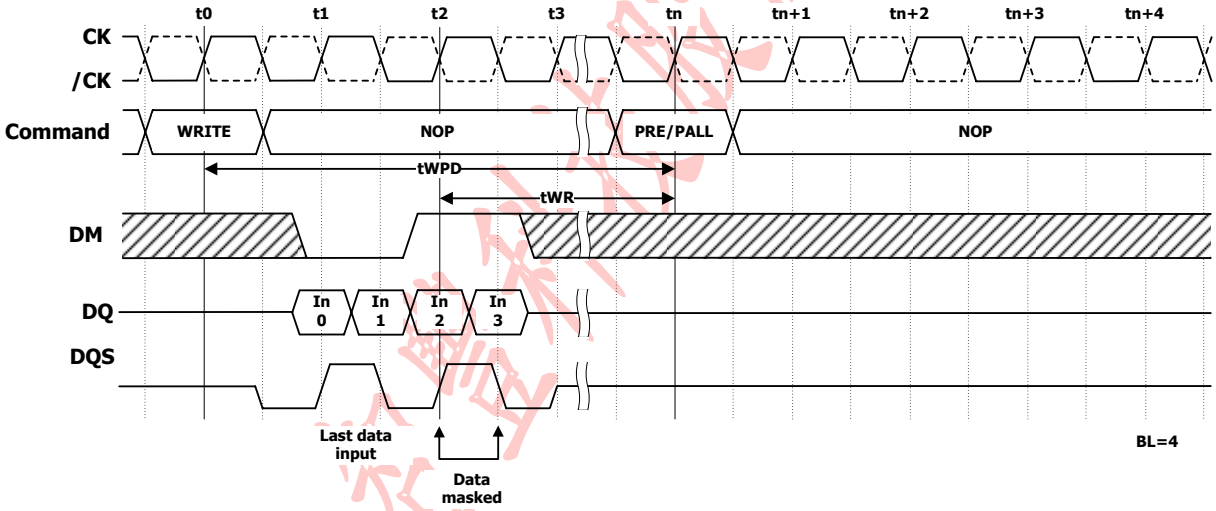
	Bank address	Operation
1	Same	The PRE and PALL command can interrupt a write operation. To complete a burst write operation, tWPD is required between the write and the precharge command. Please refer to the following timing chart.
2	Different	The PRE command does not interrupt a write command. No interval timing is required between the write and the precharge command.

WRITE to PRECHARGE Command Interval (same bank)

The minimum interval tWPD is necessary between the write command and the precharge command.



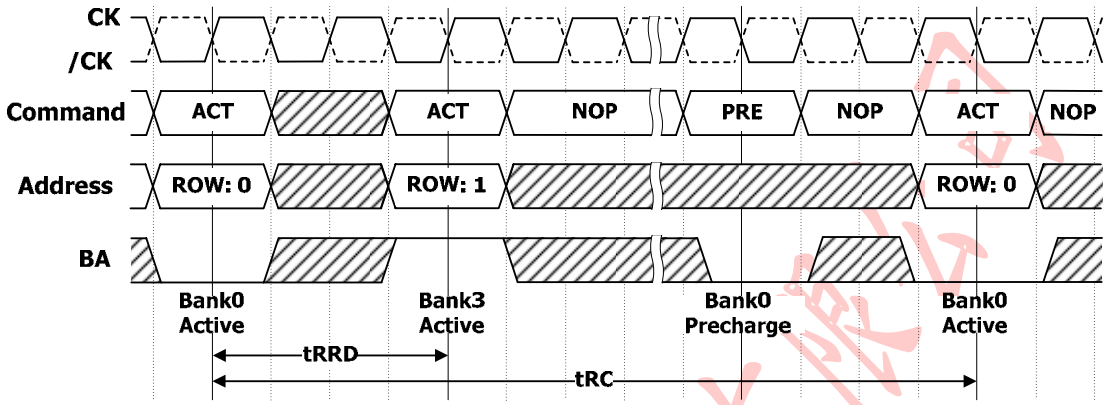
WRITE to PRECHARGE Command Interval (same bank, BL=4))



WRITE to PRE-CHARGE Command Interval (same bank, BL=4, DM to mask data)

6.9 Bank active command interval

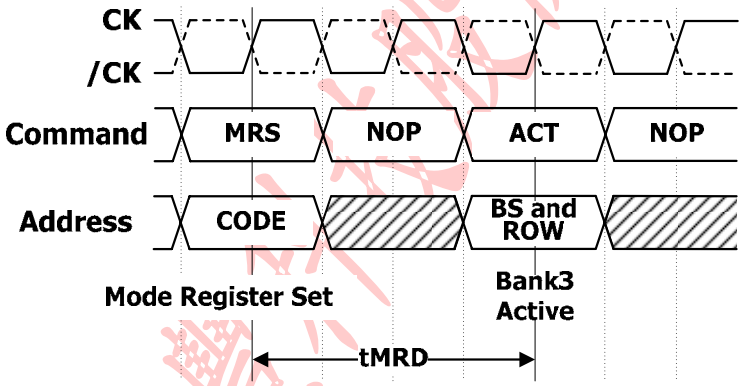
	Destination row of the consecutive ACT command			
	Bank address	Row address	State	Operation
1	Same	Any	ACTIVE	Two successive ACT commands can be issued at tRC interval. In between two successive ACT operations, pre-charge command should be executed.
2	Different	Any	ACTIVE	Precharge the bank. tRP after the pre-charge command, the consecutive ACT command can be issued.
			IDLE	tRRD after an ACT command, the next ACT command can be issued.



Bank Active to Bank Active

6.10 Mode Register set to Bank-active command interval

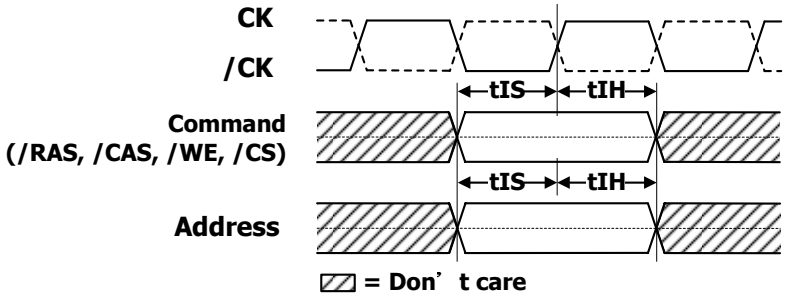
The interval between setting the mode register and executing a bank-active command must be no less than tMRD.



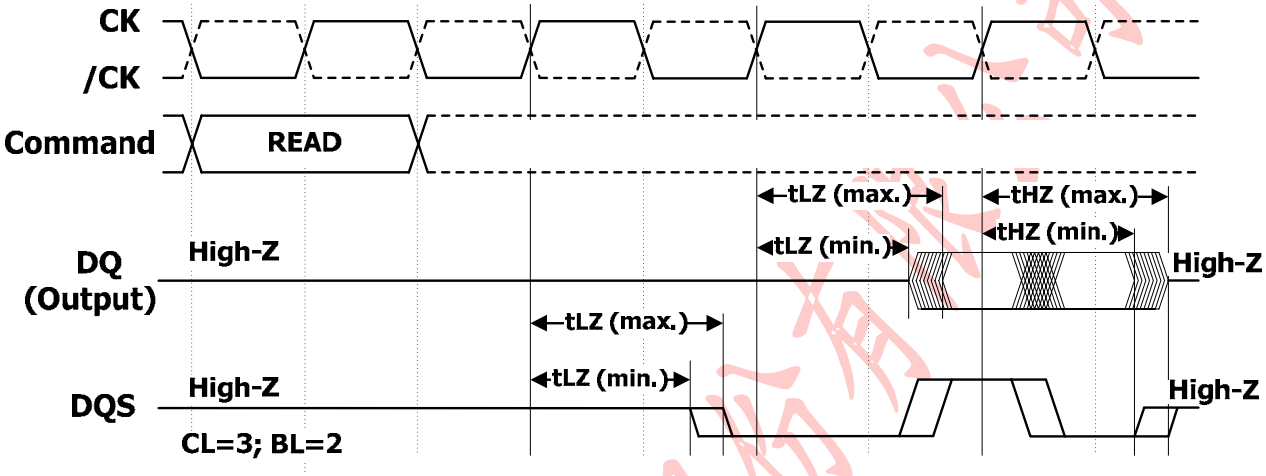
Mode Register Set to Bank Active

7 Timing Waveforms

7.1 Command and Address Input Timing Definition



7.2 Read Timing Definition (1)



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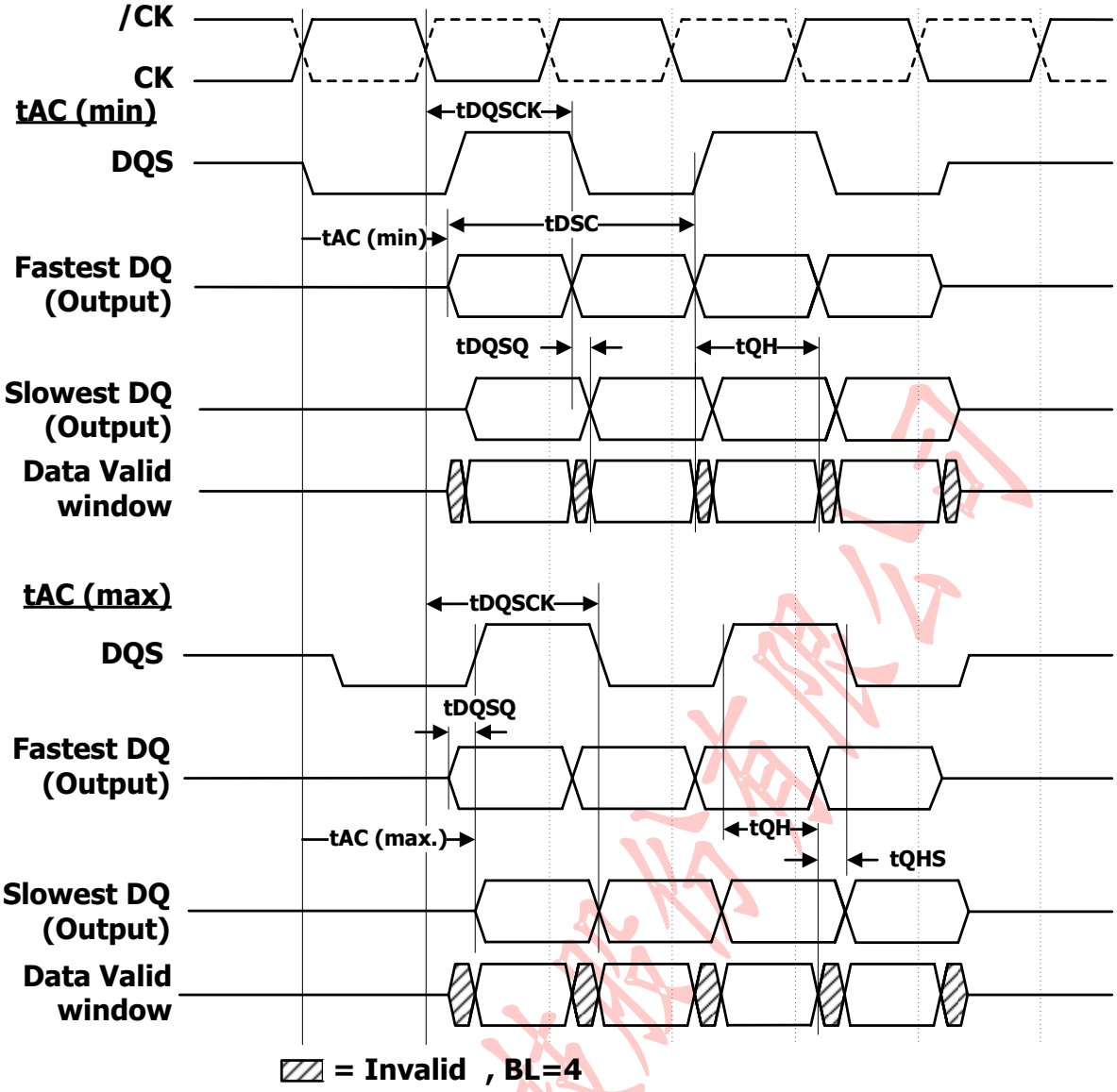
7.3 Read Timing Definition (2)



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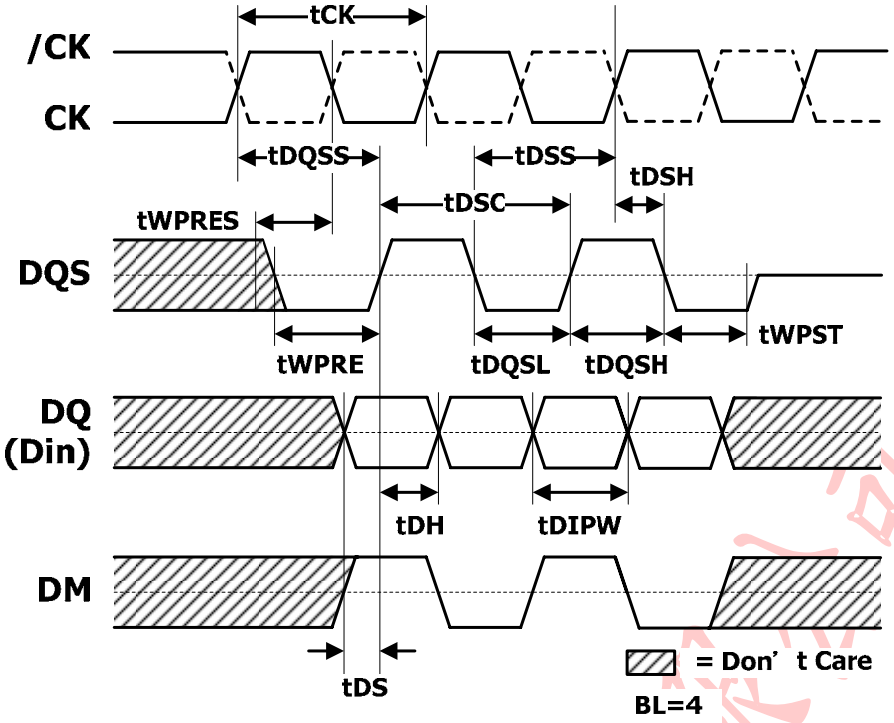
7.4 Write Timing Definition



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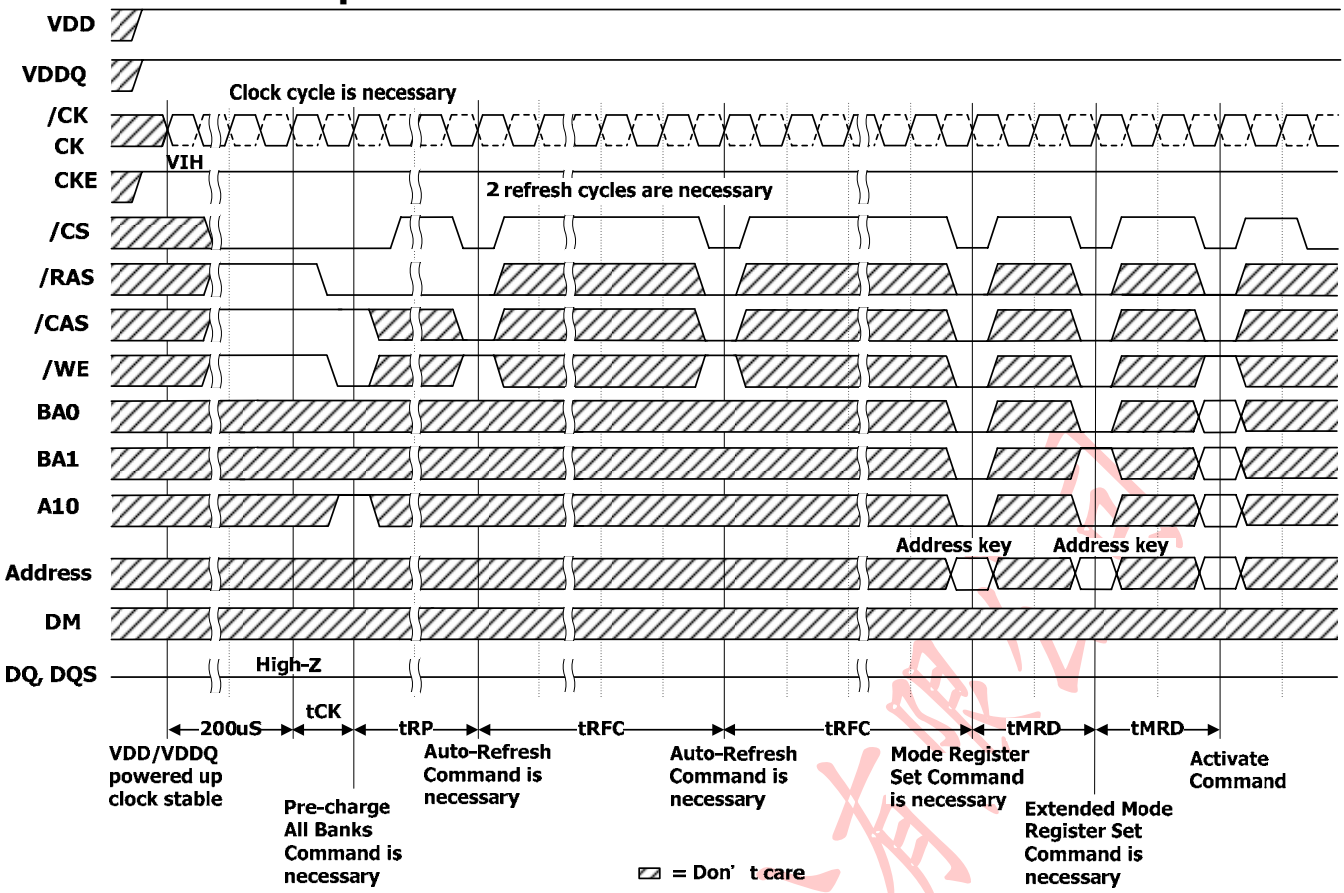
7.5 Initialize Sequence



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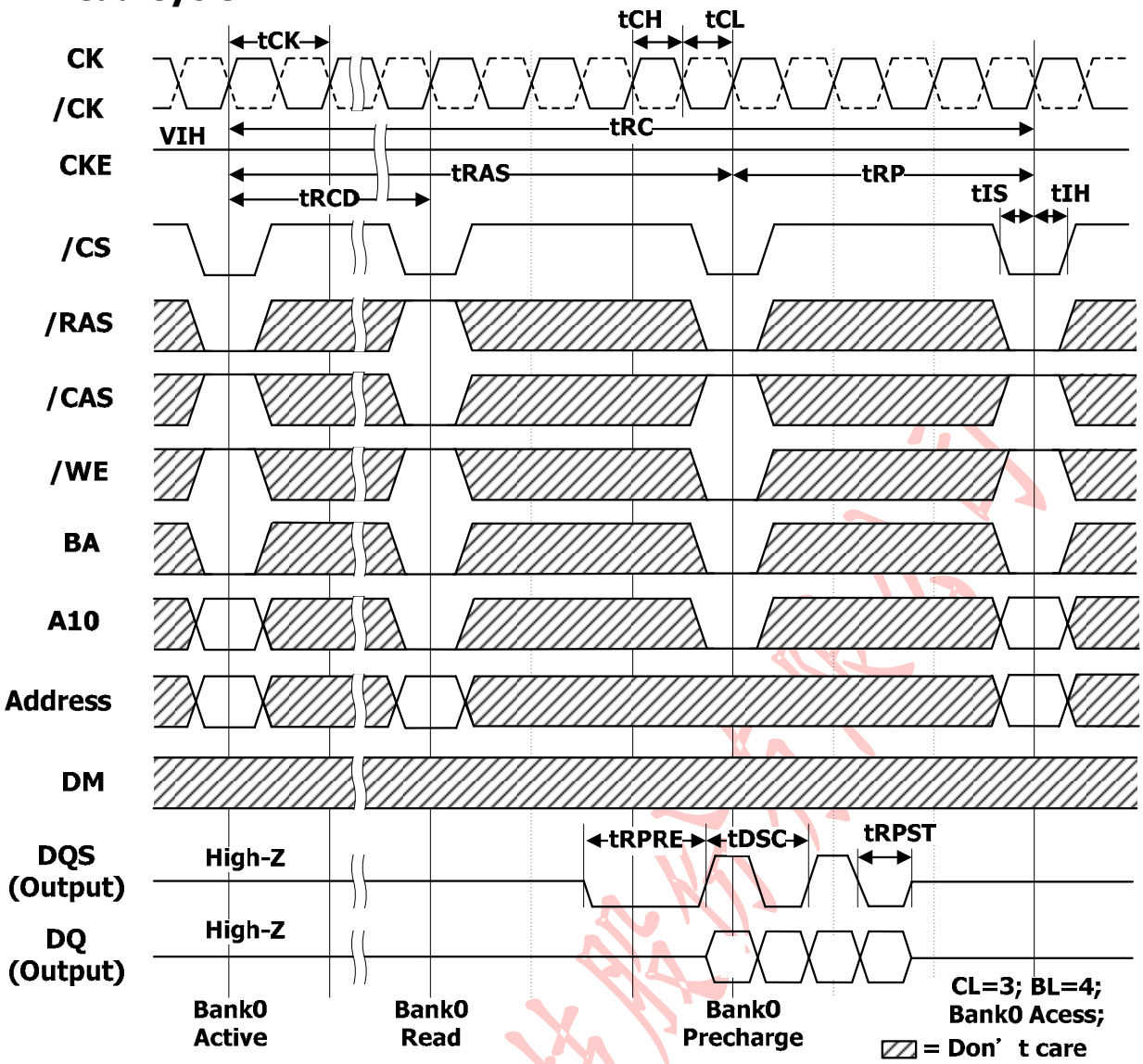
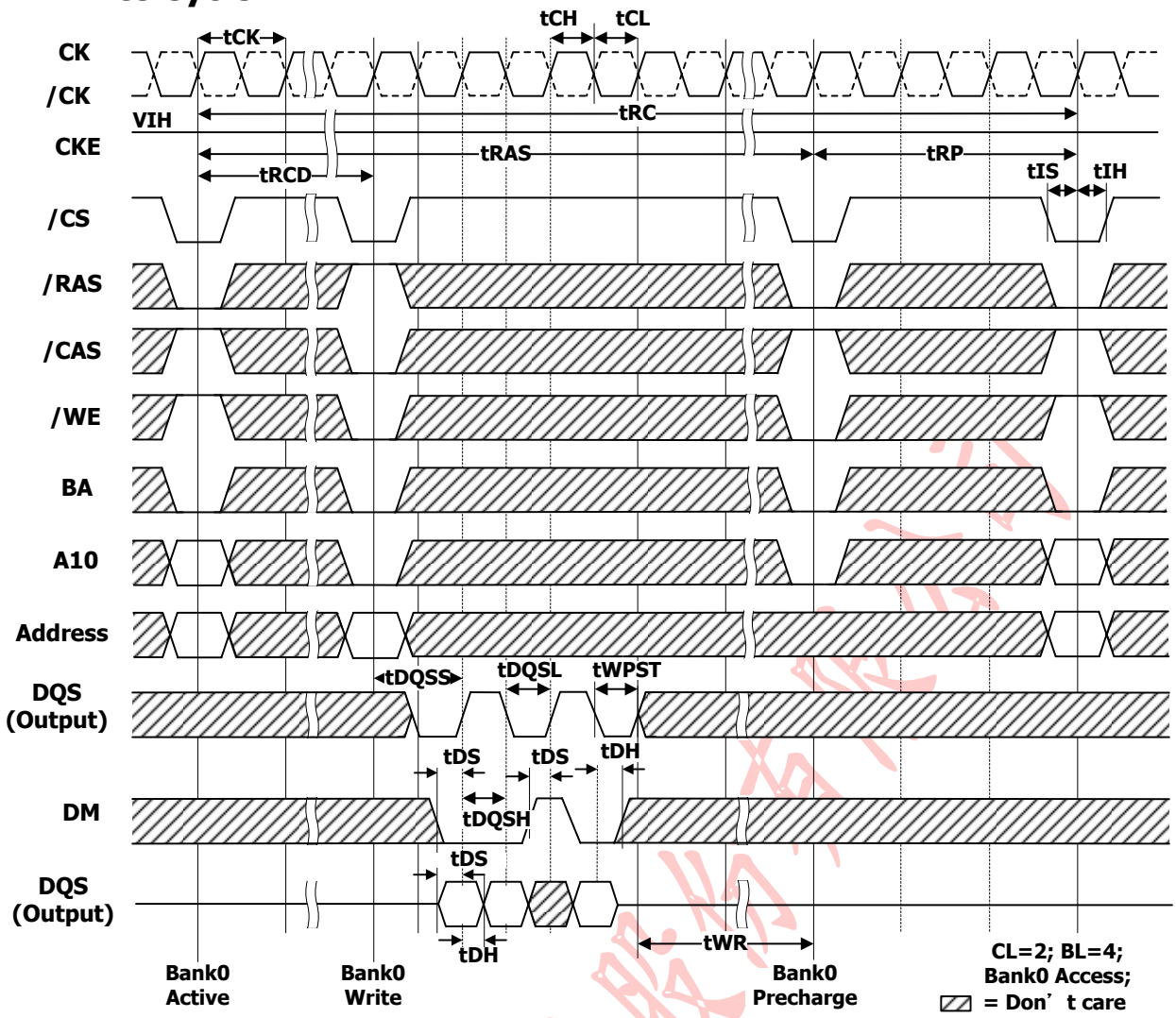
7.6 Read Cycle



7.7 Write Cycle



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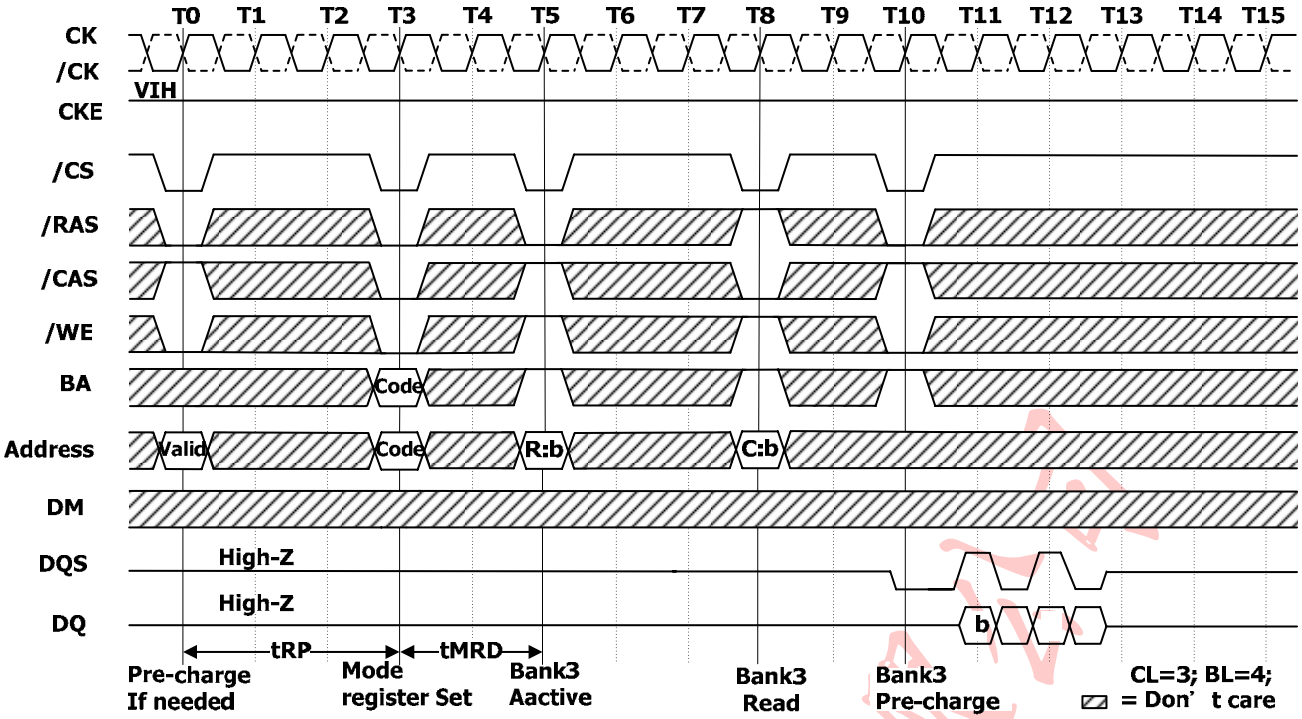
7.8 Mode Register Set Cycle



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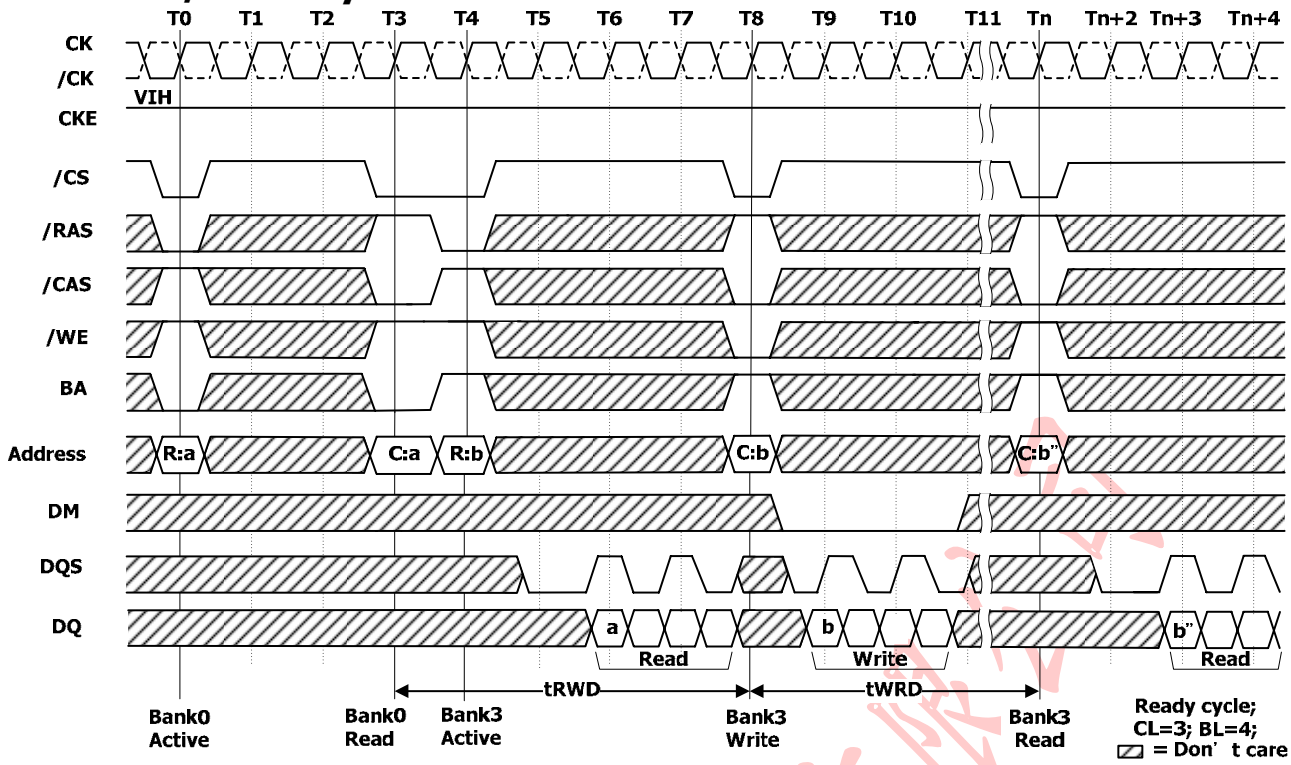
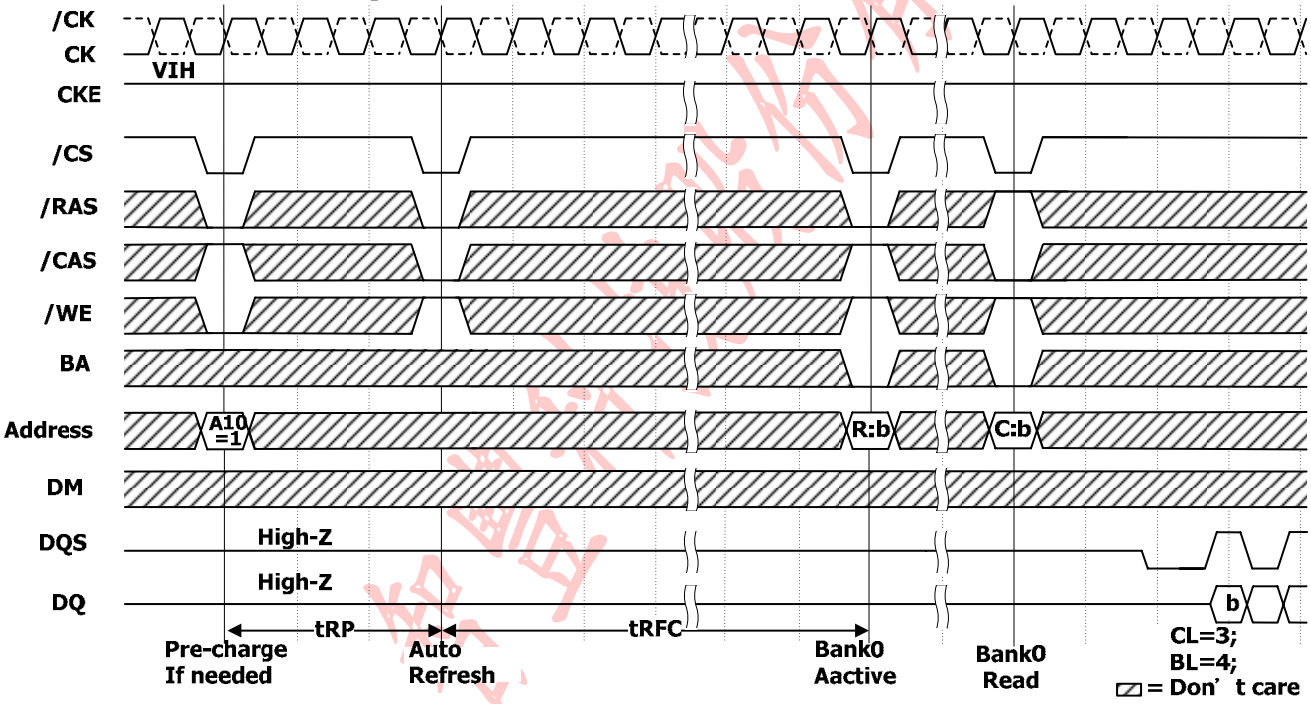
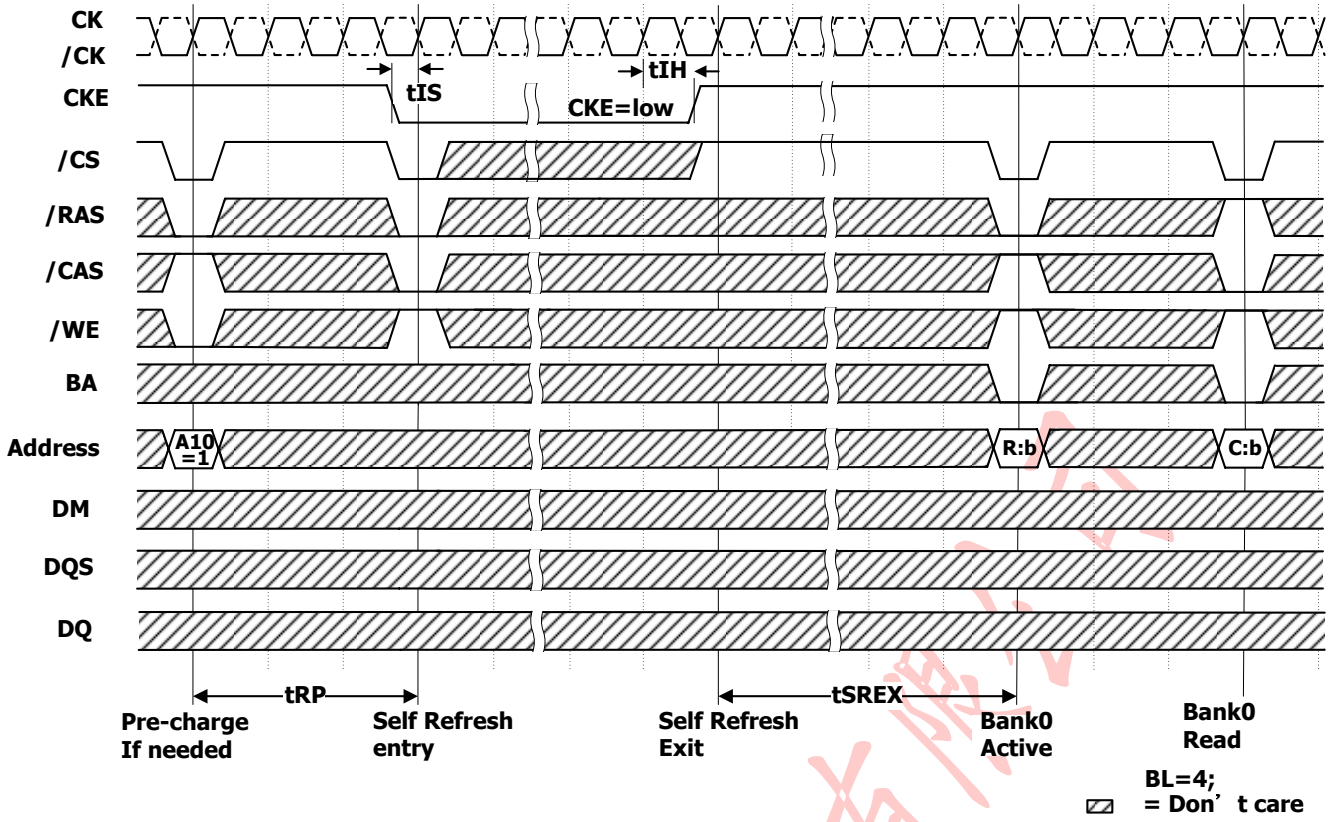
7.9 Read/Write Cycle



7.10 Auto-Refresh Cycle



7.11 Self-Refresh Cycle



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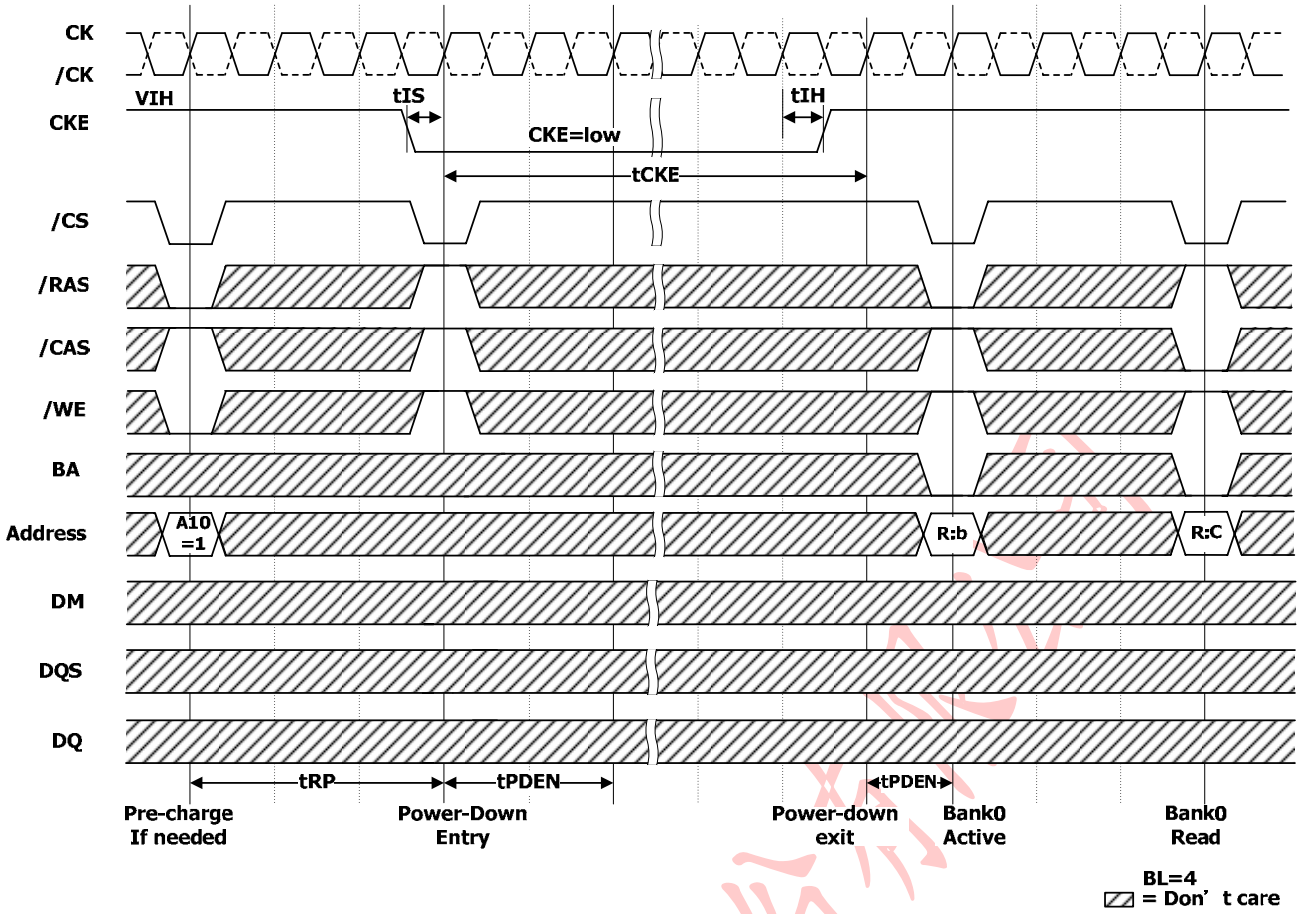
7.12 Power-Down Entry and Exit



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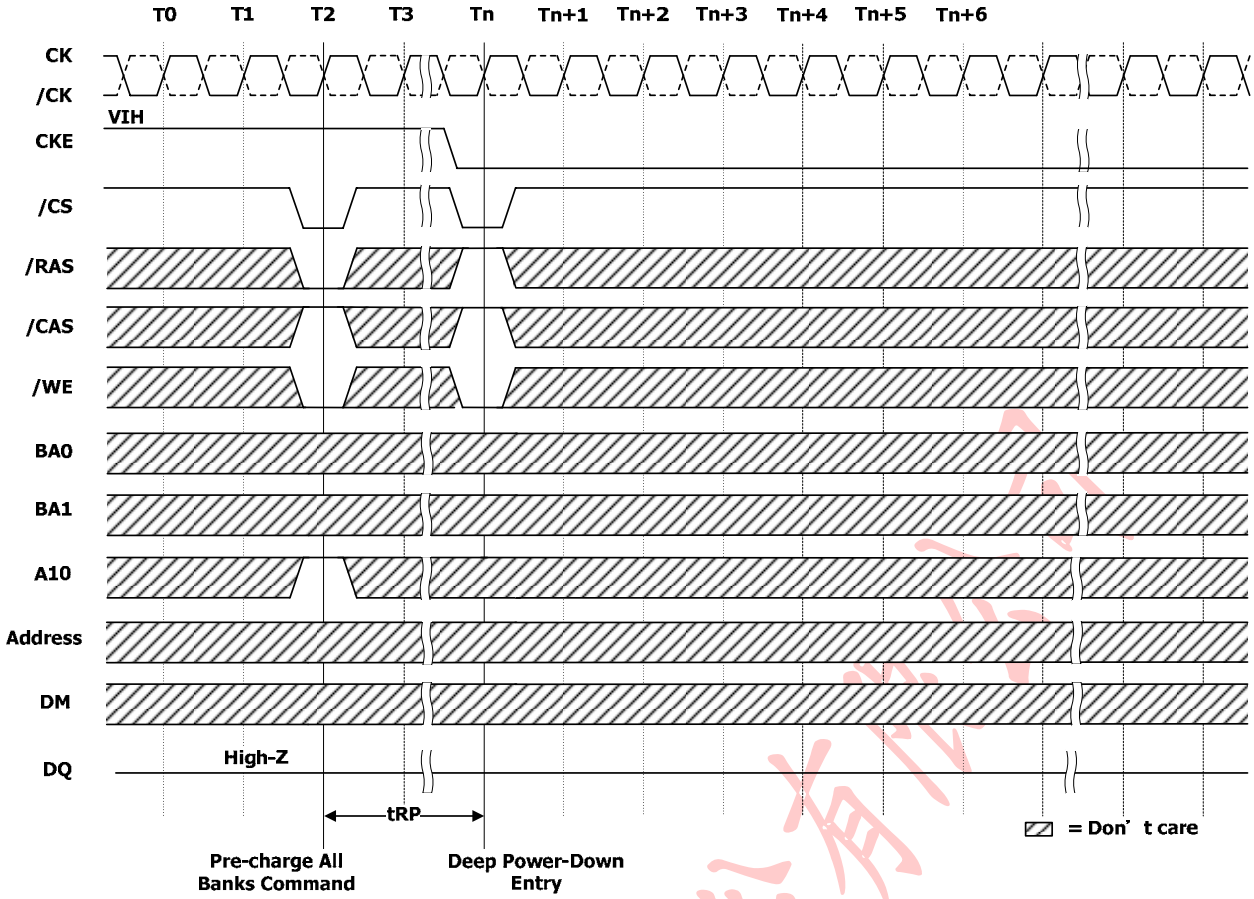
7.13 Deep Power-Down Entry



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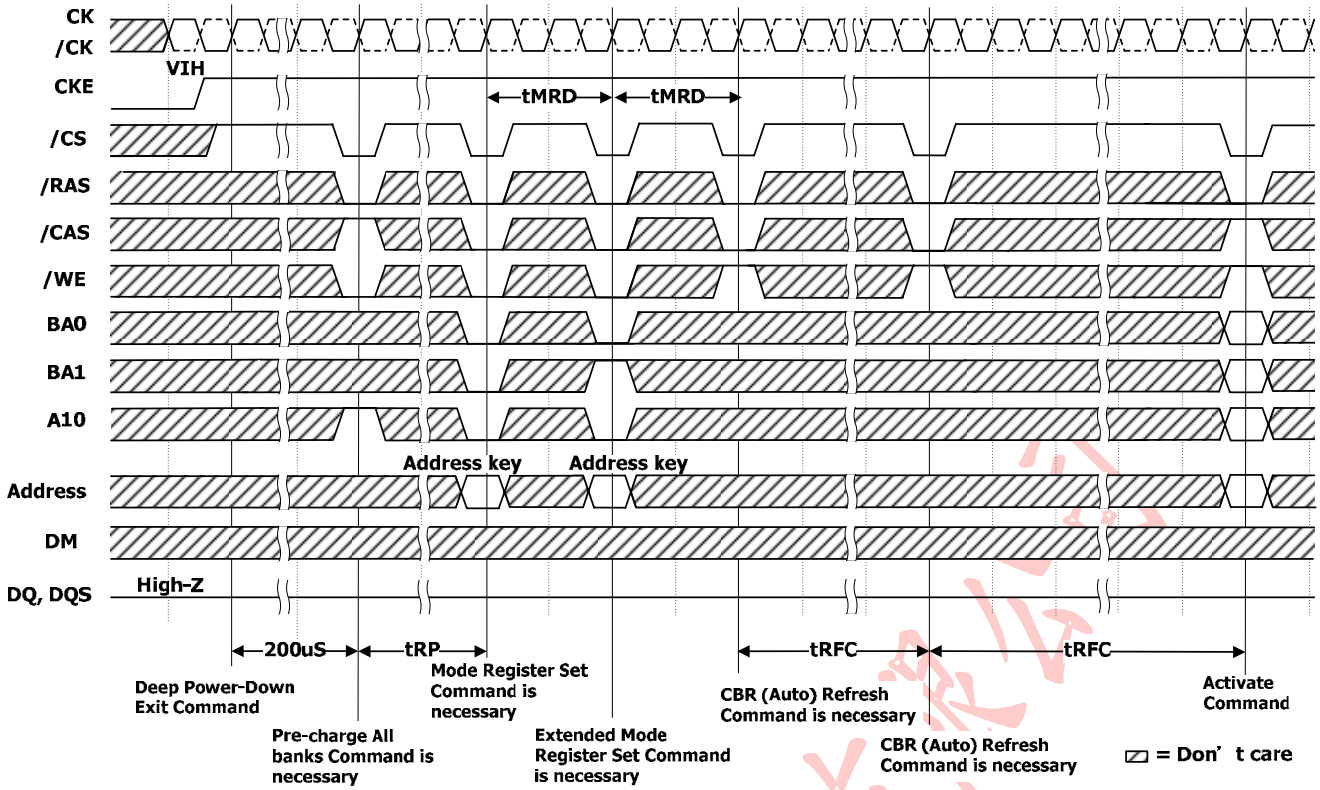
7.14 Deep Power-Down Exit



Note: The sequence of auto-refresh, mode register programming and extended mode register programming above.

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