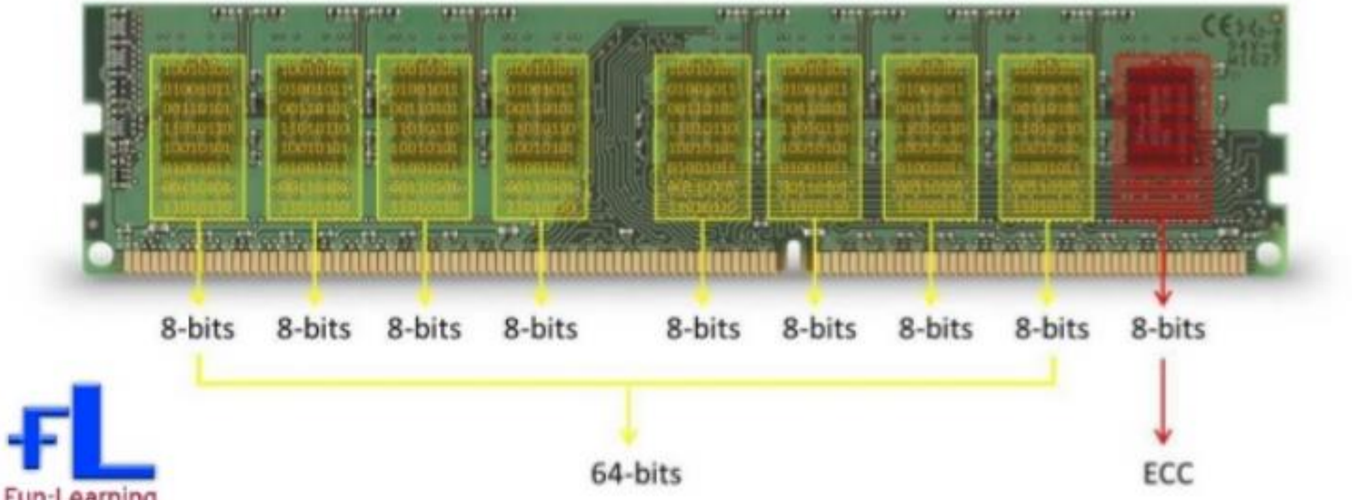
DRAM RAS Features

Mechanism Insight: Memory ECC - The Comprehensive of SEC-DED

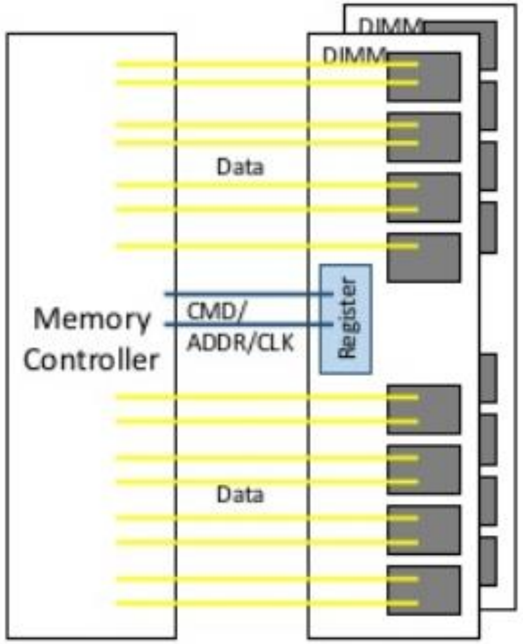
Close the gaps between academic and industrial practice.



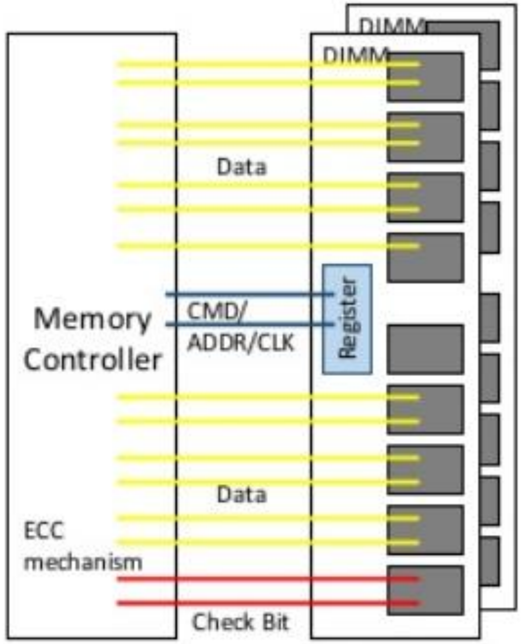
Fun-Learning

Background of ECC (Error Correction Code) for DRAM

- DRAM (Dynamic Random Access Memory)
- Error Detection and Correction (EDAC)

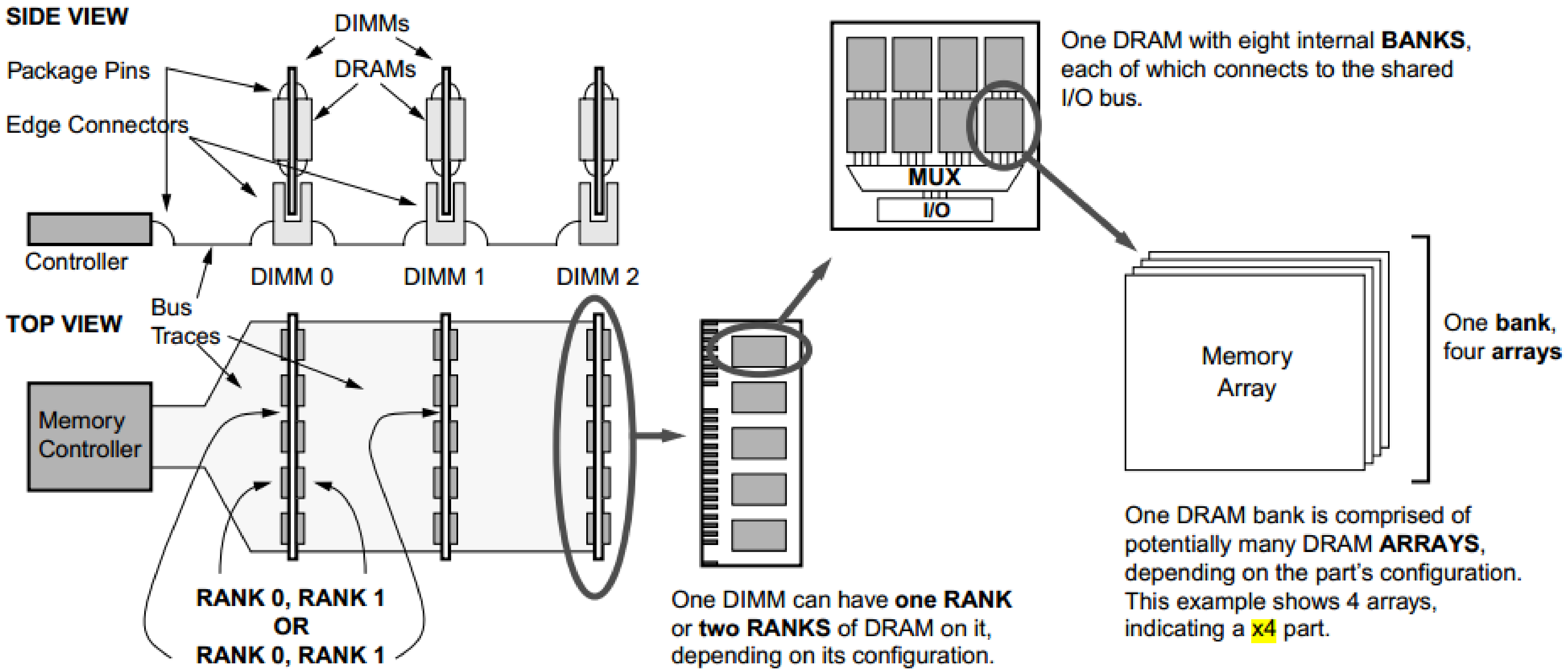


Legacy memory modules



Memory modules with Error Correction Code (ECC)

DRAM configuration



One DRAM with eight internal **BANKS**, each of which connects to the shared I/O bus.

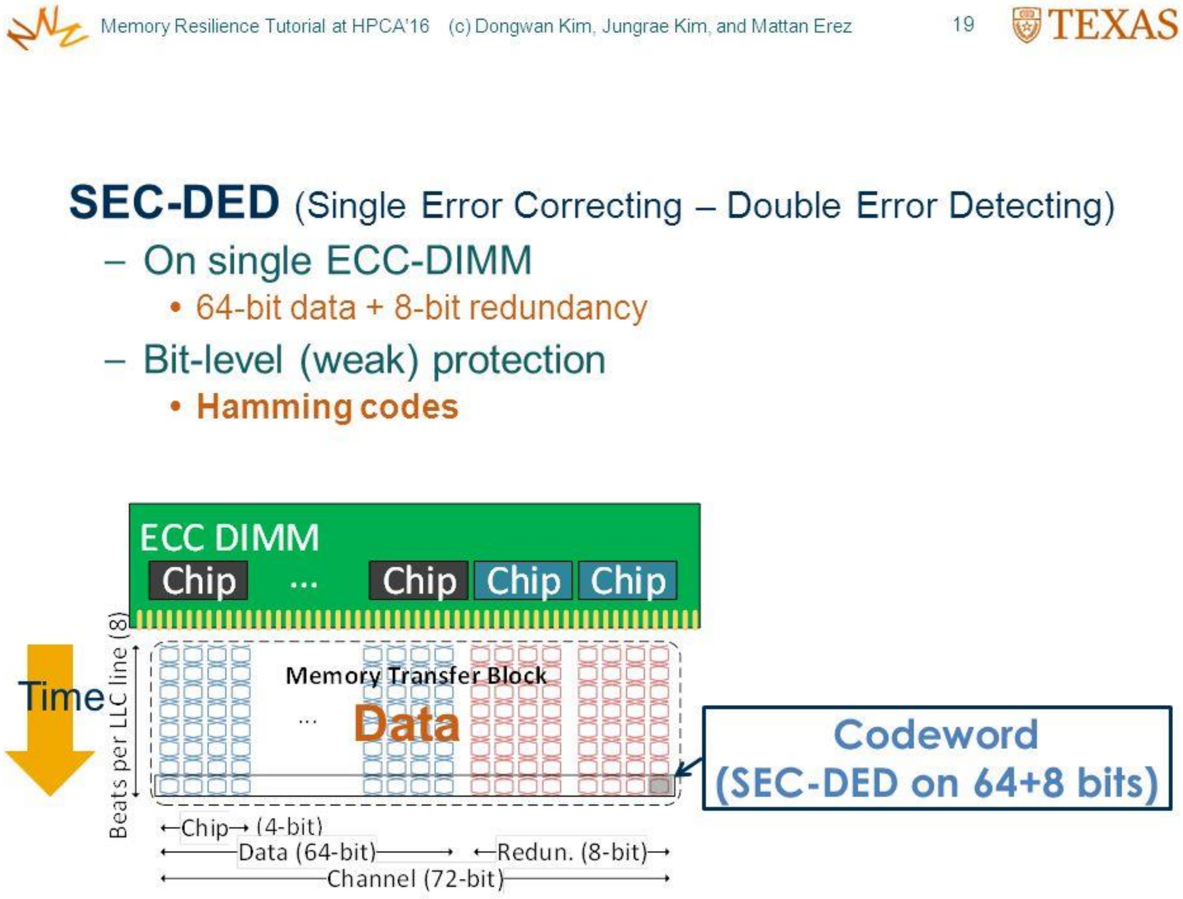
One DIMM can have **one RANK** or **two RANKS** of DRAM on it, depending on its configuration.

One DRAM bank is comprised of potentially many DRAM **ARRAYS**, depending on the part's configuration. This example shows 4 arrays, indicating a x4 part.

FIGURE 7.5: DIMMs, ranks, banks, and arrays. A system has potentially many DIMMs, each of which may contain one or more ranks. Each rank is a set of ganged DRAM devices, each of which has potentially many banks. Each bank has potentially many constituent arrays, depending on the part's data width.

The 168- and 184-pin dual in-line memory modules (DIMMs) used in servers today are built using x4 (4 data bit), x8, or x16 DRAM devices.

Any of these multibit failure modes result in a fatal error for a SEC/DED memory system, because only a single bit can be corrected by standard ECC.



Memory Resilience Tutorial at HPCA'16 (c) Dongwan Kim, Jungrae Kim, and Mattan Erez 19 TEXAS

SEC-DED (Single Error Correcting – Double Error Detecting)

- On single ECC-DIMM
  - 64-bit data + 8-bit redundancy
- Bit-level (weak) protection
  - **Hamming codes**

DRAM RAS Features - Error Correcting Codes

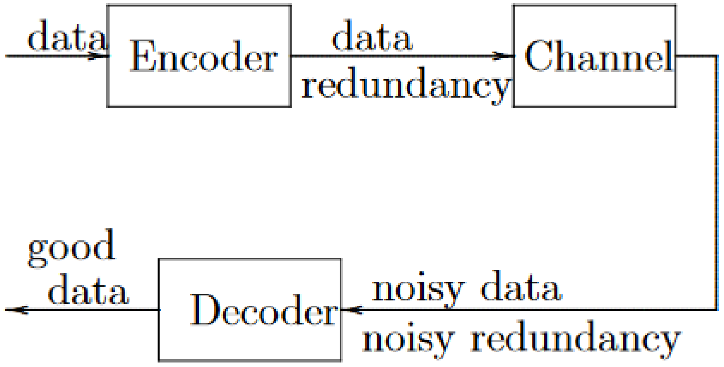
- ECC Mapping
- DRAM Device to Symbol Mapping
- Hardware Managed ECC History Mechanism
- ECC Syndromes
- Enabling and Configuring DRAM ECC

Error Correcting Codes

- DRAM is protected by an error correcting code (ECC). The memory controller supports multiple error correcting codes. Each error correcting code features an ECC word formed by a symbol based code.
  - The x4 code uses thirty-six 4-bit symbols to make a 144-bit ECC word made up of 128 data bits and 16 check bits
  - The x8 code uses eighteen 8-bit symbols to make a 144-bit ECC word made up of 128 data bits and16 check bits.

DRAM ECC features are enabled and configured

via UMC::CH::EccCtrl.



Error Correcting Codes - chipkill

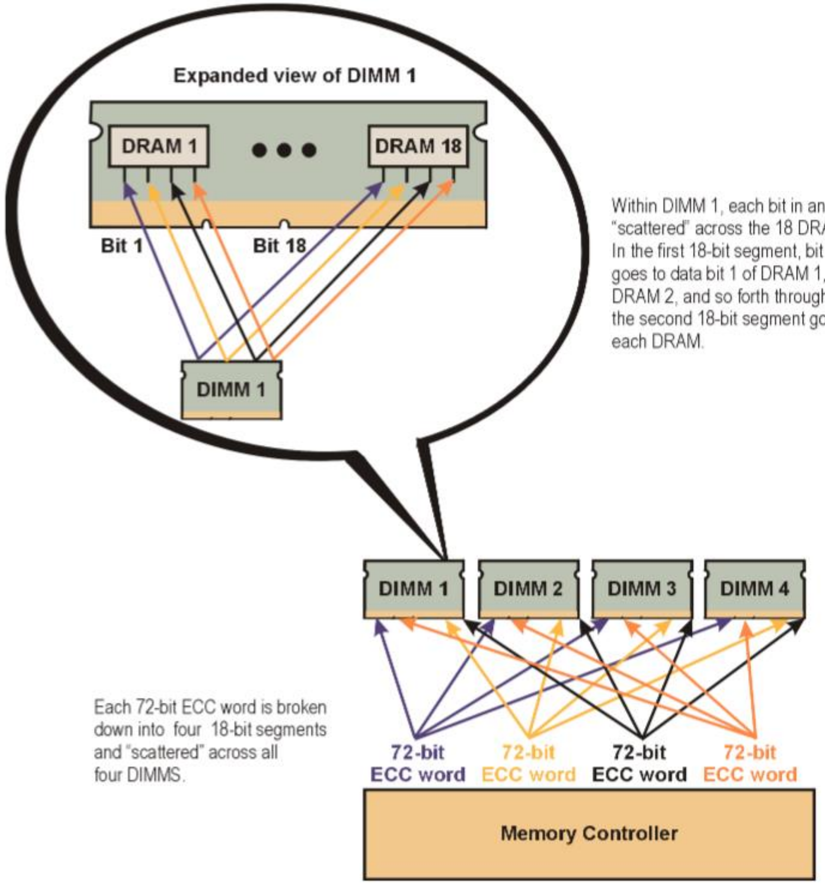
- In certain configurations, the ECC provides DRAM single device data correction, known as “chipkill" functionality; all single symbol errors caused by a failed DRAM device are corrected.

- Chipkill is only possible when indicated by UMC::CH::UmcCapHi[EccChipKillCap].

- For chipkill functionality, the symbol size must be at least twice the DRAM device width and bit interleaving must be enabled via UMC::CH::EccCtrl. For example, for a system configured with x4 devices, x8 symbols are necessary so that the failure of one device can be corrected since the device contributes 8 total bits of data confined to one symbol.

Error Correcting Codes - chipkill

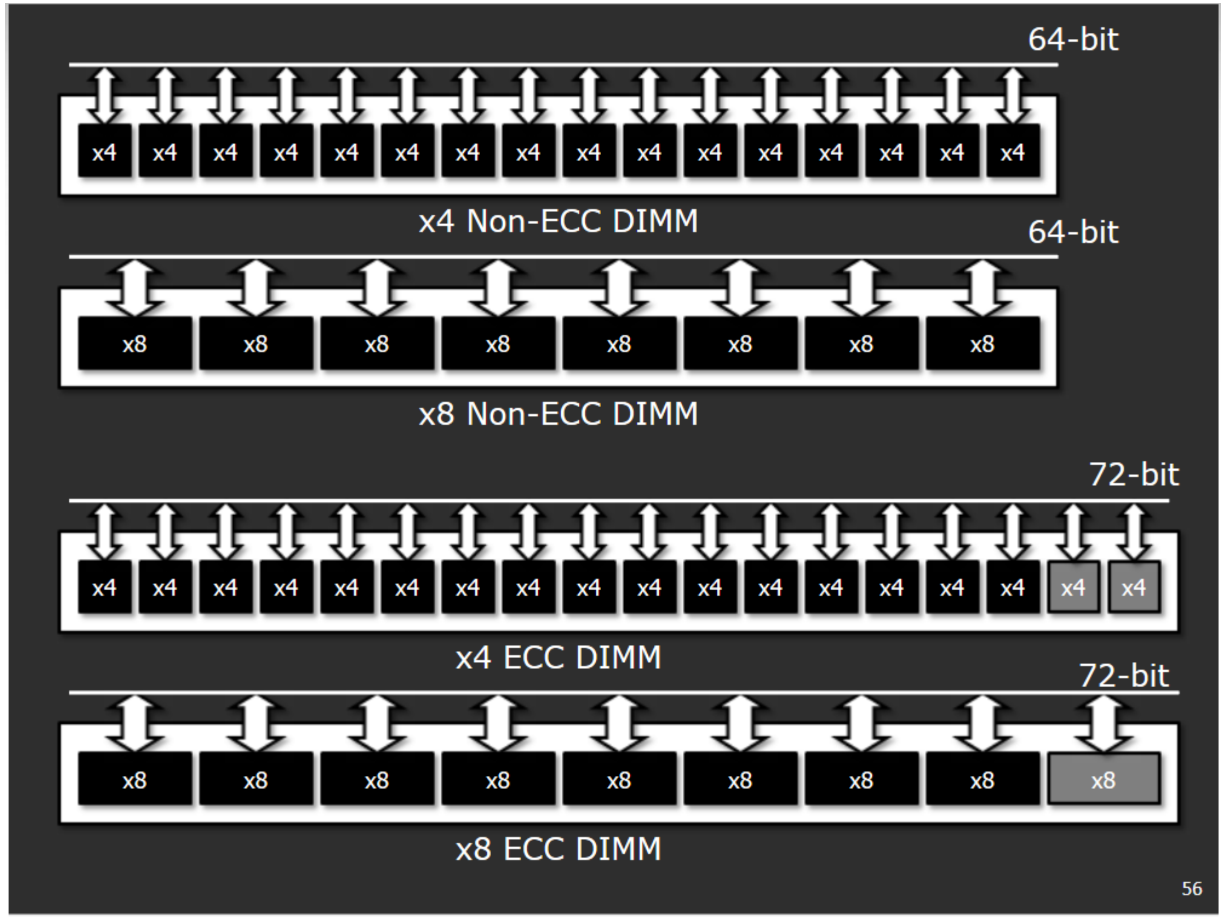
- As DRAM devices become more dense, the per-centage of errors that result in multibit failure increases. Chipkill correct is the ability of the memory system to withstand a multibit failure within a DRAM device, including a failure that causes incorrect data on all data bits of the device.



Within DIMM 1, each bit in an 18-bit segment is "scattered" across the 18 DRAMS on the DIMM. In the first 18-bit segment, bit 1 (shown in blue) goes to data bit 1 of DRAM 1, bit 2 to data bit 1 of DRAM 2, and so forth through bit 18. Each bit of the second 18-bit segment goes to data bit 2 of each DRAM.

Each 72-bit ECC word is broken down into four 18-bit segments and "scattered" across all four DIMMS.

DIMM without/with ECC support


64-bit
x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4
x4 Non-ECC DIMM
64-bit
x8 x8 x8 x8 x8 x8 x8 x8
x8 Non-ECC DIMM
72-bit
x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4 x4
x4 ECC DIMM
72-bit
x8 x8 x8 x8 x8 x8 x8 x8 x8
x8 ECC DIMM
56

Error Correcting Codes

ECC Mapping

- To understand the effects of configuration on DRAM device errors, the ECC must be mapped to the physical memory configuration, including device width and bit interleaving.

  - DRAM device width refers to the number of bits sourced simultaneously from a single memory chip. For example, a x4 device contributes 4-bits to the ECC word on each beat of data. Eighteen devices, representing one rank, contribute 72-bits on each beat.

  - Bit interleaving refers to the way bits from the two memory beats are organized to form an ECC word. When specified, even and odd bits from the two 72-bit beats can be interleaved to create a 144-bit ECC word.

    When bit interleaving is enabled, a partially failing device (e.g., pin failure) contributes two incorrect bits to the same symbol.

    When bit interleaving is not enabled, a partially failing device contributes failures to two different symbols.

Error Correcting Codes

ECC Mapping – How ECC correct and detect

- 我們把每一小塊編號為1,2,⋯,7,然後假設原來傳1101,依序把它寫在編號1,2,3,4的空格上,然後多加三個bits上去，讓每個圓圈裡面1的個數是偶數
- 所以加進去的三個bits是010,最後要傳的是1101010
- 假設第6個bit錯了,1變成0,如圖3.3a
- 假如是錯第3個bit，其他都對,如圖3.3b,那麼A有3個1有問題,B有4個1,沒有問題,C有3個1,也有問題,所以我們就可以找到3這個位置

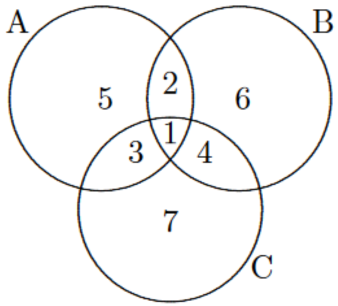


圖 3.1

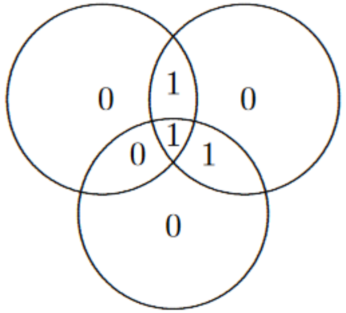


圖 3.3a

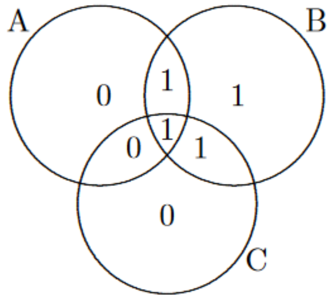


圖 3.2

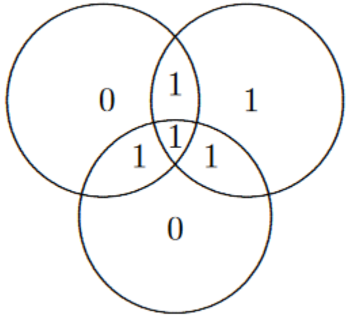


圖 3.3b

Error Correcting Codes
ECC Syndromes

- The syndrome field uniquely identifies the failing bit positions of a correctable ECC error.
- Only syndromes identified in Table 41 [x8 ECC Correctable Syndromes] are correctable by the error correcting code.

  Symbols 07h-00h map to data bits[63:0];

  Symbols 0Fh-08h map to data bits[127:64];

  Symbol 10h maps to special purpose non-data bits;

  Symbols 12h-11h map to ECC check bits for data bits[127:0] and symbol 10h.

  For details to check the which bit of symbol failed, please refer to mapping PPR section.

Software-managed Bad Symbol ID

- x8 ECC can be further augmented by a software managed algorithm to provide coverage against two symbol errors in the same ECC word by using error information across cache lines.

- Hardware uses the information that a symbol is bad as follows:
  - ➢ If an ECC word has a correctable error only in a rank and symbol identified by this register, then the error is a correctable error.
  - ➢ If an ECC word has an error in a rank identified by this register, but a different symbol, then the word is presumed to have at least two symbol errors and the error is treated as uncorrectable.

Bad Symbol ID can be enabled using UMC::CH::EccCtrl[EccBadDramSymEn] and configured using the UMC::CH::EccBadSymbol registers. There is one register per DRAM rank. The lowest-addressed register is for DRAM rank 0, the next lowest-addressed register is for DRAM rank 1, etc.

DRAM Scrubbers

- 它是指從每個電腦記憶體位置讀取資料、以一種錯誤糾錯碼（ECC）糾正位元錯誤（如果存在），然後將校正後的資料寫回到相同位置
  Scrubbers are used to periodically read cacheline sized data locations and associated tags. First, scrubbing corrects any correctable errors which are discovered before they can possibly migrate into uncorrectable errors.

  - Periodic Scrubber
    Periodic scrubber ensures that all cachelines in DRAM memory are periodically read and, if correctable errors are discovered, they are corrected.

  - Redirect Scrubber
    The redirect scrubber scrubs DRAM by issuing a writeback to a DRAM address accessed during normal operation. These scrubs are used to correct single bit correctable errors in a cache line.

Corrected Error Counters

- DRAM error counters increment on detection of a corrected ECC error. One error counter per chip select is implemented. Each counter is 16 bits. Each counter stops and latches at a count of FFFFh. The individual counters must be written to a non-FFFFh value by a handler to clear the event.

- Each counter can be configured to generate an interrupt when transitioning from FFFEh => FFFFh. Each counter is capable of generating: no interrupt, an APIC-based interrupt, or SMI.

Error Injection

- When performing error injection on multi-node systems, the registers must be programmed on the die and memory controller to which the memory is attached. Both periodic and redirect scrubbing must be disabled during the error injection process.

  ➢Explicitly Addressed Error Injection
  ➢Persistent Error Injection
  ➢One-shot Error Injection

  Error injection is disabled on production parts. Users can perform a secure-unlock procedure with the PSP.

Address/Command Parity Errors

- On server products, the memory controller supports address/command parity to protect data sent on the DRAM address/command bus. When enabled, the memory controller calculates parity on DRAM address and commands and send this to DRAM.

Write Data CRC Errors

- On server products, the memory controller supports a cyclic redundancy check (CRC) to protect data written to DRAM. When enabled, the memory controller calculates CRC on write data and send this to DRAM using two additional data beats. If a CRC error is detected, the DRAM devices notify the memory controller.

Post Package Repair