

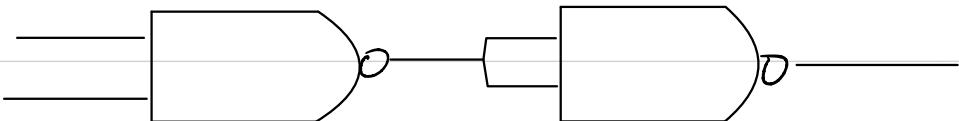
EE477L HW |

Q1)

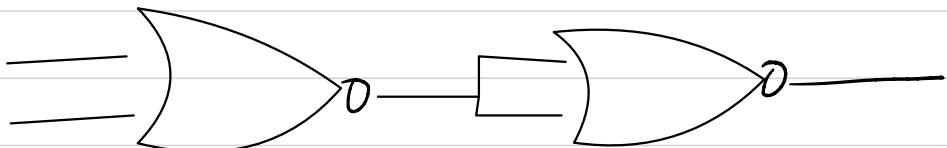
a) The NAND and NOR are called the universal gates because those are the only 2 gates can implement any digital circuit

b).

i). AND gate w/ 2 NAND.



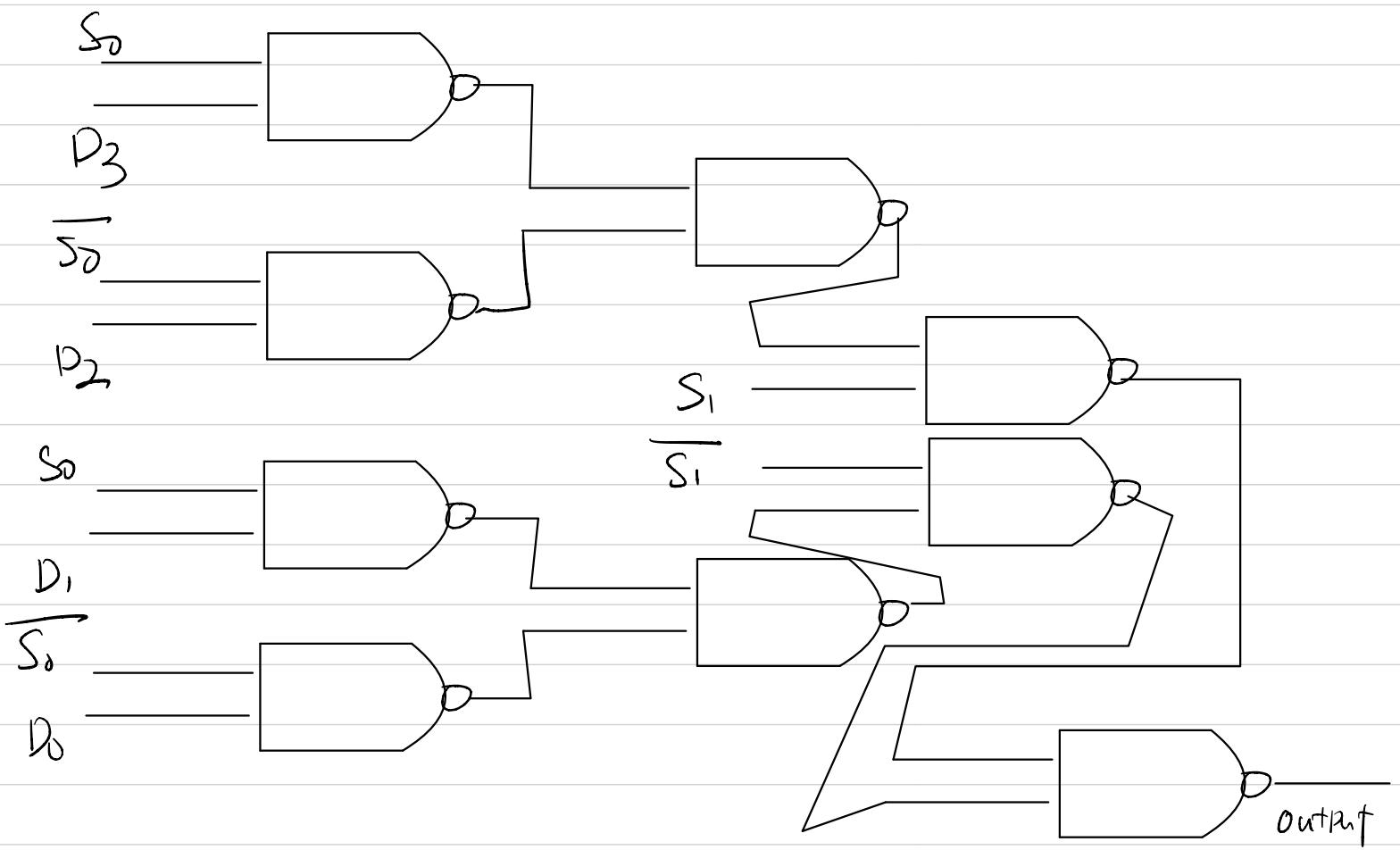
ii). OR gate w/ 2 NOR.



iii) NOT gate w/ NADD.



C)



(Q2).

Combinational logic's output is only based on the input values, and output immediately changes once input changes.

sequential logic get it's output based on both inputs and past sequence, which means a memory part is necessary and new output can be only compute after we got the last output.

But to the question, feedback loops are necessary for sequential logics because it need to store the latest output to the memory while combination logics don't

Q3)

a) Let's first implement AND and OR Gates

w/ NAND and NOT:

$$A \text{ AND } B = \text{NOT}(\text{NAND}(A, B))$$

$$A \text{ OR } B = \text{NAND}(\text{NOT}(A), \text{NOT}(B))$$

Then, XOR:

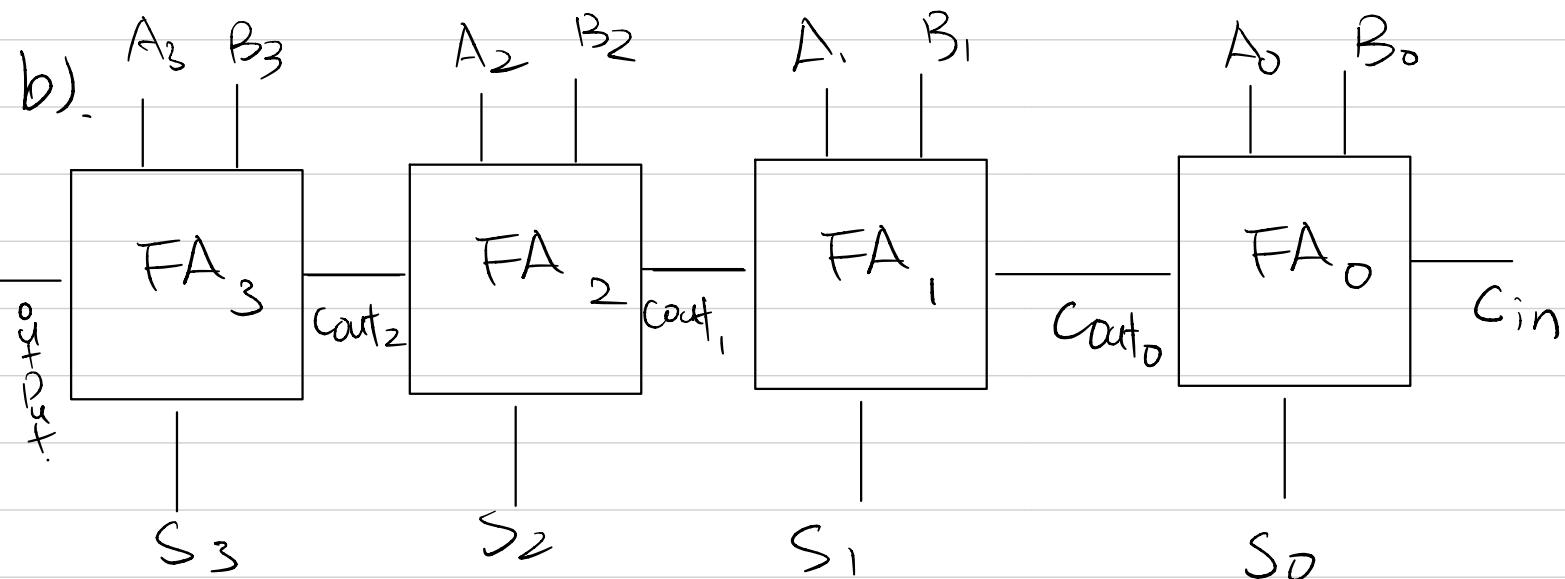
$$A \text{ XOR } B = \text{NAND}(\text{AND}(A \cdot \text{NOT}(B)), \text{AND}(\text{NOT}(A), B))$$

and we can safely assume that $A \text{ XOR } B \text{ XOR } C$

is just $X \text{ XOR } Y$ where $X = (A \text{ XOR } B), Y = C$

therefore, Sum = $A \oplus B \oplus C_{in}$

$$C_{out} = (A \cdot B) + (C_{in} \cdot (A \oplus B))$$



C)

$$\text{AND Gate delay: } 1 + \frac{4}{3}d = \frac{7}{3}d$$

$$\text{OR Gate delay} = \frac{4}{3}d + 1 = \frac{7}{3}d$$

$$\text{XOR Gate delay} = \frac{4}{3}d + \frac{7}{3}d = \frac{11}{3}d.$$

$$\text{Sum delay} = 2 \times \frac{11}{3}d = \frac{22}{3}d.$$

$$\text{Cout delay} = \frac{4}{3}d + \frac{4}{3}d + \frac{4}{3}d + \frac{7}{3}d = \frac{19}{3}d$$

so the critical path delay would be $\frac{22}{3}d$.

Q4).

Synchronous system is more popular because

it's easier to design and would potentially reduce issues caused by signal integrity and glitches,

it's also easier to predict and would make verification process easier.

$$T_{PLL} = \frac{1}{2Gf_2} \times 5 = \frac{1}{10 \text{ GHz}} = \underline{\overline{0.1 \text{ ns}}}$$

Q5).

In CMOS design, we use NMOS as PDN and PMOS as PUN because different MOS Part performs different when gate to source voltage is different

This setting can minimize Power consumption
(i.e. with NMOS, if we use it as PDN,
then we need a 10V source on a 5V vdd,
else, if NMOS used as PUN, then we
only need a 5V source on a 5V vdd.)

Q 6).

1) design PON:

For $(A+B+C) \cdot (E+F)$, either $A+B+C$ must be low, or $E+F$ must be low

For G, H, one of them need to be low.

∴ use 3 NMOS in parallel for A, B, C

use 2 NMOS parallel for E, F, directly after $A+B+C$

use 2 NMOS for G, H and connect them directly after $(A+B+C) \cdot (E+F)$.

design PUN:

For $(A+B+C) \cdot (E+F)$, either $A+B+C$ must be high, or $E+F$ must be high.

For G, H, one of them need to be high.

∴ use 3 PMOS in series for A, B, C

use 2 PMOS in series for E, F. Connect directly after $(A+B+C)$

use 2 PMOS in series for G, H, connect directly after $(A+B+C) \cdot (E+F)$

2) width of the pmos should be

$$W_P = 3 \times W_N \text{ with } \beta = 3.$$

Q7).

1) Using only NMOS:

Pros: easy to design, less transistor used, cheaper

Cons: NMOS can only pull the output respect to Gnd
Voltage may drop
can't minimize the input voltage.

2) Using only PMOS,

Pros: Better Performance

Can pull Voltage from both Vdd and Gnd

Cons: expensive
hard to design

Q8).

a) Power Consumption is the rate at energy used, measured in Watts.

Energy consumption is the total amount of energy used, measured in Joules,

relationship would be: Energy = Power \times Time.

b) No, most energy-efficient design is not necessary for power-efficient.

$$C). I = \frac{V}{R} = \frac{1V}{1500 \Omega \text{ms}} = 0.000667 A$$

$$P = I^2 R = 0.667 \times 10^{-3} \times 1500 = \boxed{1 \text{mW}}$$

Q9).

without pipeline :

stage 1 \rightarrow stage 2 \rightarrow stage 3 \rightarrow stage 4

speed : $n \times T$

with pipeline

stage 1 \rightarrow stage 2 \rightarrow stage 3 \rightarrow stage 4

stage 1 \rightarrow stage 2 \rightarrow stage 3 \rightarrow

stage 1 \rightarrow stage 2 \rightarrow

stage 1 \rightarrow

Speed: $T + 1$.

overheads: w/ Pipeline would increase the design

complexity significantly, But it helps the execution

time

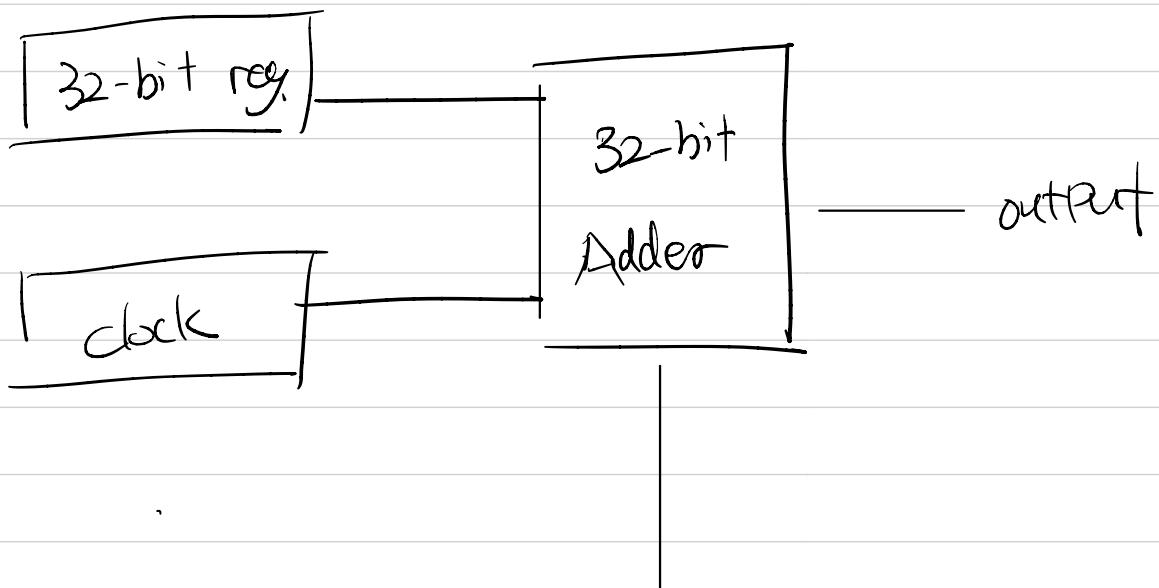
b). with 4 stages, Let's denote T as time needed for each stage , and N as number of output we need to compute .

$$\text{Non-Pipeline delay} = N \cdot 4T.$$

$$\text{Pipeline delay} = (N+3)T.$$

Q10).

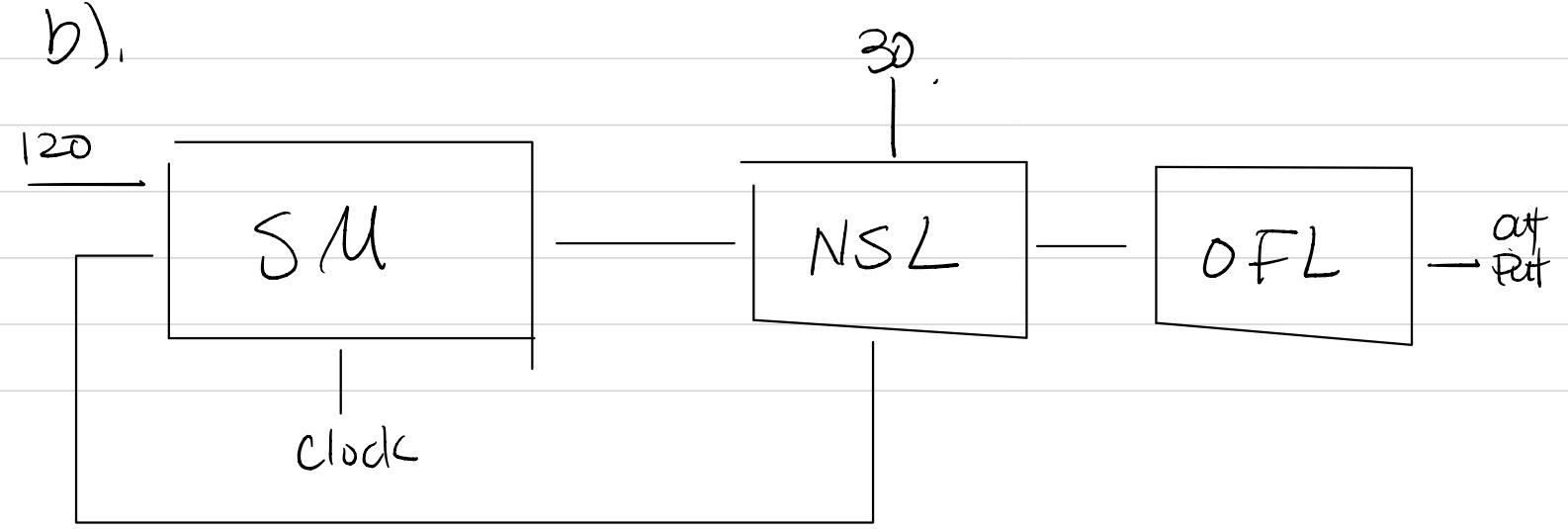
a)



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Note that we need to init. the 32-bit reg to 120.

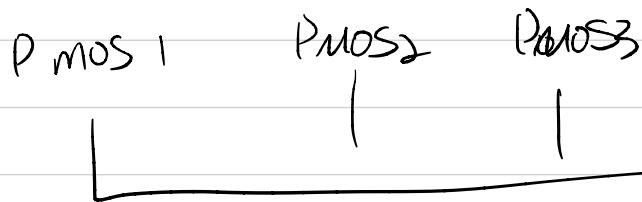
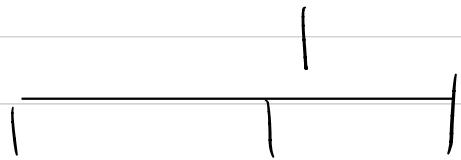
b).



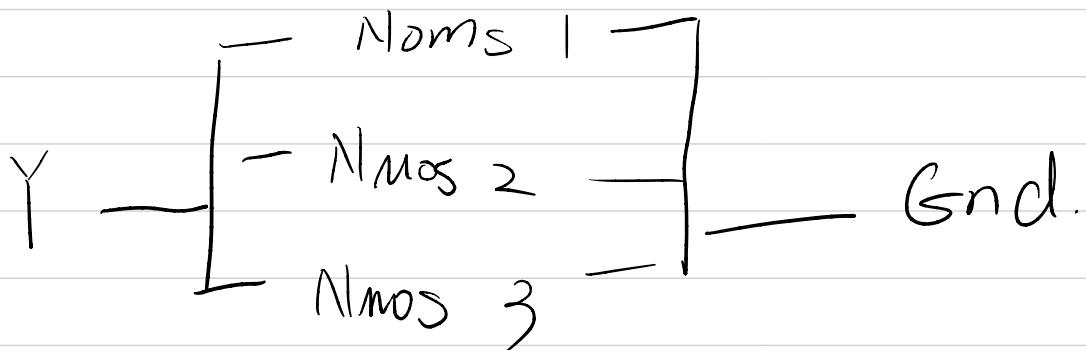
Q11).

Pmos region:

Vdd



Nmos region.



Given input = 111

for Nmos, since $V_{tn} > 0V$,

All Nmos transistors = ON = 1

for Pmos, since $V_{GS}(0V) > V_t$,

All Pmos transistors = OFF = 0

Q 12).

with moore's law.

chip size decreases each years

on the main while, # of transistor
and dram capacity increases

maximum clock freq. increase

minimal supply voltage decreases and
maximum power dissipation increase.

for freq. and voltage , as years passed, freq.
tend to increase (GHz) and Vdd tend to
decrease .

the cost for a single transistor decreases

