

## EE477L Lab3 part2

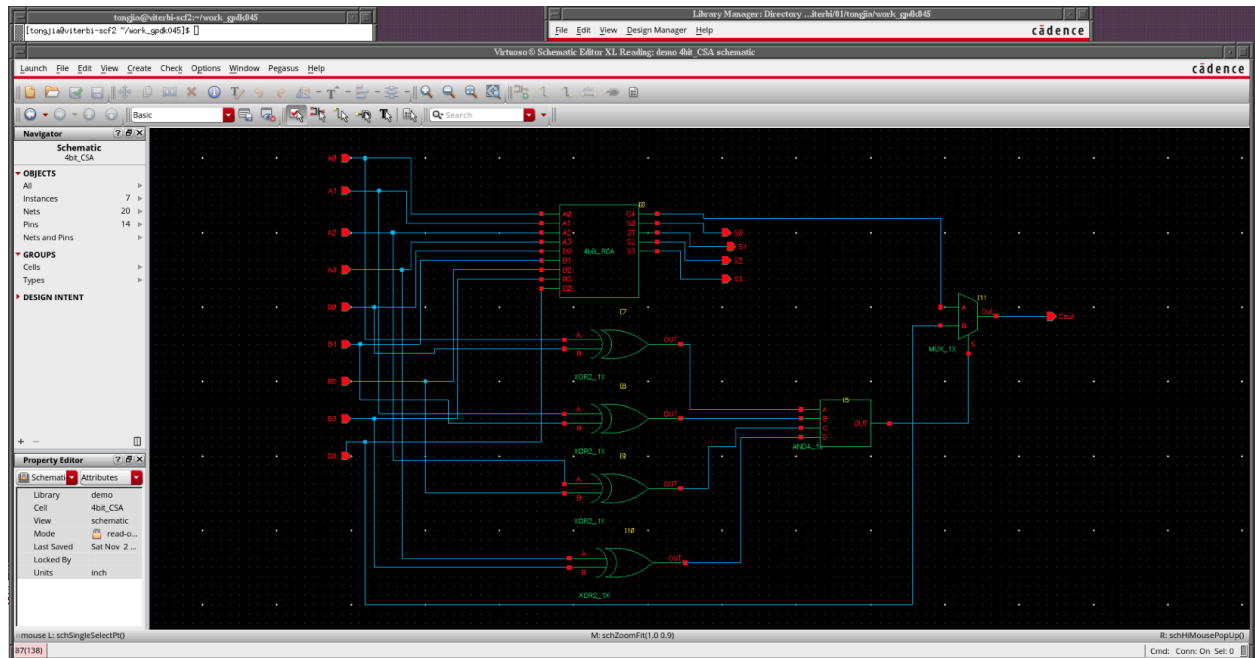
Tong Jia

4035791621

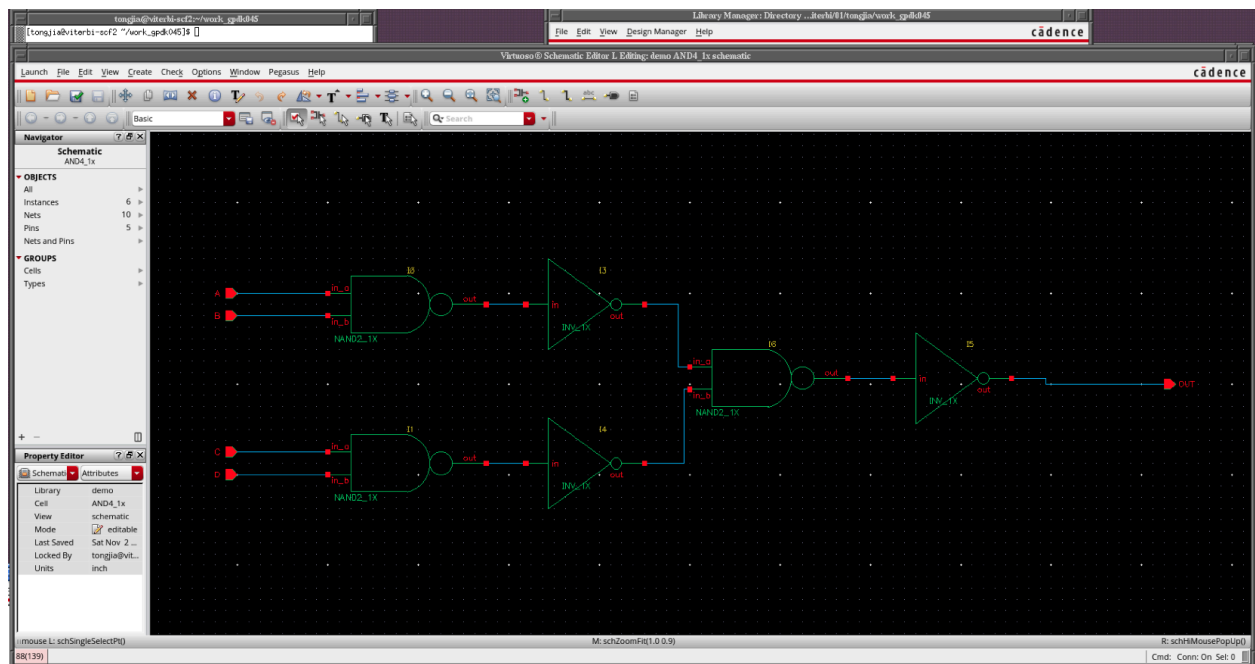
[tongjia@usc.edu](mailto:tongjia@usc.edu)

### STEP 2:

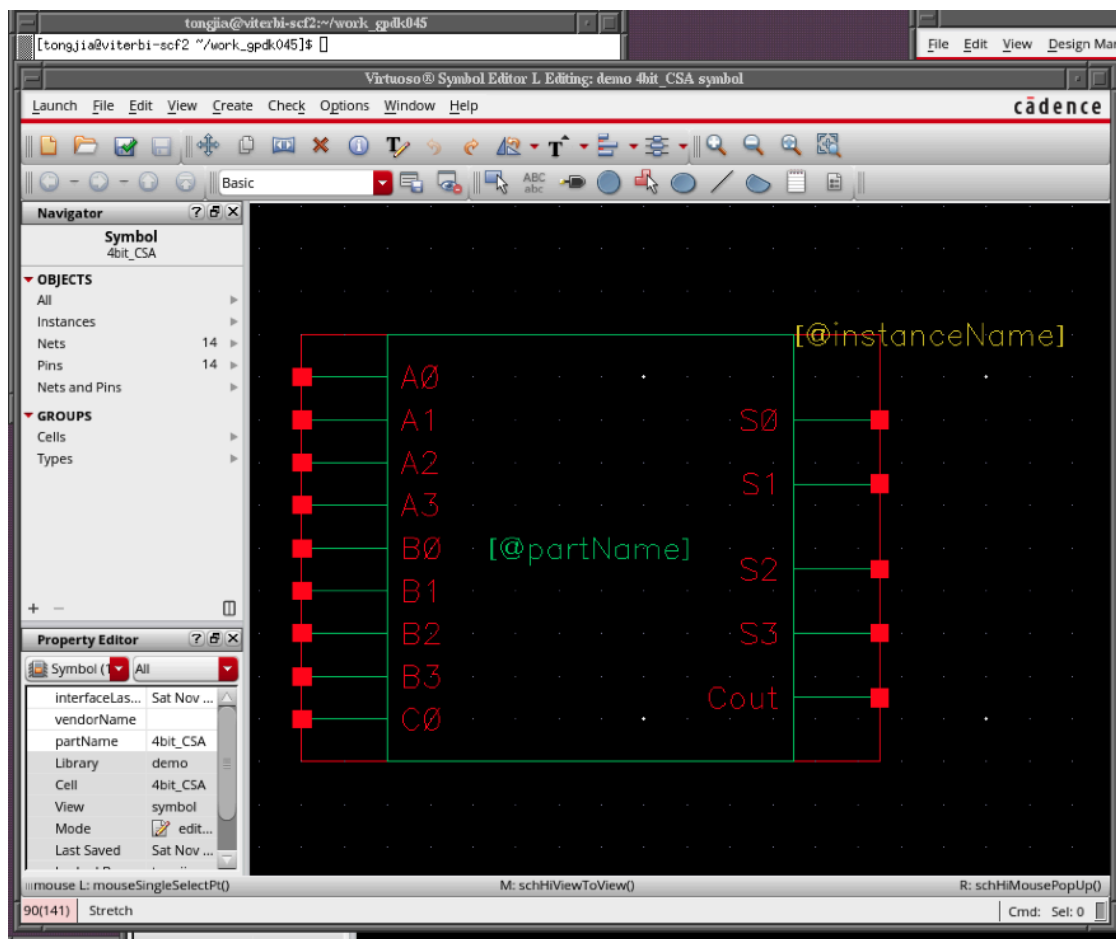
4-bit carry skip adder schematic:



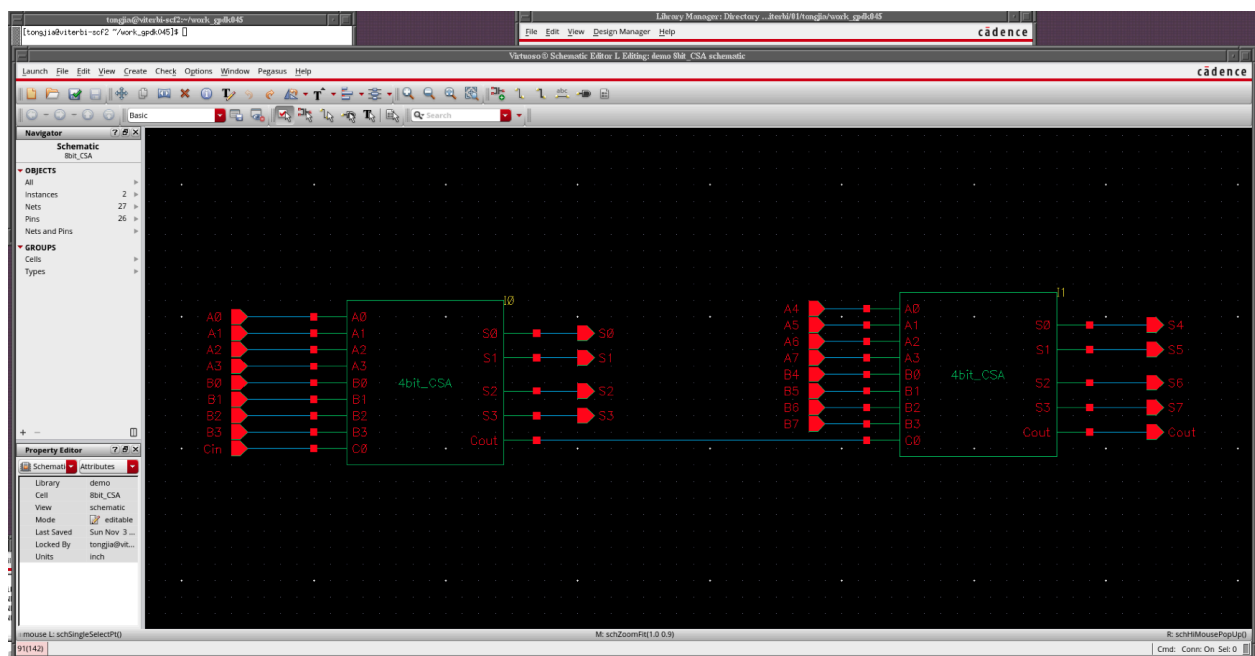
I implemented a new 4-input and gate(AND4\_1x), schematic:



4-bit carry skip adder Symbol:



8-bit carry skip adder (using two 4-bit RCAs) schematic:



### STEP 3:

test input pattern and expected result

#	A	B	Cin	Cout	Sum
0	00	00	0	0	0
1	20	30	0	0	50
2	1D	55	1	0	73
3	00	E5	1	0	E6
4	90	20	0	0	B0
5	FF	FF	0	1	FE

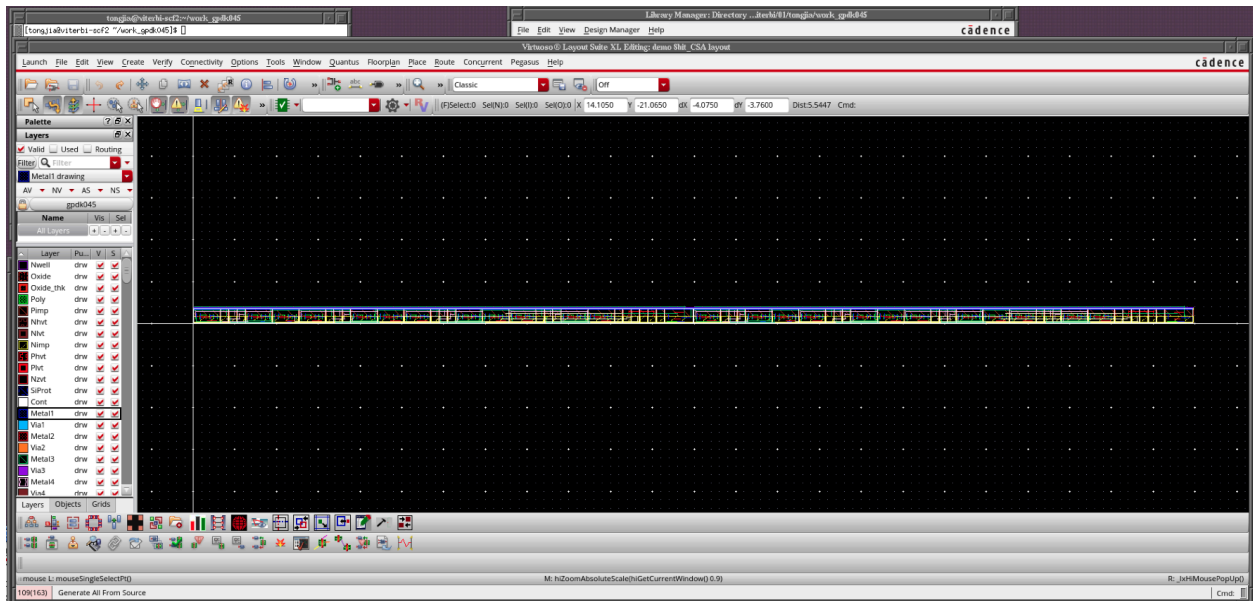
functionality verification waveform:



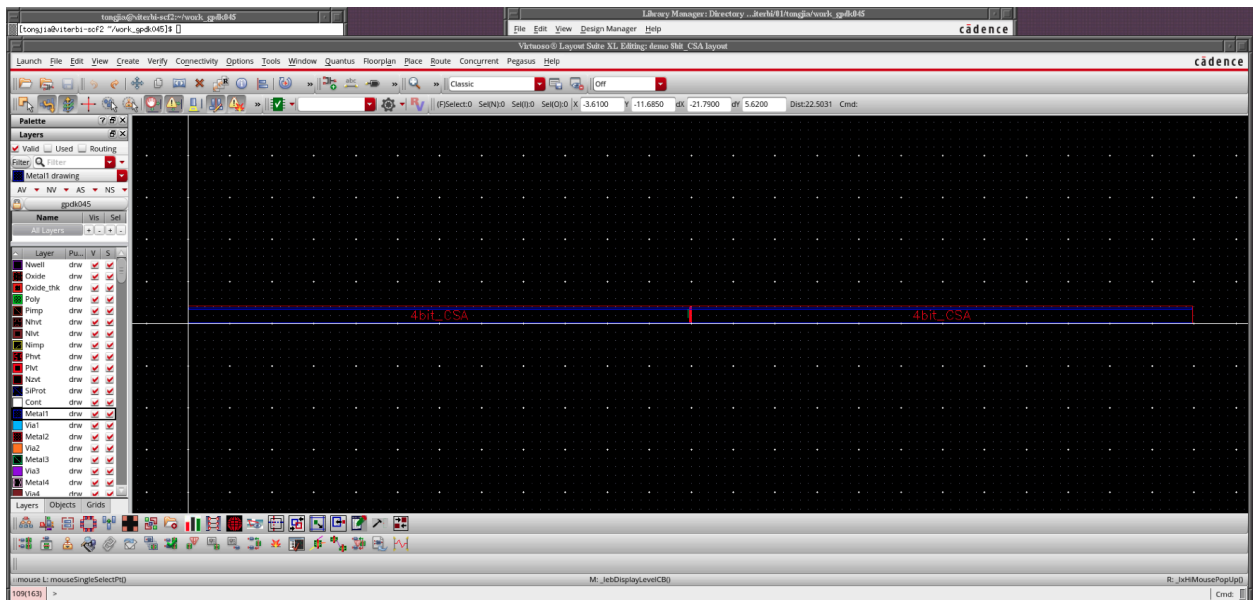
critical path would be from A0 or A1 to Cout

## STEP 4:

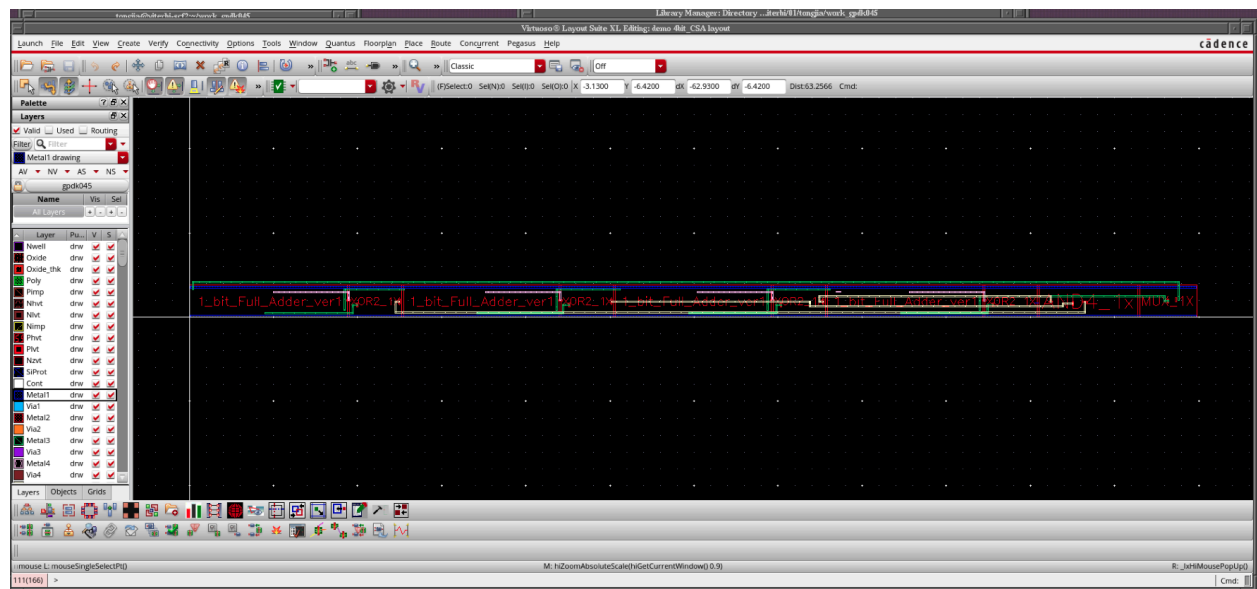
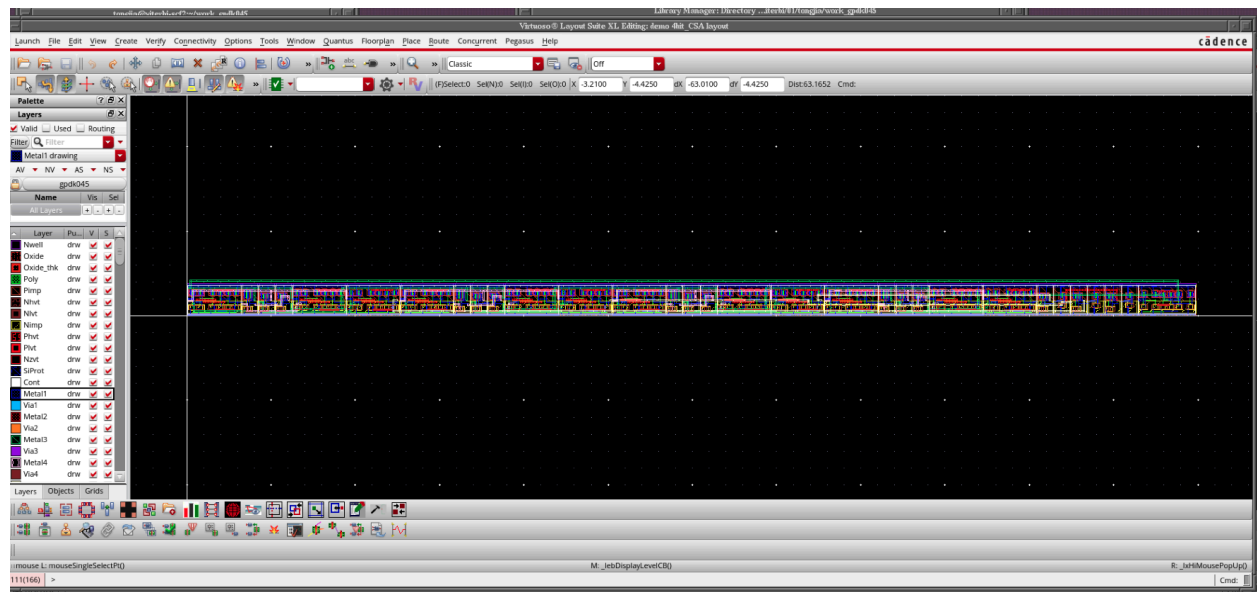
8-bit carry skip adder layout:



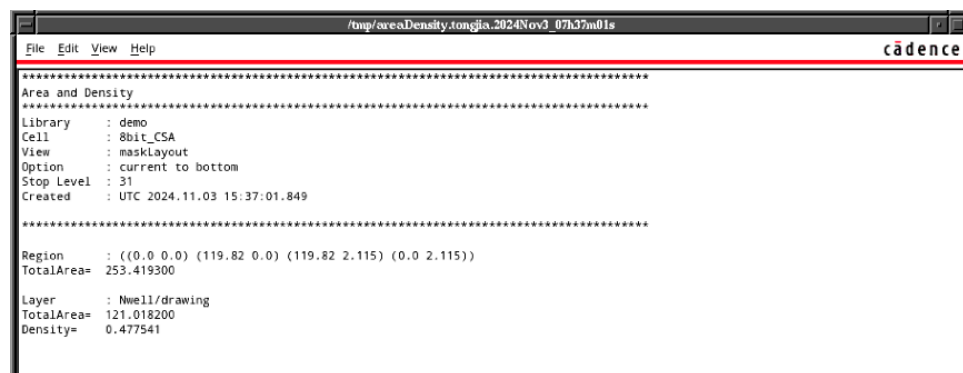
Or



```
(ps: 4 bit CSA layout)
```



AREA = 253.42



DRC:

The screenshot displays the Cadence Pegasus 22.21-64b interface. The left pane shows the DRC (Design Rule Check) results, indicating that the rule set '8bit\_CSA' was completed with no violations. The right pane shows the 'DRC Summary' table, which is currently empty, indicating zero violations. The bottom status bar confirms 'Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.'

Left Pane (DRC Results):

```
INFO: Rule 8SD_8_2 completed with no violations, 562/562
INFO: Status: Runset 100% complete as of 2024-11-03 07:41:45 Elapsed: 00:00:03
INFO: Worker: Active CPUs Total Mem(MB) Active Mem(MB) CPU time(s)
0: 1/1 23 10 1
INFO: Status: Finishing as of 2024-11-03 07:41:45 Elapsed: 00:00:03 CPU time(s)
INFO: Resource usage by worker at exit:
Worker: CPU Elapsed CPUs CPU Peak Peak engine
time(s) time(s) Allocated usage(%) Memory(MB) Memory(MB)
0: 1 3 1 64.31 23 10
Worker resource usage summary: Total CPU(s): 1 Run duration(s): 3 Max peak
Worker CPU utilization summary: 1 of 3 available CPU seconds (33.33%) with 1
Generating summary in /home/viterbi/01/tongjia/work_gpd045/DRC/8bit_CSA.sum
INFO: All selected rules completed
INFO: Total CPU Time : 2 (s)
Total Real Time : 3 (s)
Total Original Geometry : 581(13250)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
ASCII report database is /home/viterbi/01/tongjia/work_gpd045/DRC/8bit_CSA.c
INFO: Checking in all SoftShare licenses.
Pegasus finished normally. 2024-11-03 07:41:45
```

Right Pane (DRC Summary):

Cell/Rule	Color	Count
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Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

LVS:

The screenshot displays the Cadence Pegasus 22.21-64b interface. The left pane shows the LVS (Logic Versus Schematic) results, indicating that the rule set '8bit\_CSA' was completed with no violations. The right pane shows the 'LVS Summary' table, which is currently empty, indicating zero violations. The bottom status bar confirms 'Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.'

Left Pane (LVS Results):

```
#####
# Run Result : MATCH
# Run Summary : [INFO] ERC Results: Empty
# : [INFO] Extraction Clean
#
# ERC Summary File : 8bit_CSA.sum
# Extraction Report File : 8bit_CSA.rep
# Comparison Report File : 8bit_CSA.rep.cls
#####
INFO: Creating cross reference database ...
INFO: Manager summary: CPU(s): 0 Elapsed(s): 0 Peak memory(MB): 79.15
INFO: Checking in all SoftShare licenses.
INFO: Creating cross reference database completed. Sun Nov 3 07:45:07 2024
Pegasus finished normally. 2024-11-03 07:45:07
```

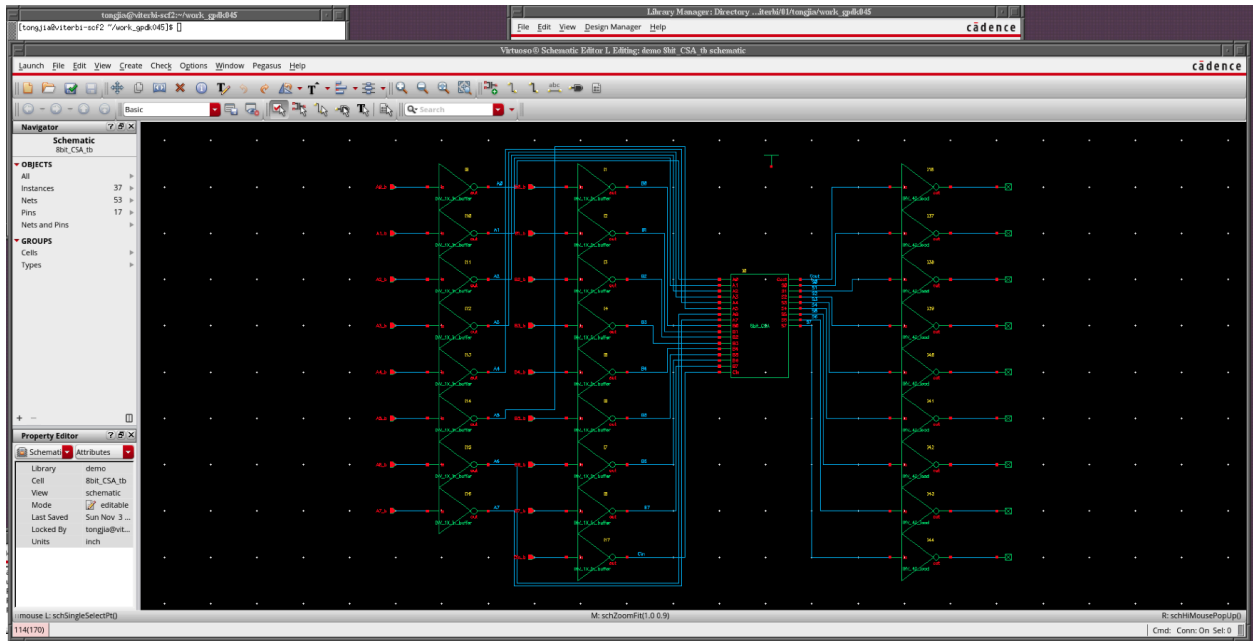
Right Pane (LVS Summary):

Cell/Rule	Color	Count
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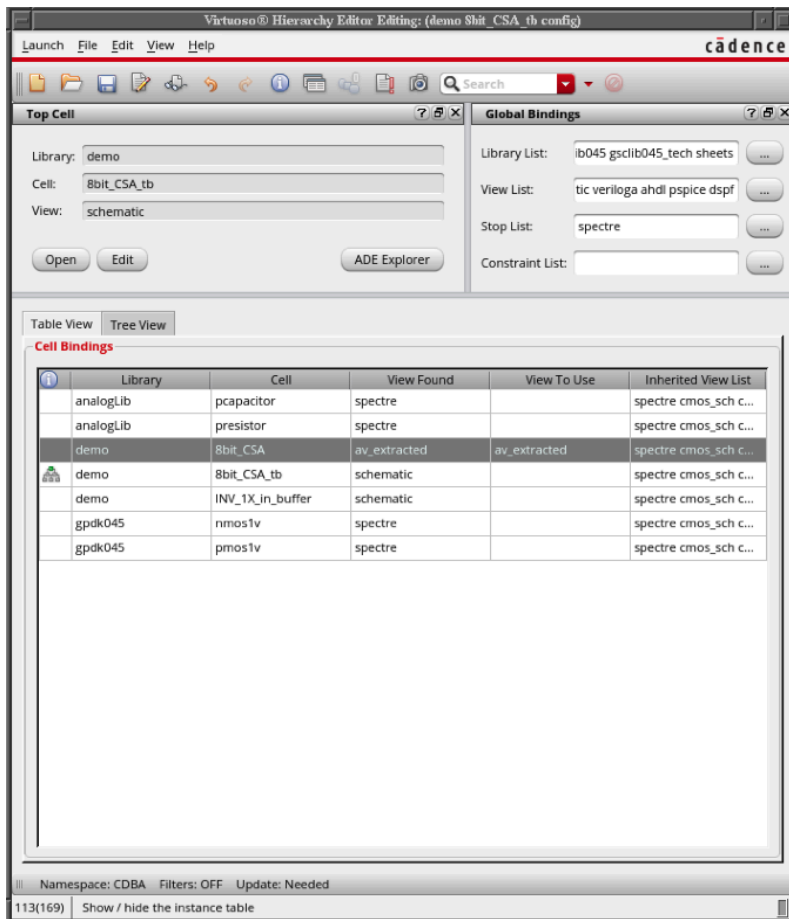
Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

## Post-layout simulation

testbench schematic:



Config:



functionality verification waveform:

