Tong Jia

EE503 HW3

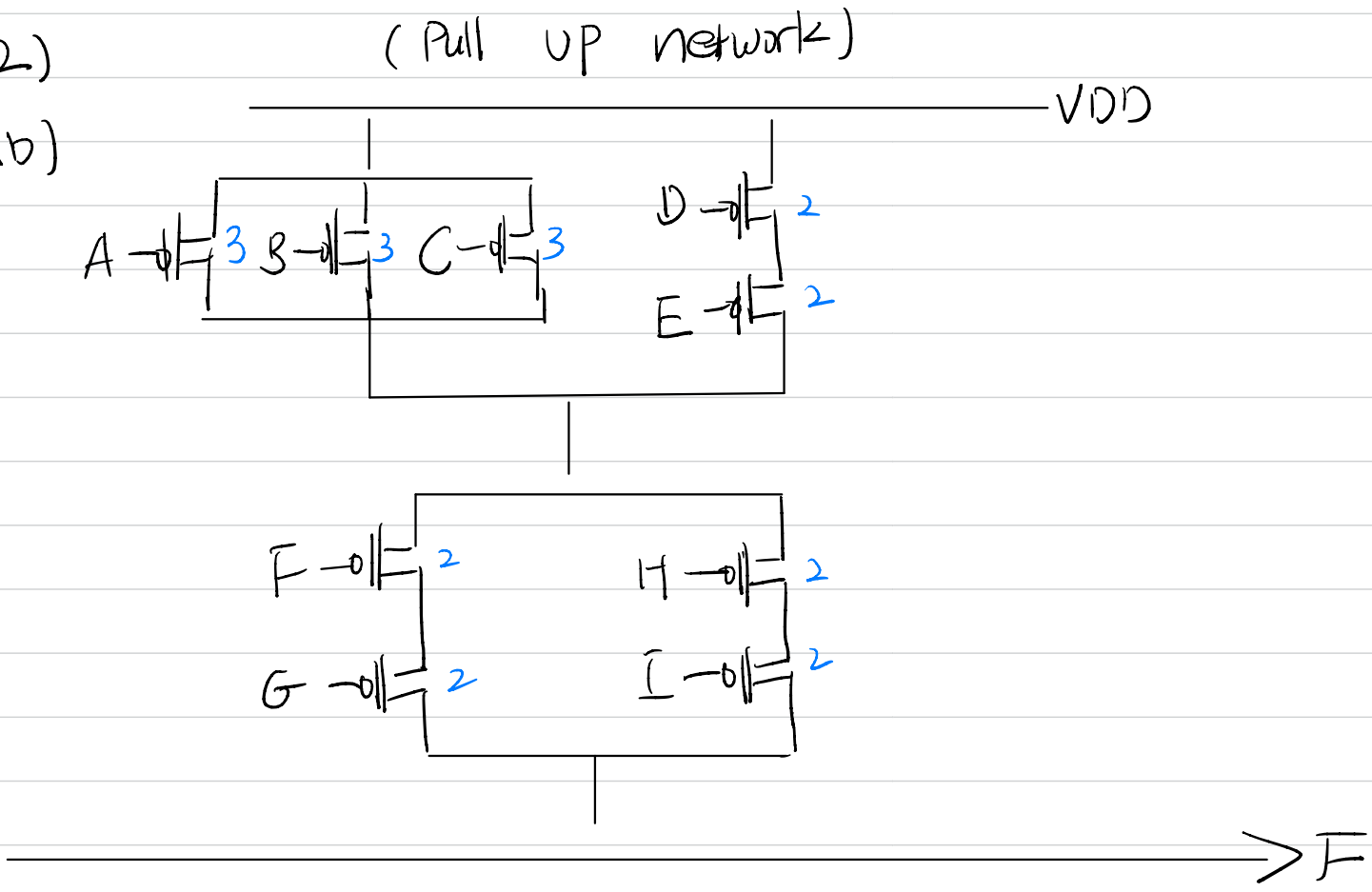
Q1)

a) Design rules are important during the physical design phase because they ensure that the desisned layout adheres to the manufacturing capability and constrains of the fabrication process.

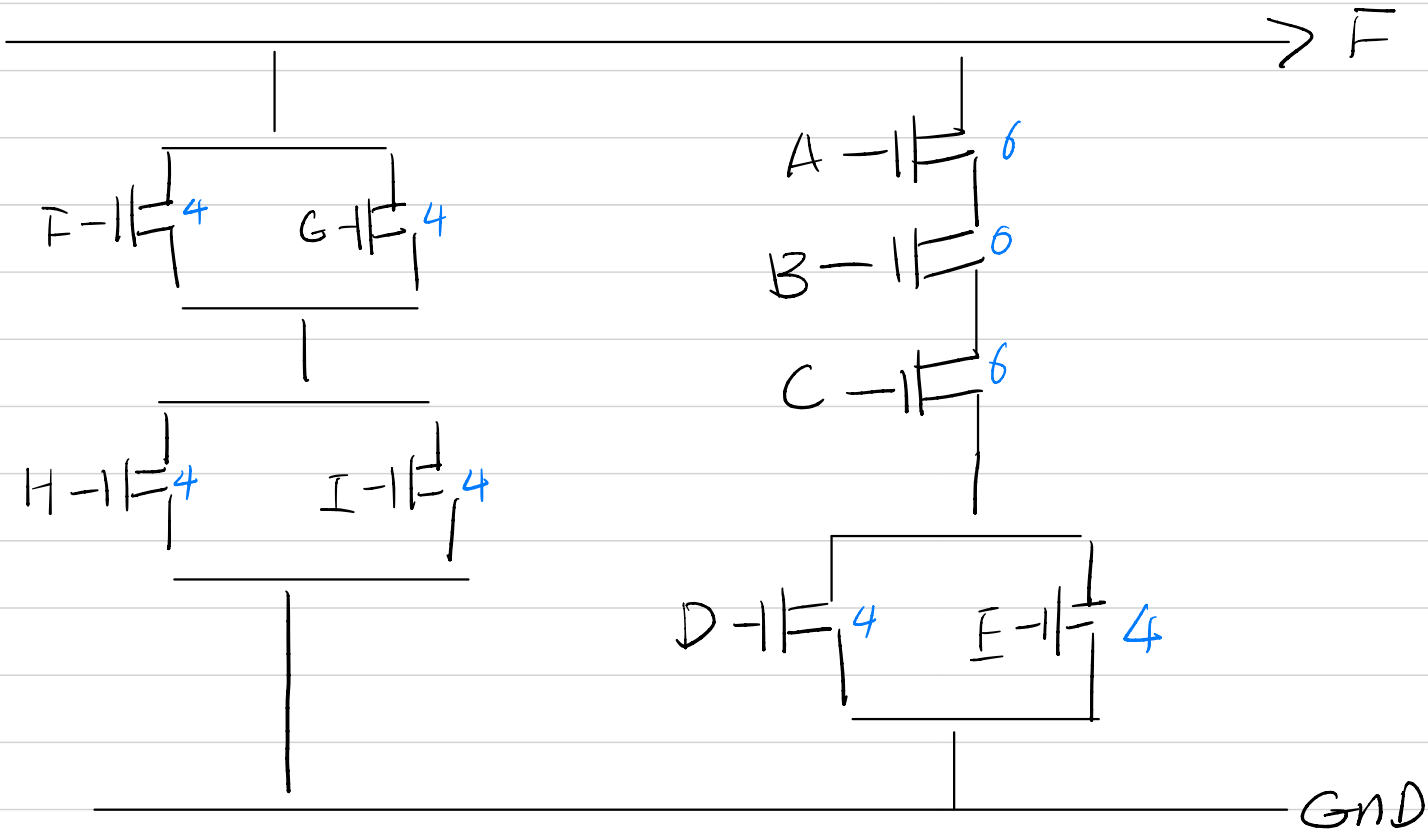
b). Partitioning : creating blocks
Floor Planning : Placement of blocks
Placement : Placing Gates on layout
Routing : wiring.

Q2)

a&b)



(Pull down network)



c)

$$u_n / u_p = R_n / R_p = 2$$

∵ worst case 3 transistor in series in PDN

best case 3 trusister in parallel in PUN

$$3R_n / R_p/3 = 2$$

∴ ratio = 9 x2 :1 = $\boxed{18:1}$

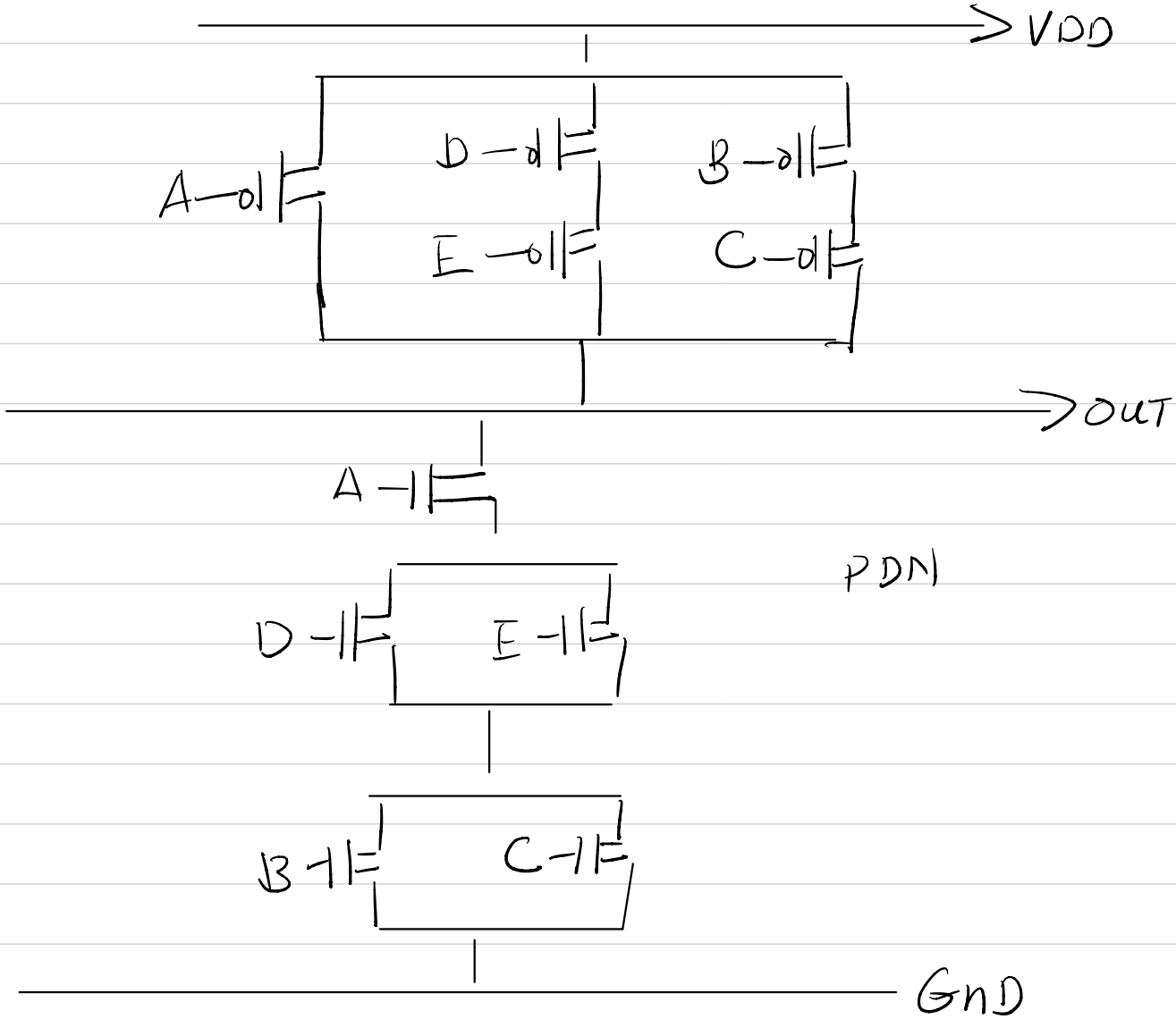
Q3).

Clock Grid: ensures low local skew by using a wide mesh of wires to minimize RC delays

H-trees = provide balanced clock signal paths w/ minimal skew by using a fractal-like structure.

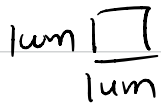
Q4)

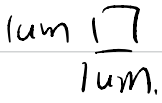
Bool equation: $OUT = \overline{A \cdot (D+E) \cdot (B+C)}$



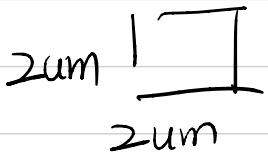
Q5).

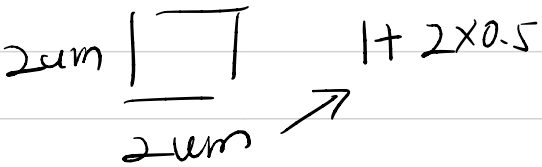
Contact layer



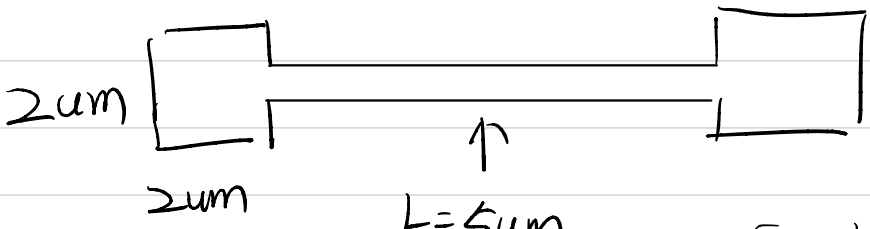


Metal layer



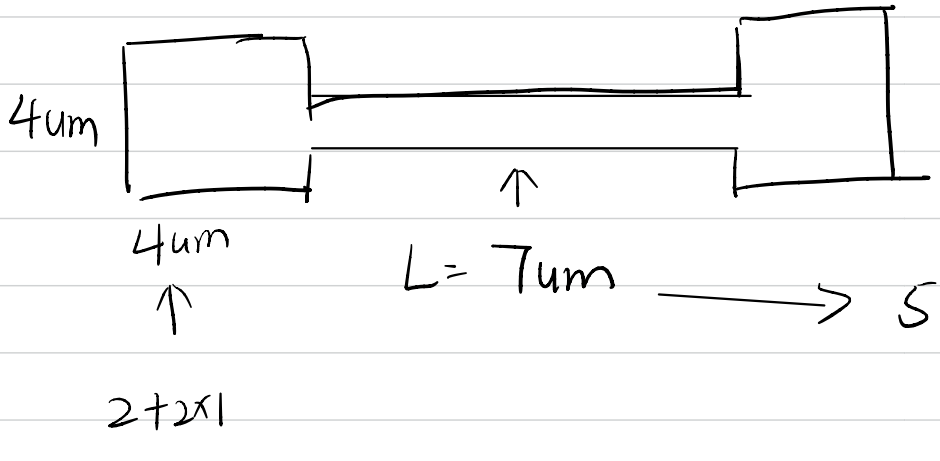


Diffusion layer



→ 500 ohms = 1um X 5um

N-well



Q6).

a) Parasitic cap : occurs when 2 Parts are separated by a dielectric material, causing unintended capacity coupling

Parasitic resistance : occurs from inherent resistance of wires, contacts and diffusion regions due to meterials' resistivity.

b) parasitic cap may slow down transistors and increase power comsumption

Porasitic resistance may lead to voltage drop and power dissipation.