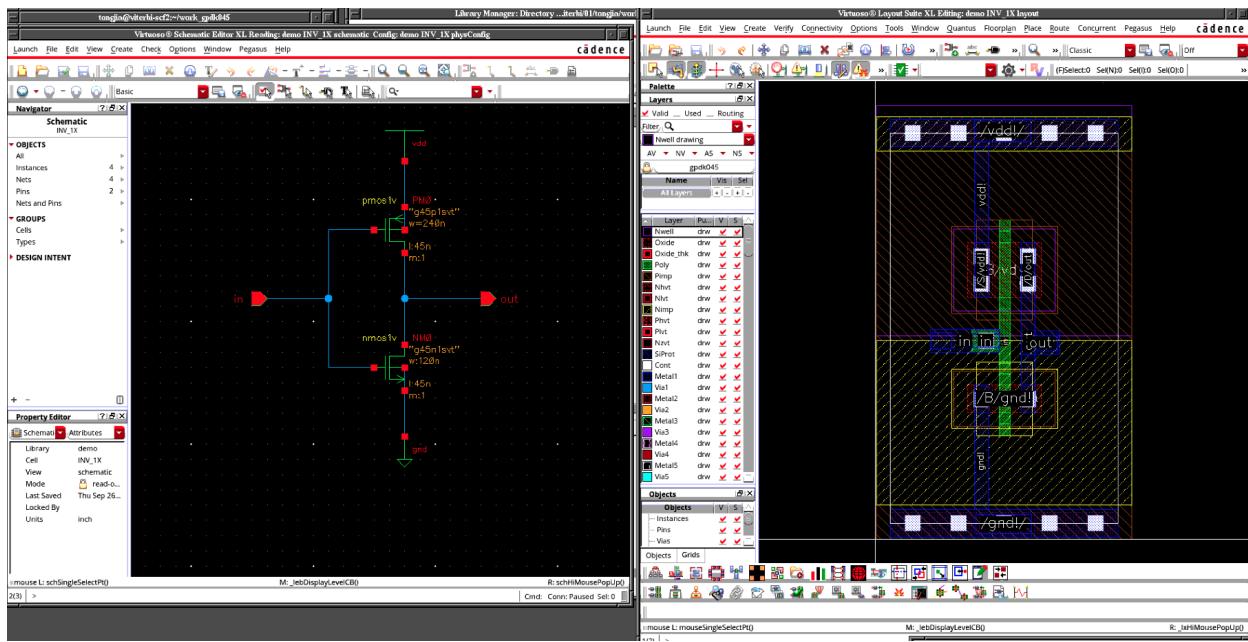


EE407L Lab1 Part2

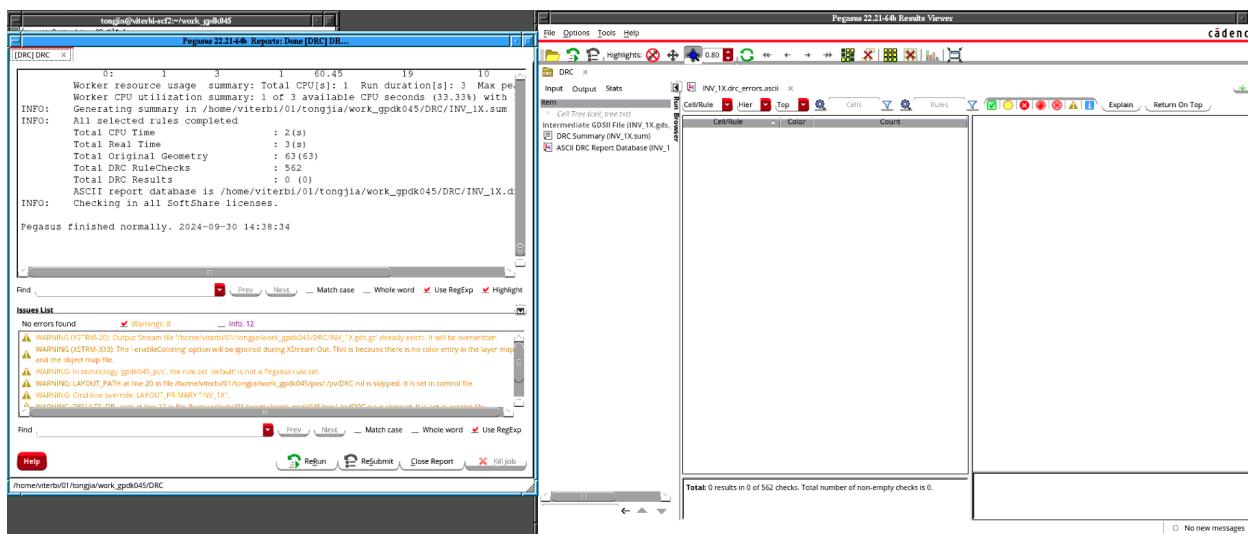
Tong Jia
4035791621
tongjia@usc.edu

Step 3

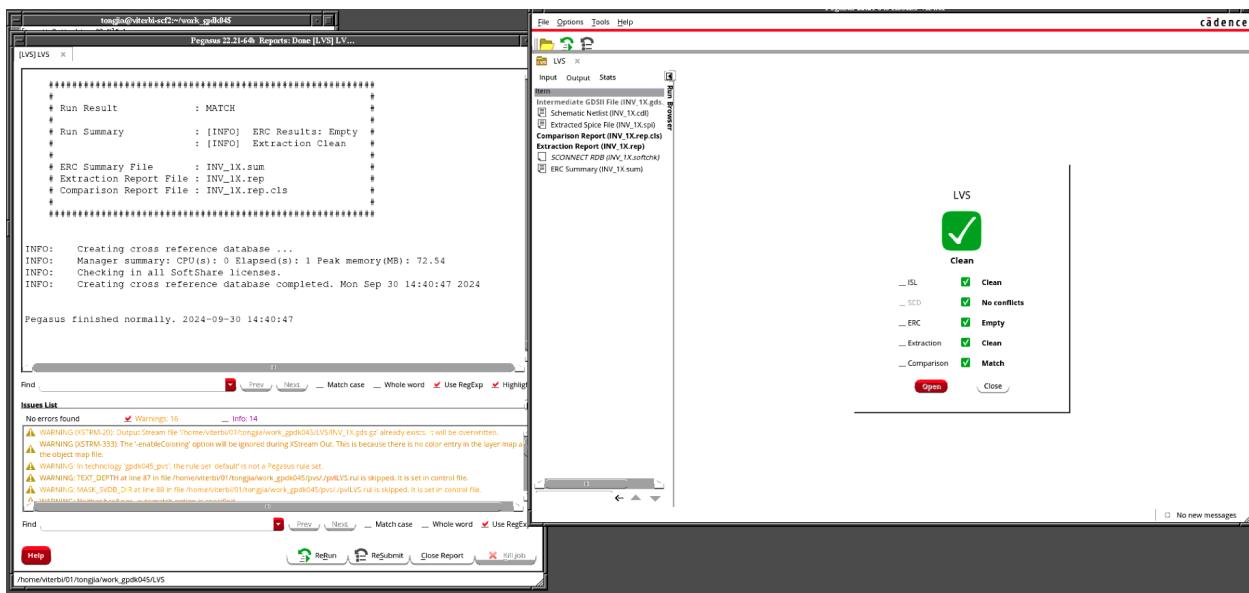
INV_1X:
layout drawing



DRC

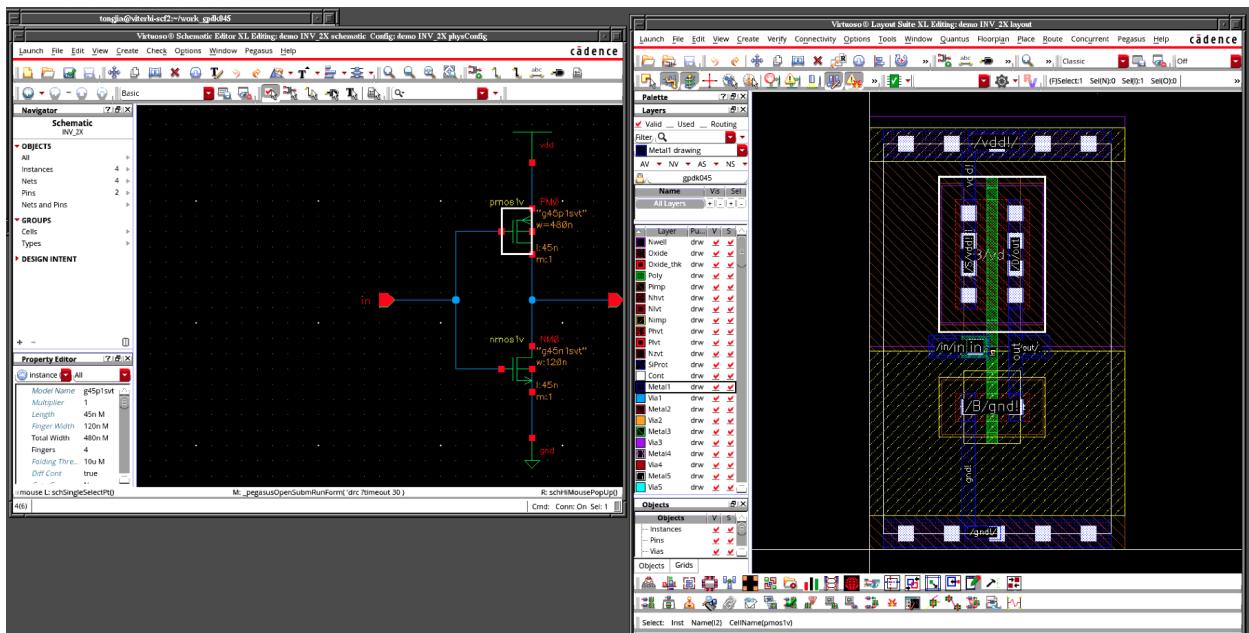


LVS



INV_2X:

layout drawing



DRC

Pegasus 22.21-6b Reports Done [DRC] DR...

```
[LVS]LVS x [DRC]DRC x
INFO: Rule ESD.8_2 completed with no violations, 562/562
INFO: Status: Runset 100% complete as of 2024-09-30 14:56:42 Elapsed: 00:00:03
Worker: Active CPUs: Total Mem(MB) Active Mem(MB) CPU time(s)
  0: 19 19 10 2
INFO: Status: Finishing as of 2024-09-30 14:56:42 Elapsed: 00:00:03 CPU time(s)
INFO: Resource usage by worker at exit:
  CPU   Elapsed CPU Peak Peak engine
Worker: time[s] time[s] Allocated usage[s] Memory [MB] Memory [MB]
  0: 2 3 1 62.75 19 10
Worker resource usage summary: Total CPU[s]: 2 Run duration[s]: 3 Max peak
Worker CPU utilization summary: 2 of 3 available CPU seconds (66.67%) with 1
INFO: Generating summary in /home/viterbi/01/tongjia/work_gpdk045/DRC/INV_2X.sum
INFO: All selected rules completed
Total CPU Time : 2(s)
Total Real Time : 3(s)
Total Original Geometry : 167
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
ASCII report database is /home/viterbi/01/tongjia/work_gpdk045/DRC/INV_2X.drc
INFO: Checking in all SoftShare licenses.
Pegasus finished normally. 2024-09-30 14:56:42
```

Find: Prev Next Match case Whole word Use RegExp Highlight

Issues List: No errors found Warnings: 7 Info: 12

- ⚠️ WARNING (ISTRM-333): The 'enableColoring' option will be ignored during XStream Out. This is because there is no color entry in the layer map.
- ⚠️ WARNING: In technology 'gpdk045.pvt', the rule set 'default' is not a Pegasus rule set.
- ⚠️ WARNING: LAYOUT_PATH at line 20 in file /home/viterbi/01/tongjia/work_gpdk045/pvt/pvIDRC.rul is skipped. It is set in control file.
- ⚠️ WARNING: Cmdline override LAYOUT_PRIMARY 'INV_2X';
- ⚠️ WARNING: RESULTS_DB_asat in line 22 in file /home/viterbi/01/tongjia/work_gpdk045/pvt/pvIDRC.rul is skipped. It is set in control file.
- ⚠️ WARNING: TEXT_DEPTH at line 87 in file /home/viterbi/01/tongjia/work_gpdk045/pvt/pvIDRC.rul is skipped. It is set in control file.
- ⚠️ WARNING: MASK_SVDB_DIR at line 88 in file /home/viterbi/01/tongjia/work_gpdk045/pvt/pvIDRC.rul is skipped. It is set in control file.
- ⚠️ WARNING: Masked rule 'rule 100' is not defined. Action is specified.

Find: Prev Next Match case Whole word Use RegExp Highlight

Help: ReRun Resubmit Close Report Kill Job

/home/viterbi/01/tongjia/work_gpdk045/DRC

Pegasus 22.21-6b Results Viewer

DRC x

File Options Tools Help

Input Output Stats

CellTree (cell_tree.txt)
Intermediate GDSII File (INV_2X.gds)
DRC Summary (INV_2X.sum)
ASCII DRC Report Database (INV_2

Return On Top CellRule Color Count

Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

No new messages

LVS

Pegasus 22.21-6b Reports Done [LVS] LV...

```
[LVS]LVS x
=====
# Run Result : MATCH
# Run Summary : [INFO] ERC Results: Empty
# : [INFO] Extraction Clean
#
# ERC Summary File : INV_2X.sum
# Extraction Report File : INV_2X.rep
# Comparison Report File : INV_2X.rep.cls
=====

INFO: Creating cross reference database ...
INFO: Manager summary: CPUs: 0 Elapsed(s): 0 Peak memory(MB): 73.30
INFO: Checking in all SoftShare licenses.
INFO: Creating cross reference database completed. Mon Sep 30 15:08:53 2024

Pegasus finished normally. 2024-09-30 15:08:53
```

Find: Prev Next Match case Whole word Use RegExp Highlight

Issues List: No errors found Warnings: 16 Info: 14

- ⚠️ WARNING (ISTRM-20): Output Stream file '/home/viterbi/01/tongjia/work_gpdk045/LVSINV_2X.gds' already exists. It will be overwritten.
- ⚠️ WARNING (ISTRM-333): The 'enableColoring' option will be ignored during XStream Out. This is because there is no color entry in the layer map.
- ⚠️ WARNING: In technology 'gpdk045.pvt', the rule set 'default' is not a Pegasus rule set.
- ⚠️ WARNING: TEXT_DEPTH at line 87 in file /home/viterbi/01/tongjia/work_gpdk045/pvt/pvLVS.rul is skipped. It is set in control file.
- ⚠️ WARNING: MASK_SVDB_DIR at line 88 in file /home/viterbi/01/tongjia/work_gpdk045/pvt/pvLVS.rul is skipped. It is set in control file.
- ⚠️ WARNING: Masked rule 'rule 100' is not defined. Action is specified.

Find: Prev Next Match case Whole word Use RegExp Highlight

Help: ReRun Resubmit Close Report Kill Job

/home/viterbi/01/tongjia/work_gpdk045/LVS

Pegasus 22.21-6b Results Viewer

LVS x

File Options Tools Help

Input Output Stats

Intermediate GDSII File (INV_2X.gds)
Schematic Netlist (INV_2X.cdl)
Extracted Spice File (INV_2X.spf)
Comparison Report (INV_2X.rep.cls)
Extraction Report (INV_2X.rep)

SCONNECT DB (INV_2X.sconrk)
DRC Summary (INV_2X.sum)

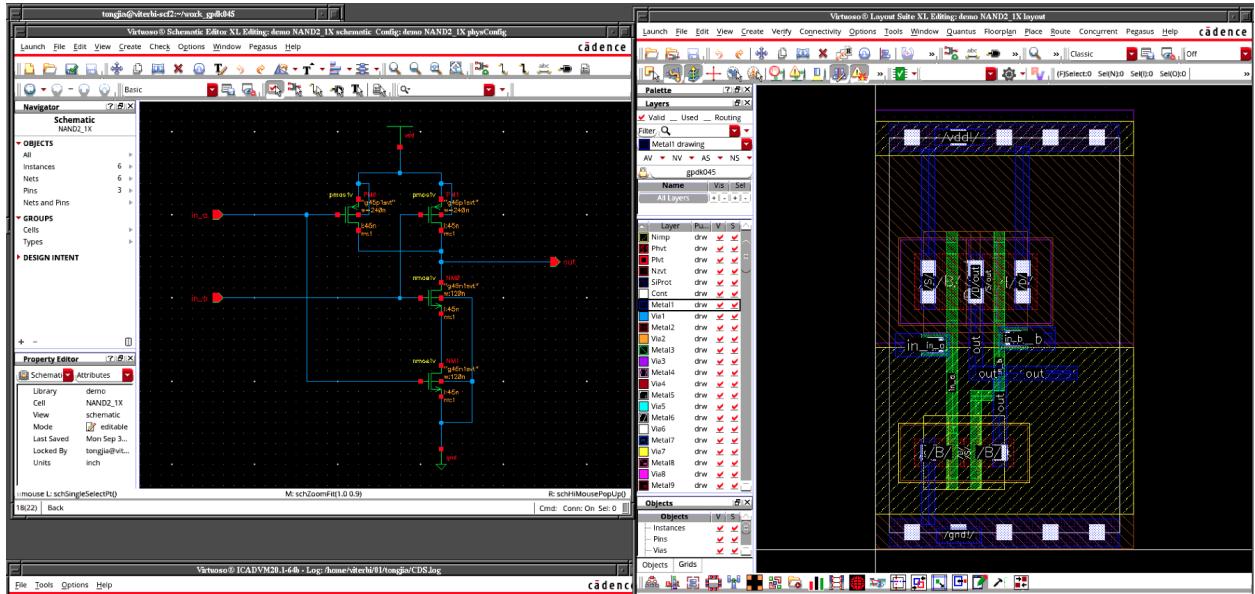
Clean

ISL Clean
SCD Clean
ERC Clean
Extraction Clean
Comparison Clean

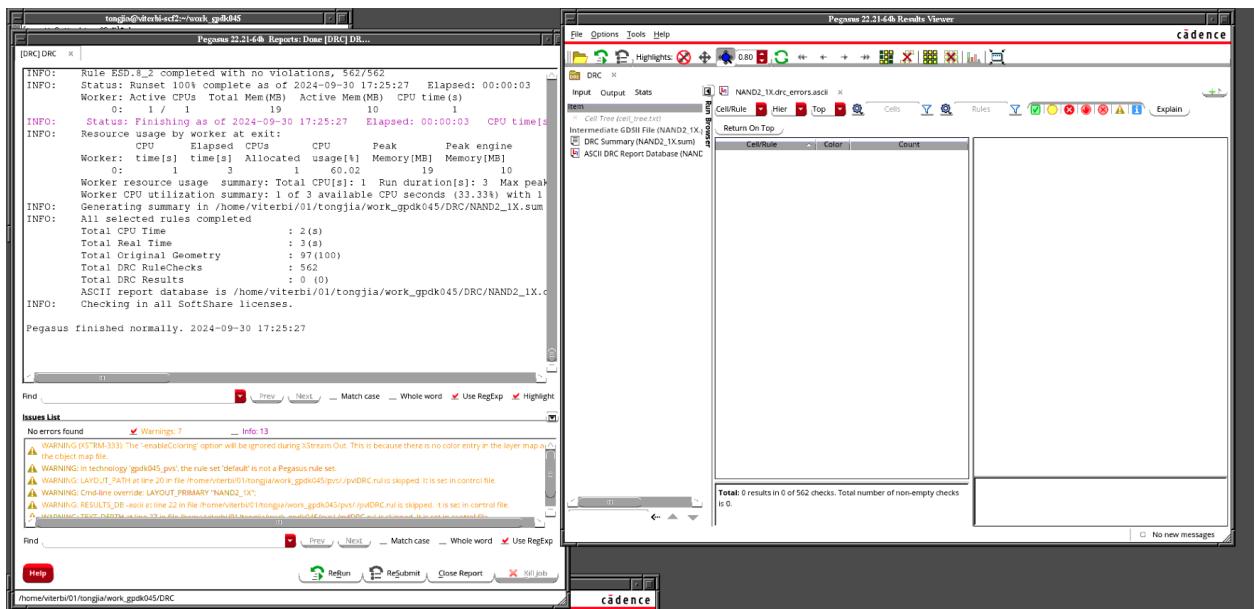
Close

No new messages

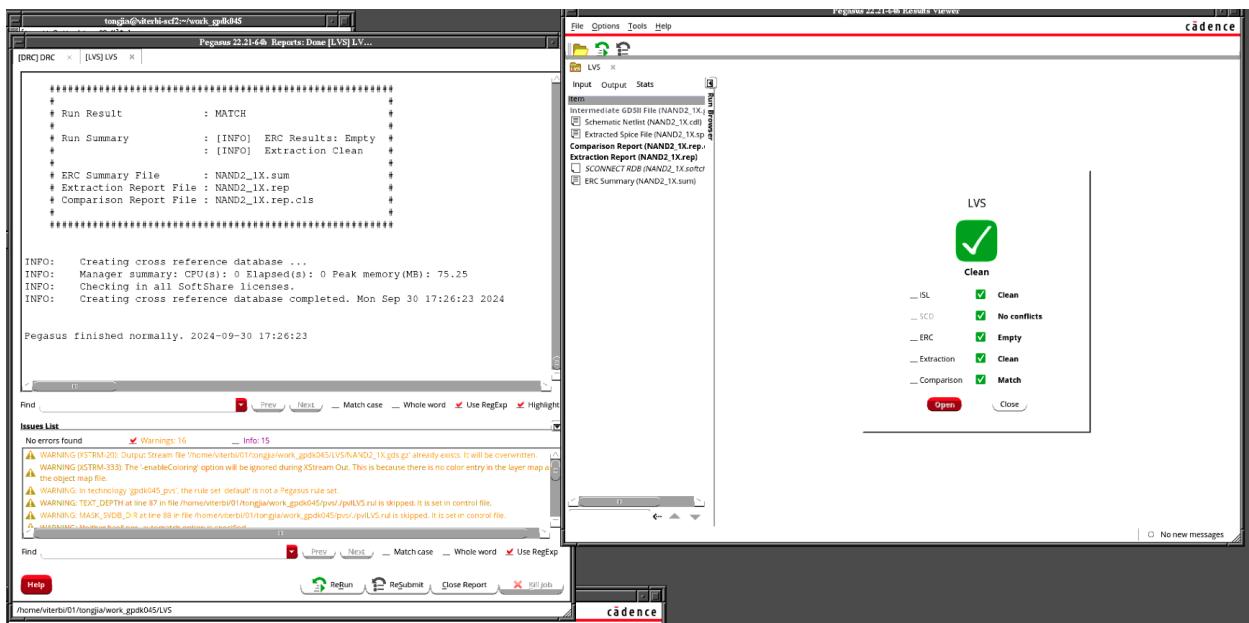
NAND2_1X: layout drawing



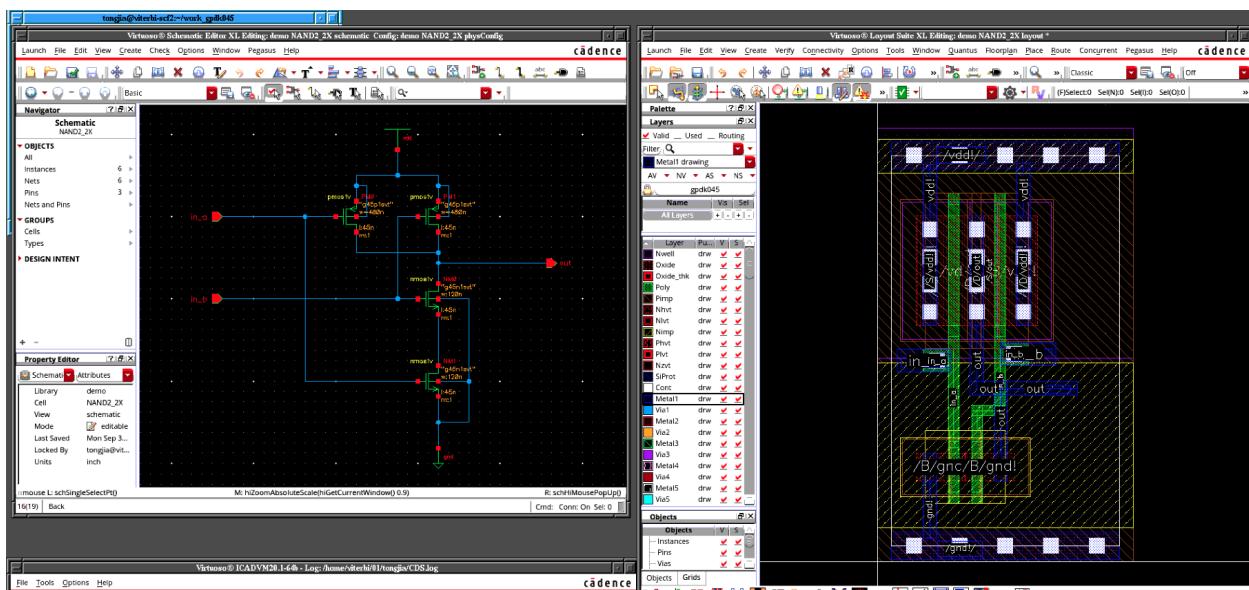
DRC



LVS



NAND2_2X: layout drawing



DRC

Pegasus 22.31-6b Reports Done [DRC] DR...

```
[INFO: Rule ESD.8_2 completed with no violations, 562/562
INFO: Status: Runset 100% complete as of 2024-09-30 16:59:23 Elapsed: 00:00:03
Worker: Active CPUs Total Mem(MB) CPU time(s)
0 1 19 10
INFO: Status: Finishing as of 2024-09-30 16:59:23 Elapsed: 00:00:03 CPU time(s)
INFO: Resource usage by worker at exit:
CPU Elapsed CPUs CPU Peak Peak engine
Worker: time[s] time[s] Allocated usage[%] Memory[MB] Memory[MB]
0 1 3 1 60.49 19 10
Worker resource usage summary: Total CPU(s): 1 Run duration(s): 3 Max peak
Worker CPU utilization summary: 1 of 3 available CPU seconds (33.33%) with 1
INFO: Generating summary in /home/viterbi/01/tongjia/work_gpdk045/DRC/NAND2_2X.sum
INFO: All selected rules completed
Total CPU time: 2(s)
Total Real Time: 3(s)
Total Original Geometry: 103(106)
Total DRC Rulechecks: 562
Total DRC Results: 0(0)
ASCII report database is /home/viterbi/01/tongjia/work_gpdk045/DRC/NAND2_2X.sum
INFO: Checking in all SoftShare licenses.
Pegasus finished normally. 2024-09-30 16:59:23
```

Find: Prev Next Match case Whole word Use RegExp Highlight

Issues List: No errors found Warnings: 8 Info: 14

- WARNING: PSTM-20: Output Stream file '/home/viterbi/01/tongjia/work_gpdk045/DRC/NAND2_2X.gds' already exists. It will be overwritten.
- WARNING: DSTM-333: The '-enableColoring' option will be ignored during XStream Out. This is because there is no color entry in the layer map of the object map file.
- WARNING: In technology gpdk045.pvt, the rule set default is not a Pegasus rule set.
- WARNING: LAYOUT_PATH at line 20 in file /home/viterbi/01/tongjia/work_gpdk045/pv/DRC.nlu is skipped. It is set in control file.
- WARNING: Circ-line override: LAYOUT_PRIMARY 'NAND2_2X'.
- WARNING: TEXT_DEPTH at line 77 in the documentation file /home/viterbi/01/tongjia/work_gpdk045/pv/DRC.nlu is skipped. It is set in control file.

Find: Prev Next Match case Whole word Use RegExp Highlight

Help: [ReRun](#) [Resubmit](#) [Close Report](#) [Kill jobs](#)

/home/viterbi/01/tongjia/work_gpdk045/DRC

Pegasus 22.31-6b Results Viewer

File Options Tools Help

NAND2_2X.drc_errors.ascii

DRC

Cell/Rule Hier Top Cells Rules Explain

Intermediate OSDB File (NAND2_2X.sum)

DRC Summary (NAND2_2X.sum)

ASCII DRC Report Database (NAND2_2X.sum)

Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

No new messages

LVS

Pegasus 22.31-6b Reports Done [LVS] LVS...

```
[DRC] DRC < [LVS] LVS <
```

```
#####
# Run Result : MATCH
#
# Run Summary : [INFO] ERC Results: Empty
#               : [INFO] Extraction Clean
#
# ERC Summary File : NAND2_2X.sum
# Extraction Report File : NAND2_2X.rep
# Comparison Report File : NAND2_2X.rep.cis
#####

INFO: Creating cross reference database ...
INFO: Manager summary: CPU(s): 0 Elapsed(s): 0 Peak memory(MB): 74.87
INFO: Checking in all SoftShare licenses.
INFO: Creating cross reference database completed. Mon Sep 30 17:01:04 2024

Pegasus finished normally. 2024-09-30 17:01:04
```

Find: Prev Next Match case Whole word Use RegExp Highlight

Issues List: No errors found Warnings: 16 Info: 16

- WARNING: PSTM-20: Output Stream file '/home/viterbi/01/tongjia/work_gpdk045/LVS/NAND2_2X.gds' already exists. It will be overwritten.
- WARNING: DSTM-333: The '-enableColoring' option will be ignored during XStream Out. This is because there is no color entry in the layer map of the object map file.
- WARNING: In technology gpdk045.pvt, the rule set default is not a Pegasus rule set.
- WARNING: TEXT_DEPTH at line 87 in file /home/viterbi/01/tongjia/work_gpdk045/pv/LVS.nlu is skipped. It is set in control file.
- WARNING: MASK_SVDR_D9 at line 88 in file /home/viterbi/01/tongjia/work_gpdk045/pv/LVS.nlu is skipped. It is set in control file.
- WARNING: Miscellaneous warning about unused soft links was suppressed.

Find: Prev Next Match case Whole word Use RegExp Highlight

Help: [ReRun](#) [Resubmit](#) [Close Report](#) [Kill jobs](#)

/home/viterbi/01/tongjia/work_gpdk045/LVS

Pegasus 22.31-6b Results Viewer

LVS

File Options Tools Help

Schematic Netlist (NAND2_2X.ofl)

Extracted Spice File (NAND2_2X.sp)

Comparison Report (NAND2_2X.rep)

Extraction Report (NAND2_2X.rep)

CONNECT RDB (NAND2_2X.rdb)

ERC Summary (NAND2_2X.sum)

Clean

ISL Clean

SCD Clean

ERC Clean

Extraction Clean

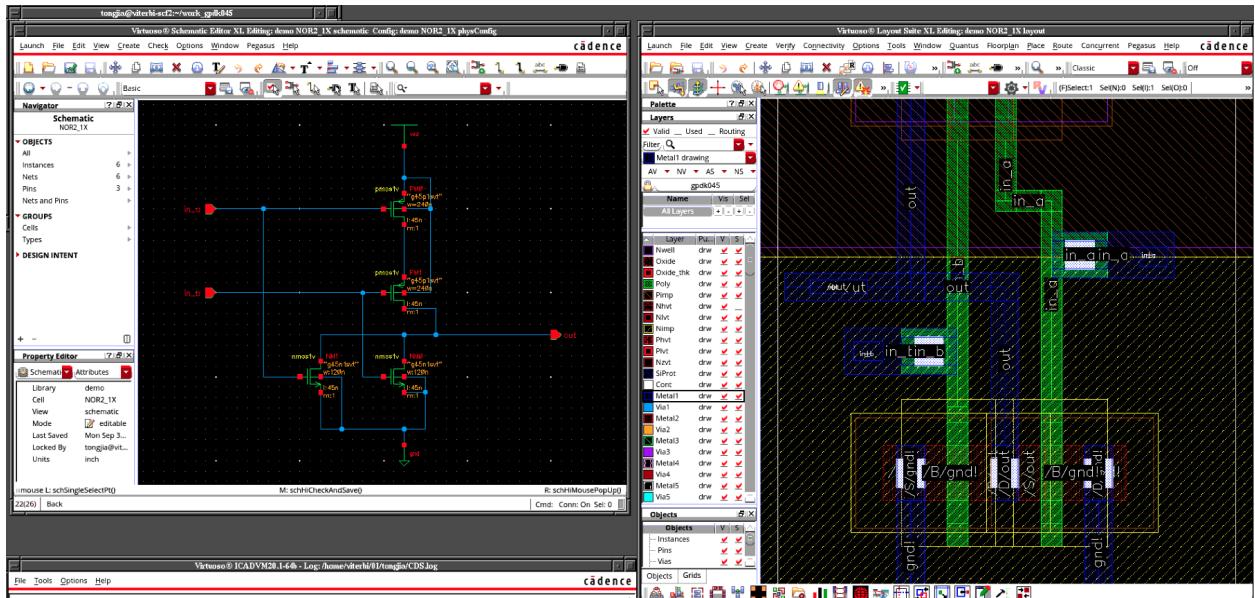
Comparison Clean

Match

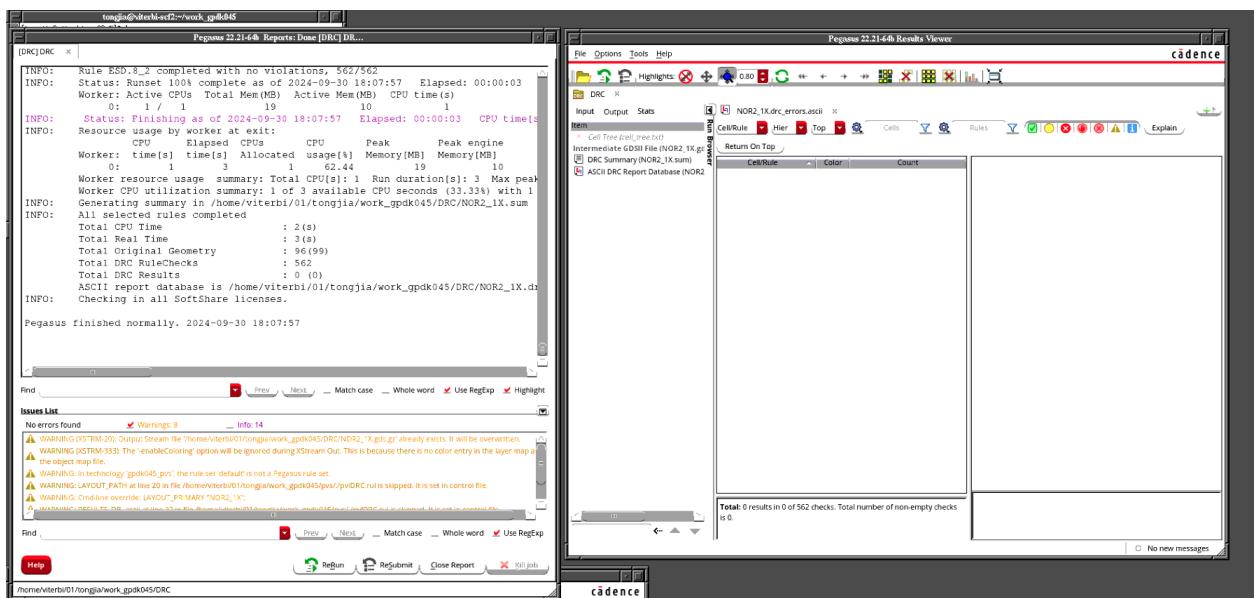
Open Close

No new messages

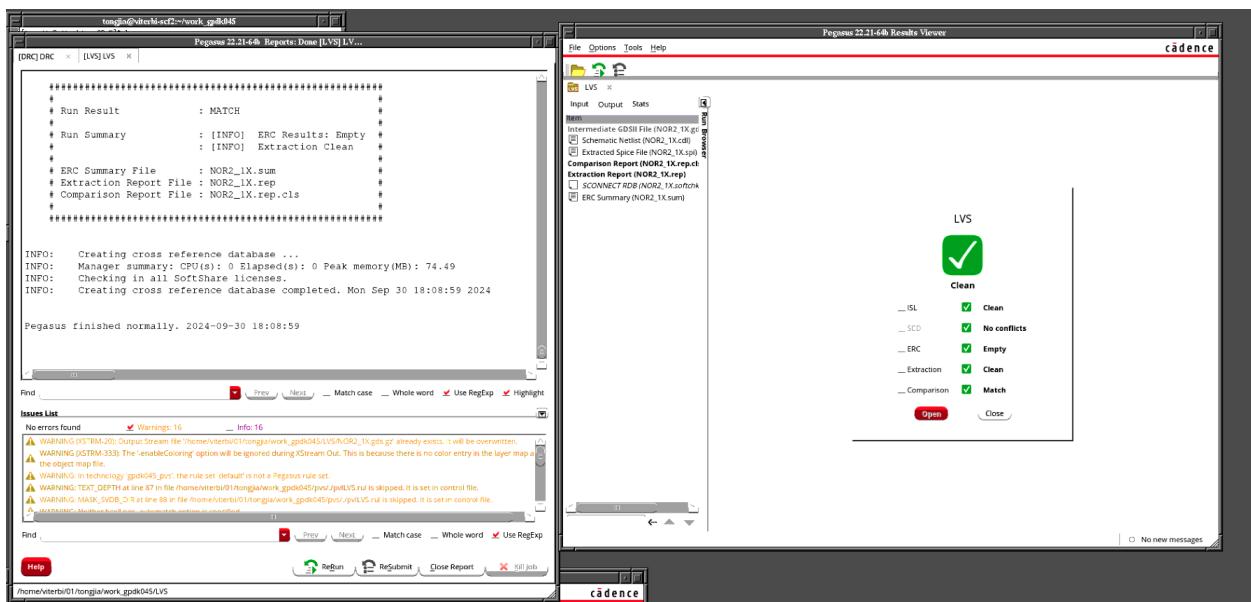
NOR2_1X: layout drawing



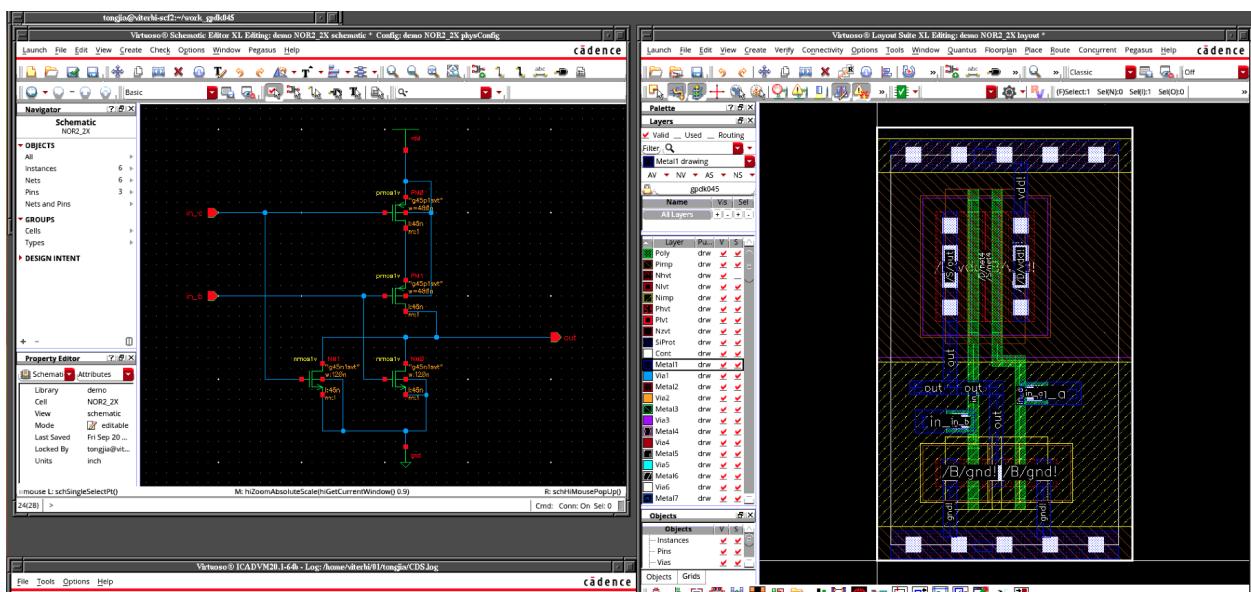
DRC



LVS



NOR2_2X:
layout drawing



DRC

terminal output:

```
tongjia@sterbi-scf2:~/work_gpdk045$ Pegasus 22.31-64 Reports Done [DRC] DRC...
[DRC] DRC x | NOR2_2X.drc x | NOR2_2X.sum x | NOR2_2X.drc_errors.escl x | NOR2_2X.ksum x | NOR2_2X.sum
[INFO]: Rule ESD_8_2 completed with no violations, 562/562
[INFO]: Status: Runset 100% complete as of 2024-09-30 18:17:18 Elapsed: 00:00:03
[Worker]: Active Workers Total Mem(MB) Active Mem(MB) CPU time(s)
[0]: 0 0 / 1 19 19 10
[INFO]: Status: Finishing as of 2024-09-30 18:17:18 Elapsed: 00:00:03 CPU time(s)
[INFO]: Resource usage by worker at exit:
[CPU] Elapsed CPUs CPU Peak engine
[Worker]: time(s) time(s) Allocated usage(%) Memory[MB] Memory[MB]
[0]: 0 1 65.07 19 10
[INFO]: Worker resource usage summary: Total CPU(s) 1 Run duration(s): 3 Max peak
[INFO]: Worker CPU utilization summary: of 3 available CPU seconds (31.33%) with 1
[INFO]: Generating summary in /home/viterbi/01/tongjia/work_gpdk045/DRC/NOR2_2X.sum
[INFO]: All selected rules completed
[Total CPU Time : 2(s)
[Total Real Time : 3(s)
[Total Original Geometry : 100(103)
[Total DRC Checks : 562
[Total DRC Results : 0 (0)
[ASCII report database is /home/viterbi/01/tongjia/work_gpdk045/DRC/NOR2_2X.dci
[INFO]: Checking in all SoftShare licenses.

Pegasus finished normally. 2024-09-30 18:17:18
```

Issues List:

- No errors found
- Warnings: 7
- Info: 14

Results Viewer:

- Input, Output, Stats
- Intermediate GDSII File (NOR2_2X.gds)
- Schematic Netlist (NOR2_2X.cdl)
- Extraction Report File (NOR2_2X.rep)
- Comparison Report (NOR2_2X.rep)
- Extraction Report (NOR2_2X.rep)
- SCONNET RDB (NOR2_2X.sconch)
- ERC Summary (NOR2_2X.sum)

Total: 0 results in 0 of 562 checks. Total number of non-empty checks is 0.

LVS

terminal output:

```
tongjia@sterbi-scf2:~/work_gpdk045$ Pegasus 22.31-64 Reports Done [LVS] LVS...
[DRC] DRC x | [LVS] LVS x | NOR2_2X.sum x | NOR2_2X.lvs x | NOR2_2X.ksum x | NOR2_2X.sum
#####
# Run Result : MATCH
#
# Run Summary : [INFO] ERC Results: Empty
#               : [INFO] Extraction Clean
#
# ERC Summary File : NOR2_2X.sum
# Extraction Report File : NOR2_2X.rep
# Comparison Report File : NOR2_2X.rep.cls
#
#####

[INFO]: Creating cross reference database ...
[INFO]: Manager summary: CPU(s): 0 Elapsed(s): 0 Peak memory(MB): 74.11
[INFO]: Checking in all SoftShare licenses.
[INFO]: Creating cross reference database completed. Mon Sep 30 18:18:46 2024

Pegasus finished normally. 2024-09-30 18:18:46
```

Issues List:

- No errors found
- Warnings: 15
- Info: 16

Results Viewer:

- Input, Output, Stats
- Intermediate GDSII File (NOR2_2X.gds)
- Schematic Netlist (NOR2_2X.cdl)
- Extraction Report File (NOR2_2X.rep)
- Comparison Report (NOR2_2X.rep)
- Extraction Report (NOR2_2X.rep)
- SCONNET RDB (NOR2_2X.sconch)
- ERC Summary (NOR2_2X.sum)

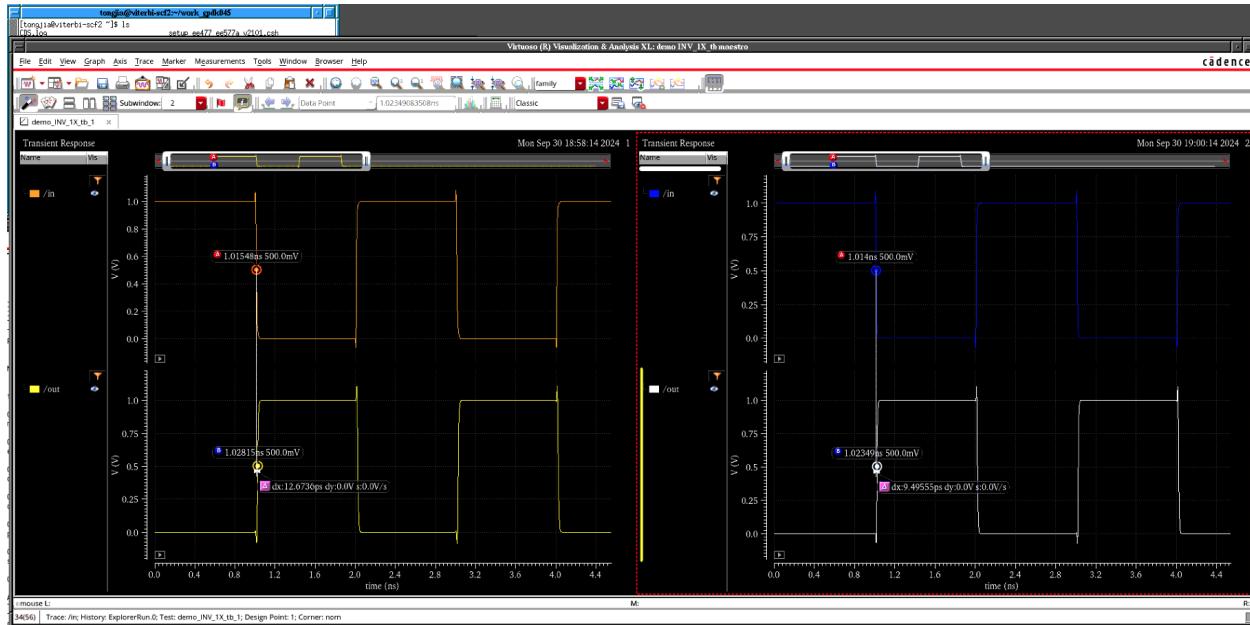
LVS Status:

- Clean
- ISL: Clean
- SCD: No conflicts
- ERC: Empty
- Extraction: Clean
- Comparison: Match

STEP 4

INV_1X:

input and output waveforms(function verification)
(left: av_extracted | right: schematic)



propagation delays for av_extracted INV_1X(input = (A))

| Rising delay(ps) | Falling delay(ps) |
|------------------|-------------------|
| (A) = (1) -> (0) | 12.674 |

(Worst case delay is shown in bold)

propagation delays for schematic INV_1X(input = (A))

| Rising delay(ps) | Falling delay(ps) |
|------------------|-------------------|
| (A) = (1) -> (0) | 9.496 |

(Worst case delay is shown in bold)

Comparison of worst case propagation delays

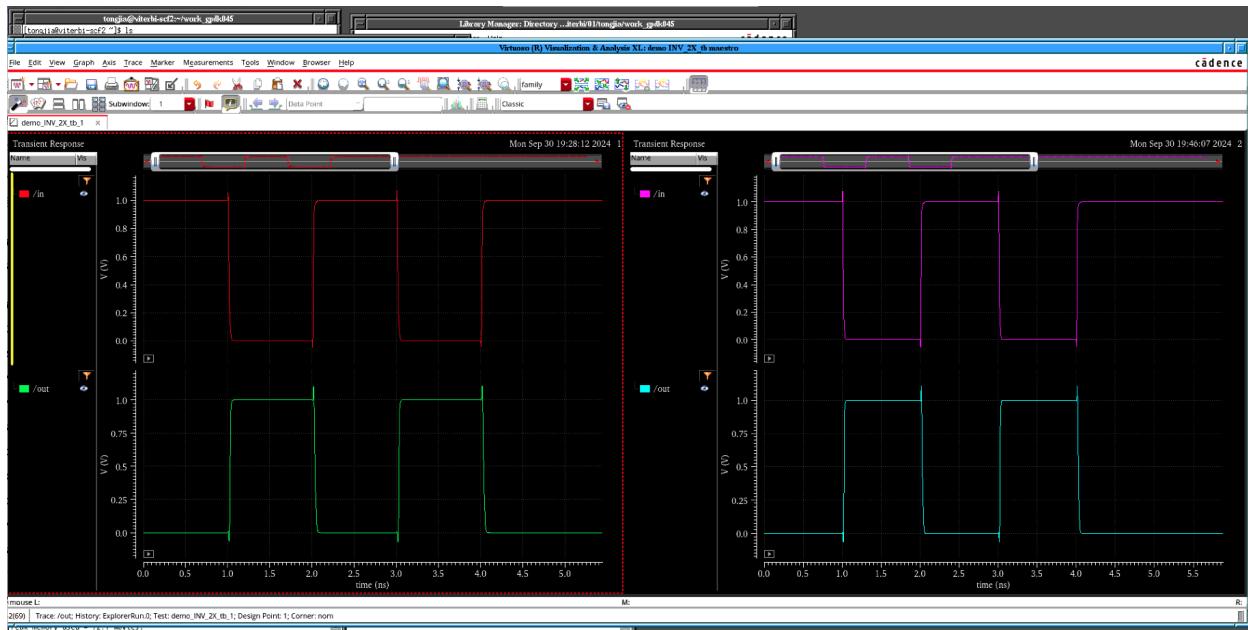
| Rising delay(ps) | Falling delay(ps) |
|------------------|-------------------|
| av_extracted | 12.674 |
| schematic | 9.496 |

(Worst case delay is shown in bold)

For INV_1X, the layout shows approximately 3ps more compared to the schematic. I believe this is happening because the schematic does not consider parasitic effects, wire lengths, and interconnect delays, while the layout includes these factors.

INV_2X:

input and output waveforms(function verification)
(left: av_extracted | right: schematic)



propagation delays for av_extracted INV_2X(input = (A))

| Rising delay(ps) | | Falling delay(ps) | |
|------------------|---------------|-------------------|---------------|
| (A) = (1) -> (0) | 13.467 | (A) = (0) -> (1) | 18.902 |

(Worst case delay is shown in bold)

propagation delays for schematic INV_2X(input = (A))

| Rising delay(ps) | | Falling delay(ps) | |
|------------------|---------------|-------------------|---------------|
| (A) = (1) -> (0) | 10.095 | (A) = (0) -> (1) | 14.569 |

(Worst case delay is shown in bold)

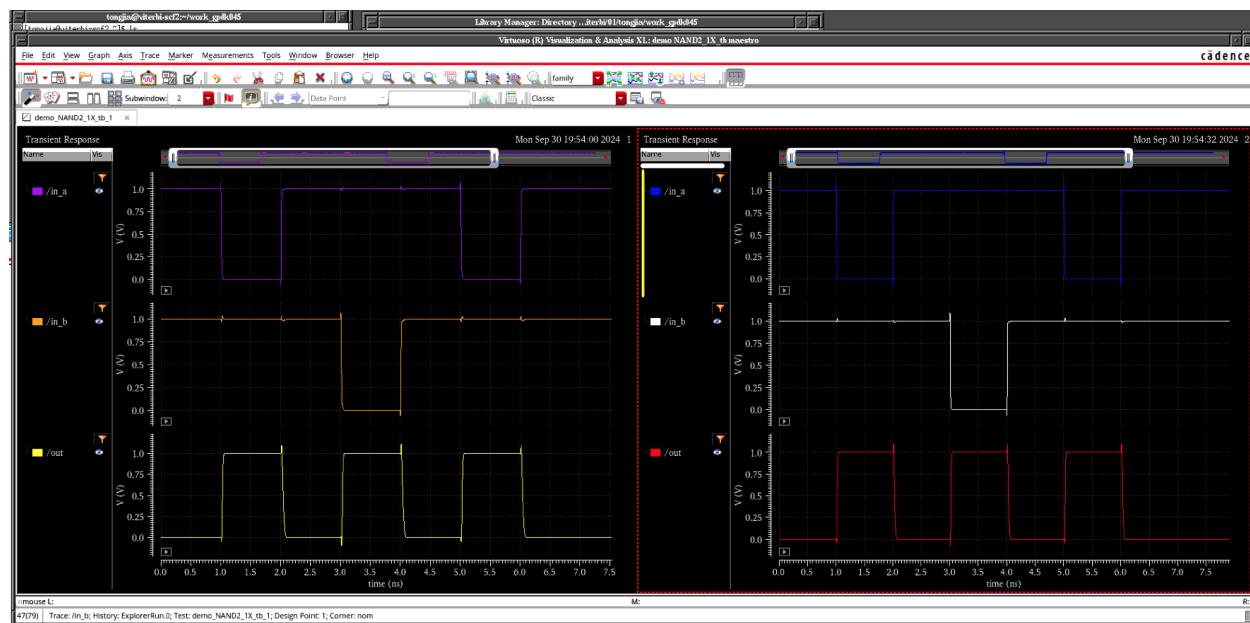
| Comparison of worst case propagation delays | | | |
|---|---------------|-------------------|---------------|
| Rising delay(ps) | | Falling delay(ps) | |
| av_extracted | 13.467 | av_extracted | 18.902 |
| schematic | 10.095 | schematic | 14.569 |

(Worst case delay is shown in bold)

For INV_2X, the layout shows approximately 3 - 4ps more compared to the schematic. I believe this is happening because the schematic does not consider parasitic effects, wire lengths, and interconnect delays, while the layout includes these factors.

NAND2_1X:

input and output waveforms(function verification)
(left: av_extracted | right: schematic)



| Worst case delays av_extracted NAND2_1X(input = (A,B)) | | | |
|--|---------------|------------------------|---------------|
| Rising delay(ps) | | Falling delay(ps) | |
| (A,B) = (1,1) -> (0,1) | 17.204 | (A,B) = (0,1) -> (1,1) | 30.010 |
| (A,B) = (1,1) -> (1,0) | 17.584 | (A,B) = (1,0) -> (1,1) | 29.426 |

(Worst case delay is shown in bold)

| Worst case delays schematic NAND2_1X(input = (A, B)) | | | |
|--|---------------|---------------------------|---------------|
| Rising delay(ps) | | Falling delay(ps) | |
| (A, B) = (1, 1) -> (0, 1) | 11.124 | (A, B) = (0, 1) -> (1, 1) | 21.547 |
| (A, B) = (1, 1) -> (1, 0) | 10.119 | (A, B) = (1, 0) -> (1, 1) | 18.543 |

(Worst case delay is shown in bold)

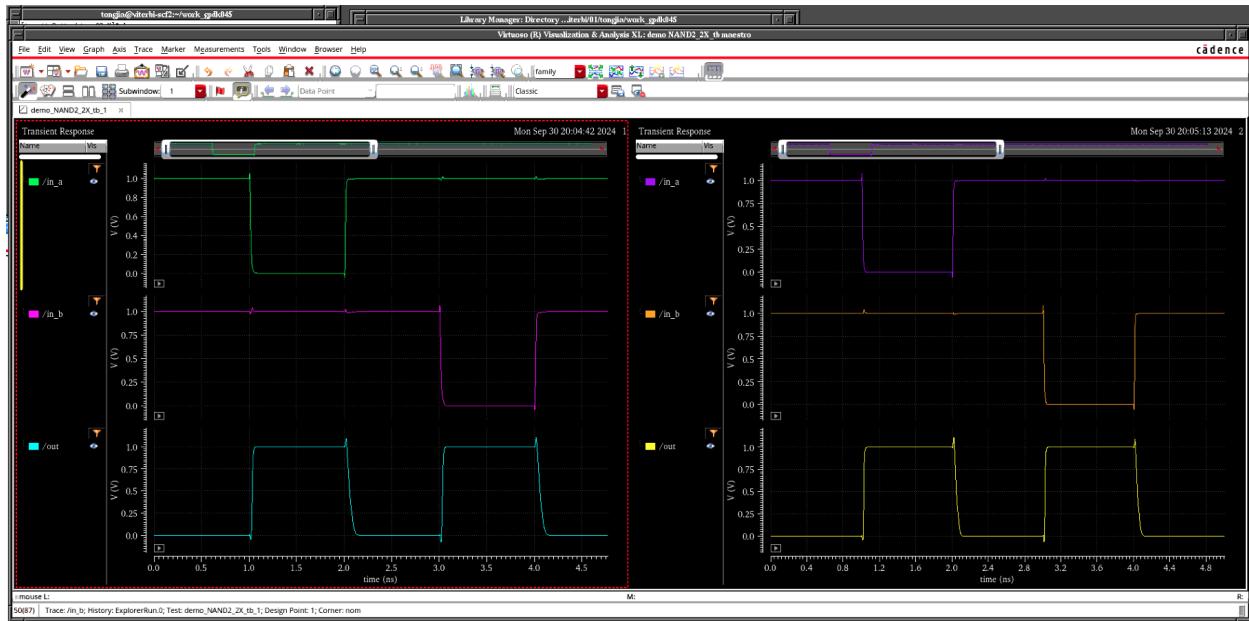
| Comparison of worst case propagation delays | | | |
|---|---------------|-------------------|---------------|
| Rising delay(ps) | | Falling delay(ps) | |
| av_extracted | 17.584 | av_extracted | 30.010 |
| schematic | 11.124 | schematic | 21.547 |

(Worst case delay is shown in bold)

For NAND2_1X, the layout Rising delay shows approximately 7ps more compared to the schematic, and the layout Falling delay shows approximately 9ps more compared to the schematic. I believe this is happening because the schematic does not consider parasitic effects, wire lengths, and interconnect delays, while the layout includes these factors.

NAND2_2X:

input and output waveforms(function verification)
 (left: av_extracted | right: schematic)



Worst case delays av_extracted NAND2_2X(input = (A,B))

| Rising delay(ps) | | Falling delay(ps) | |
|------------------------|---------------|------------------------|---------------|
| (A,B) = (1,1) -> (0,1) | 17.023 | (A,B) = (0,1) -> (1,1) | 43.097 |
| (A,B) = (1,1) -> (1,0) | 17.404 | (A,B) = (1,0) -> (1,1) | 42.403 |

(Worst case delay is shown in bold)

Worst case delays schematic NAND2_2X(input = (A,B))

| Rising delay(ps) | | Falling delay(ps) | |
|------------------------|---------------|------------------------|---------------|
| (A,B) = (1,1) -> (0,1) | 11.864 | (A,B) = (0,1) -> (1,1) | 33.487 |
| (A,B) = (1,1) -> (1,0) | 11.356 | (A,B) = (1,0) -> (1,1) | 30.374 |

(Worst case delay is shown in bold)

Comparison of worst case propagation delays

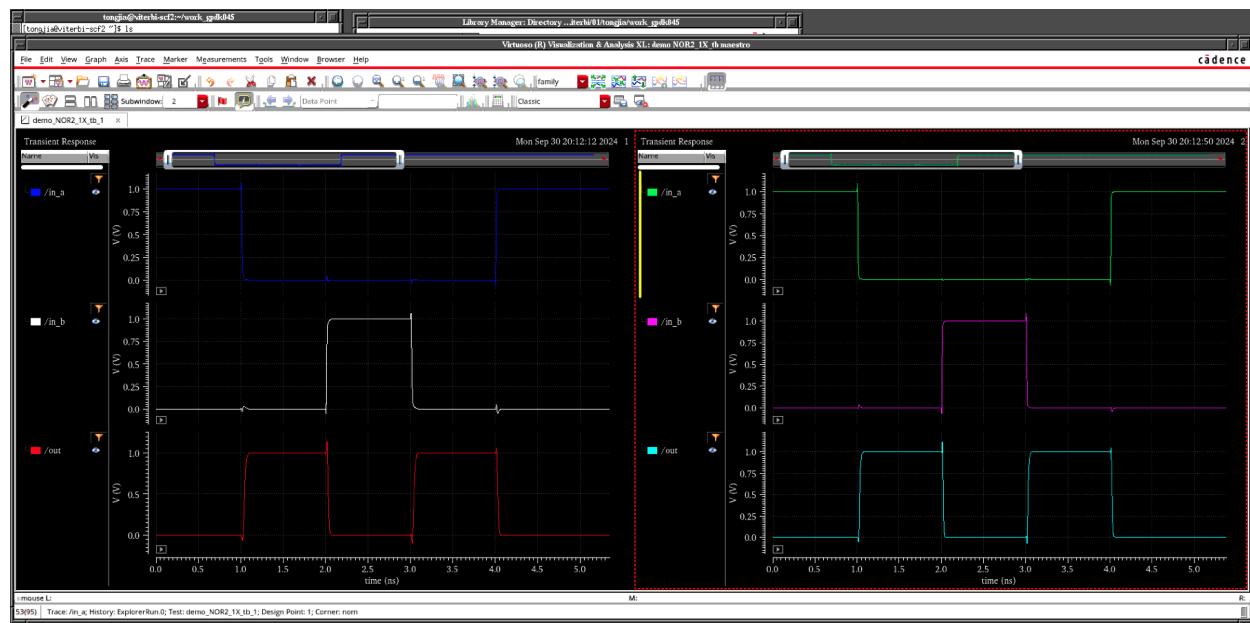
| Rising delay(ps) | | Falling delay(ps) | |
|------------------|---------------|-------------------|---------------|
| av_extracted | 17.404 | av_extracted | 43.097 |
| schematic | 11.864 | schematic | 33.487 |

(Worst case delay is shown in bold)

For NAND2_2X, the layout Rising delay shows approximately 6ps more compared to the schematic, and the layout Falling delay shows approximately 10ps more compared to the schematic. I believe this is happening because the schematic does not consider parasitic effects, wire lengths, and interconnect delays, while the layout includes these factors.

NOR2_1X:

input and output waveforms(function verification)
(left: av_extracted | right: schematic)



| Worst case delays av_extracted NOR2_1X(input = (A,B)) | | | |
|---|---------------|------------------------|---------------|
| Rising delay(ps) | | Falling delay(ps) | |
| (A,B) = (1,0) -> (0,0) | 28.496 | (A,B) = (0,0) -> (1,0) | 18.680 |
| (A,B) = (0,1) -> (0,0) | 25.209 | (A,B) = (0,0) -> (0,1) | 17.424 |

(Worst case delay is shown in bold)

| Worst case delays schematic NOR2_1X(input = (A,B)) | | | |
|--|---------------|------------------------|---------------|
| Rising delay(ps) | | Falling delay(ps) | |
| (A,B) = (1,0) -> (0,0) | 19.425 | (A,B) = (0,0) -> (1,0) | 13.708 |
| (A,B) = (0,1) -> (0,0) | 14.032 | (A,B) = (0,0) -> (0,1) | 10.779 |

(Worst case delay is shown in bold)

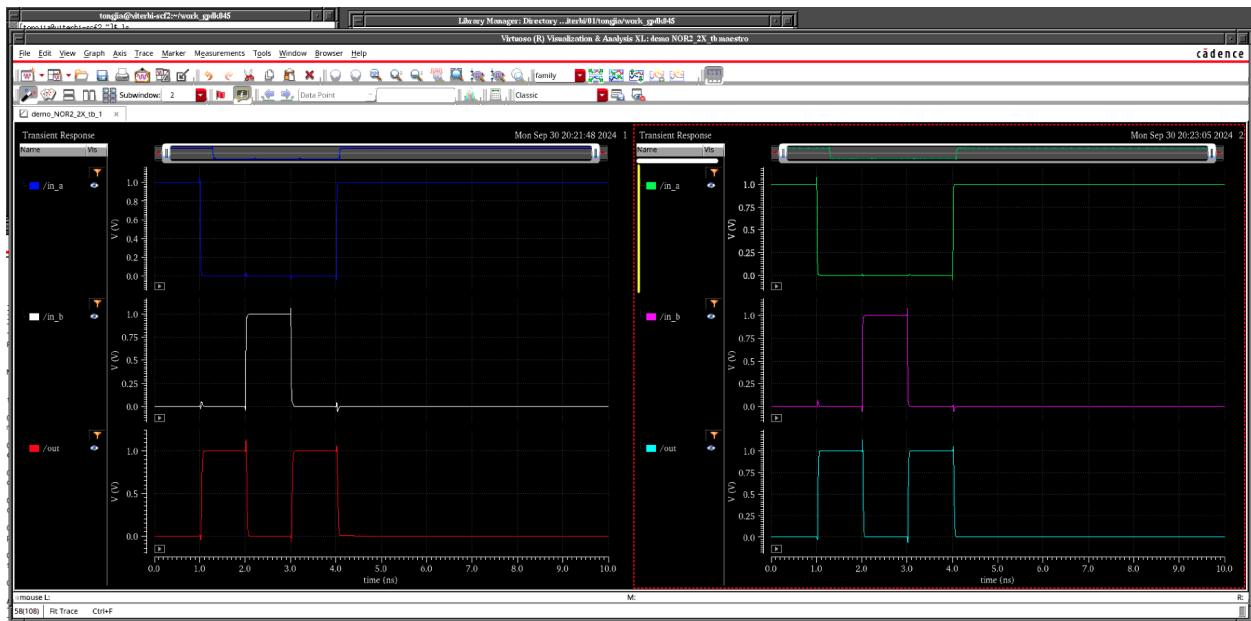
| Comparison of worst case propagation delays | | | |
|---|---------------|-------------------|---------------|
| Rising delay(ps) | | Falling delay(ps) | |
| av_extracted | 28.496 | av_extracted | 18.680 |
| schematic | 19.425 | schematic | 13.708 |

(Worst case delay is shown in bold)

For NOR2_1X, the layout Rising delay shows approximately 9ps more compared to the schematic, and the layout Falling delay shows approximately 5ps more compared to the schematic. I believe this is happening because the schematic does not consider parasitic effects, wire lengths, and interconnect delays, while the layout includes these factors.

NOR2_2X:

input and output waveforms (function verification)
 (left: av_extracted | right: schematic)



Worst case delays av_extracted NOR2_2X(input = (A,B))

| Rising delay(ps) | | Falling delay(ps) | |
|-----------------------------------|---------------|-----------------------------------|---------------|
| $(A,B) = (1,0) \rightarrow (0,0)$ | 27.241 | $(A,B) = (0,0) \rightarrow (1,0)$ | 26.816 |
| $(A,B) = (0,1) \rightarrow (0,0)$ | 21.997 | $(A,B) = (0,0) \rightarrow (0,1)$ | 22.605 |

(Worst case delay is shown in bold)

Worst case delays schematic NOR2_2X(input = (A,B))

| Rising delay(ps) | | Falling delay(ps) | |
|-----------------------------------|---------------|-----------------------------------|---------------|
| $(A,B) = (1,0) \rightarrow (0,0)$ | 20.209 | $(A,B) = (0,0) \rightarrow (1,0)$ | 22.250 |
| $(A,B) = (0,1) \rightarrow (0,0)$ | 13.731 | $(A,B) = (0,0) \rightarrow (0,1)$ | 15.935 |

(Worst case delay is shown in bold)

| Comparison of worst case propagation delays | | | |
|---|---------------|-------------------|---------------|
| Rising delay(ps) | | Falling delay(ps) | |
| av_extracted | 27.241 | av_extracted | 26.816 |
| schematic | 20.209 | schematic | 22.250 |

(Worst case delay is shown in bold)

For NOR2_2X, the layout Rising delay shows approximately 7ps more compared to the schematic, and the layout Falling delay shows approximately 4ps more compared to the schematic. I believe this is happening because the schematic does not consider parasitic effects, wire lengths, and interconnect delays, while the layout includes these factors.