EE477L Lab3 part1

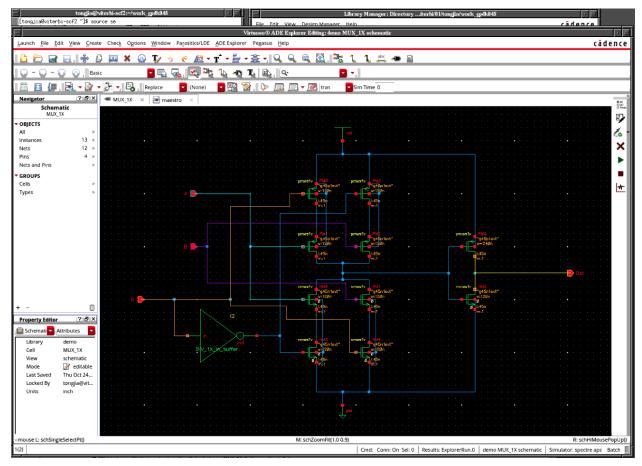
Tong Jia 4035791621

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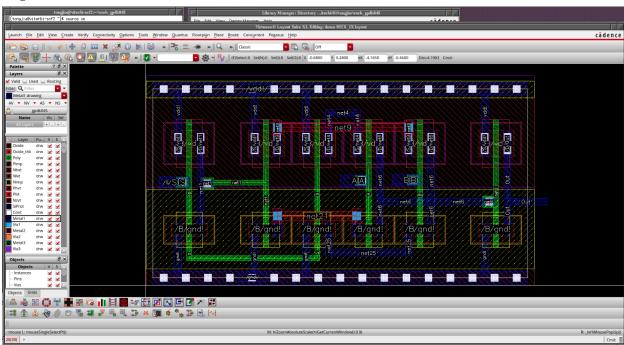
For All MUX below, Use a k-ratio of 2, VDD = 1V, rise/fall transition time = 10ps

MUX_1X:

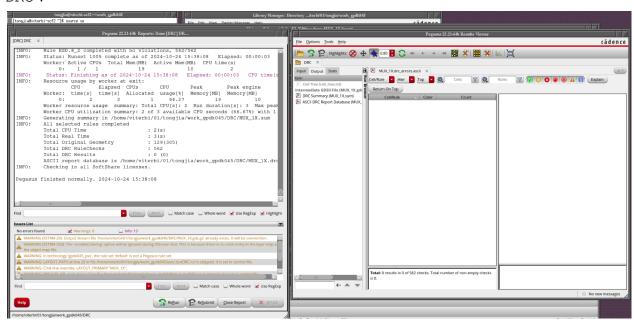
Schematic:



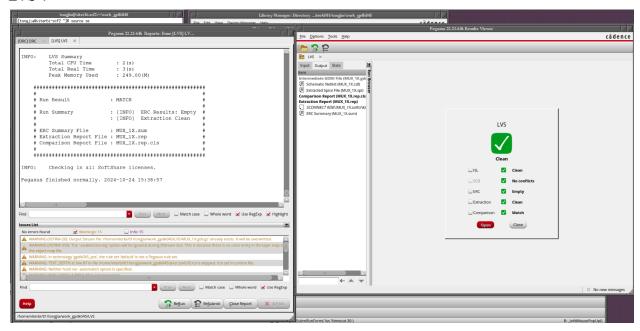
Layout:



DRC:

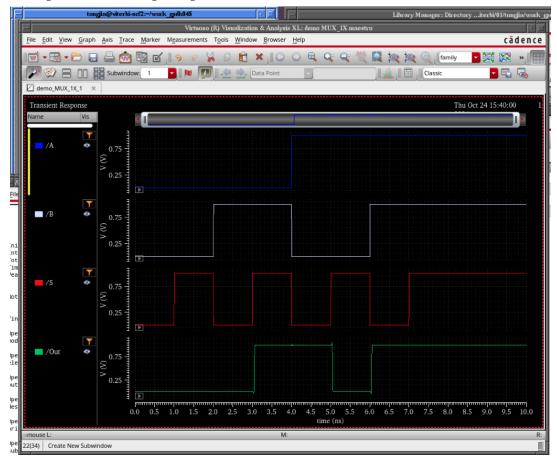


LVS:



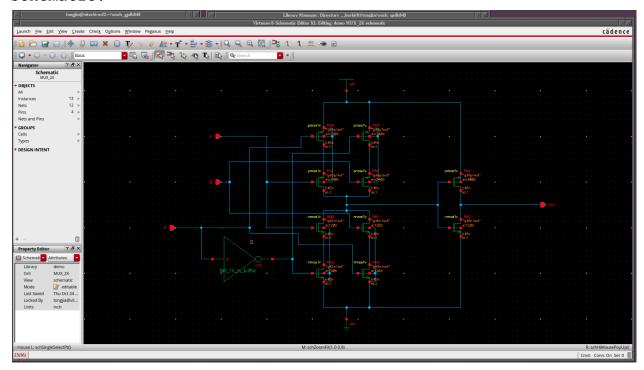
Functionality verification:

(A = 00001111, B = 00110011, S = 01010101, which contains all the possible input patterns)

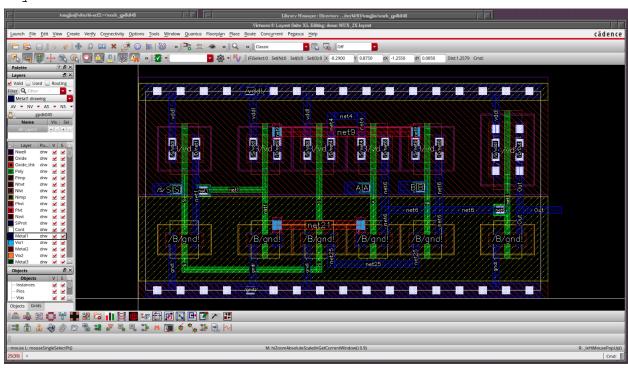


MUX 2X:

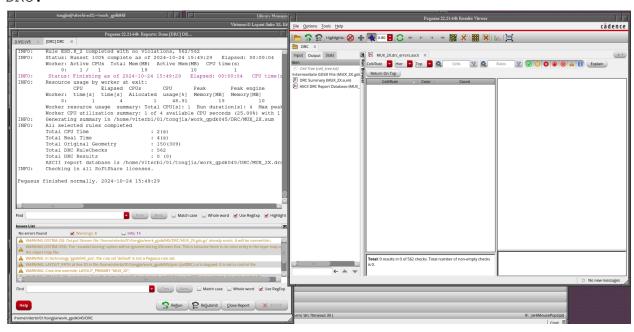
Schematic:



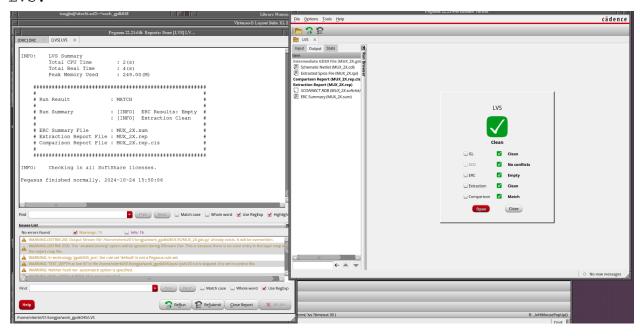
Layout:



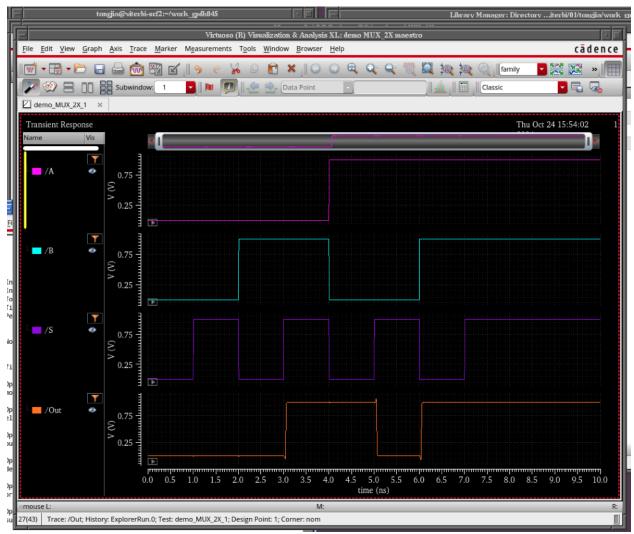
DRC:



LVS:

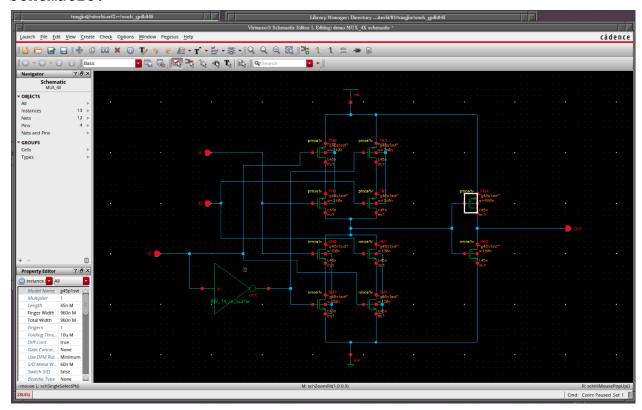


Functionality verification: (A = 00001111, B = 00110011, S = 01010101, which contains all the possible input patterns)

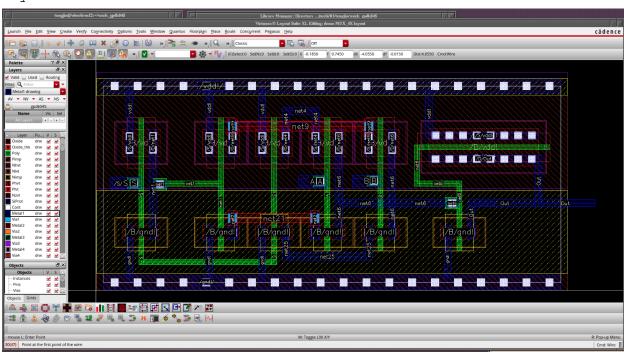


MUX 4X:

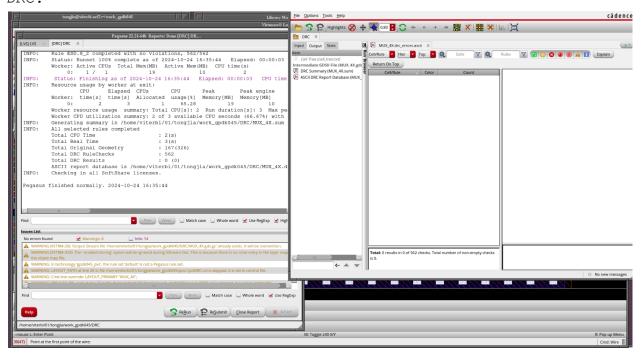
Schematic:



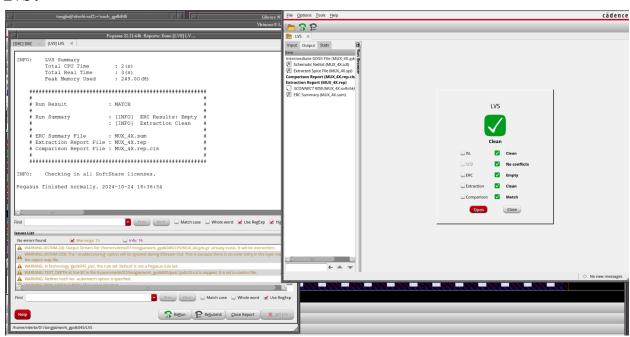
Layout:



DRC:



LVS:



Functionality verification: (A = 00001111, B = 00110011, S = 01010101, which contains all the possible input patterns)

