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EE 477L HW 0

Q1).

- Q.1. The switch in the circuit shown in Fig. 1 has been in the closed position for an extended period and is opened at $t = 0$. Determine the voltage $v(t)$ for $t \geq 0$. Also, compute the initial energy stored in the capacitor.

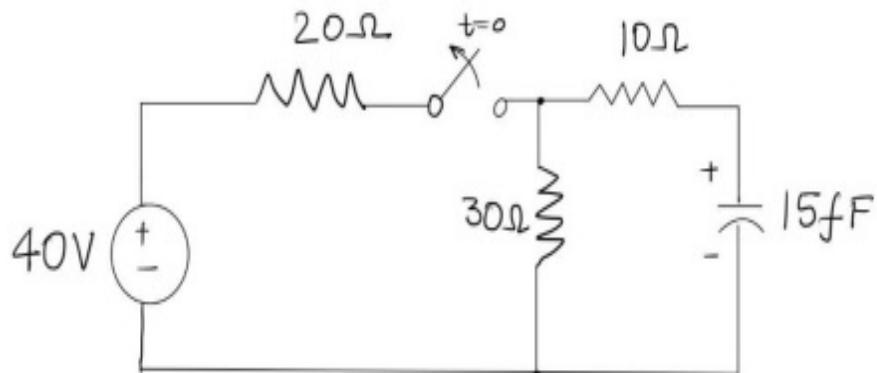


Fig. 1

$$\text{Initial energy } V_C = 40V \cdot \frac{30}{30+20}$$

$$= \underline{\underline{124 \text{ V}}}$$

$$V(t) = V(\infty) + (V(0) - V(\infty)) e^{-\frac{t}{T}}$$

where $V(\infty) = 0$ for $t = \infty$ since there's no more active source incoming, $T = \frac{1}{(R_1 + R_2)C} = \frac{1}{40 \times 10 \times 15^{-15}}$

$$\therefore V(t) = 24e^{-\frac{t}{9.135 \times 10^{-16}}} \text{ V}$$

(Q2)

Q.2.

- a. The logical operation carried out by the 4:1 MUX circuit in Fig. 2 is, assuming that GND is treated as logic '0'. Realize the digital logic circuit.

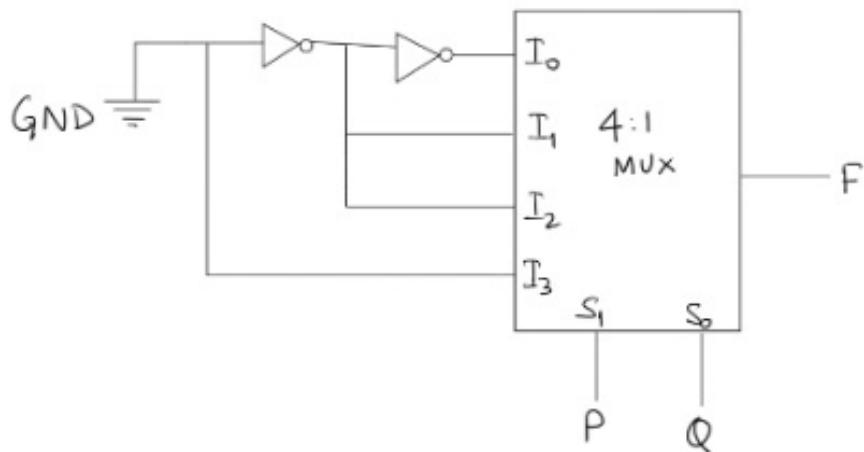


Fig. 2

- b. Realize the Boolean expression using Boolean postulates ONLY.

$$F = x_1 x_2 + \bar{x}_1 x_3 + x_2 x_3$$

Draw the corresponding digital logic circuit using NAND gates ONLY.

a).

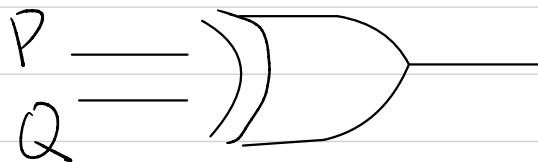
the 4:1 MUX by truth table.

P	Q	F
1	1	I_3
0	1	I_2
1	0	I_1
0	0	I_0

If GND is treated as logic "0"

We can write the reduced boolean exp as.

$$F = \overline{P} \overline{Q} \cdot 0 + \overline{P} Q \cdot 1 + P \overline{Q} \cdot 1 + P Q \cdot 0 \\ = \overline{P} Q + P \overline{Q} = P \oplus Q.$$

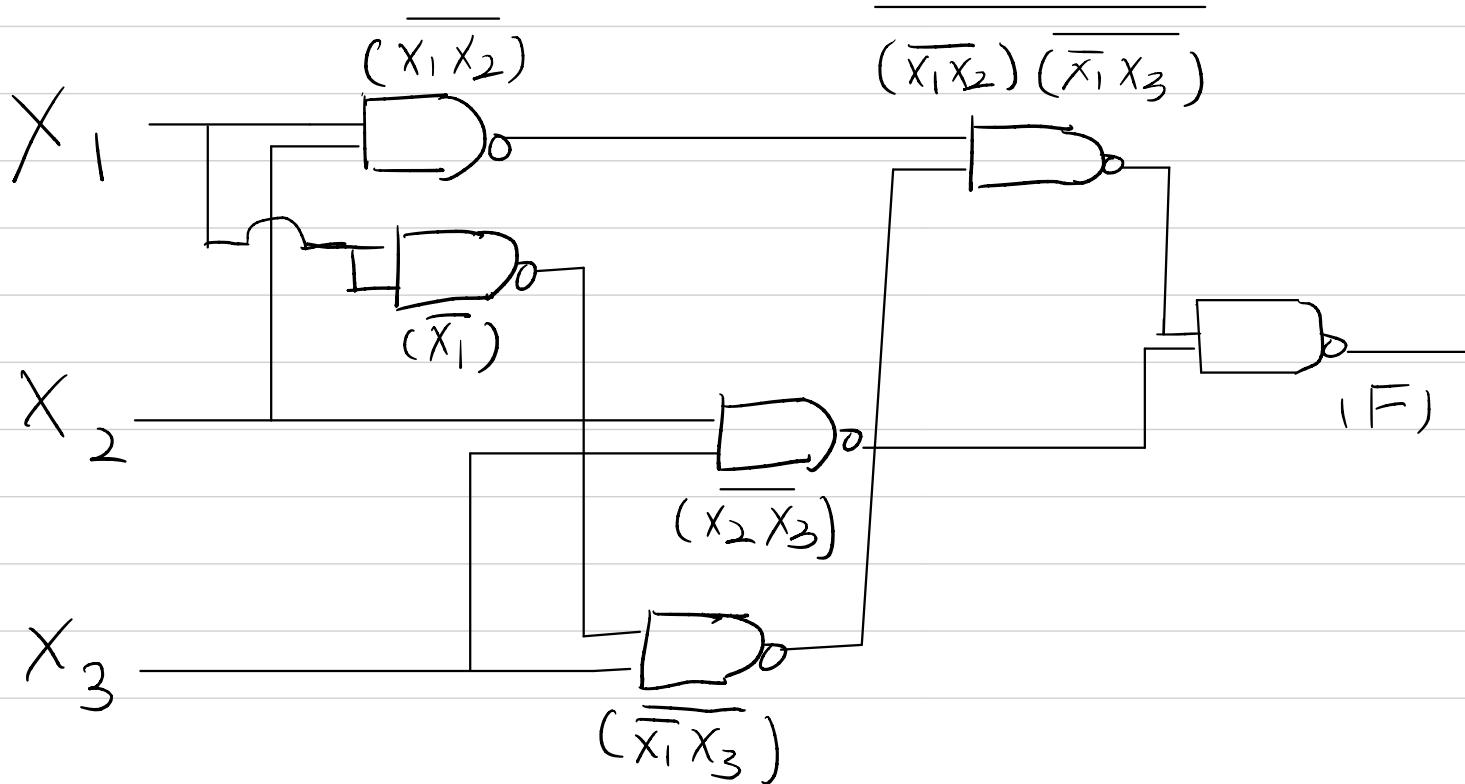


b).

$$F = X_1 X_2 + \overline{X}_1 X_3 + X_2 X_3$$

$$= (\overline{X_1 X_2}) (\overline{\overline{X}_1 X_3}) + X_2 X_3$$

$$= \left(\overline{(X_1 X_2)} \overline{(\overline{X}_1 X_3)} \right) (\overline{X_2 X_3})$$



Q3)

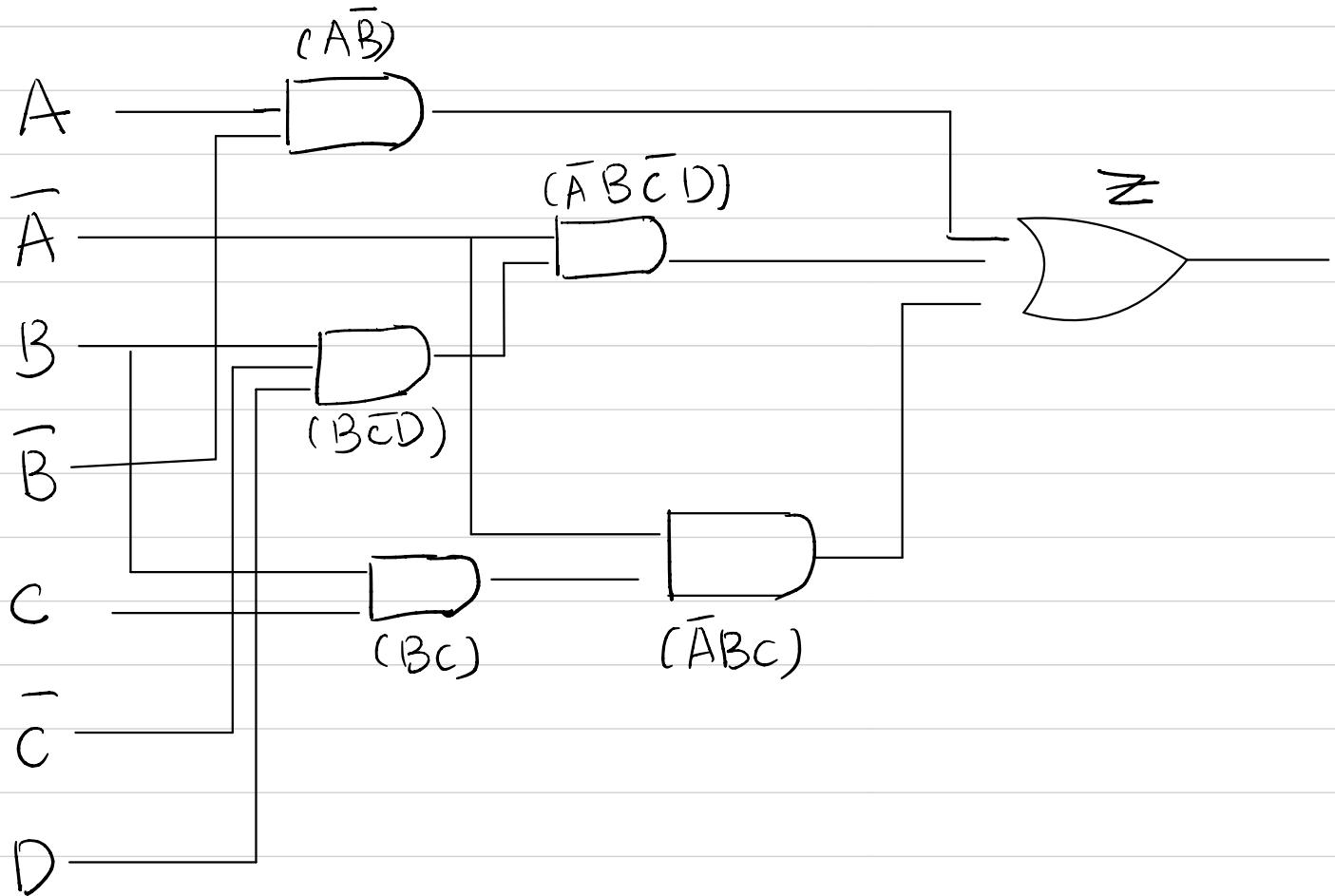
Truth table for output $z = 1$ when $5 \leq ABCD \leq 11$

Binary #	A	B	C	D	Z
≤ 4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	1
7	0	1	1	1	1
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	0
≥ 13	1	1	0	1	0

$$\text{Therefore, } Z = \overline{A} \overline{B} \overline{C} D + \overline{A} B C + A \overline{B}$$

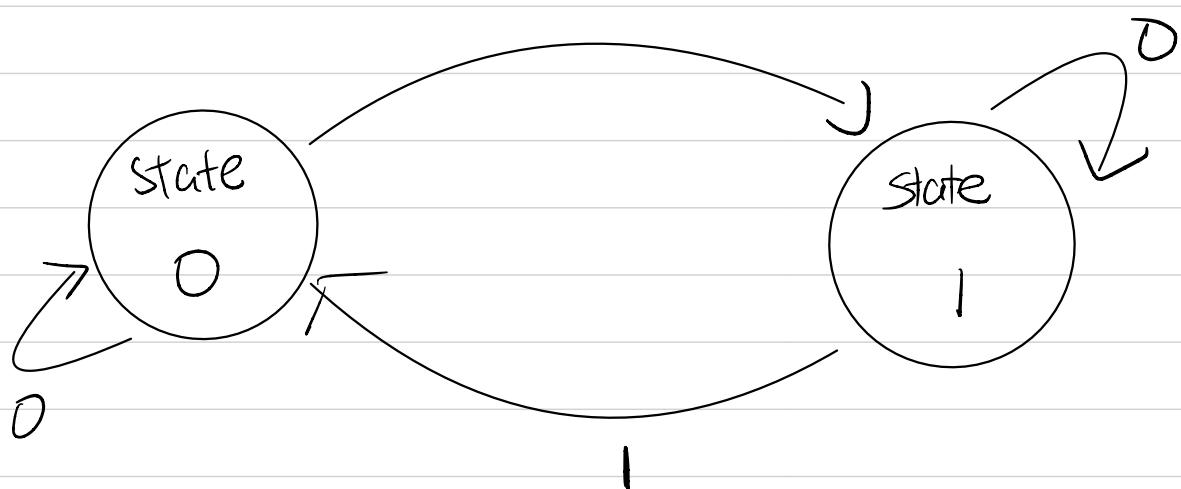
And since I'm allowed to use complement form of ABCD as input.

(next page)



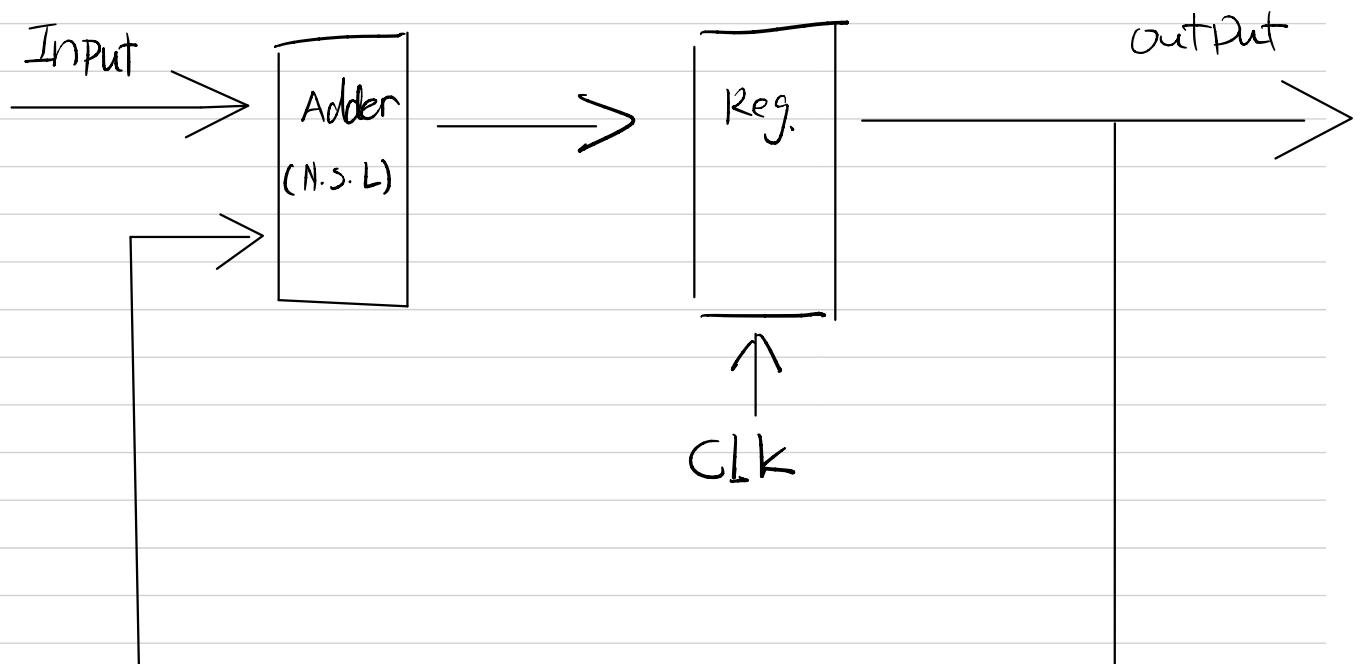
Q4).

FSM

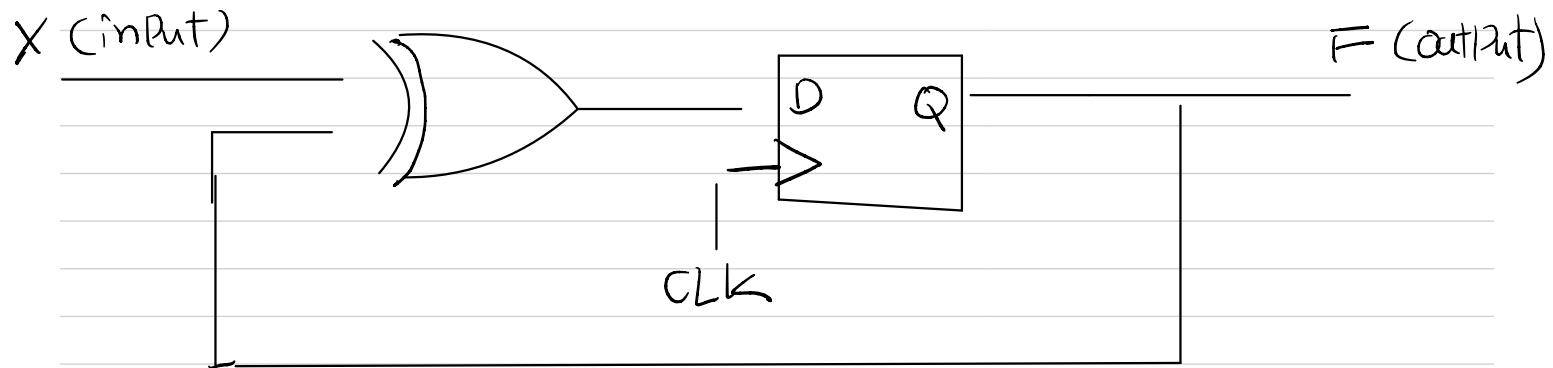


N.S.L truth table:

input	State	state'
1	1	0
0	1	1
1	0	1
0	0	0



Using basic digital component:



- Q5). If the delay for a single FA is 10ps and the delay for a MUX is 6ps. Calculate the total delay for the 8-bit FA illustrated below Fig 3. Assume that the inputs $X[7:0]$ and $Y[7:0]$ are available and valid starting at time $t = 0$. Consider all interconnect delays have zero delay.

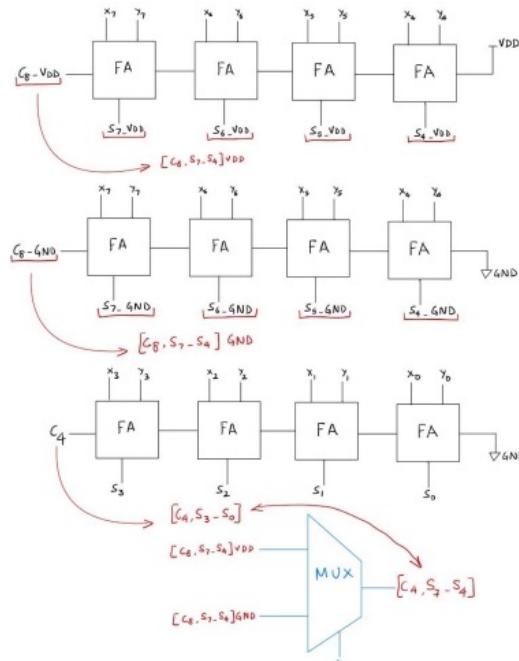


Fig. 3

With given structure, we can observe that $[C_8, S_7 - S_4] V_{DD}$, $[C_8, S_7 - S_4] GND$ and $[C_4, S_3 - S_0] GND$ are parallel and can be compute at the same time, therefore, the total delay for the 8-bit FA is $10 \text{ ps} \times 4 + 6 \text{ ps} = \boxed{46 \text{ ps}}$

Q6).

- The first goal is to improve Full custom ASIC design skills.
 - different styles of logic /design
i.e FSM design
- Another goal is to prepare for interviews and job referrals.
 - From companies, former students or other Prof.
- optional goal is to help us start with Researches

Q7) Let's do this question by define some variable first.

Given that the Jefferson Blvd and McClintock ave intersection is designed to let all pedestrian cross at the same time for all 4 directions,

Let PB = pedestrian pushed button at any time in any direction.

Let JBT = timer for Jefferson blvd's, once it reach the limit, Jefferson blvd should change its light to yellow

Let MAT = timer for McClintock Ave's traffic light, once it reach the limit, McClintock Ave should change it to yellow.

Let JBS = sensor on Jefferson blvd, once it detect there's no vehicles present on Jefferson blvd in the certain time Period, it will

turn Jefferson's blvd to yellow

Let MAS = sensor on McClintock Ave, once it detect there's no vehicles present on McClintock Ave for a period of time, it will turn McClintock Ave to Yellow

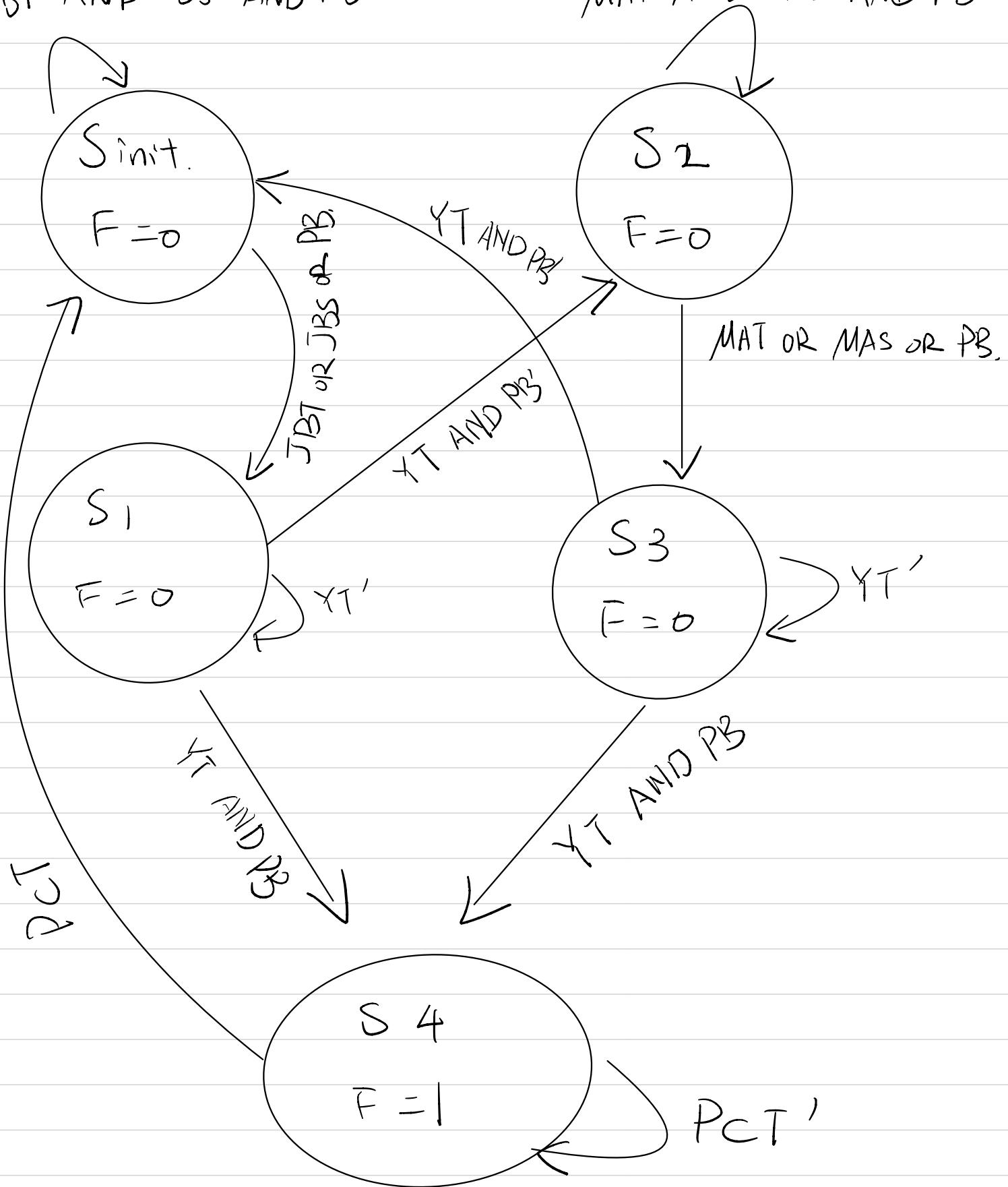
Let YT = Yellow light timer, when it reach to limit, indicate the light should change from yellow to red.

Let PCT = Pedestrian crossing timer, once it hit the limit, pedestrian should not cross the intersection any more.

Let F = output, since this is a one-hot encoded FSM, $F=0$ represents pedestrian should not cross the intersection, else, $F=1$ means pedestrian can cross the intersection (see next page for FSM)

JBT' AND JBS' AND PB'

MAT' AND MAS' AND PB'



Define states:

S_{init} = when Jefferson blvd has a green light, and McClintock has a red light

S_1 = when Jefferson blvd has a yellow light, and McClintock Ave has a red light

S_2 = when McClintock Ave has a green light and Jefferson blvd has a red light,

S_3 = when McClintock Ave has a yellow light, and Jefferson blvd has a red light.

(Pedestrians should not cross the intersection at any states above)

S_4 = when both Jefferson blvd and McClintock ave have red lights, and Pedestrians can cross the intersection.

The truth table for the FSM above is too big, I'll split into different truth tables, each represents one state's transition

For state init

JBT	JBS	PB	MAT, MAS, YT, PCT	next state	F
1	1	1	*	S ₁	0
1	1	0	*	S ₁	0
1	0	1	*	S ₁	0
1	0	0	*	S ₁	0
0	1	1	*	S ₁	0
0	1	0	*	S ₁	0
0	0	1	*	S ₁	0
0	0	0	*	Sinit	0

For State 1

YT	PB	JBT, MAT, JBS, MAS, PCT	next state	F
1	1	*	S ₄	1
1	0	*	S ₂	0
0	1	*	S ₁	0
0	0	*	S ₁	0

For State 2

MAT	MAS	PB	JBT, JBS, YT, PCT	next state	F
1	1	1	*	S ₃	0
1	1	0	*	S ₃	0
1	0	1	*	S ₃	0
1	0	0	*	S ₃	0
0	1	1	*	S ₃	0
0	1	0	*	S ₃	0
0	0	1	*	S ₃	0
0	0	0	*	S ₂	0

For State 3

YT	PB	JBT, JBS, MAT, MAS, PCT	next state	F
1	1	*	S ₄	1
1	0	*	Sinit	0
0	1	*	Sinit	0
0	0	*	Sinit	0

For State 4

PCT	PB, YT, JBT, JBS - MAT, MAS, PCT	Next state	F
1	*	Sinit	0
0	*	S ₄	1

Ref)

Q1) physics . nmu . edu / ~ddonovan / classes / Nph 320 /
Homework / ch08 / ch08P06 D10 . pdf .

Q7) unm . edu / ~zbaker / ece238 / slides / 19 . pdf

All) 2024 EE - 477 lecture materials .