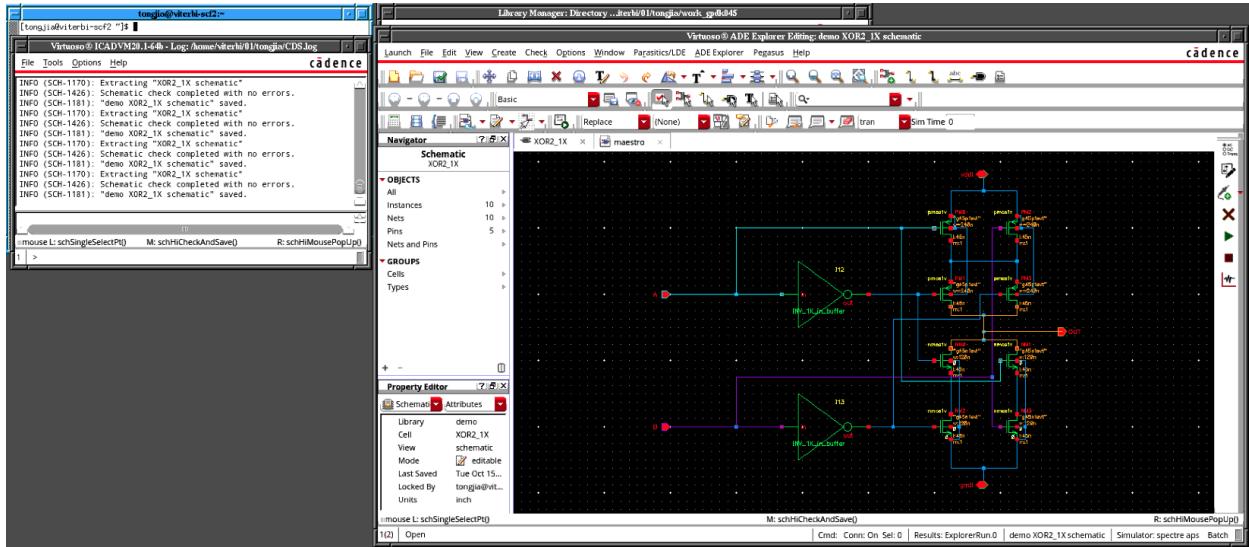


EE407L Lab1 Part2

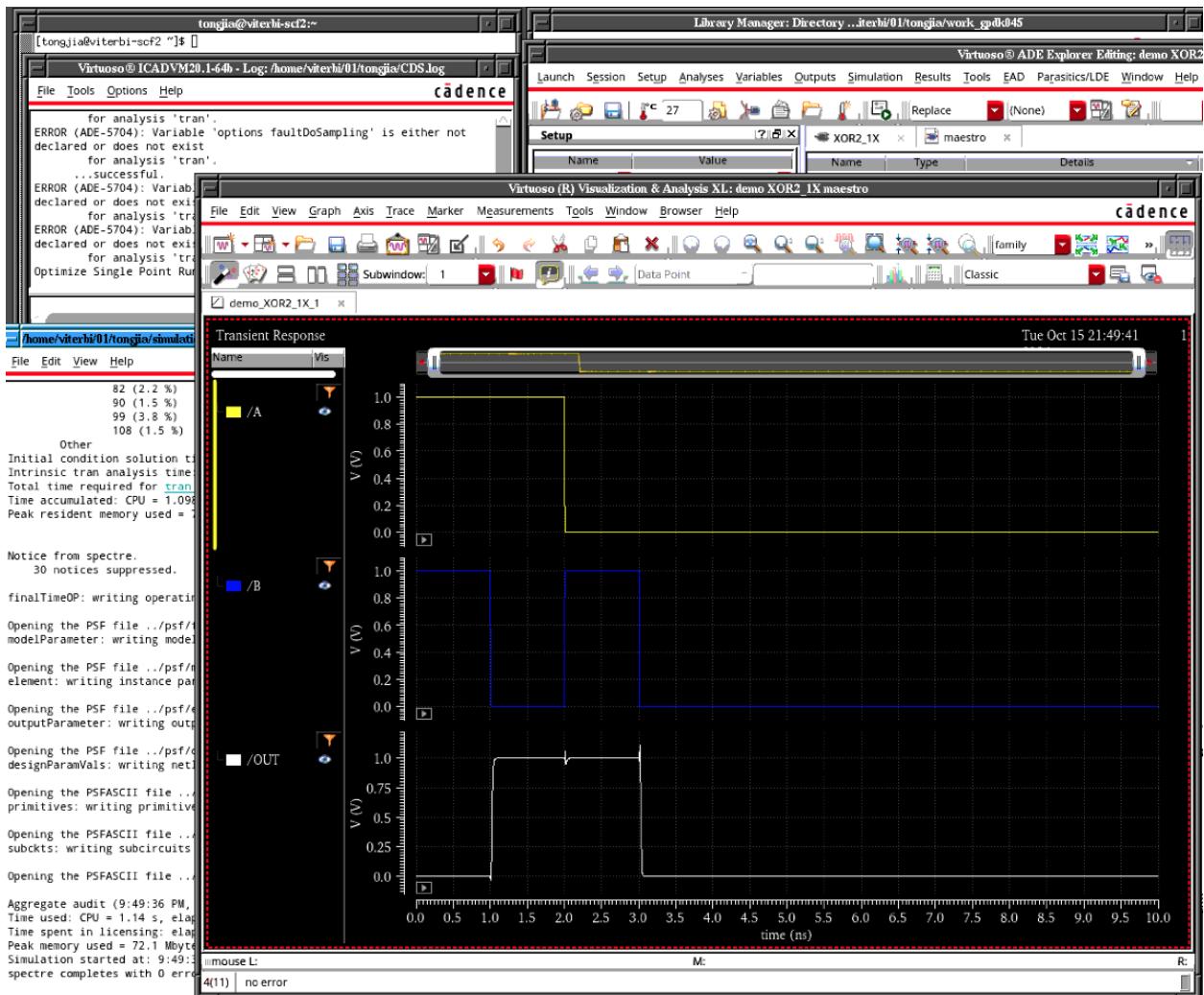
Tong Jia
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Part1)

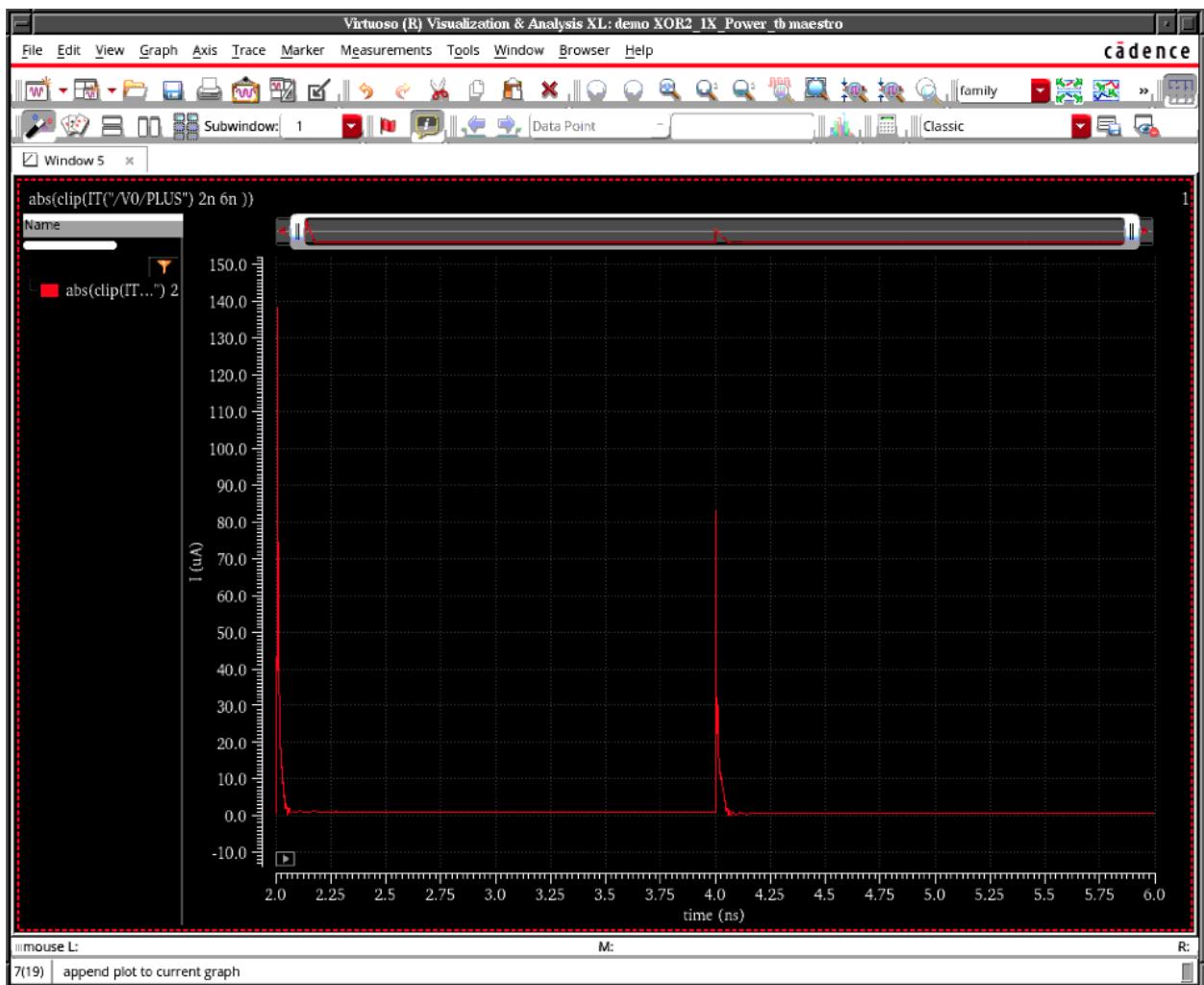
XOR schematic



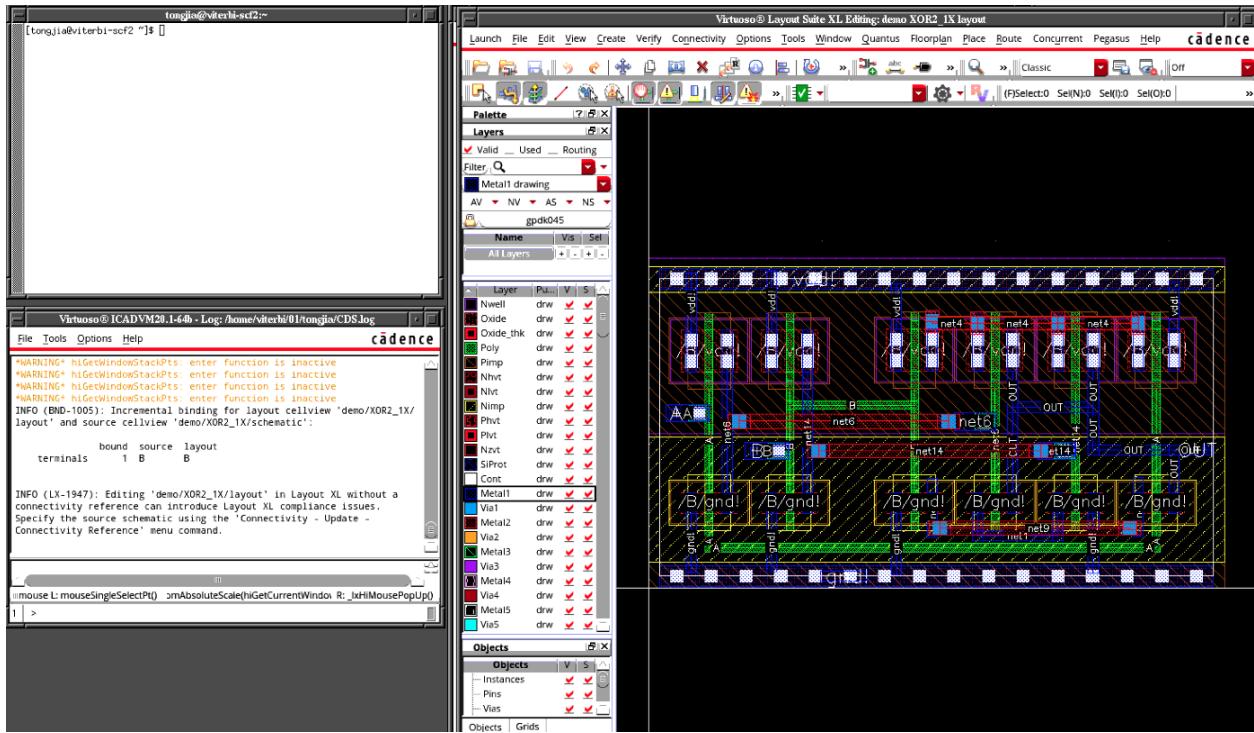
Functionality waveform on schematic



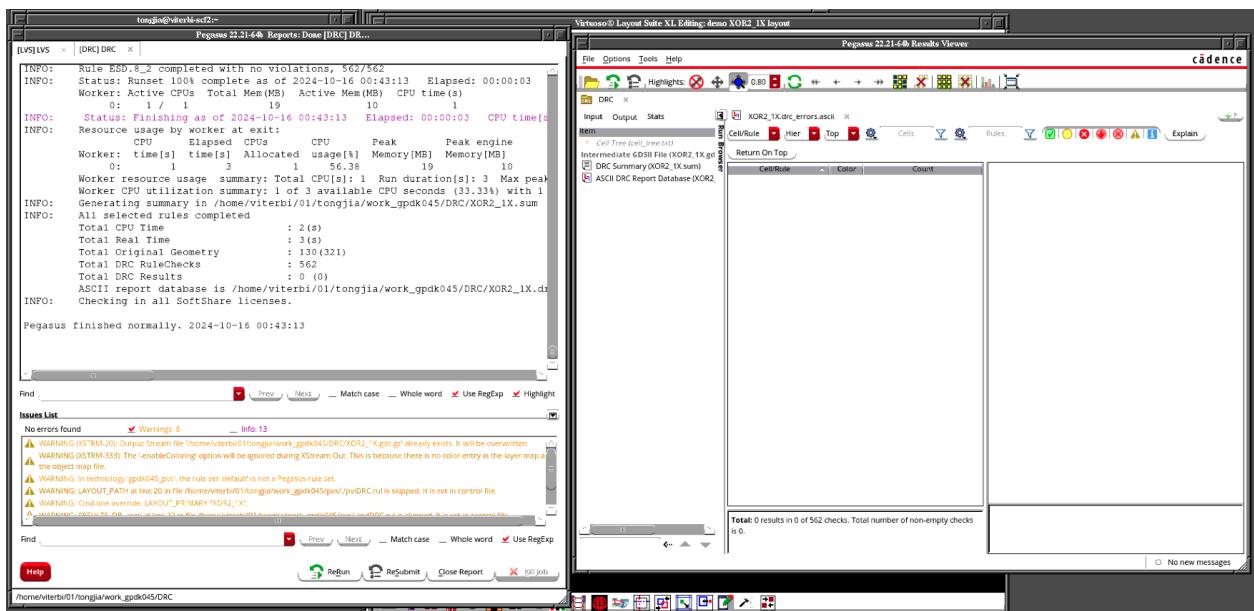
Average power measurement on schematic



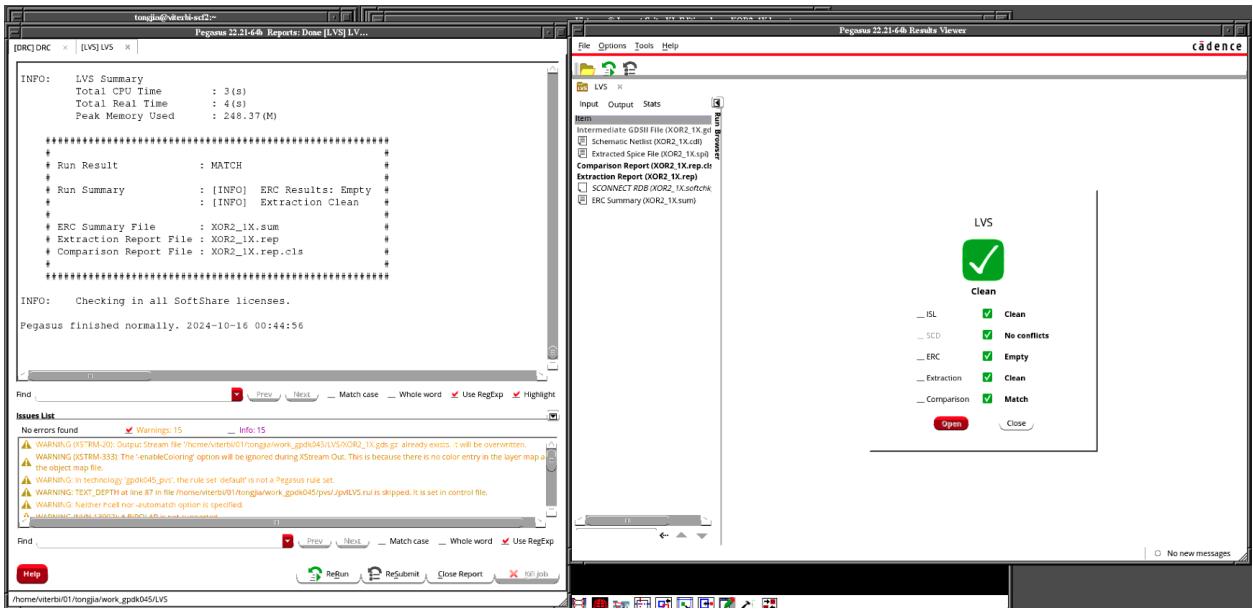
XOR layout



DRC



LVS



Part2 a)

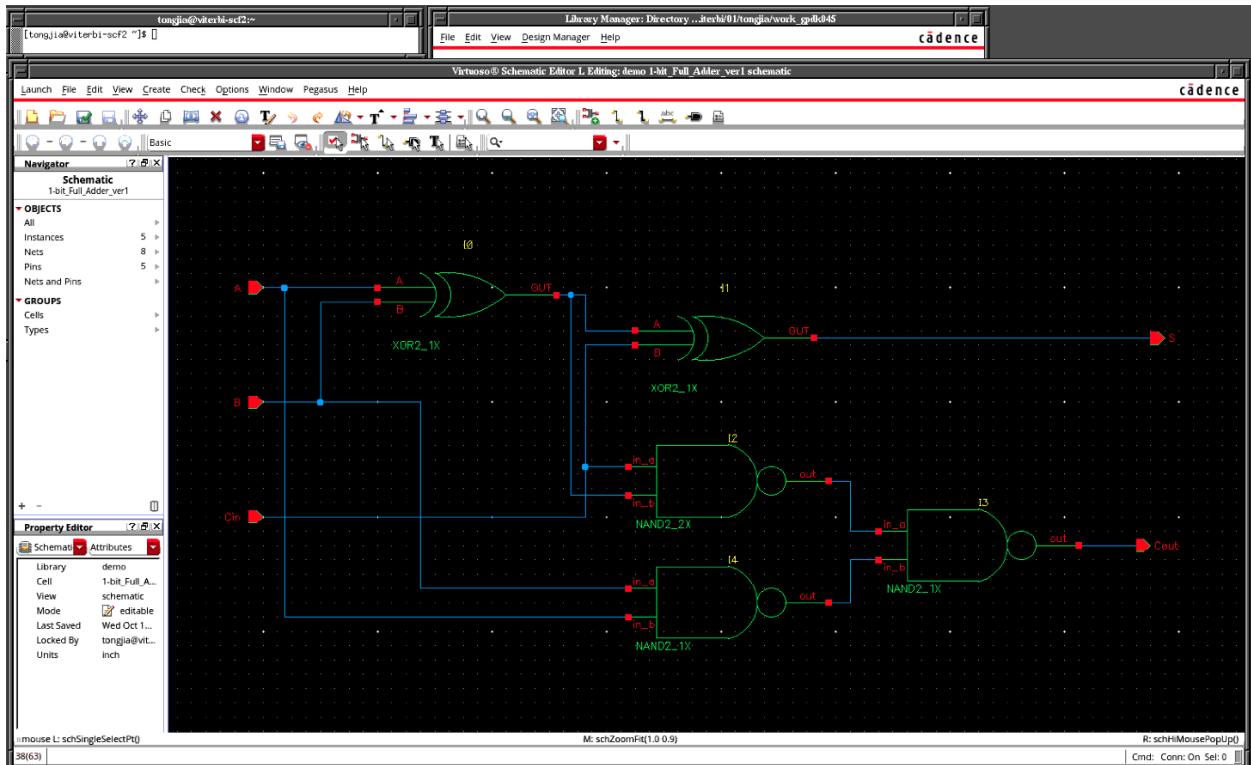
Comb1 (P = NAND2_2X, Q = NAND2_1X) ave delay = **54.25ps**

Comb2 (P = NAND2_4X, Q = NAND2_2X) ave delay = 71.43ps

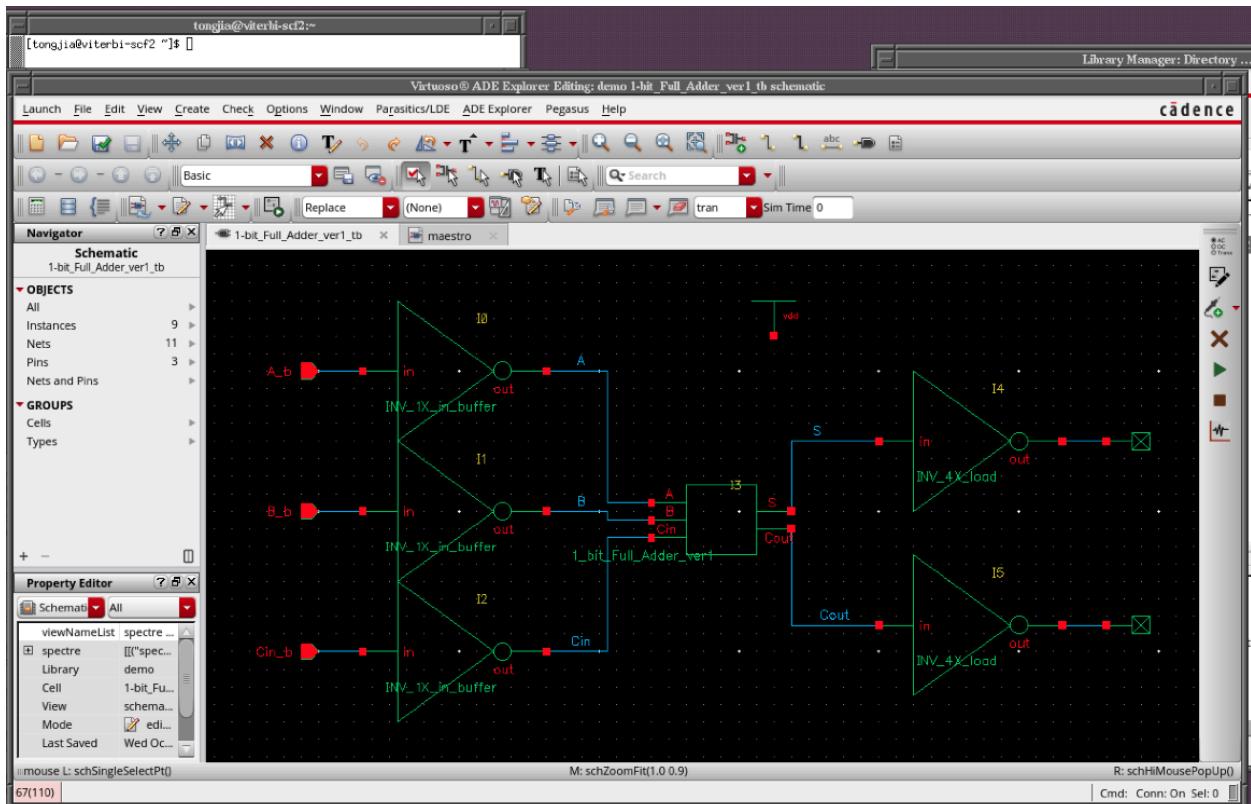
Comb3 (P = NAND2_4X, Q = NAND2_4X) ave delay = 83.22ps

Hence, comb1 (P = NAND2_2X, Q = NAND2_1X) has the least average delay

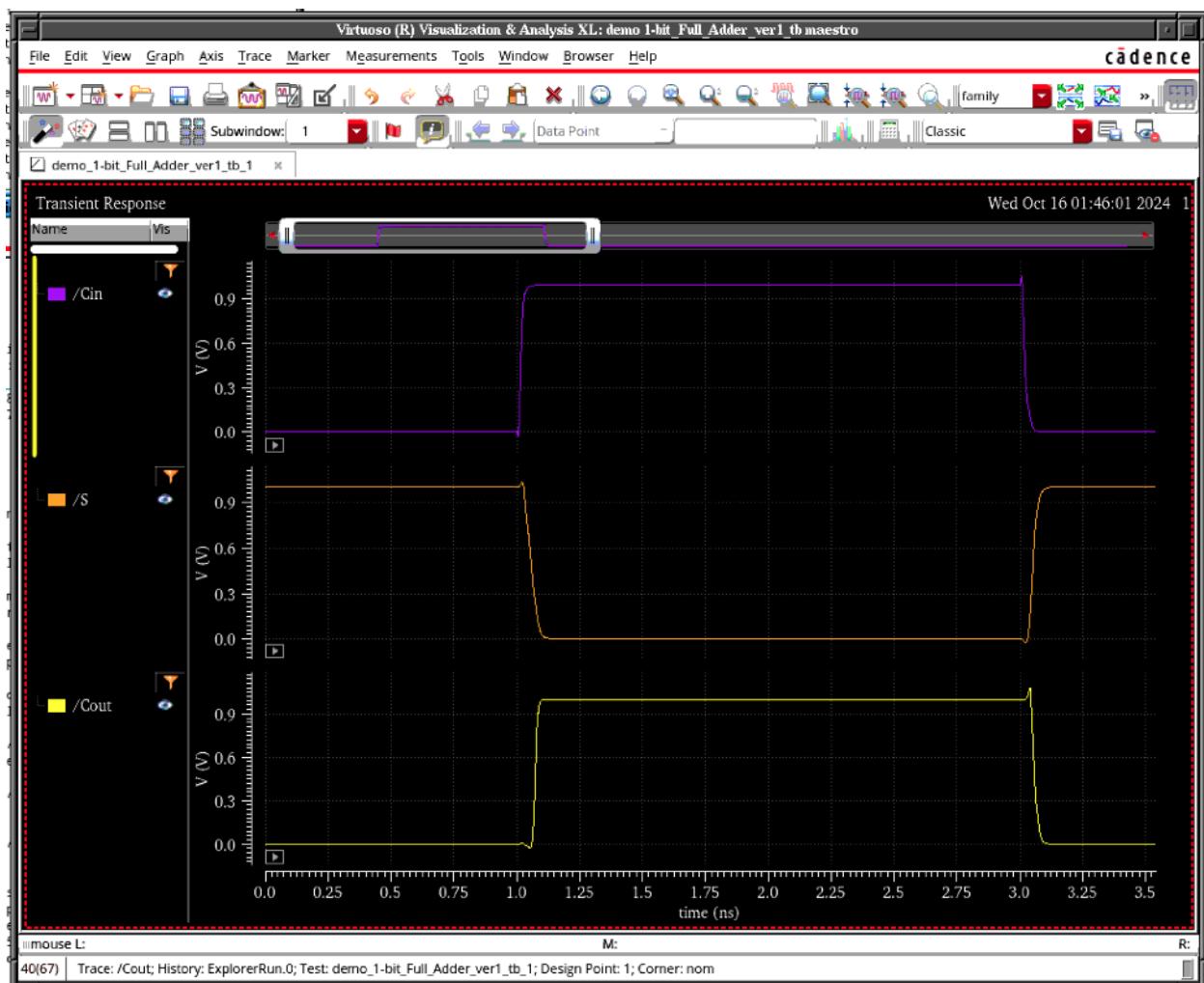
Schematic of final design which gives the least average delay from Cin to Cout.



(DUT, not required)



Functionality waveforms (with A = 0, B = 1)



DUT schematic (with A = 0, B = 1):
 Schematic Cout rising delay = 62.45ps



Schematic Cout falling delay = 46.05ps



Schematic Sum falling delay = 48.32ps

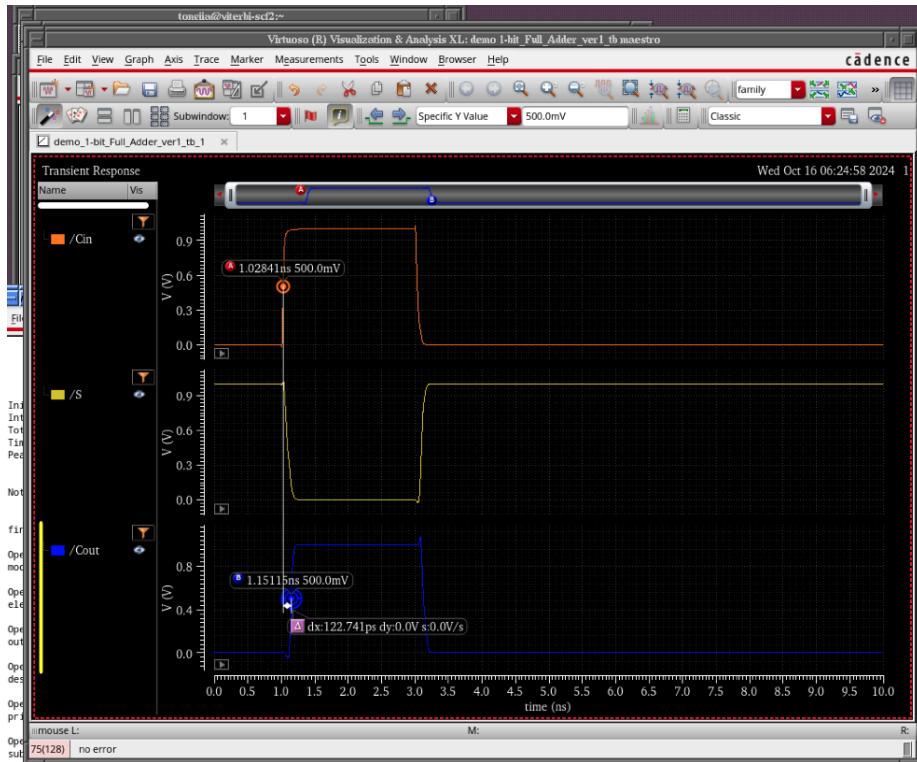


Schematic Sum rising delay = 44.32ps



DUT layout (with A = 0, B = 1):

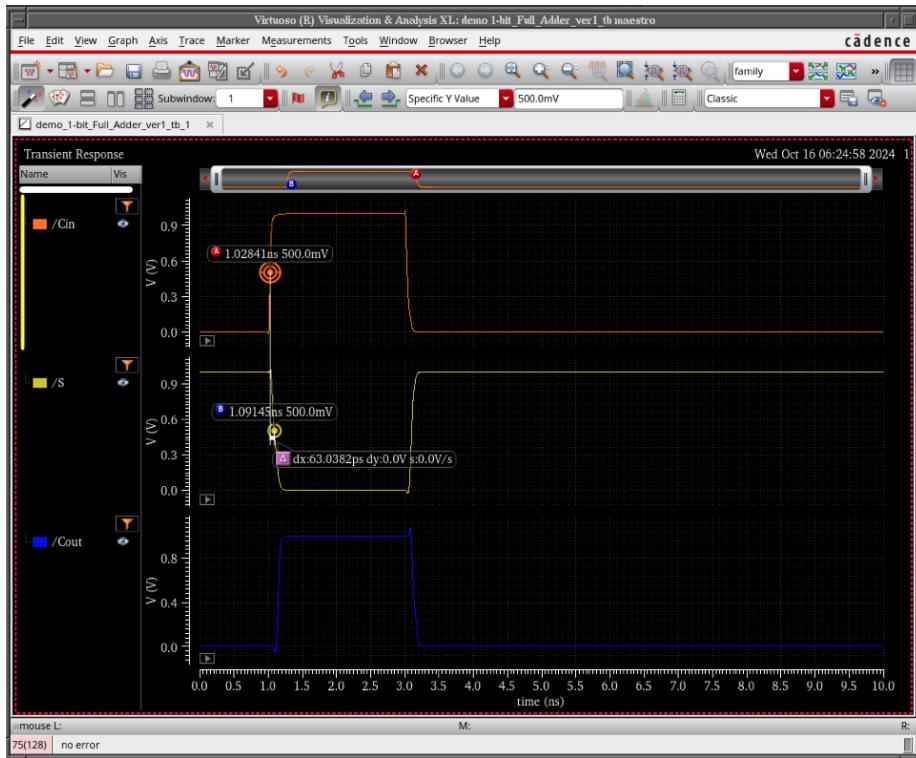
Layout Cout rising delay = 122.74ps



Layout Cout falling delay = 89.40ps



Layout Sum falling delay = 63.04ps



Layout Sum rising delay = 62.82ps



Therefore:

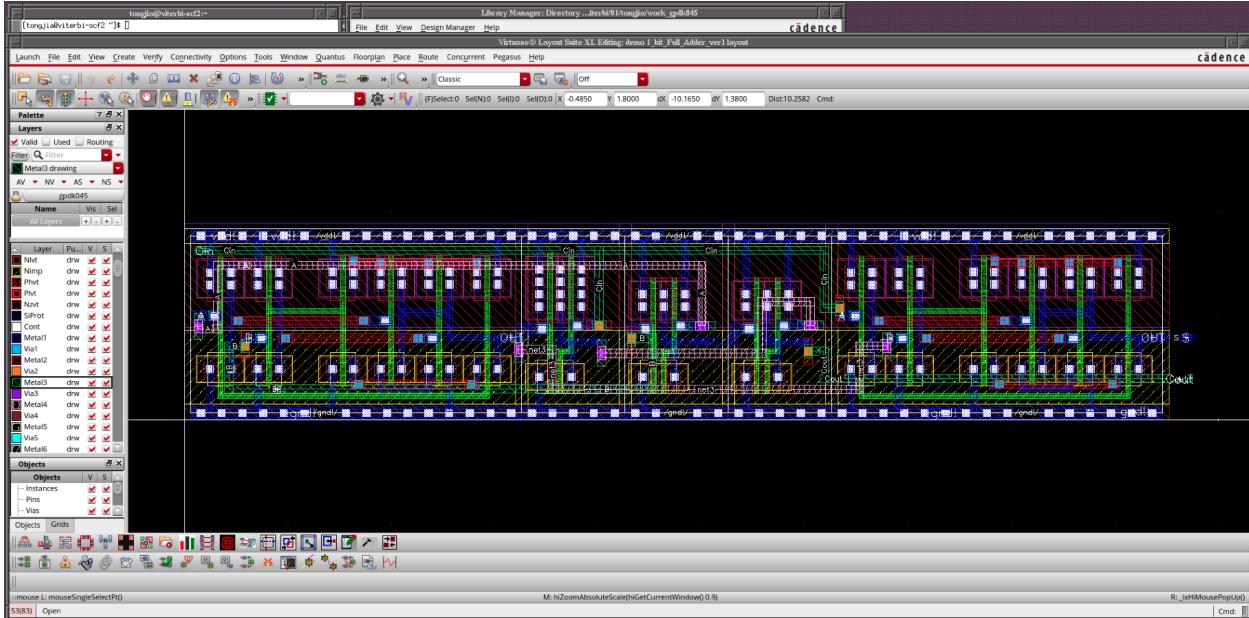
Average delay for Schematic from Cin to Cout = 54.25ps

Average delay for Schematic from Cin to Sum = 46.32ps

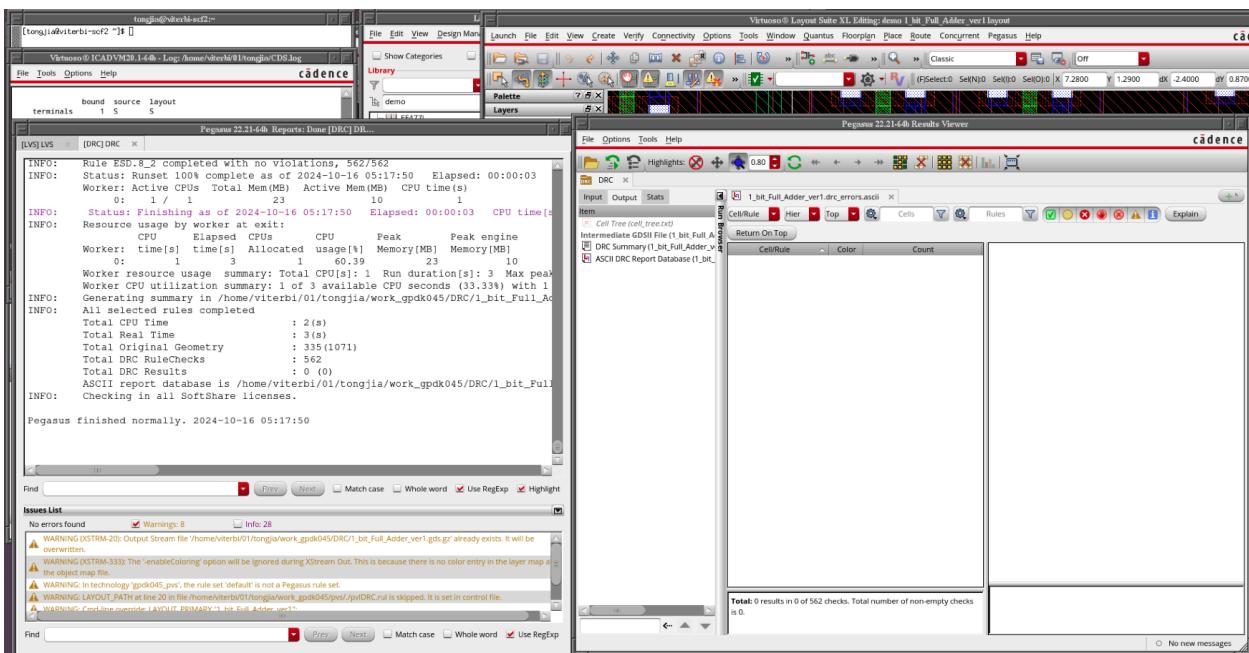
Average delay for Layout from Cin to Cout = 106.07ps

Average delay for Layout from Cin to Sum = 125.86ps

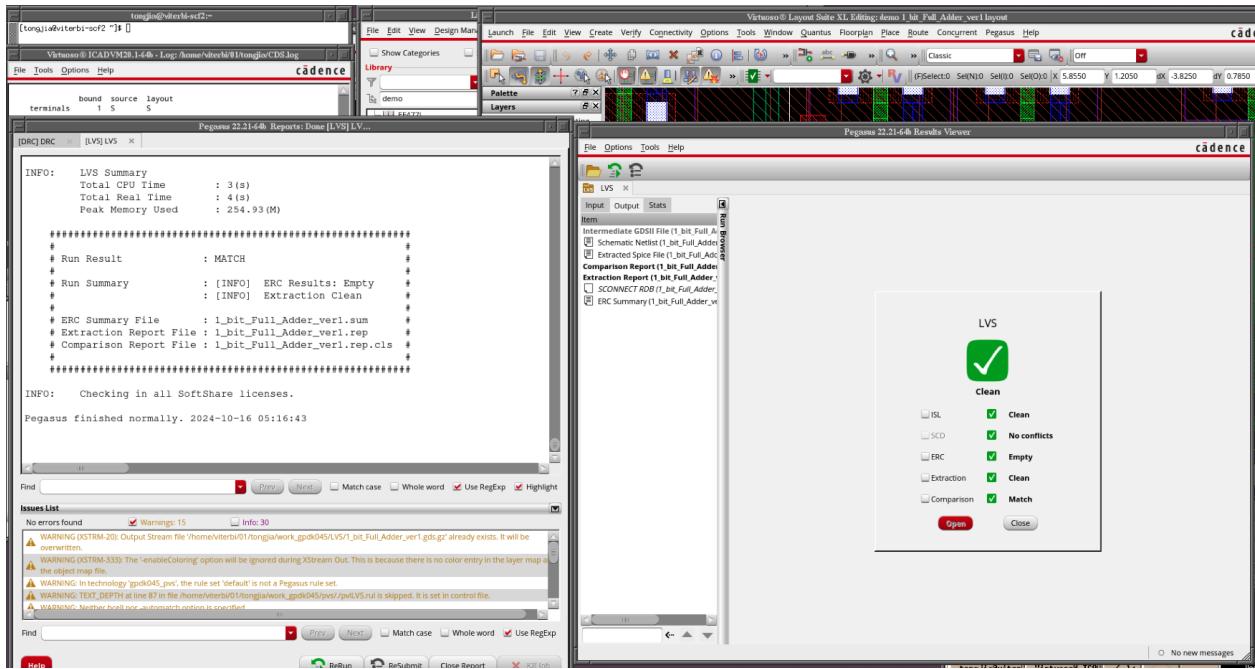
Layout



DRC

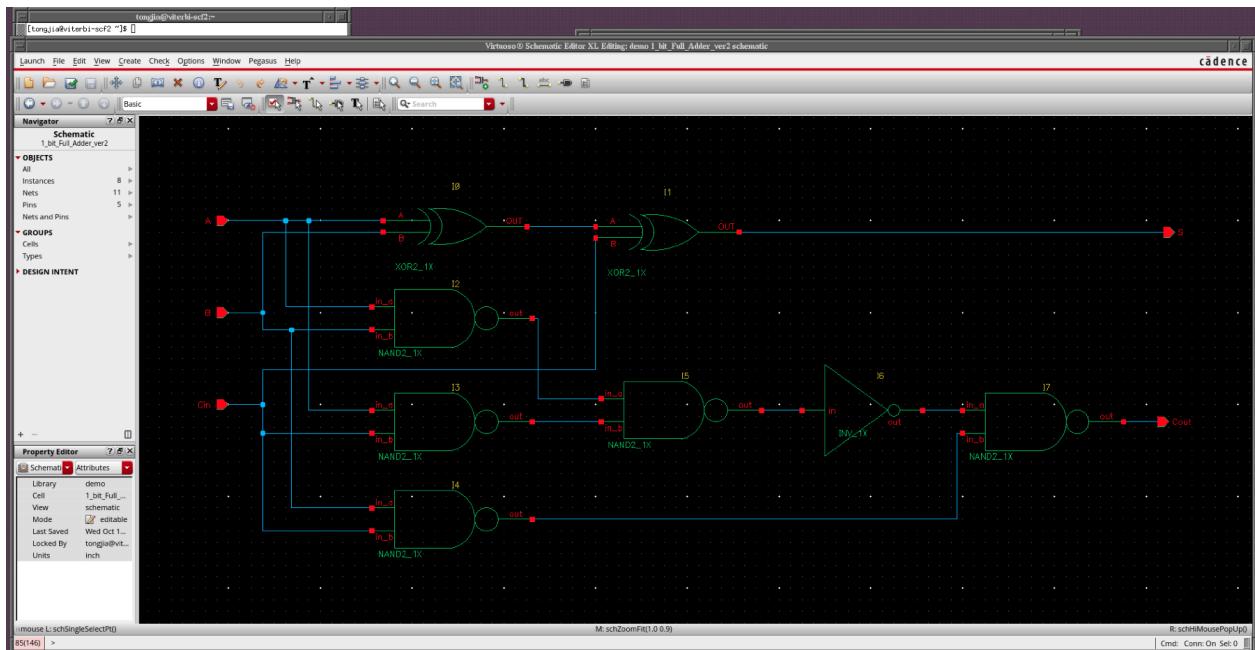


LVS

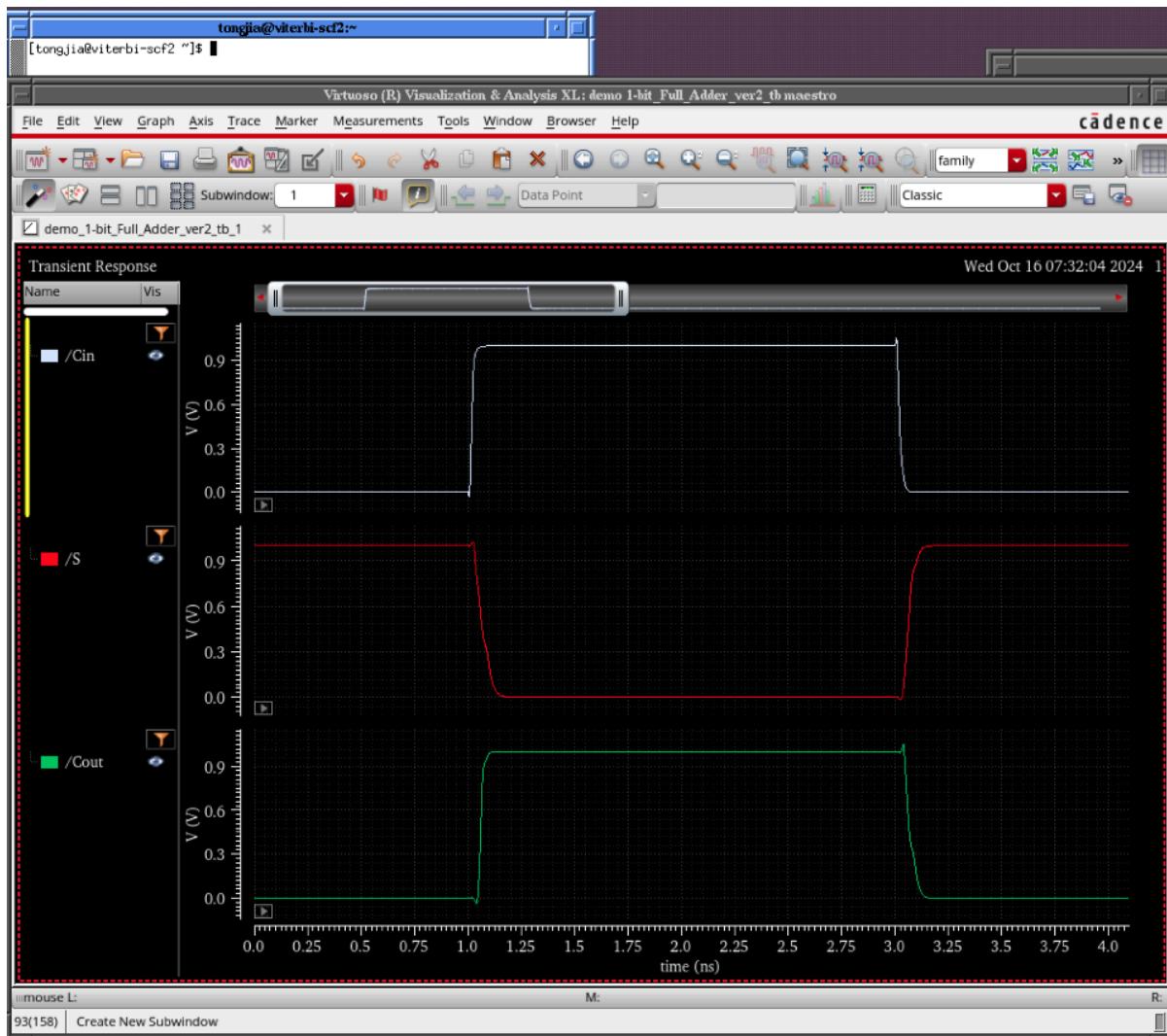


Part2 b)

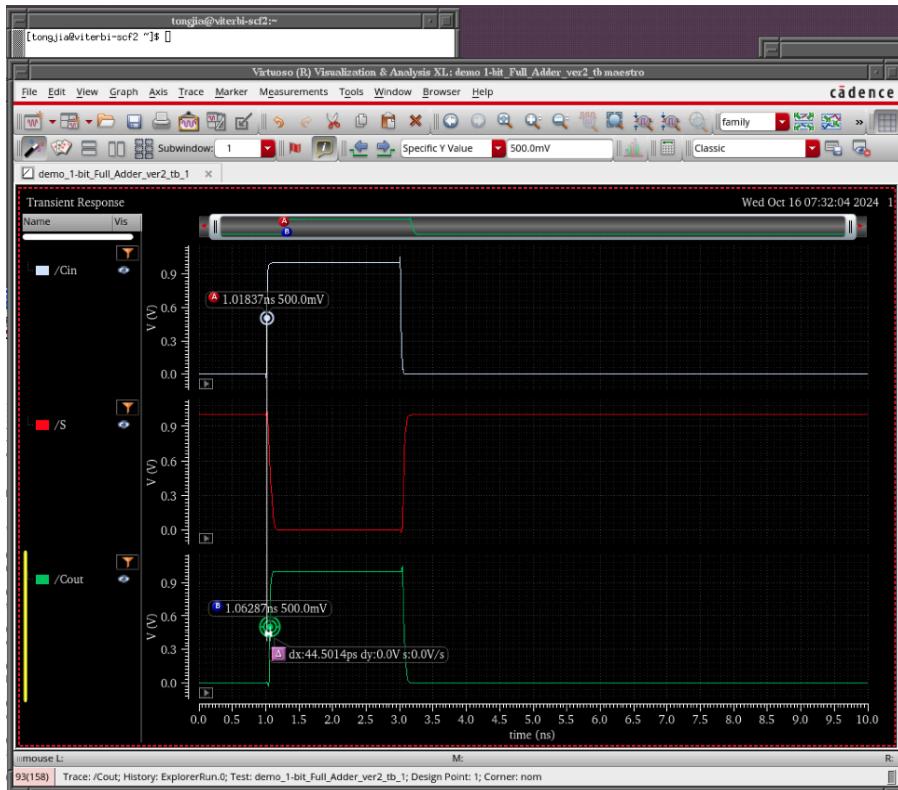
Schematic of design



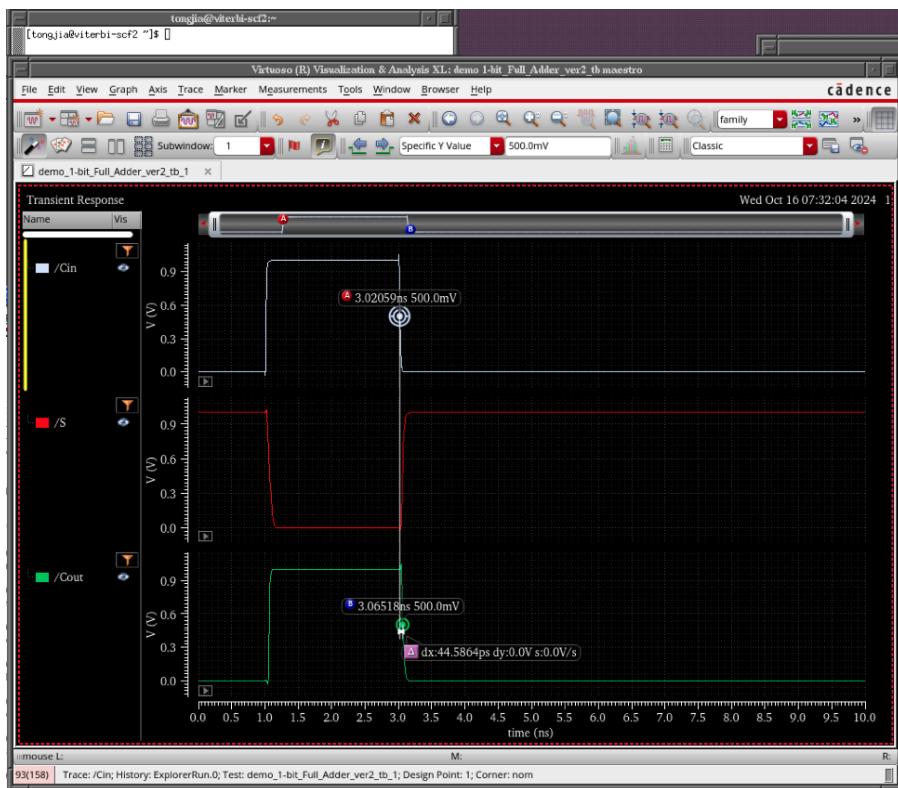
Functionality waveforms (with A = 0, B = 1)



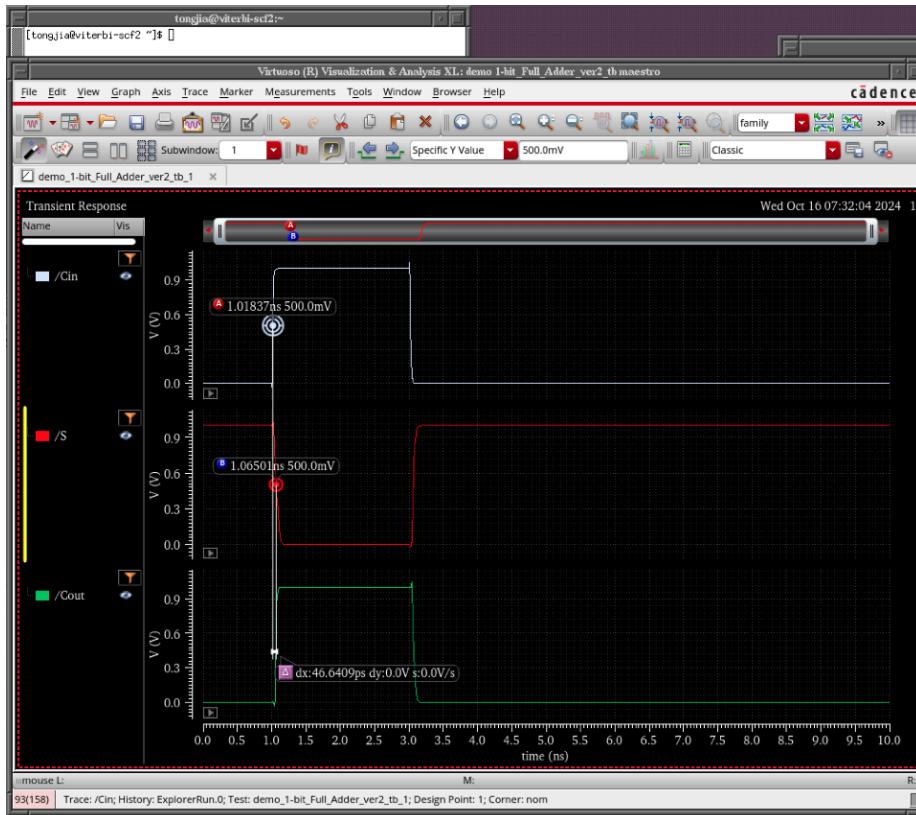
DUT schematic (with A = 0, B = 1):
 Schematic Cout rising delay = 44.50ps



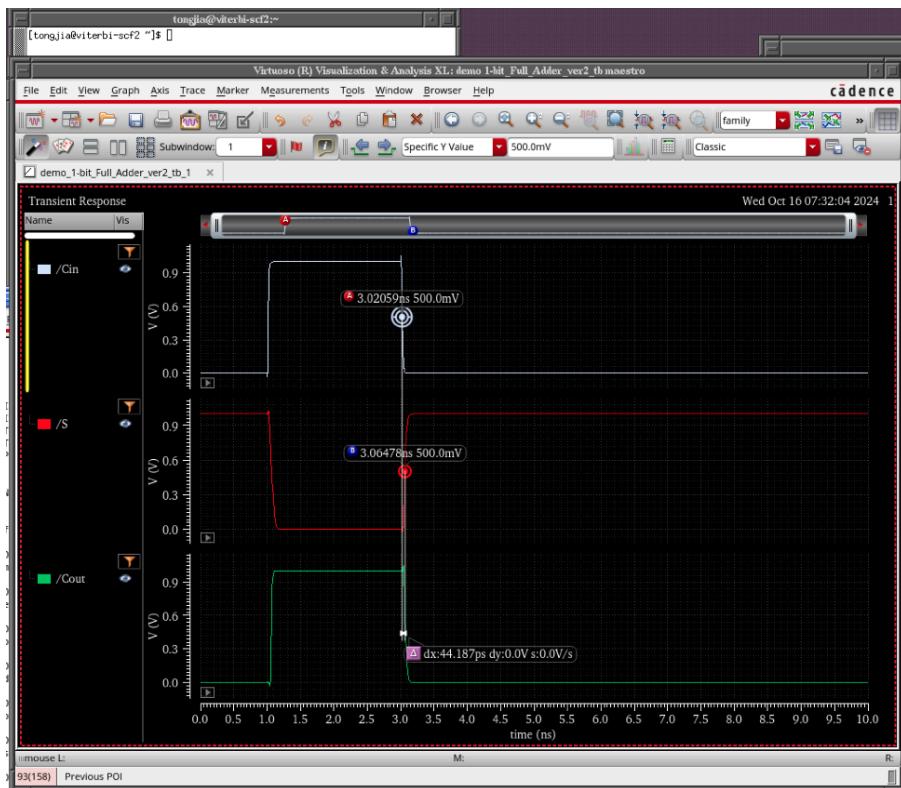
Schematic Cout falling delay = 44.59ps



Schematic Sum falling delay = 46.64ps



Schematic Sum rising delay = 44.19ps



Therefore:

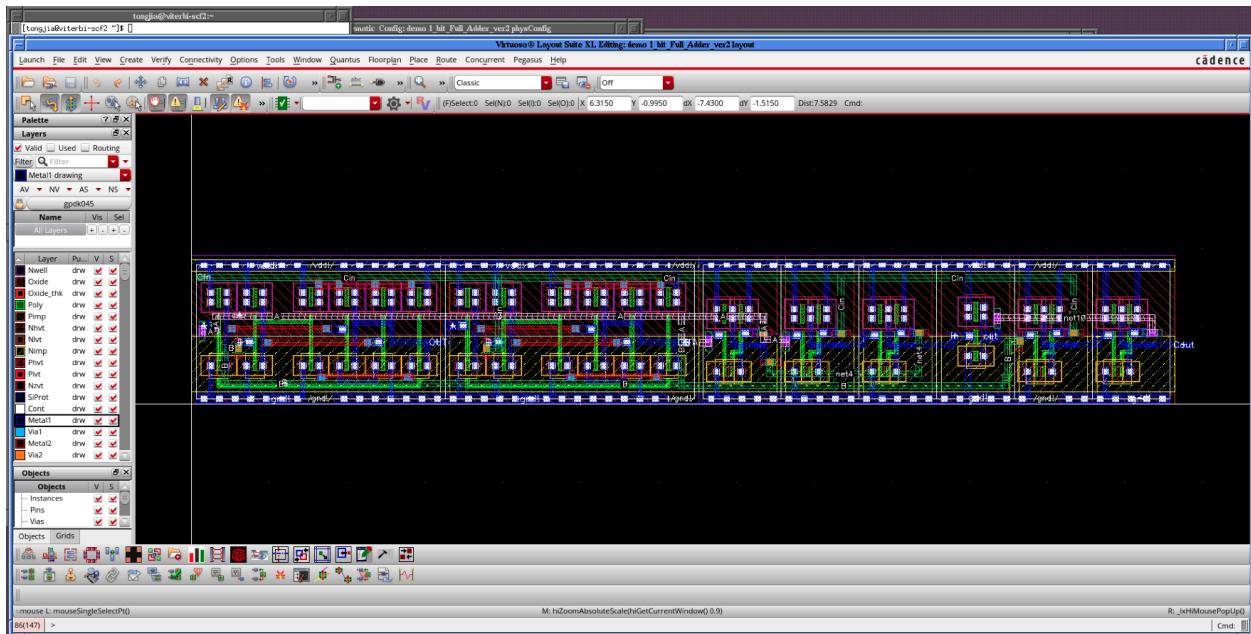
Average delay for *Schematic* from Cin to Cout = 44.55ps

Average delay for *Schematic* from Cin to Sum = 45.42ps

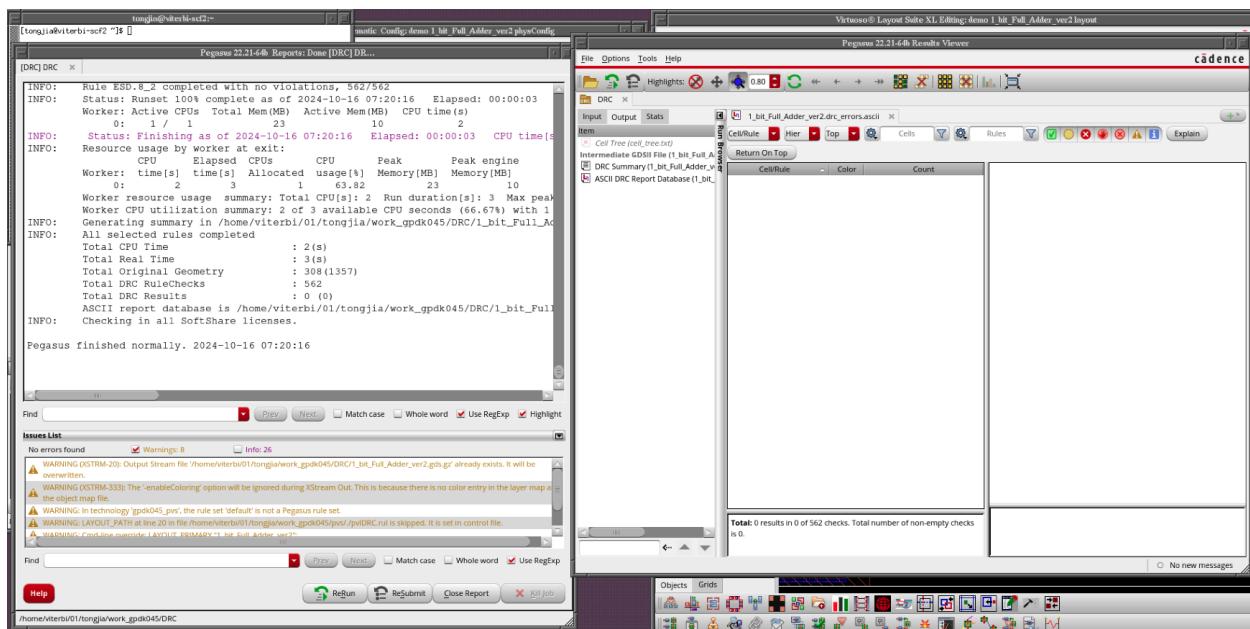
The average delay from Cin to Cout is approximately 10 ps less than in part a, while the average delay from Cin to Sum remains roughly the same.

I believe the lower delay in part b is due to some of NAND gates receiving inputs directly from the input pins, whereas in part a, one of the NAND gates takes input from the output of an XOR gate.

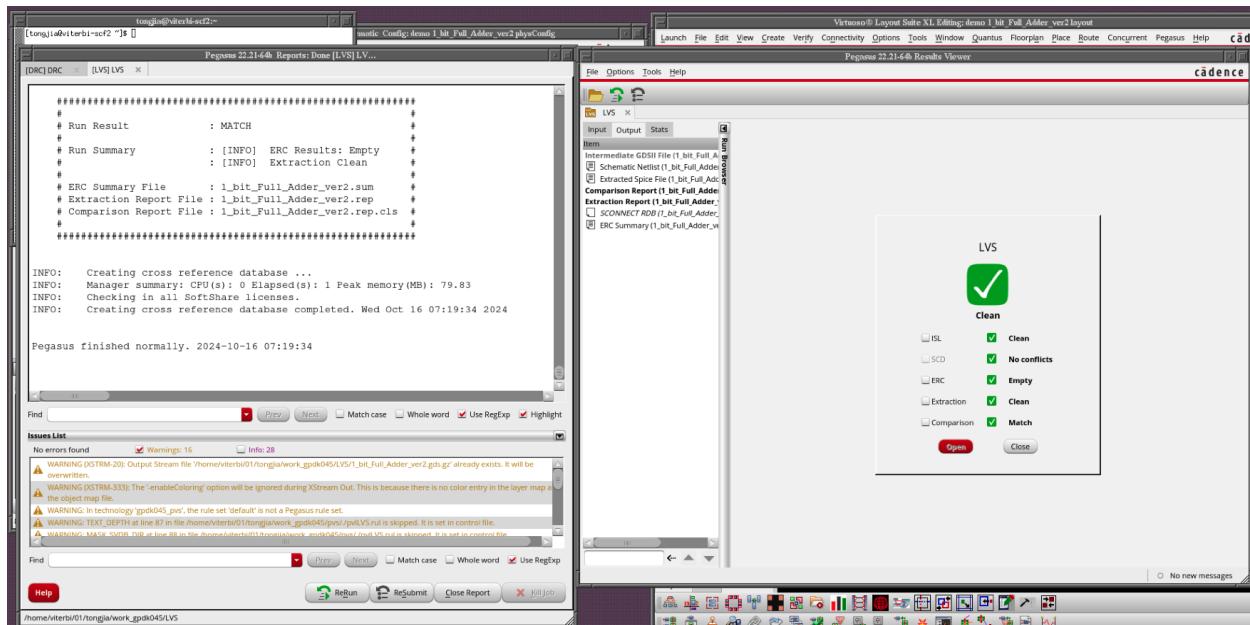
Layout



DRC

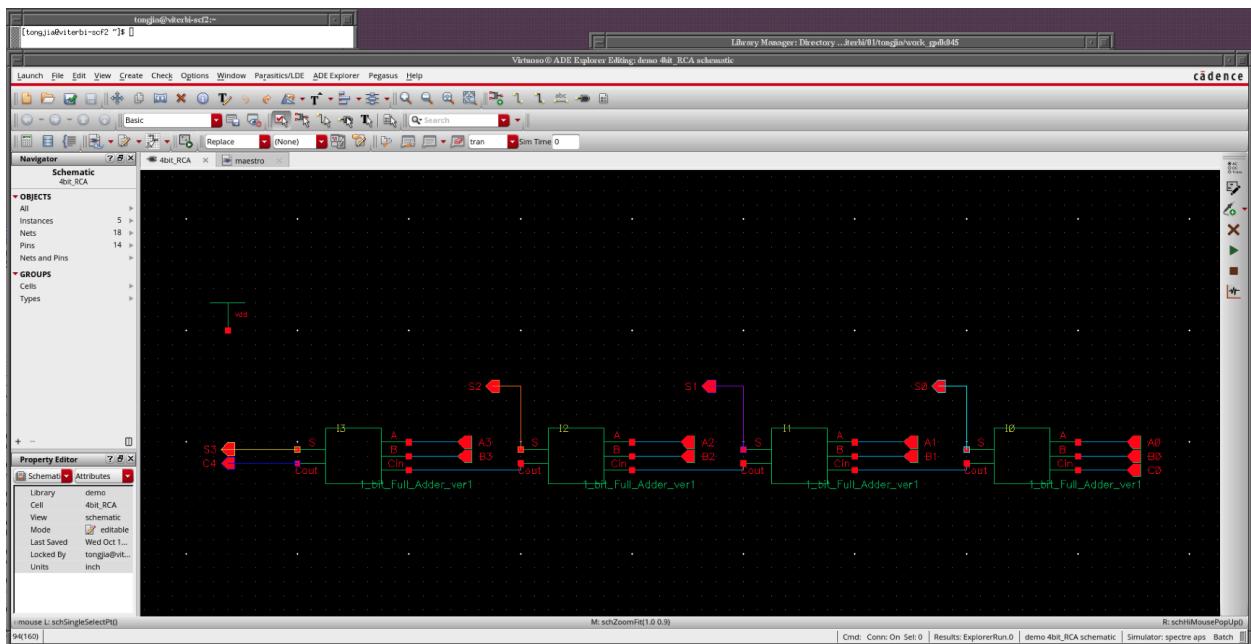


LVS



Part3)

Schematic

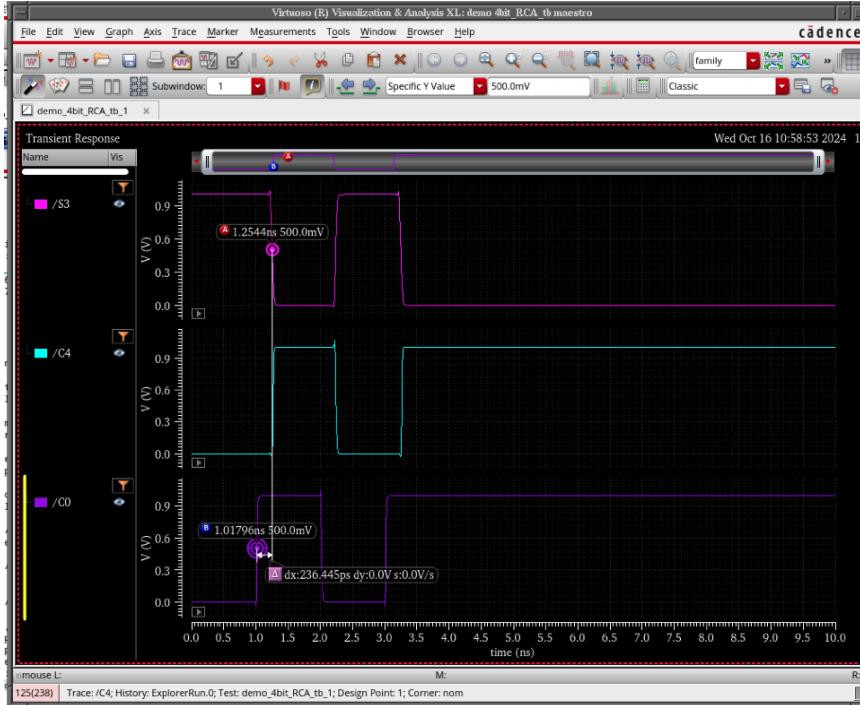


Functionality waveforms (A = 15, B = 15, C0 = 1)

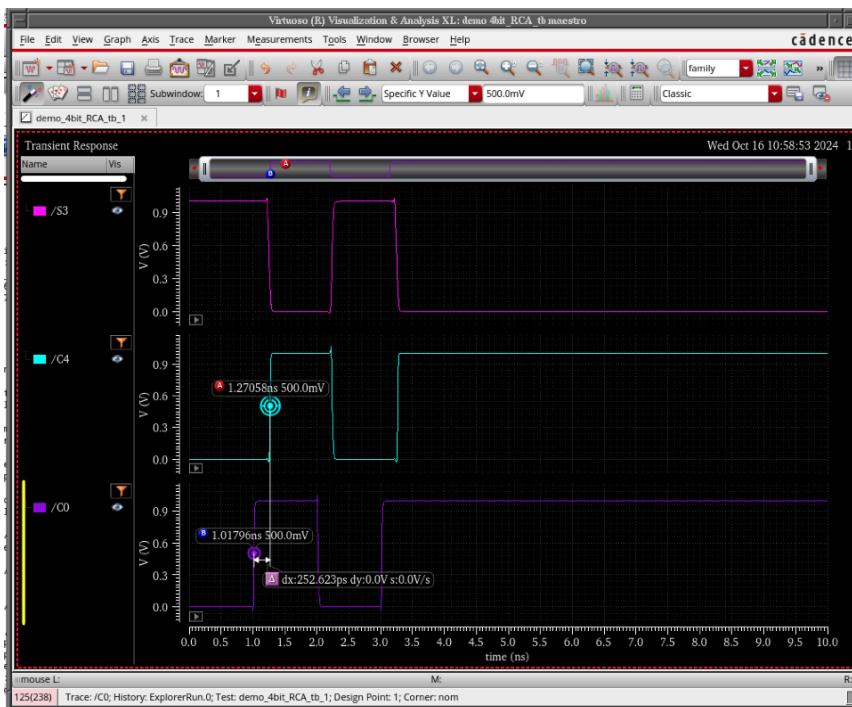


For worst case scenario, I choose [000011110] → [000011111]
 (for [A3,A2,A1,A0,B3,B2,B1,B0,C0])

worst case delay for S3 = 236.45ps

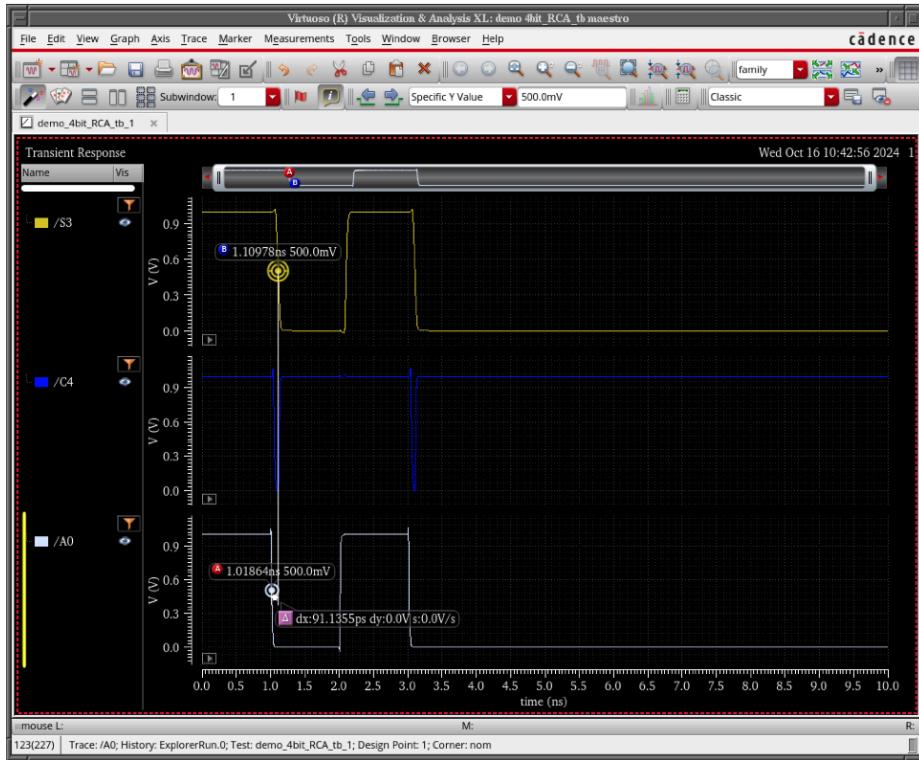


worst case delay for C4 = 252.62ps

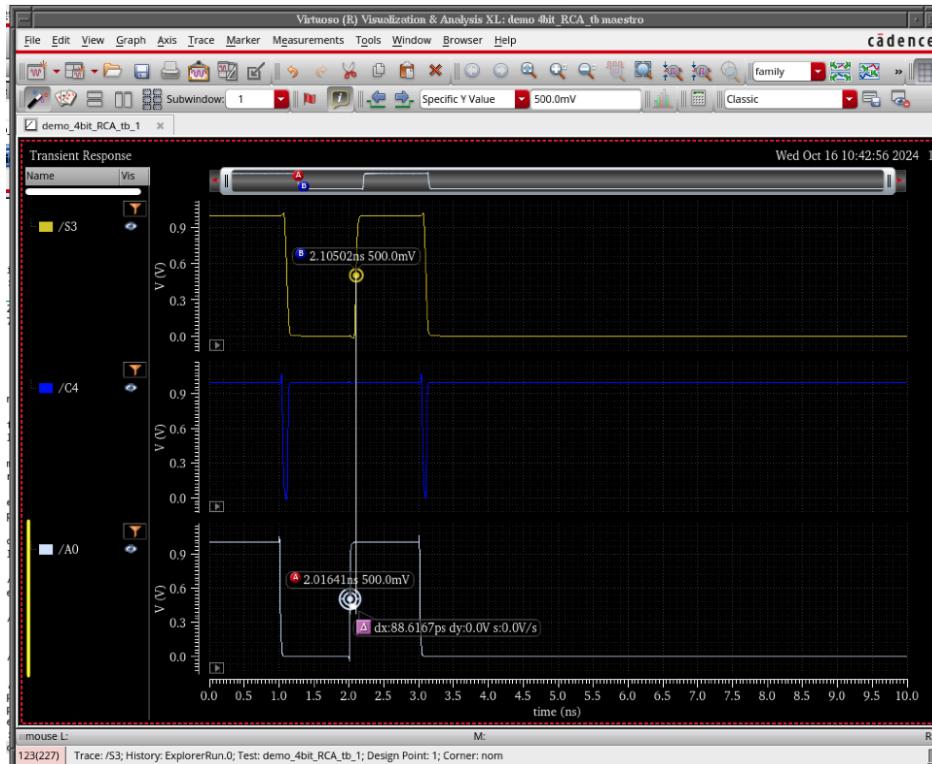


Average delays for S3 and C4:

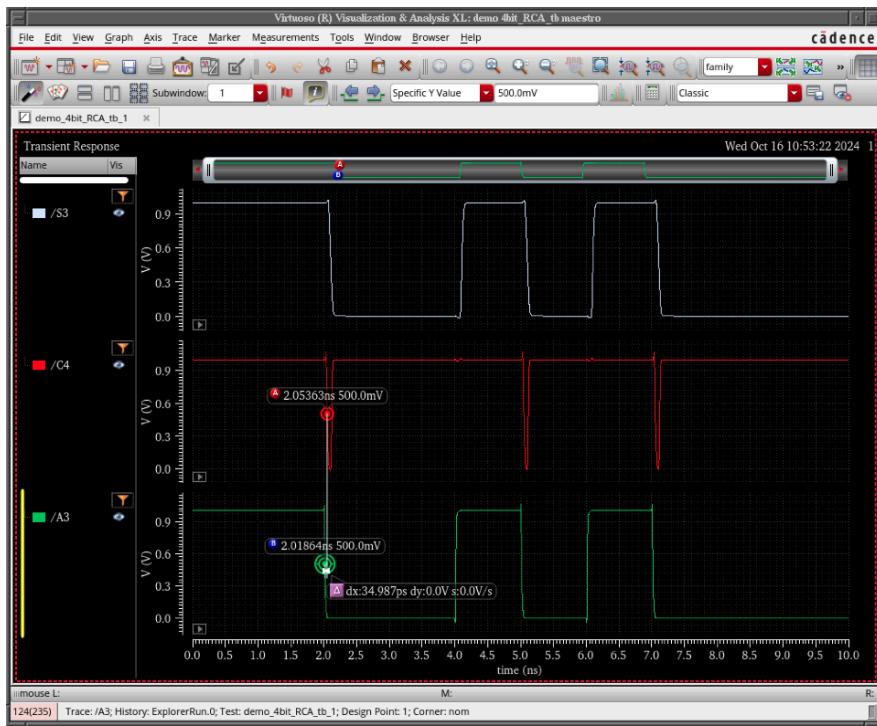
S3 falling delay = 91.14ps



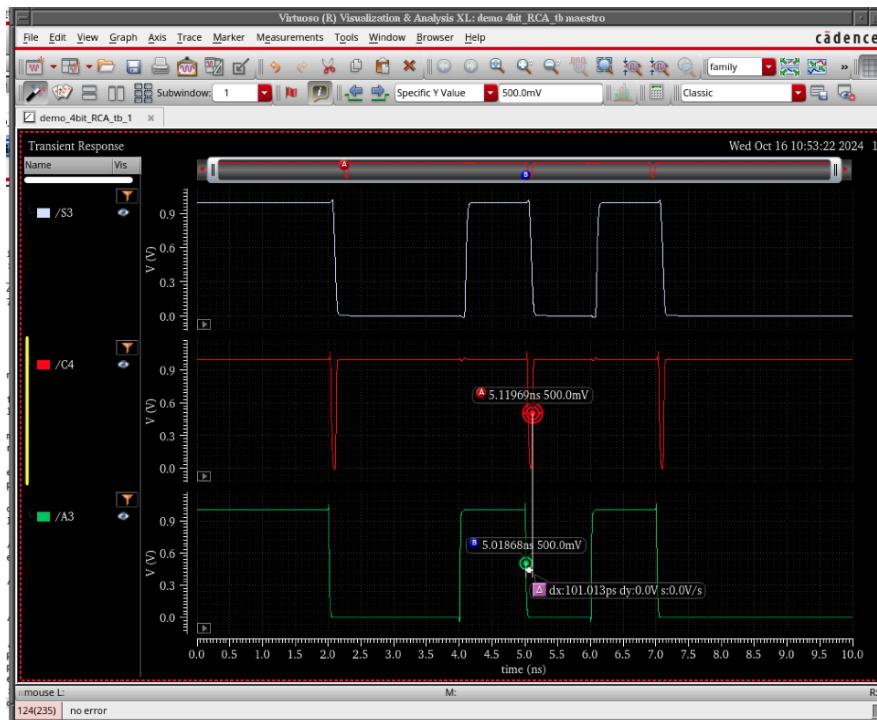
S3 rising delay = 88.62ps



C4 falling delay = 91.14ps



C4 rising delay = 101.01ps

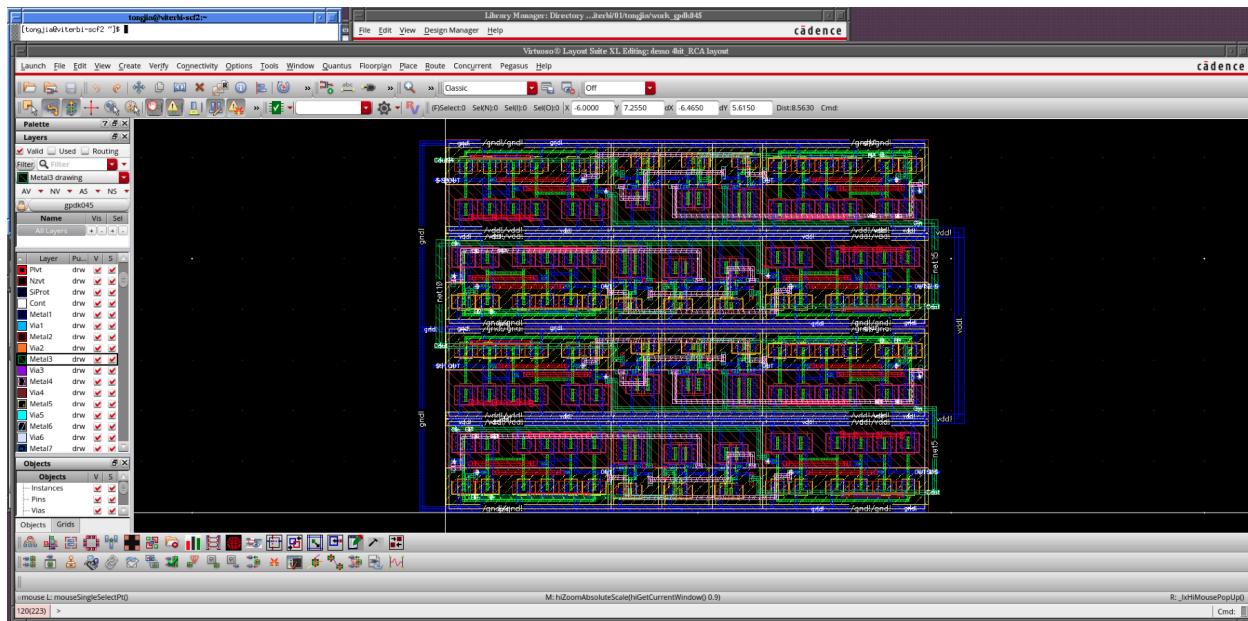


Therefore:

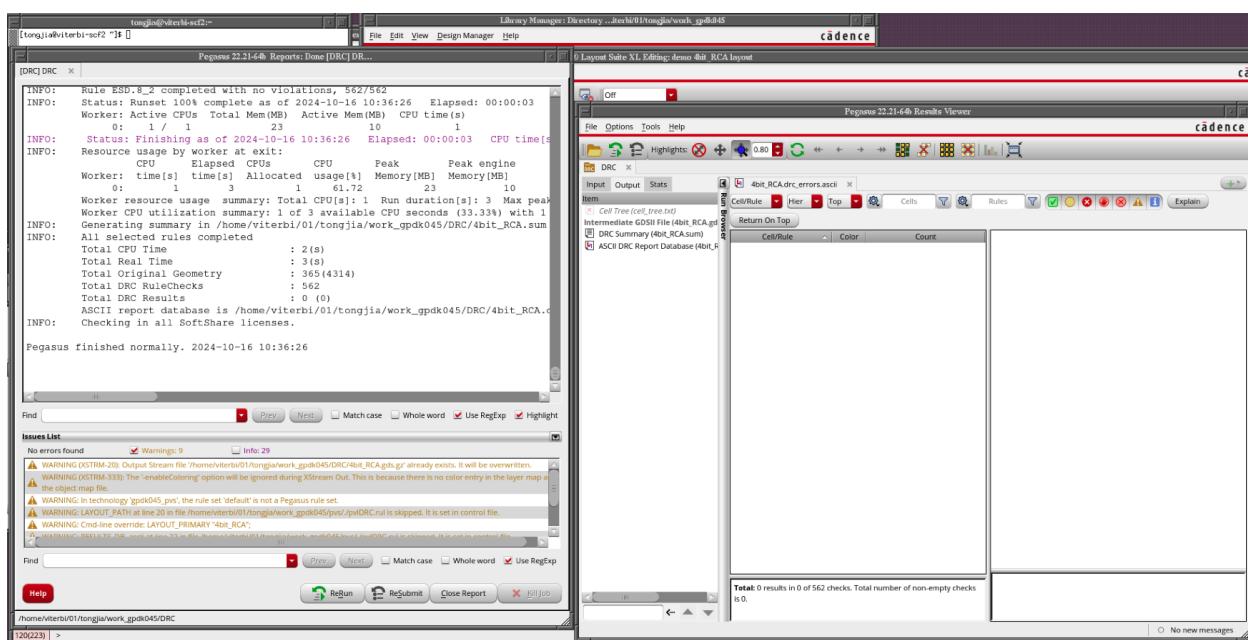
S3 average delay = 89.88ps

C4 average delay = 96.08ps

Layout



DRC



LVS

