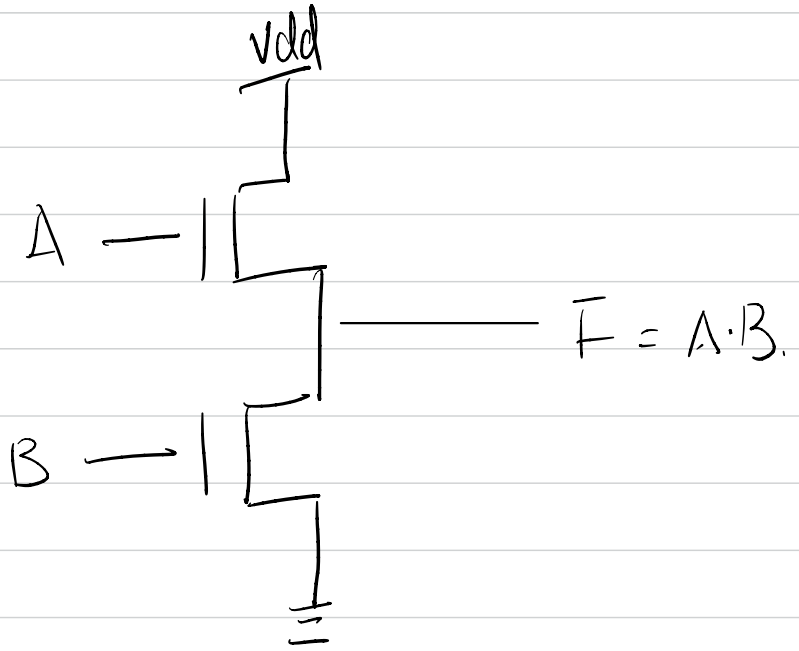
Tony Jiq

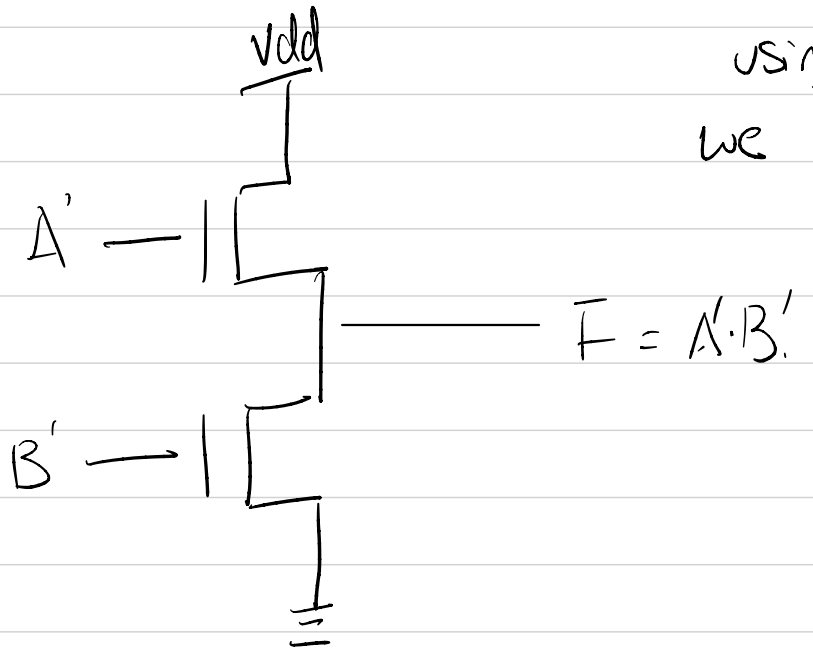
EE 477L HW2

Q1)

a)

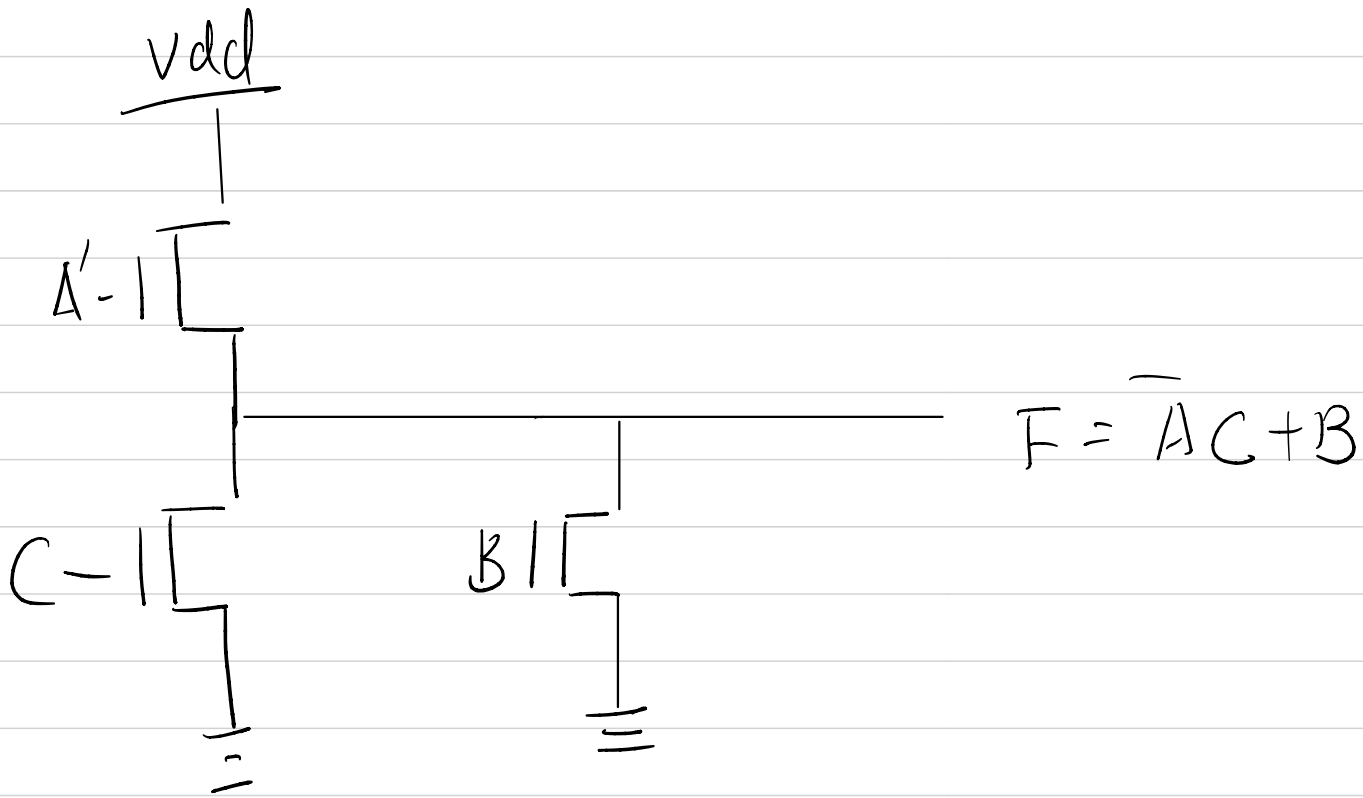


b).

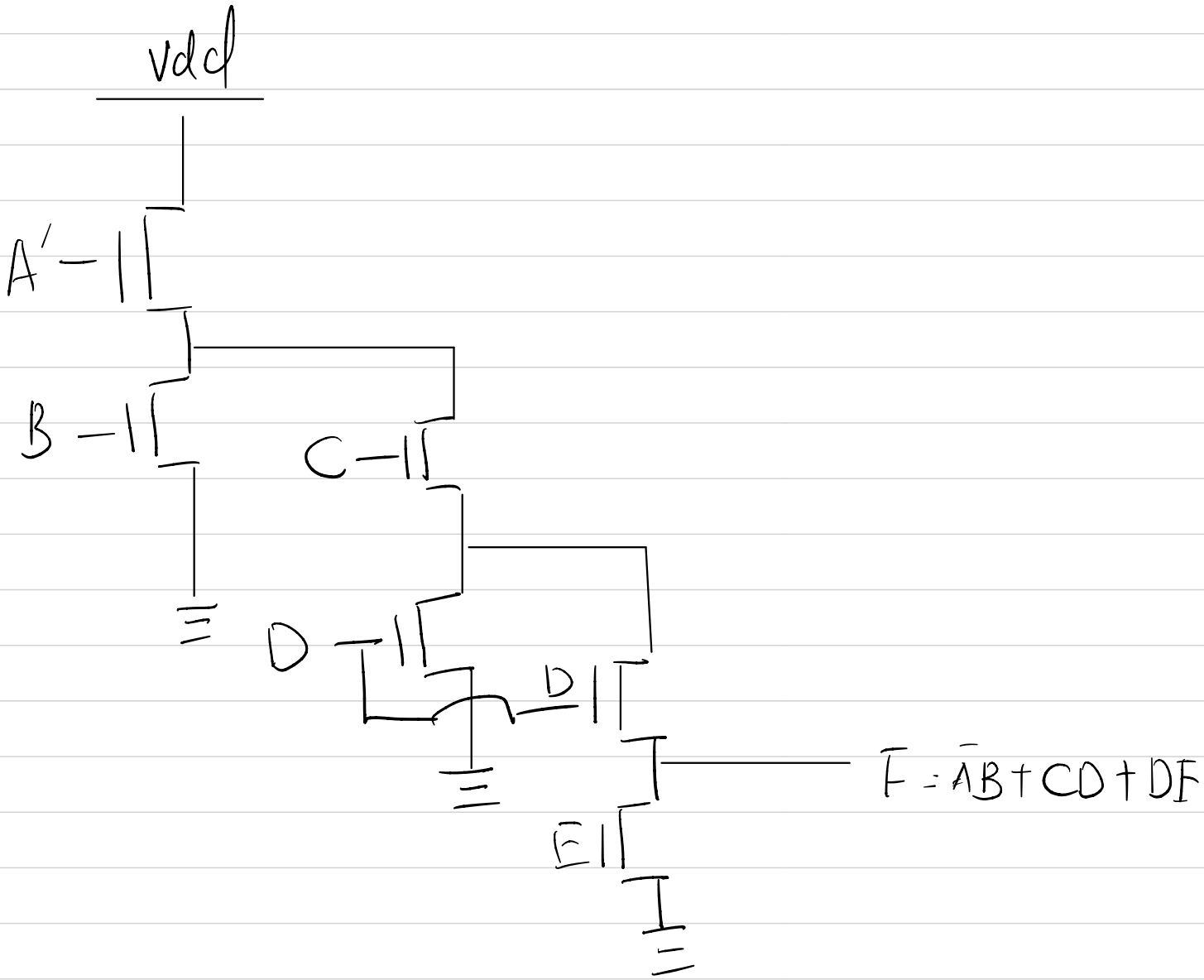


using de morgan's,
we set $(A+B)' = A'B'$

c)



d).



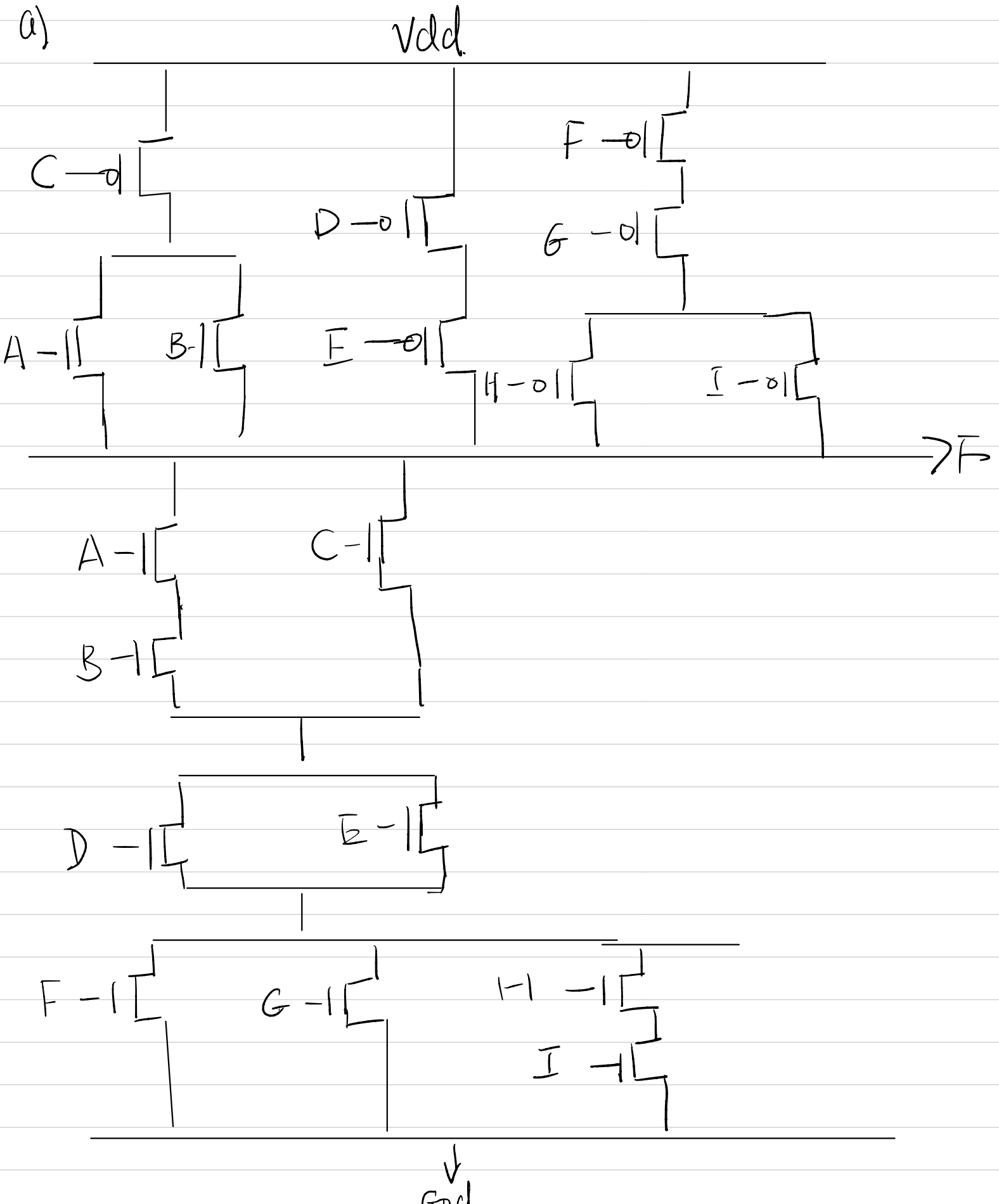
(Q2).

Because NAND is more Power-efficient compare w/ NOR, and it's also easier to implement.

But NOR may be perffered because it's faster than NAND.

Q3)

a)



b) (I didn't really get this question ...)

w/ mobility ratio of 2, it means the PMOS transistors should be 2x width of the NMOS transistors.

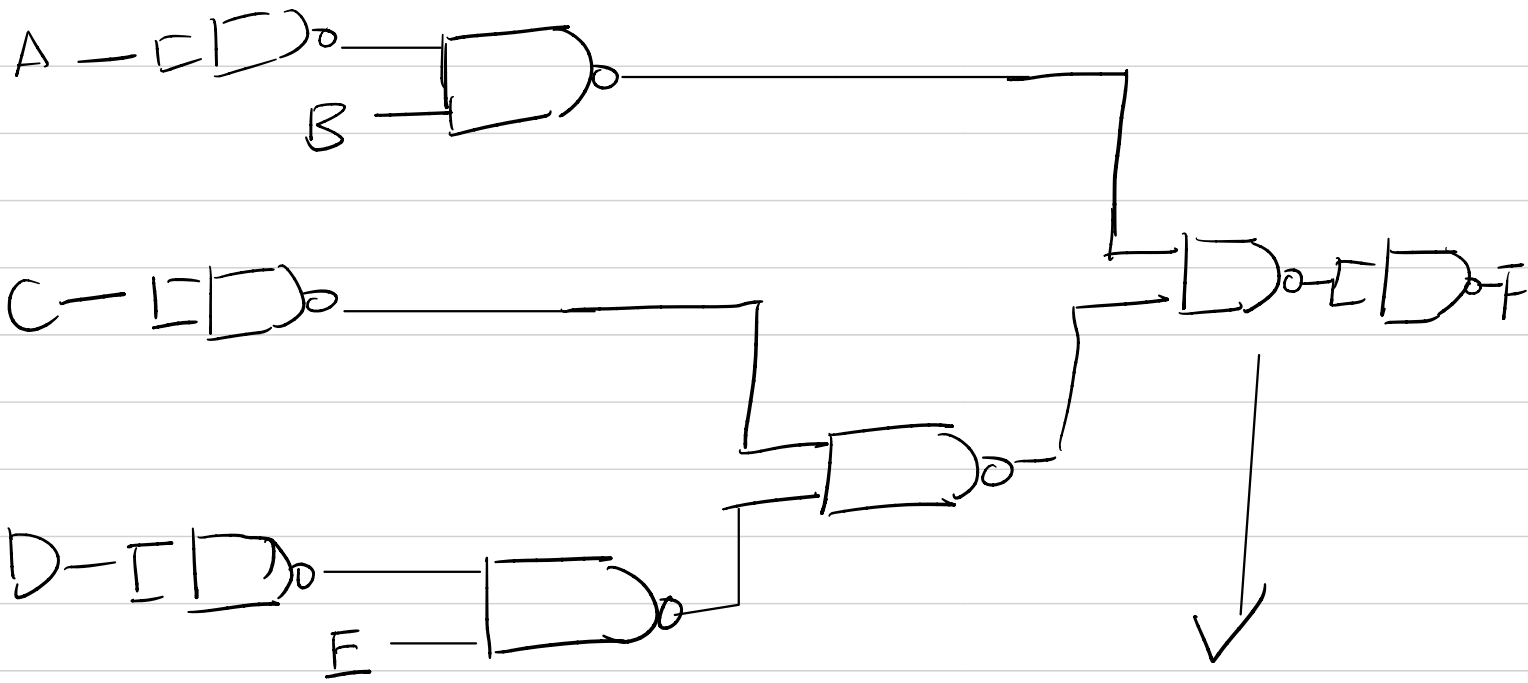
Q4)

$$(A + \bar{B}) = \overline{\bar{A}\,B}$$

$$(C + D\bar{E}) = \overline{(\bar{C}\,\overline{\bar{D}\,E})}$$

$$\therefore F = \overline{(\bar{A}\,B)}\,\overline{(\bar{C}\,\overline{\bar{D}\,E})}$$

Using NAND:



using 2 NAND
to perform us AND

Q5).

a) The green thing is N-well, which helps to isolates PMOS transistors, Nmos does not need it because it won't bias even without the N-well, No-change would made if we add n-well around N-mos. since Nmos can directly fabricate from P-type substrate.

b)