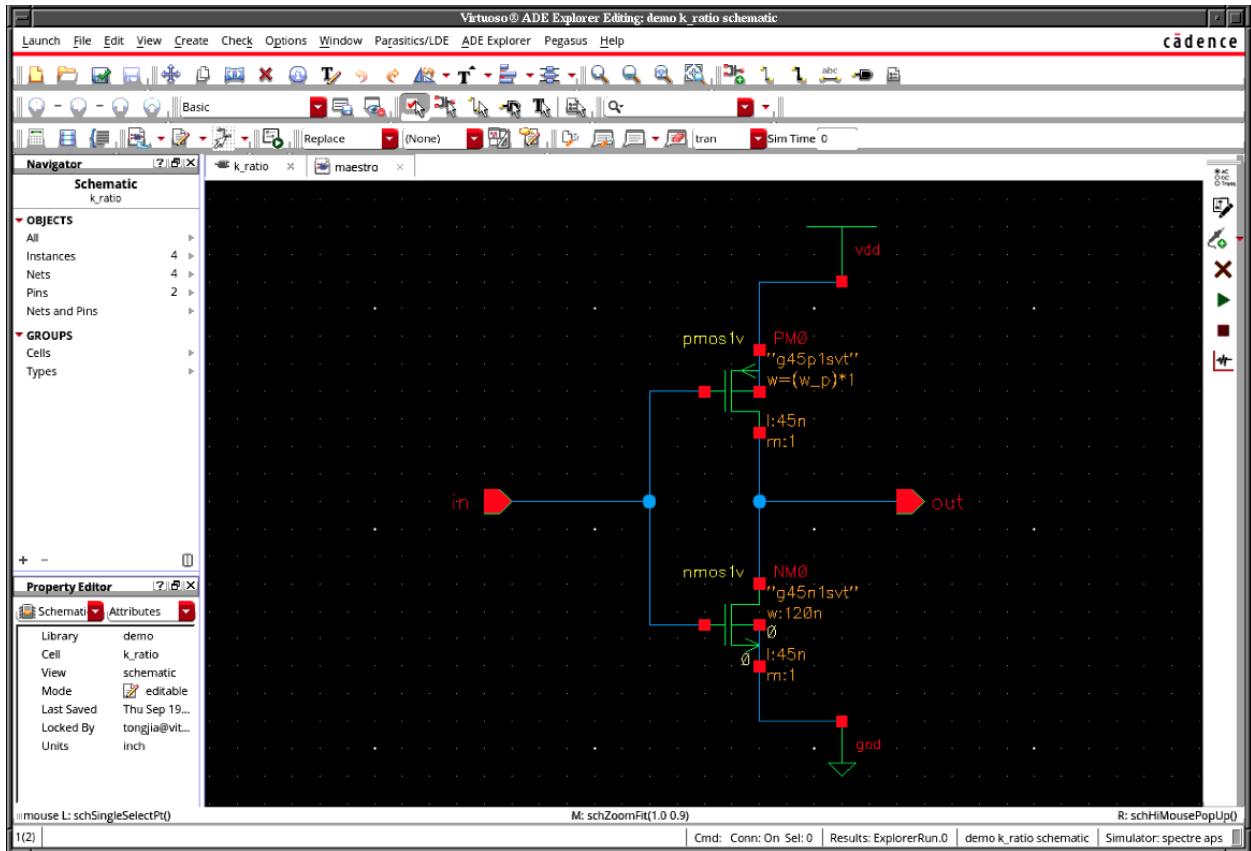


Step 1

schematic of the inverter:



For pmos:

Width = (w_p) * 1

Length = 45ns

Where w_p = 120ns, 180ns, and 240ns

For nmos:

Width = 120ns

Length = 45ns

At 120ns:

Falling delay = 5.617ps

Rising delay = 6.464ps

| Tphl - Tplh | / min (Tphl, Tplh) = 0.151

K-ratio = 0.869



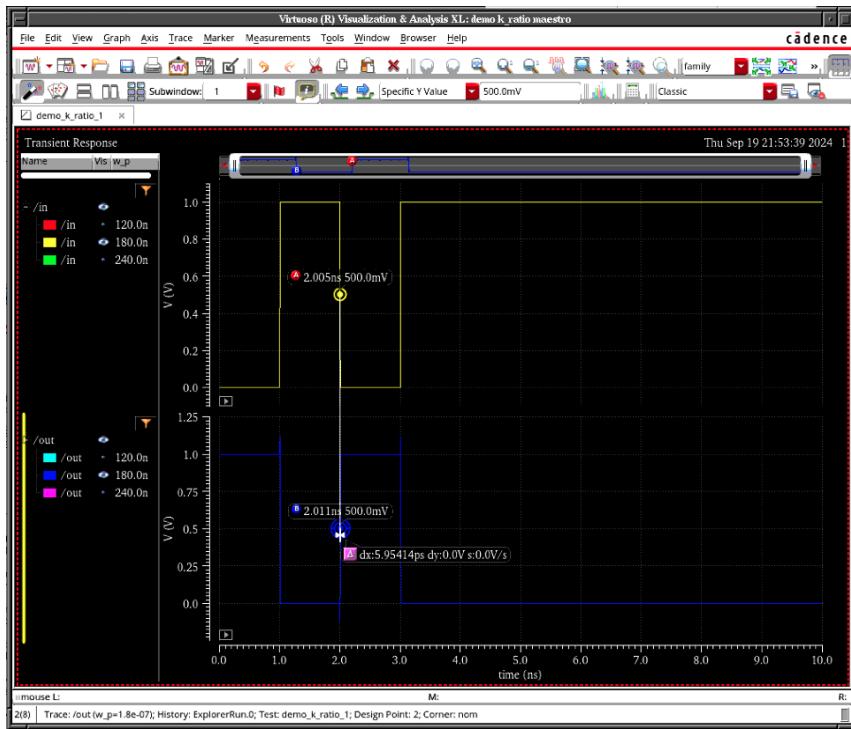
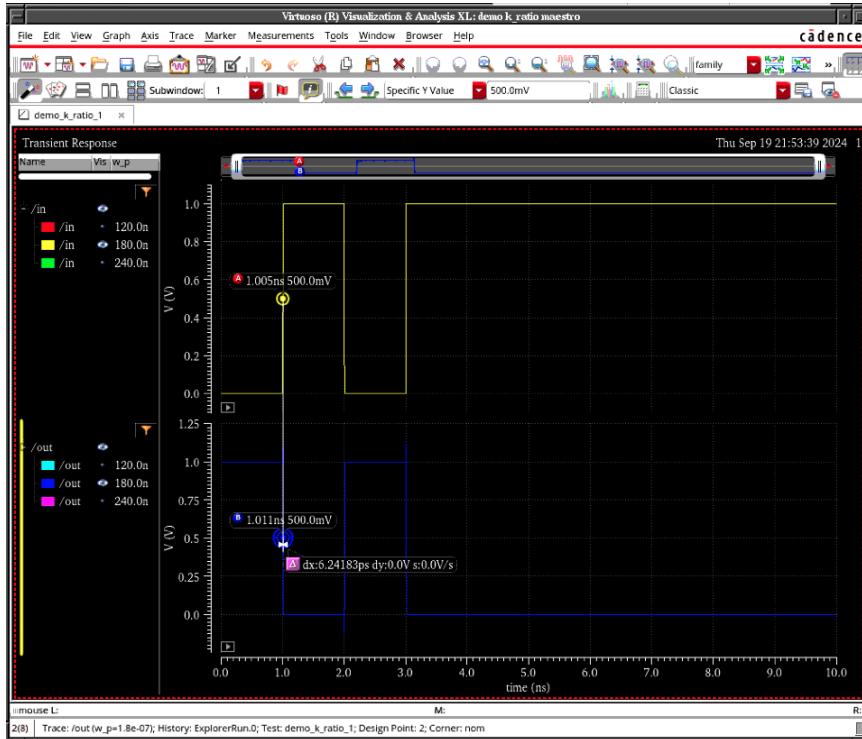
At 180ns:

Falling delay = 6.242ps

Rising delay = 5.954ps

$$| T_{phl} - T_{plh} | / \min(T_{phl}, T_{plh}) = 0.048$$

K-ratio = 1.048



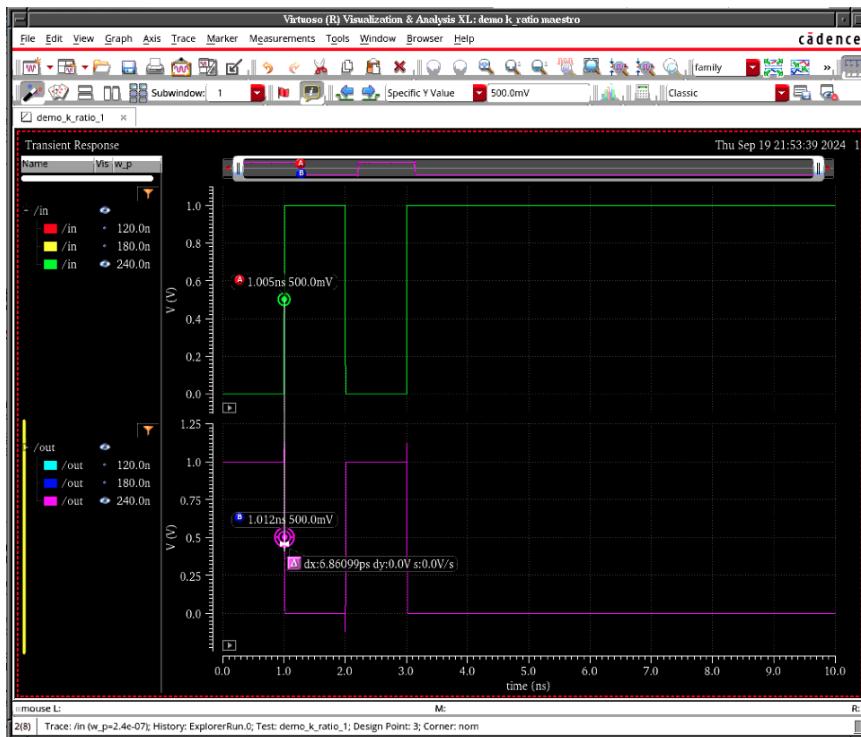
At 240ns:

Falling delay = 6.861ps

Rising delay = 5.707ps

| Tphl - Tplh | / min (Tphl, Tplh) = 0.202

K-ratio = 1.202

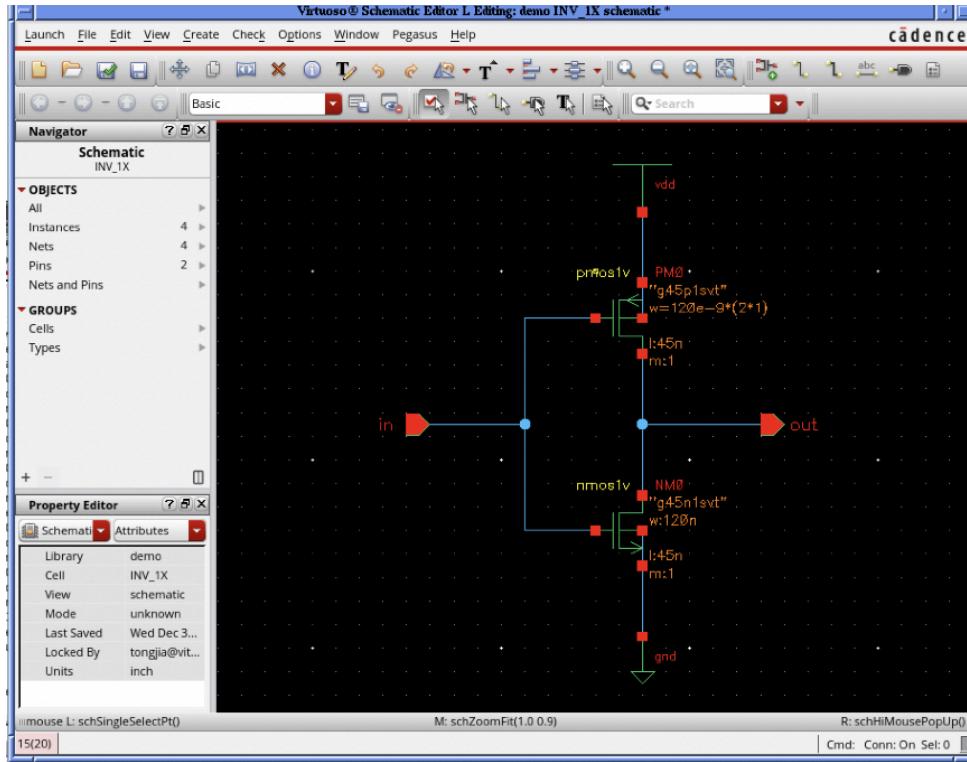


$| T_{ph1} - T_{plh} | / \min(T_{ph1}, T_{plh})$ at 180ns fulfills the requirement, which = **0.048** < 0.1, and the k ratio at 180ns is **1.048**

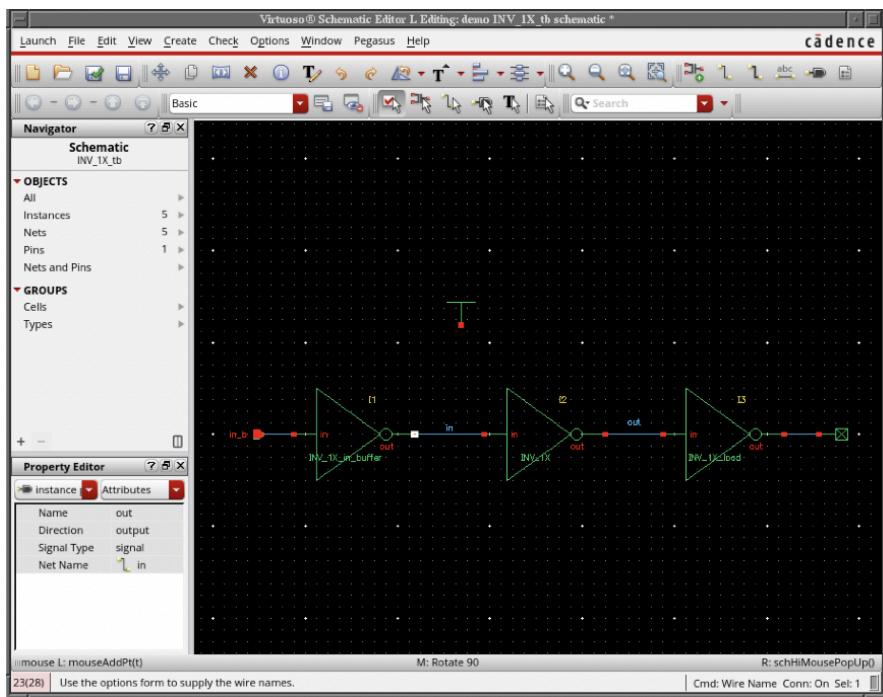
Step 2

For INV_1X:

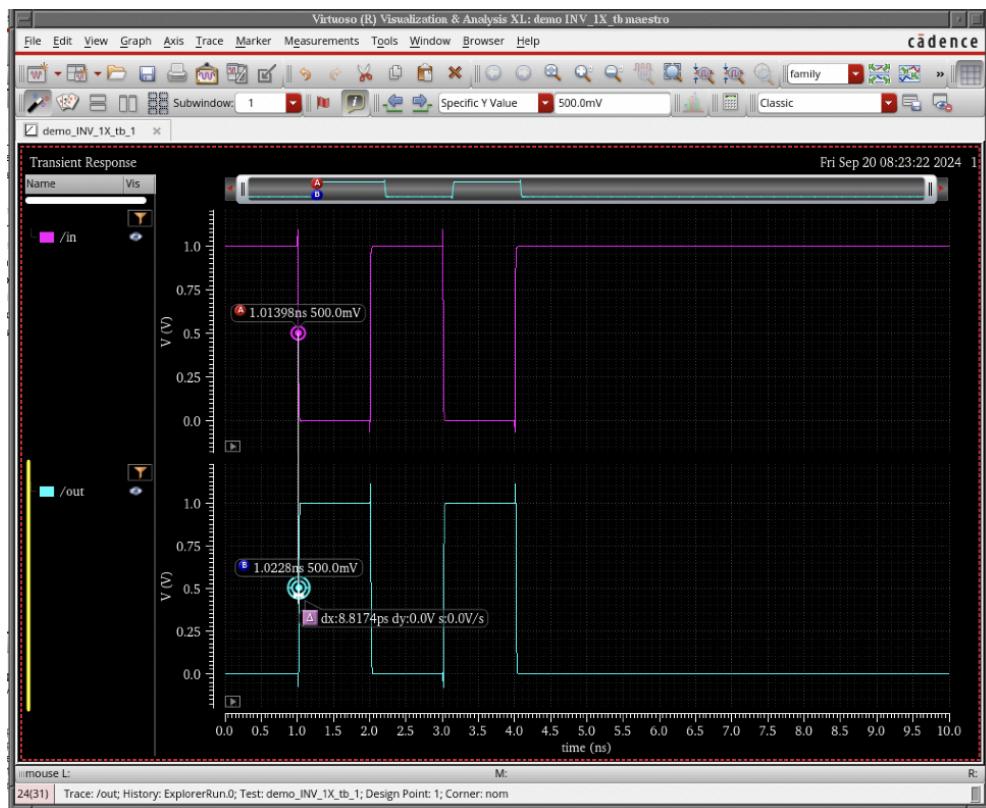
INV_1X, INV_1X_in_buffer and INV_1X_load all use the same schematic as following:



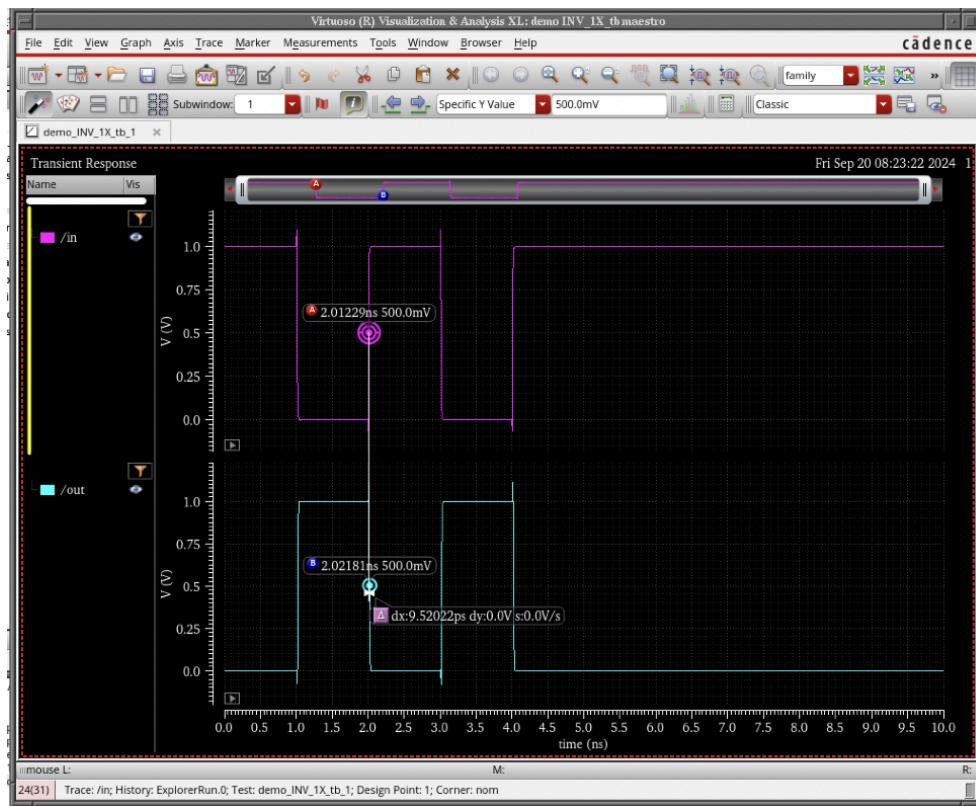
INV_1X testbench schematic:



INV_1X Falling delay: **8.817ps**

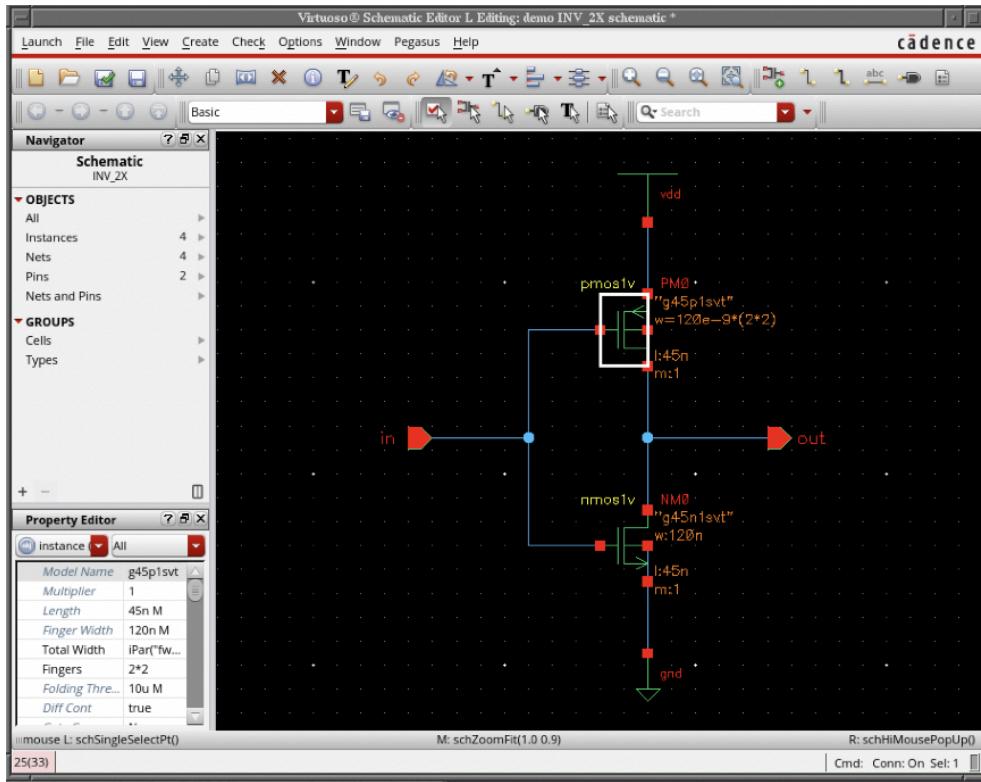


INV_1X Rising delay: **9.520ps**

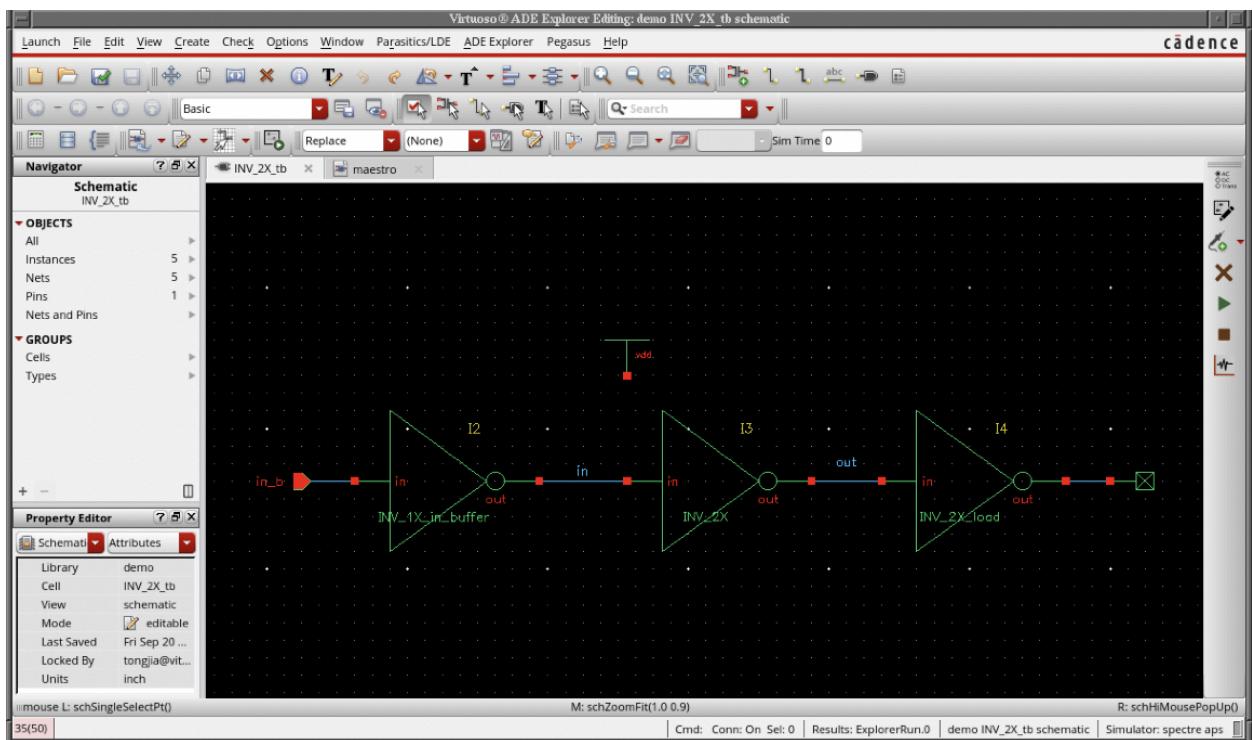


For INV_2X:

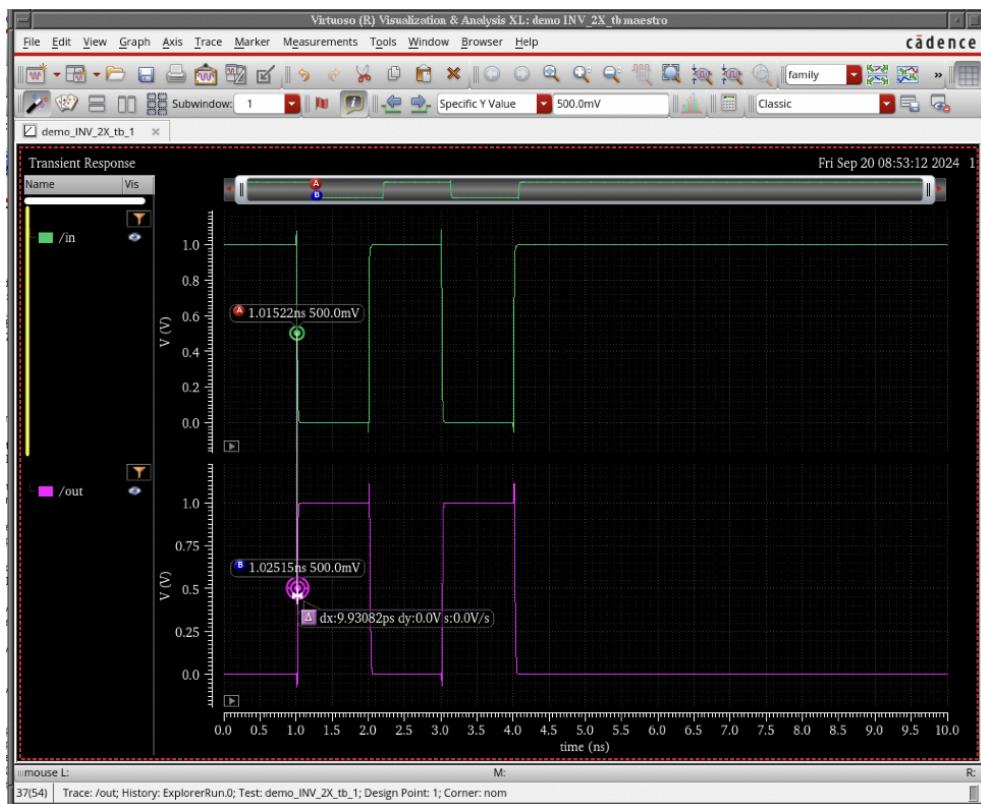
INV_2X and INV_2X_load use the same schematic as following:



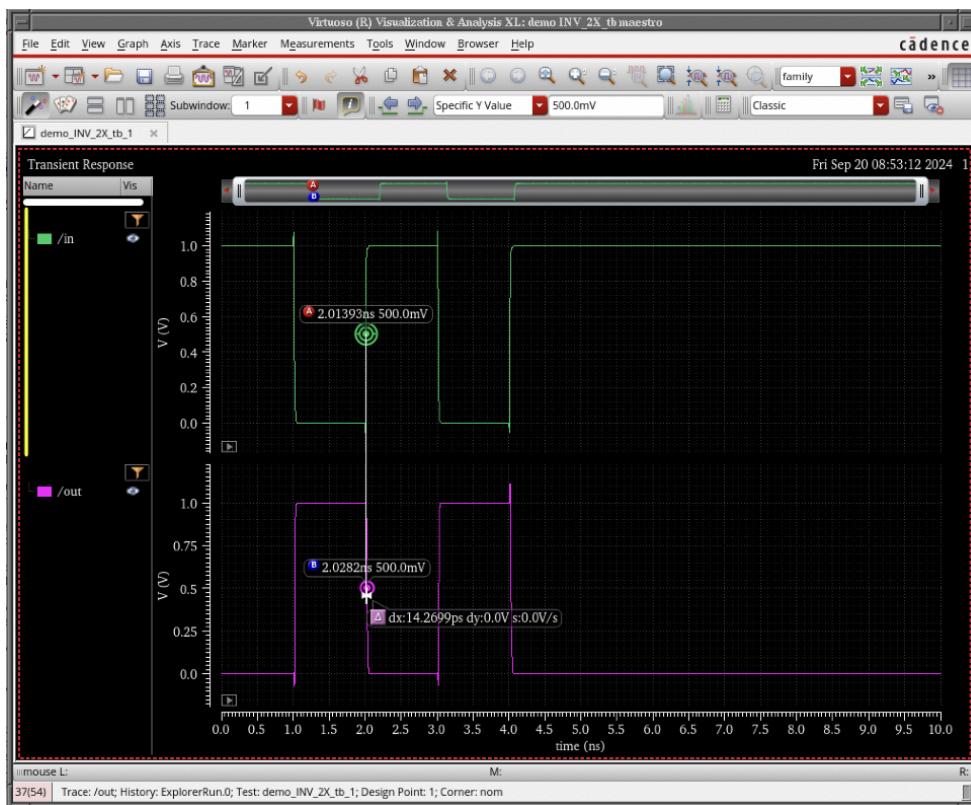
INV_2X testbench schematic:



INV_2X Falling delay: 9.931ps

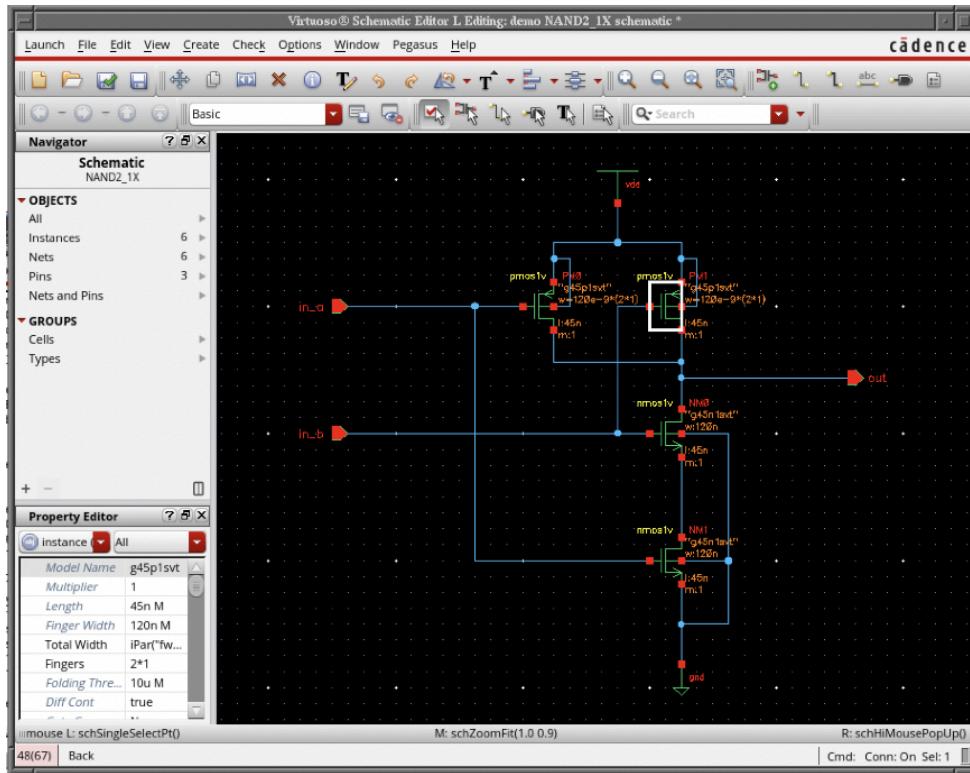


INV_2X Rising delay: 14.2699ps

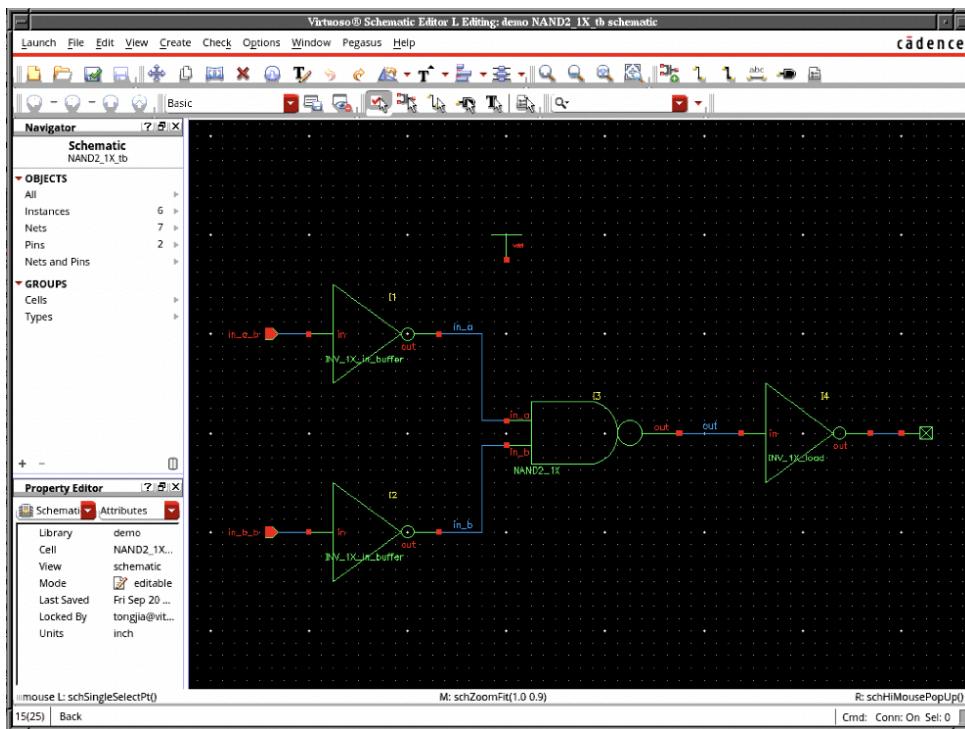


For NAND2_1X:

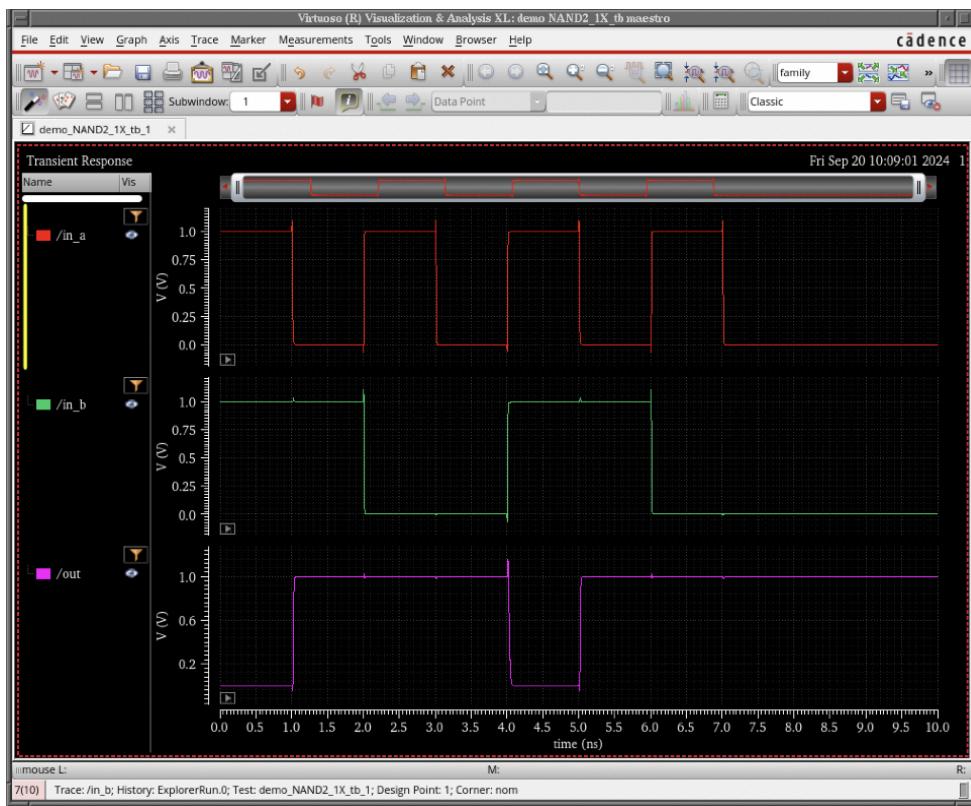
NAND2_1X schematic:



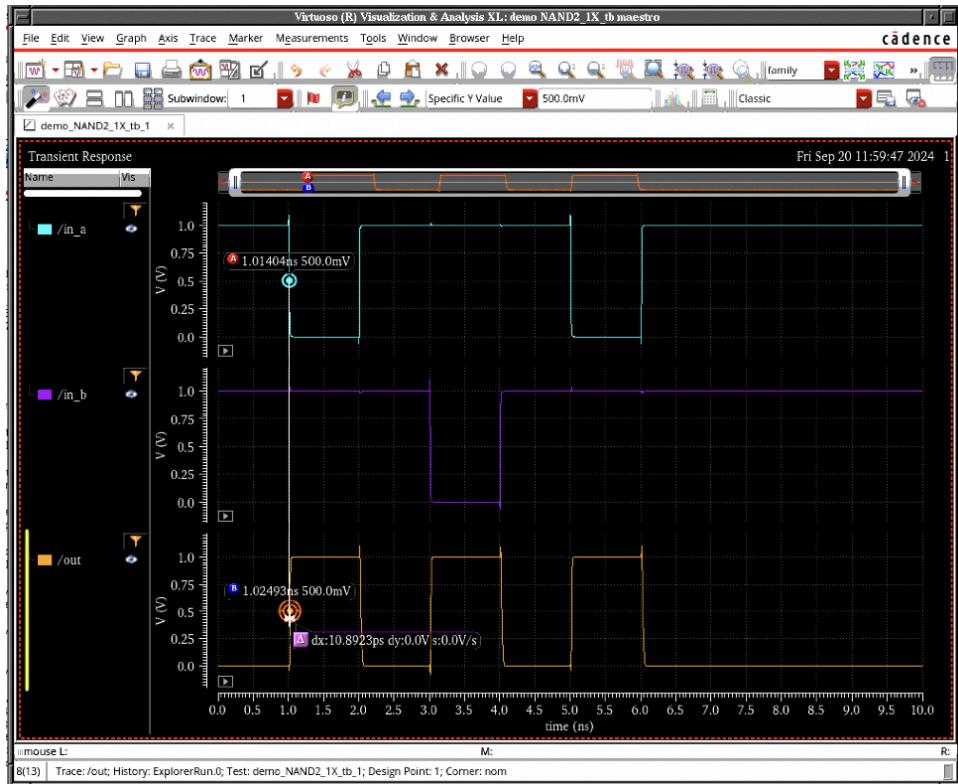
NAND2_1X testbench schematic:



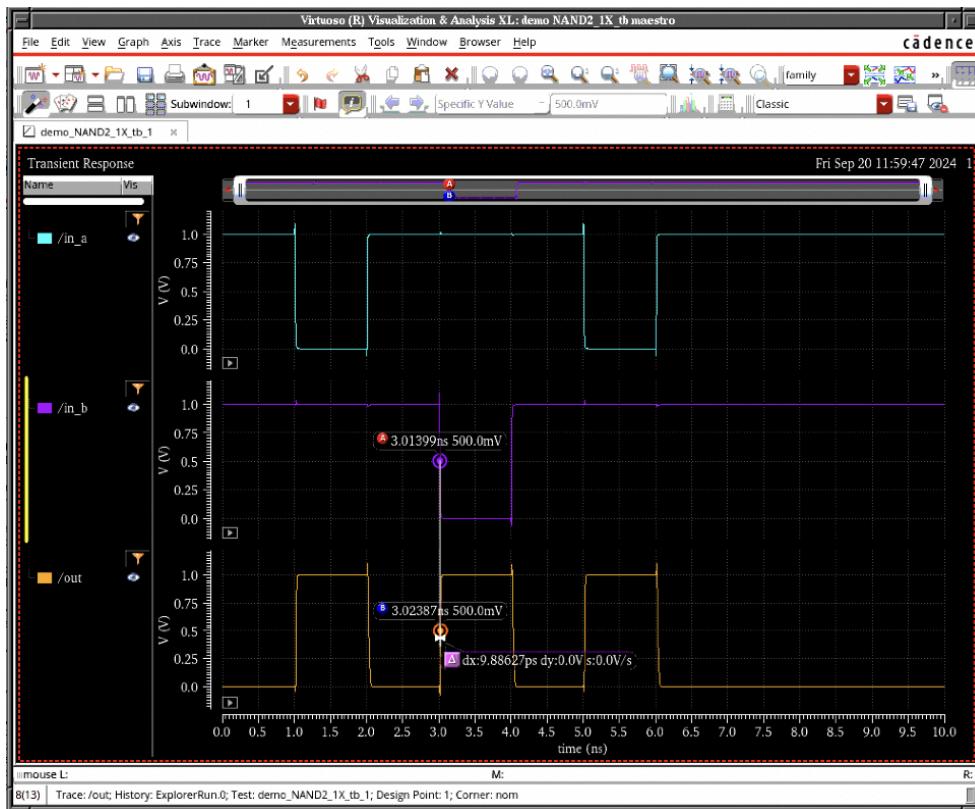
input-output waveforms (function verification) :



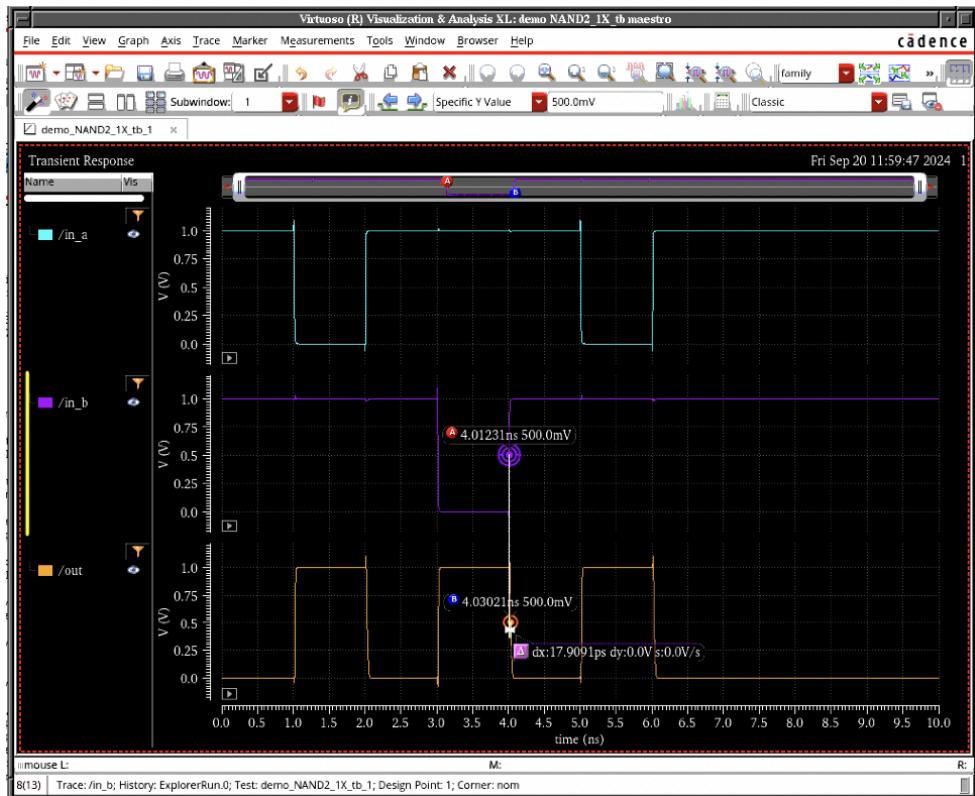
NAND2_1X (1,1) -> (0,1) Rising delay: 10.892ps



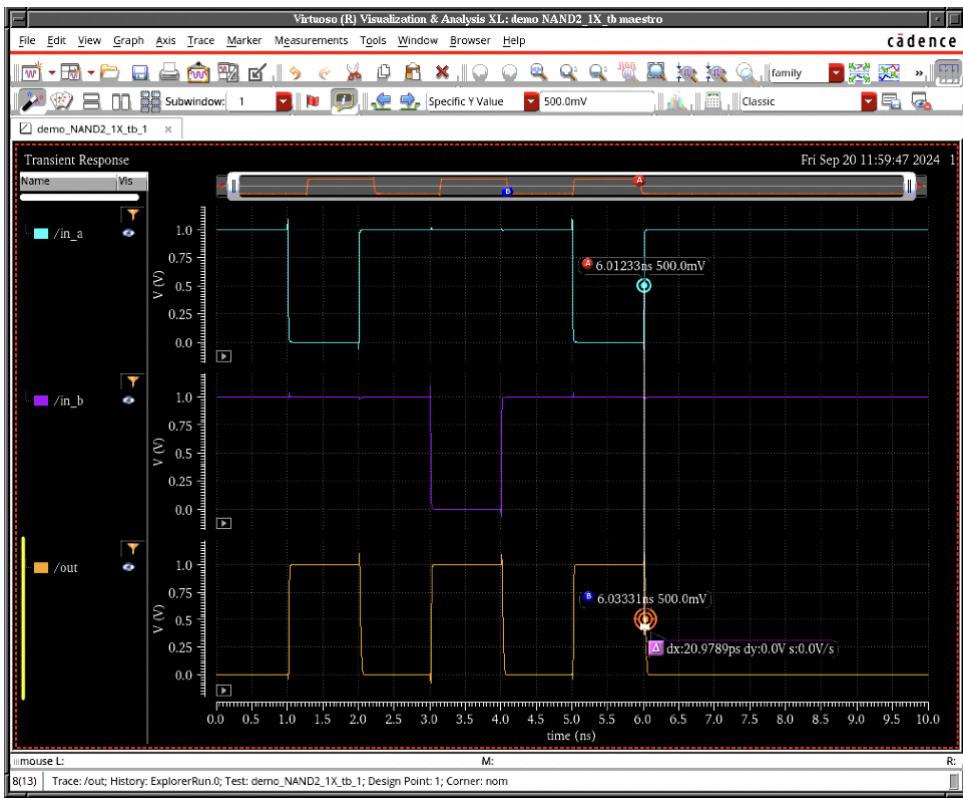
NAND2_1X (1,1) -> (1,0) Rising delay: 9.886ps



NAND2_1X (1,0) -> (1,1) Falling delay: 17.909ps



NAND2_1X (0,1) -> (1,1) Falling delay: 20.979ps

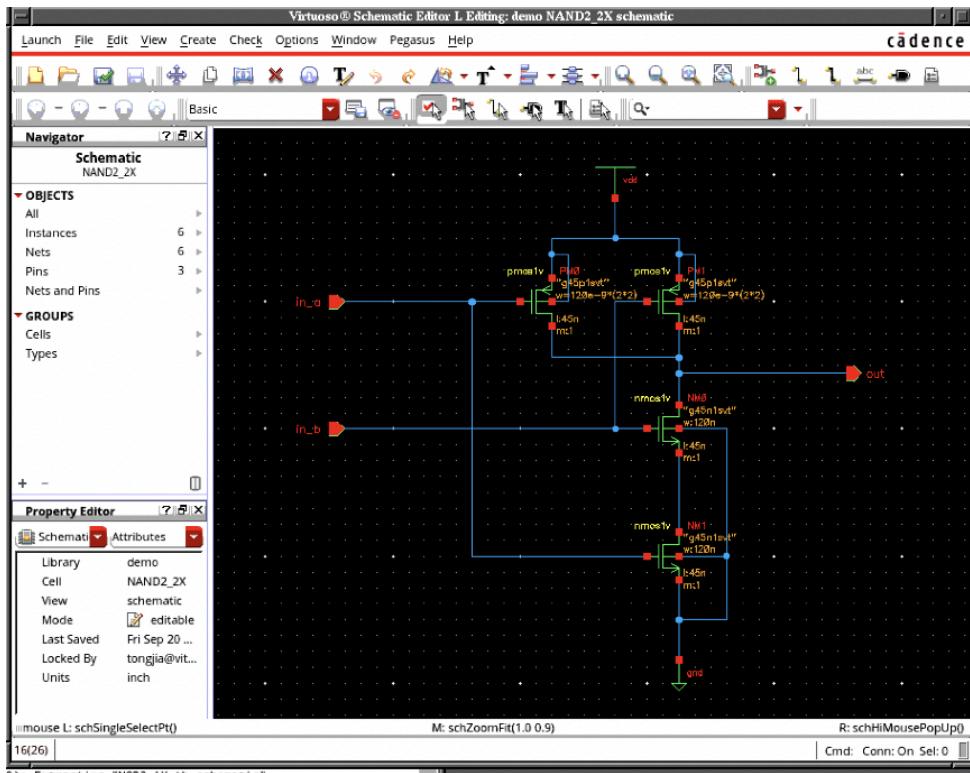


Worst case delays NAND2_1X(input = (A,B))

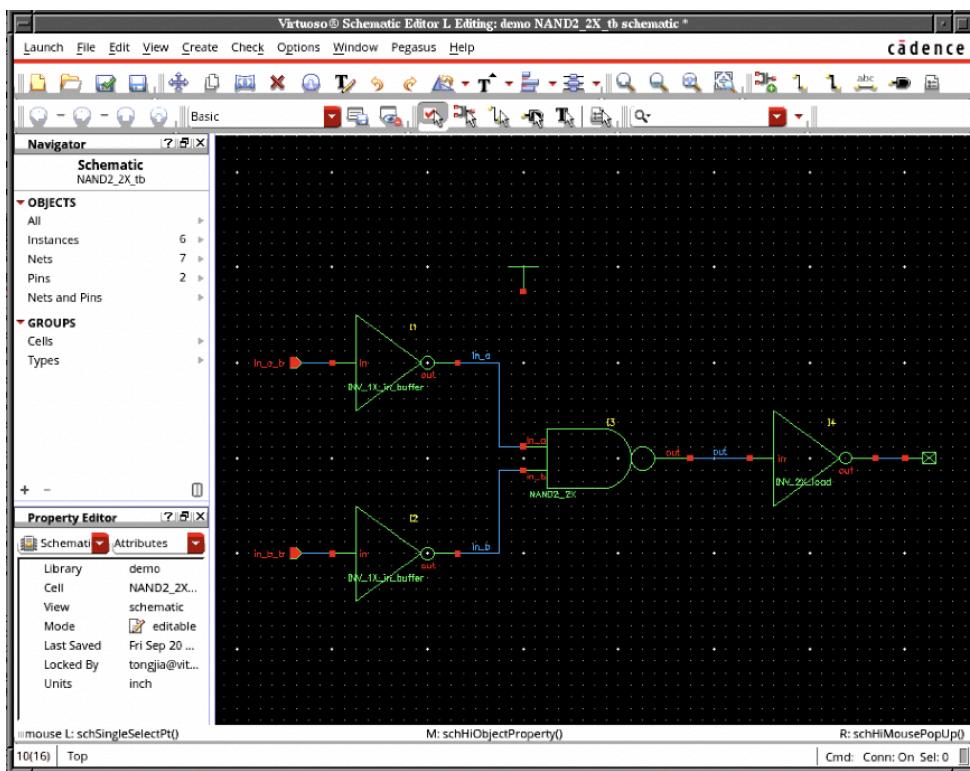
Rising delay(ps)		Falling delay(ps)	
(A,B) = (1,1) -> (0,1)	10.892	(A,B) = (0,1) -> (1,1)	20.979
(A,B) = (1,1) -> (1,0)	9.886	(A,B) = (1,0) -> (1,1)	17.909

For NAND2_2X:

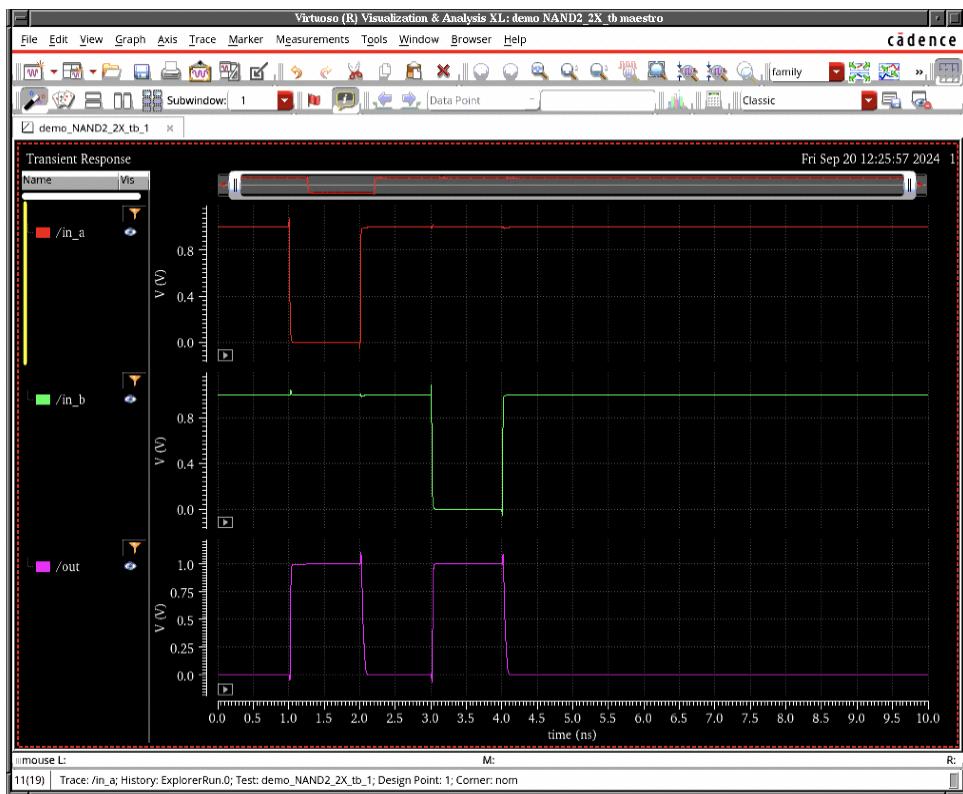
NAND2_2X schematic:



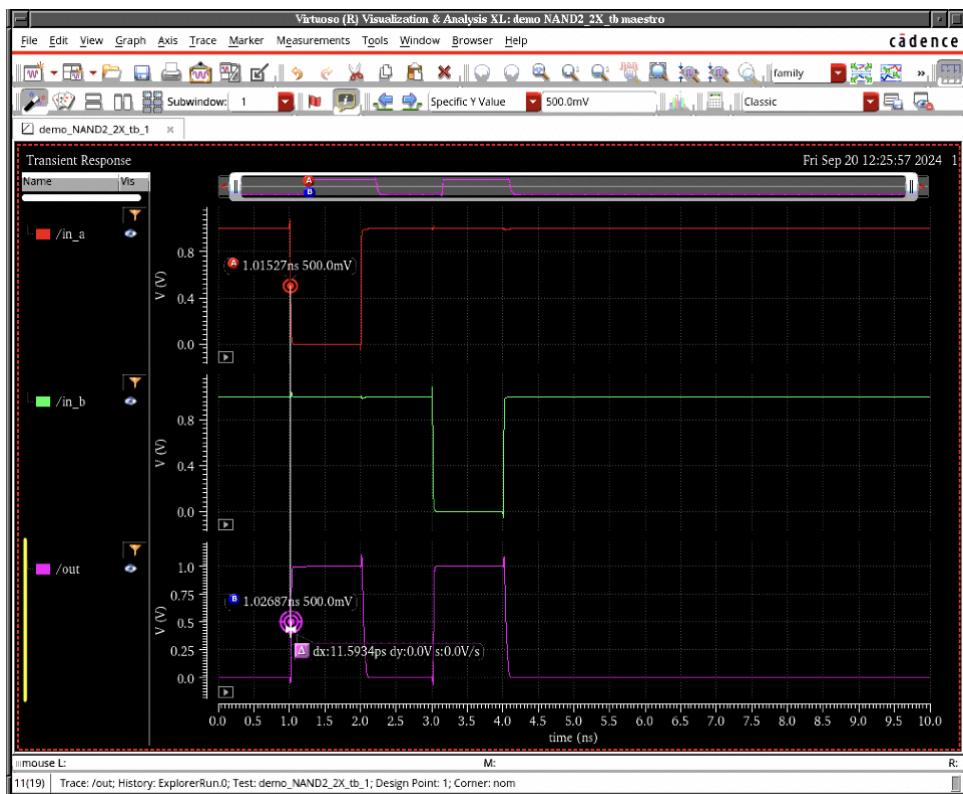
NAND2_2X testbench schematic:



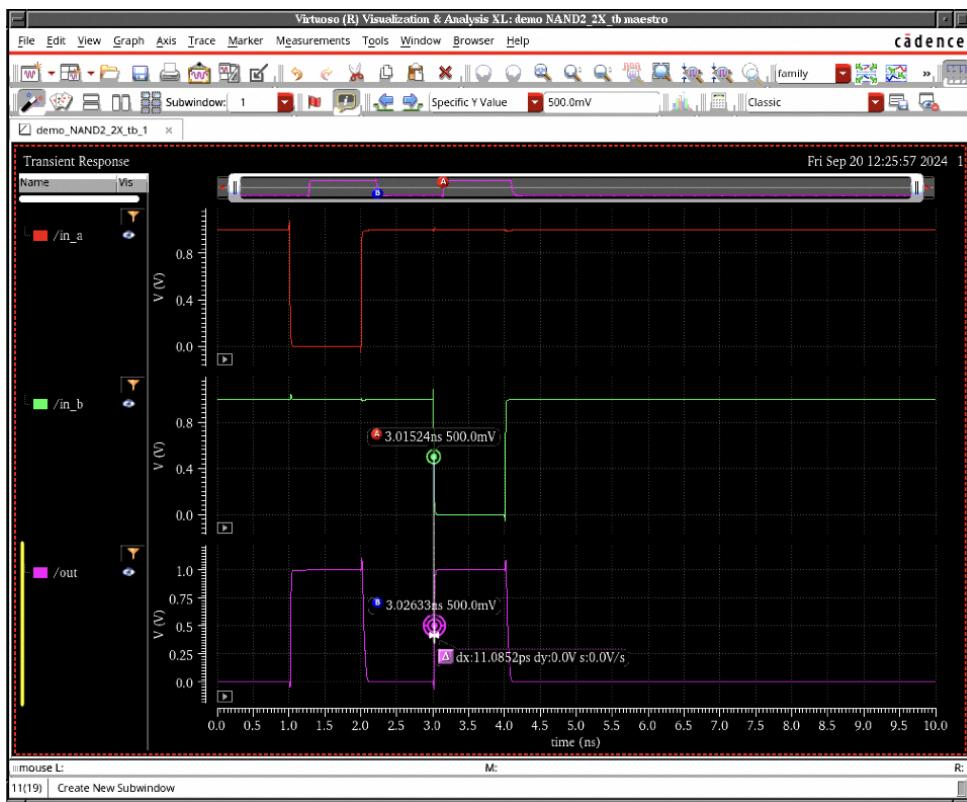
input-output waveforms (function verification) :



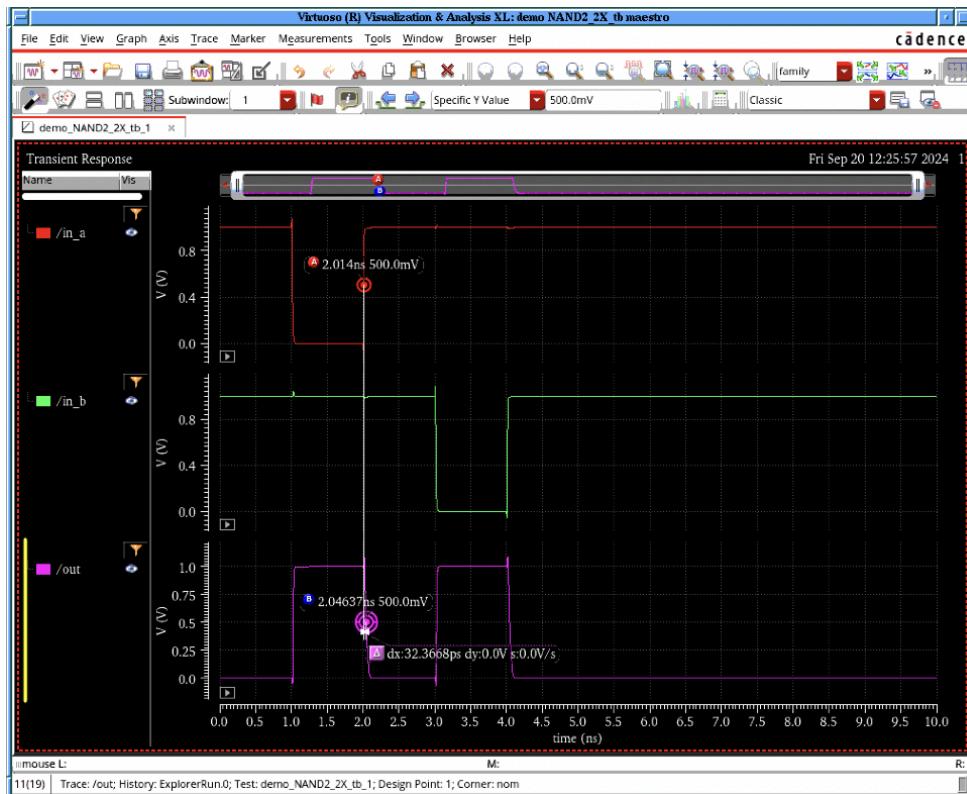
NAND2_2X (1,1) -> (0,1) Rising delay: 11.593ps



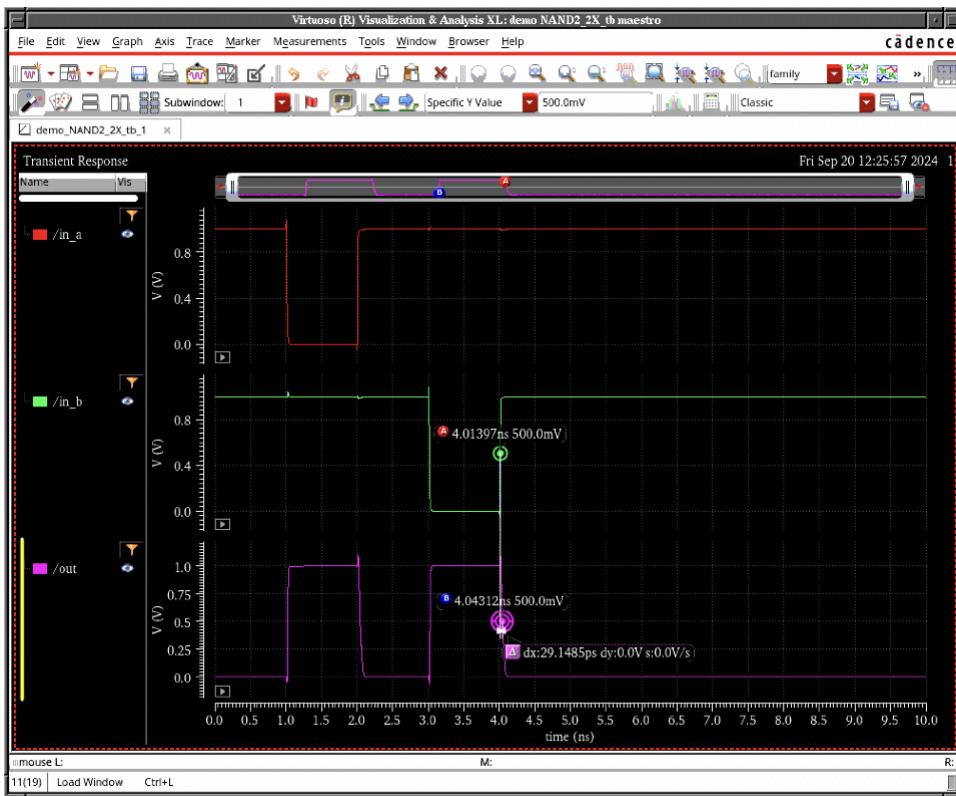
NAND2_2X (1,1) -> (1,0) Rising delay: 11.085ps



NAND2_2X (0,1) -> (1,1) Falling delay: 32.367ps



NAND2_2X (1, 0) -> (1, 1) Falling delay: 29.149ps

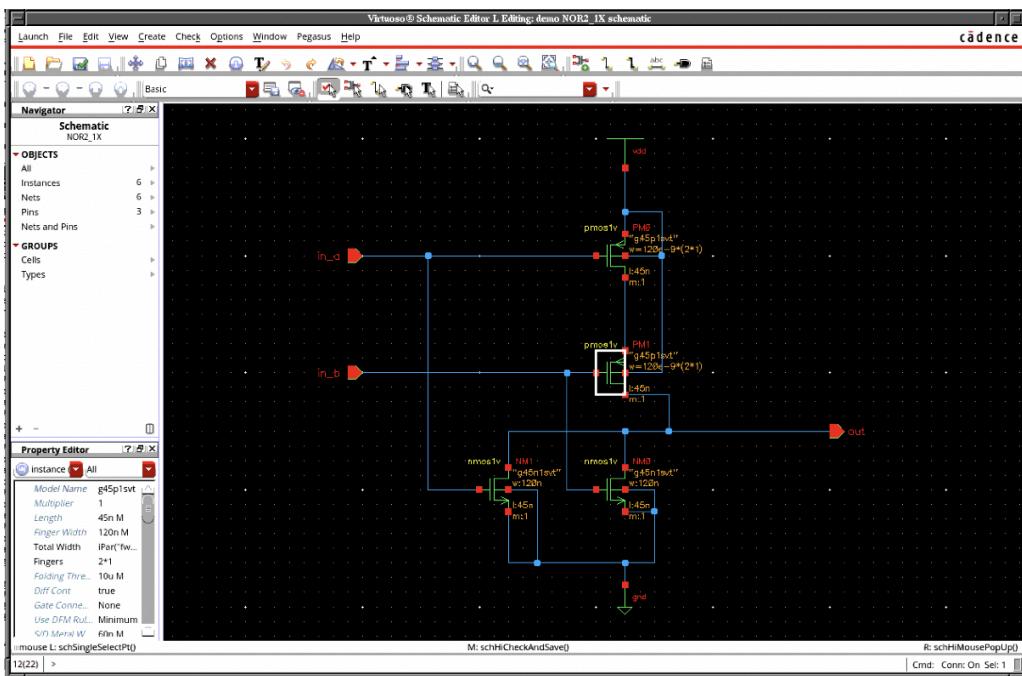


Worst case delays NAND2_2X(input = (A, B))

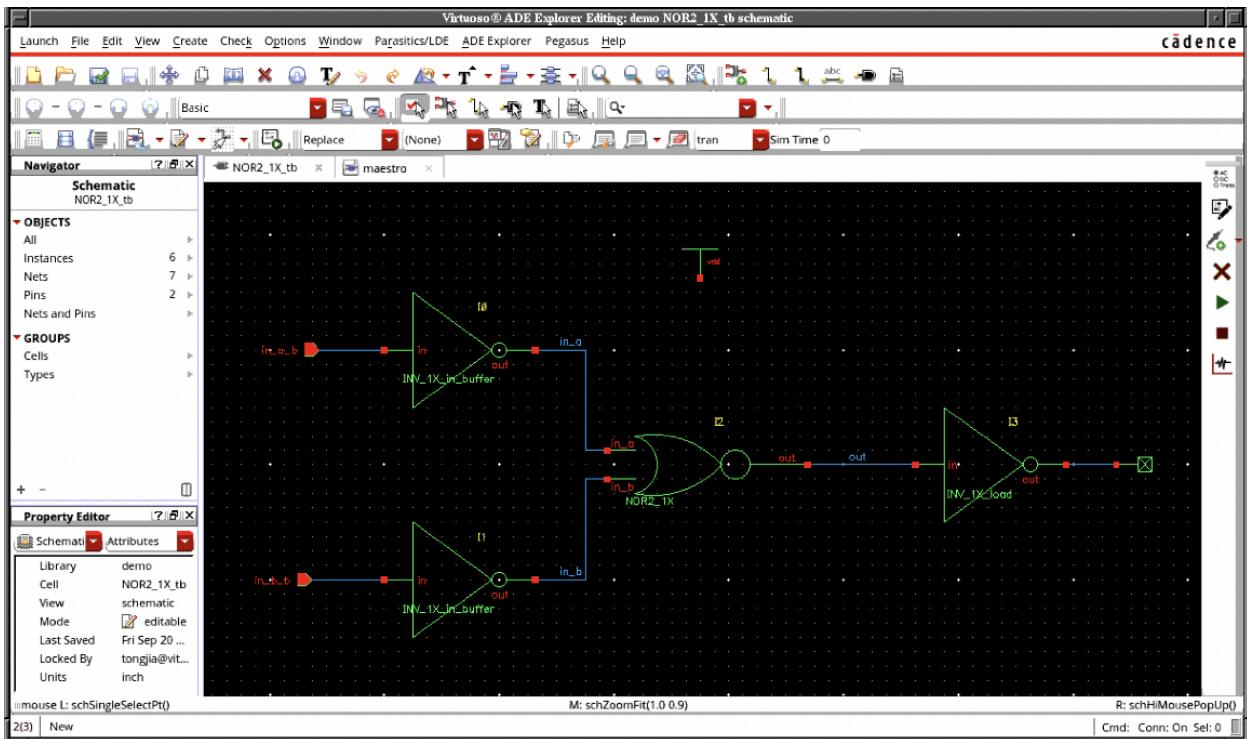
Rising delay(ps)		Falling delay(ps)	
(A, B) = (1, 1) -> (0, 1)	11.593	(A, B) = (0, 1) -> (1, 1)	32.367
(A, B) = (1, 1) -> (1, 0)	11.085	(A, B) = (1, 0) -> (1, 1)	29.149

For Nor2_1X:

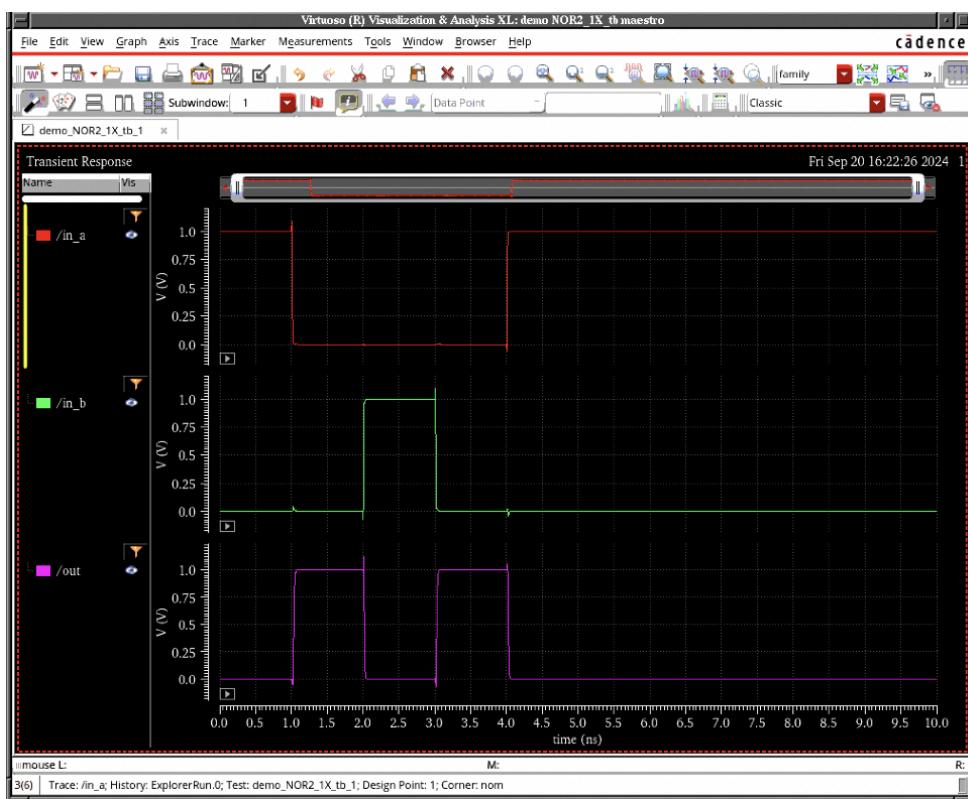
NOR2_1X schematic:



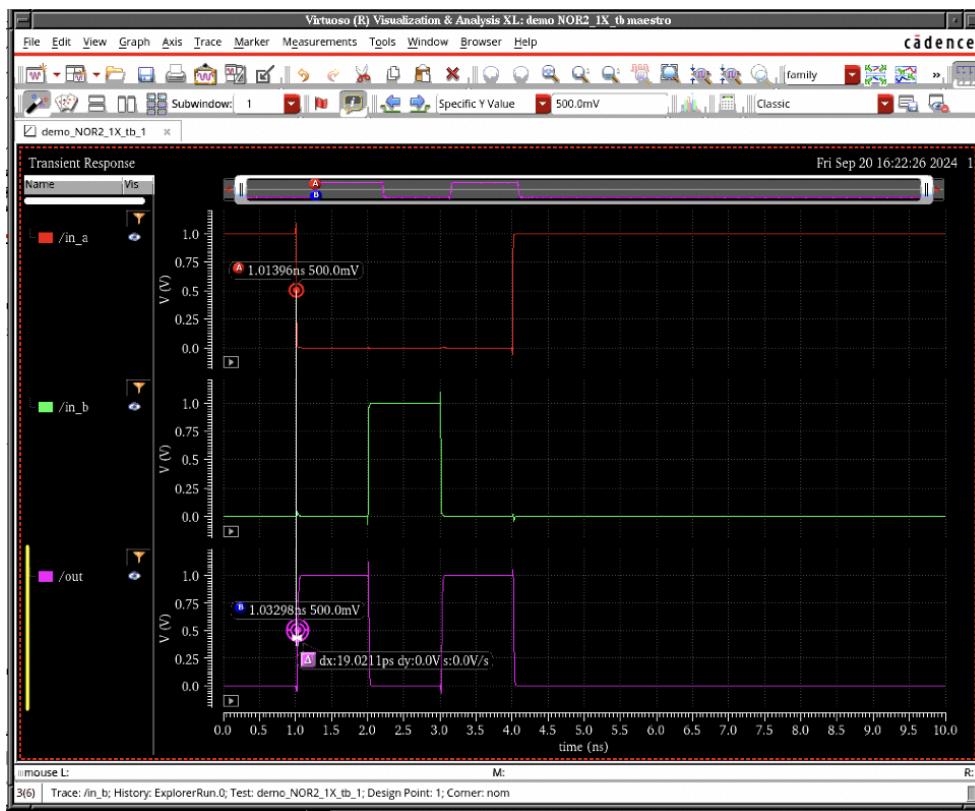
NOR2_1X testbench schematic:



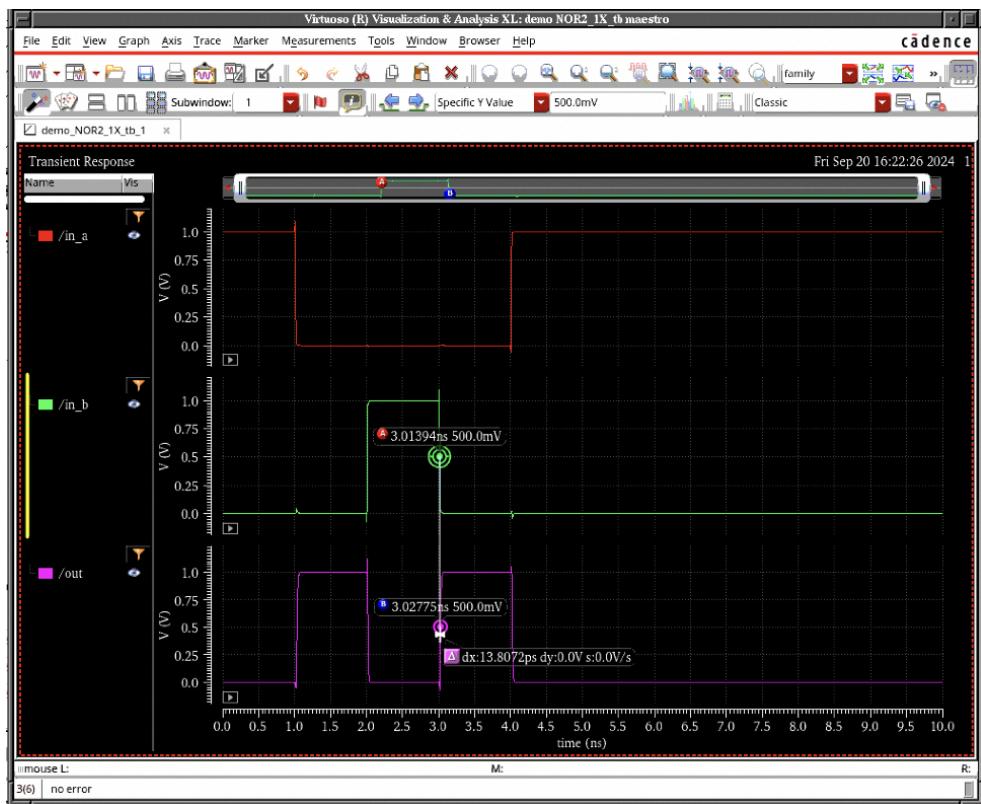
input-output waveforms (function verification) :



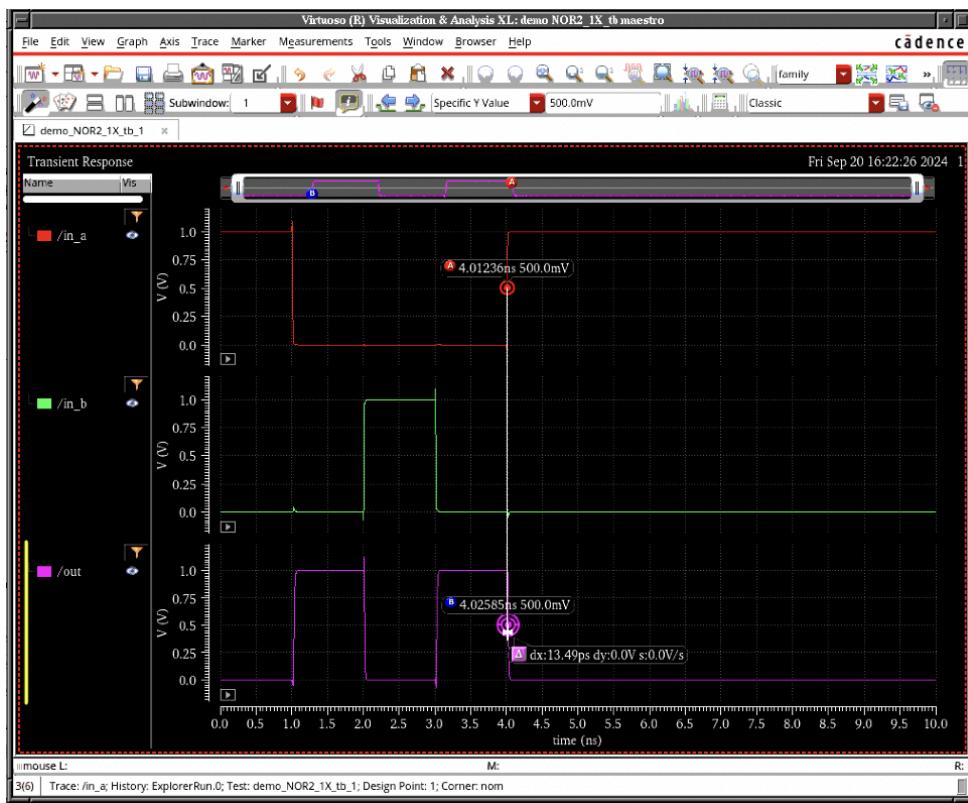
NOR2_1X (1,0) -> (0,0) Rising Delay: 19.021ps



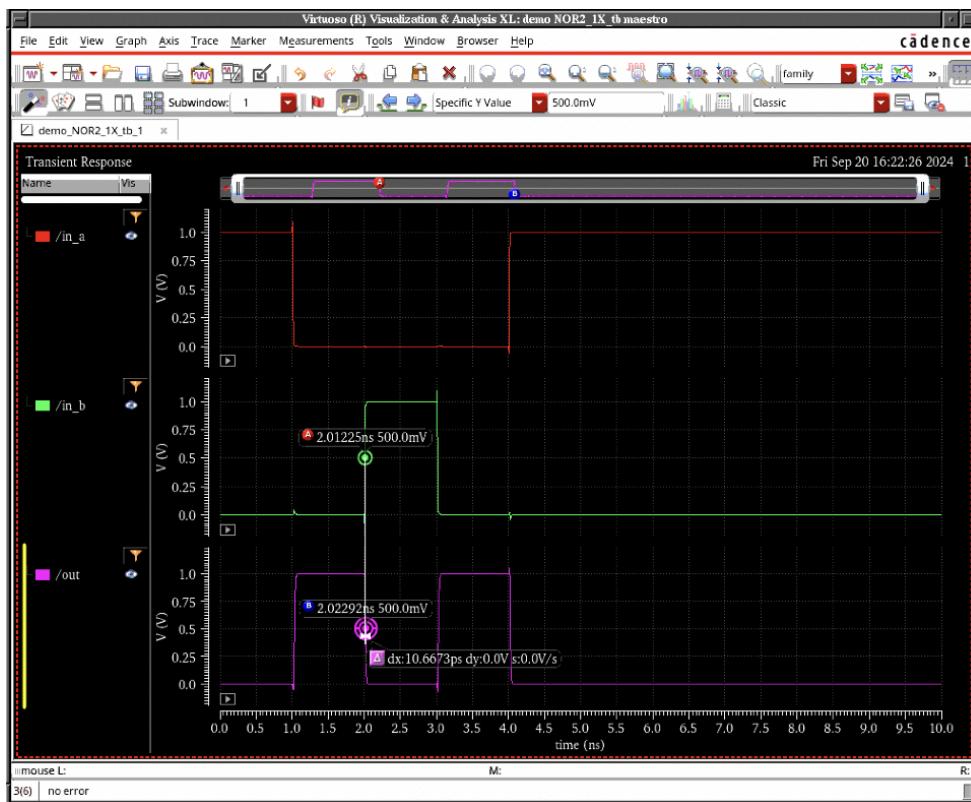
NOR2_1X (0,1) -> (0,0) Rising Delay:13.807ps



NOR2_1X (0,0) -> (1,0) Falling Delay: 13.490ps



NOR2_1X (0,0) -> (0,1) Falling Delay: 10.667ps

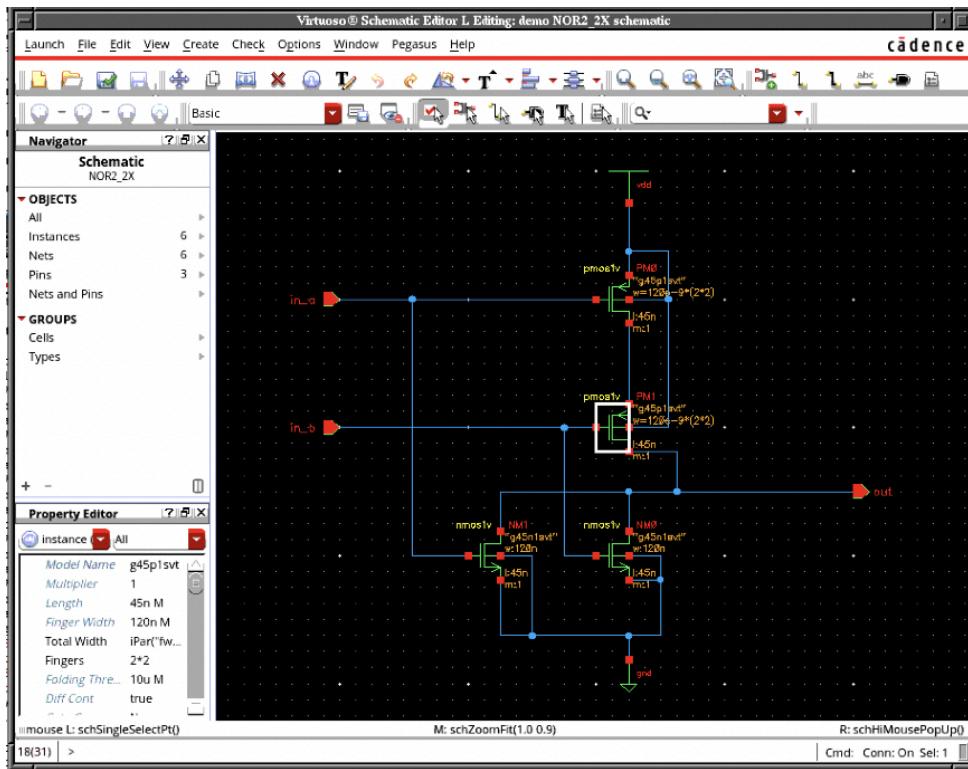


Worst case delays NOR2_1X(input = (A,B))

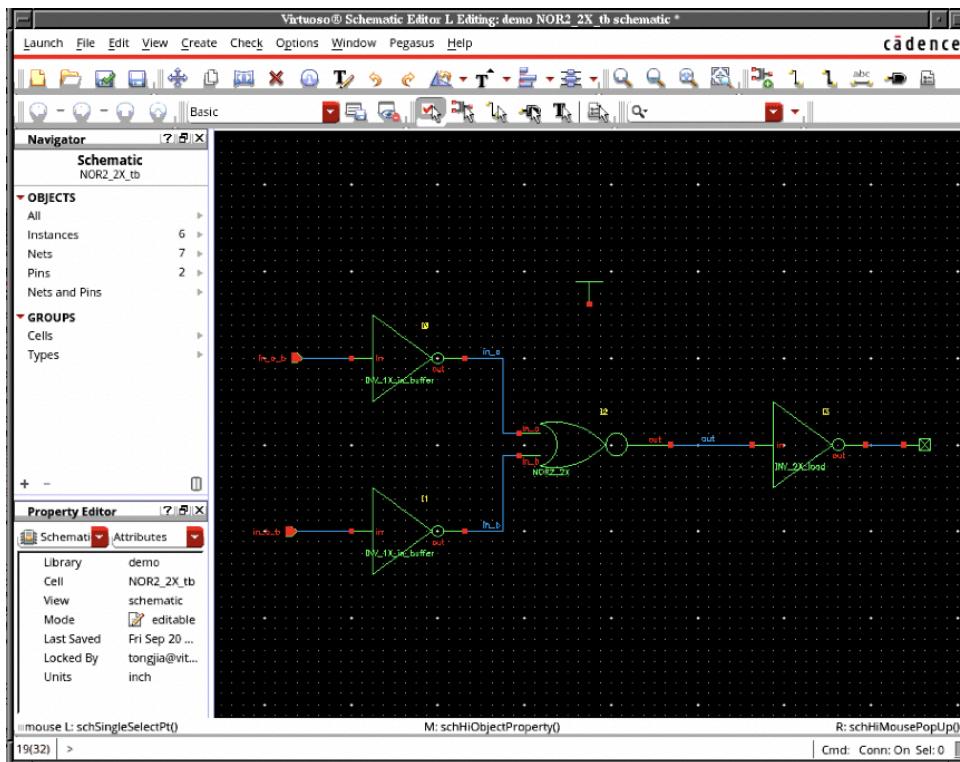
Rising delay(ps)		Falling delay(ps)	
(A,B) = (1,0) -> (0,0)	19.021	(A,B) = (0,0) -> (1,0)	13.490
(A,B) = (0,1) -> (0,0)	13.807	(A,B) = (0,0) -> (0,1)	10.667

For Nor2_2X:

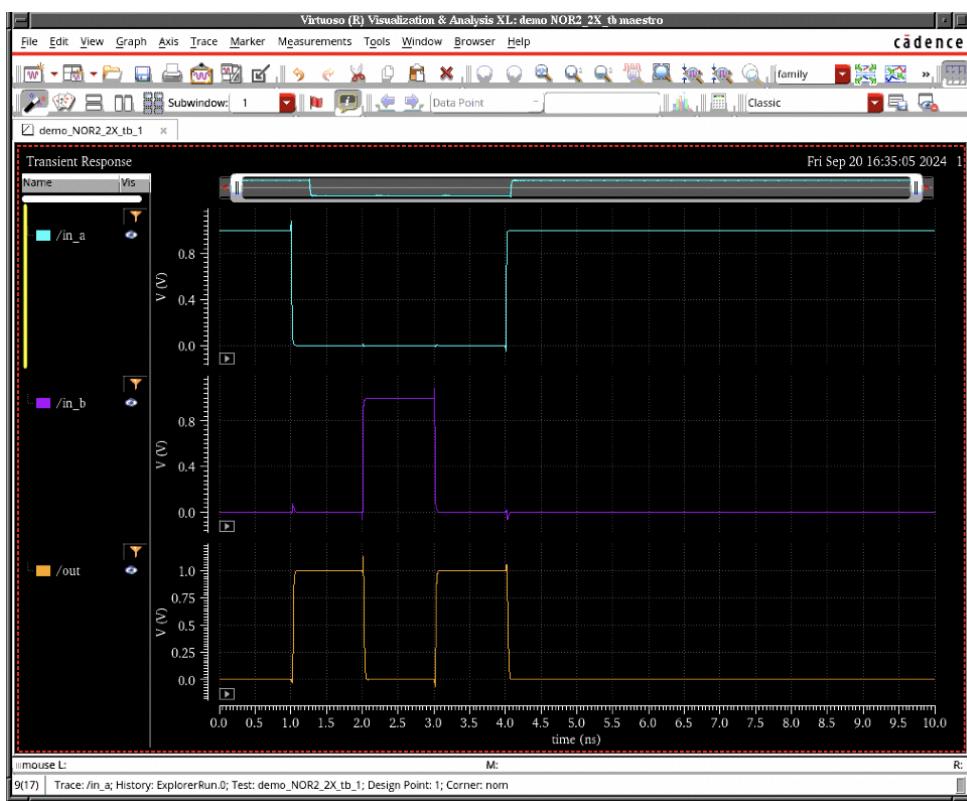
NOR2_2X schematic:



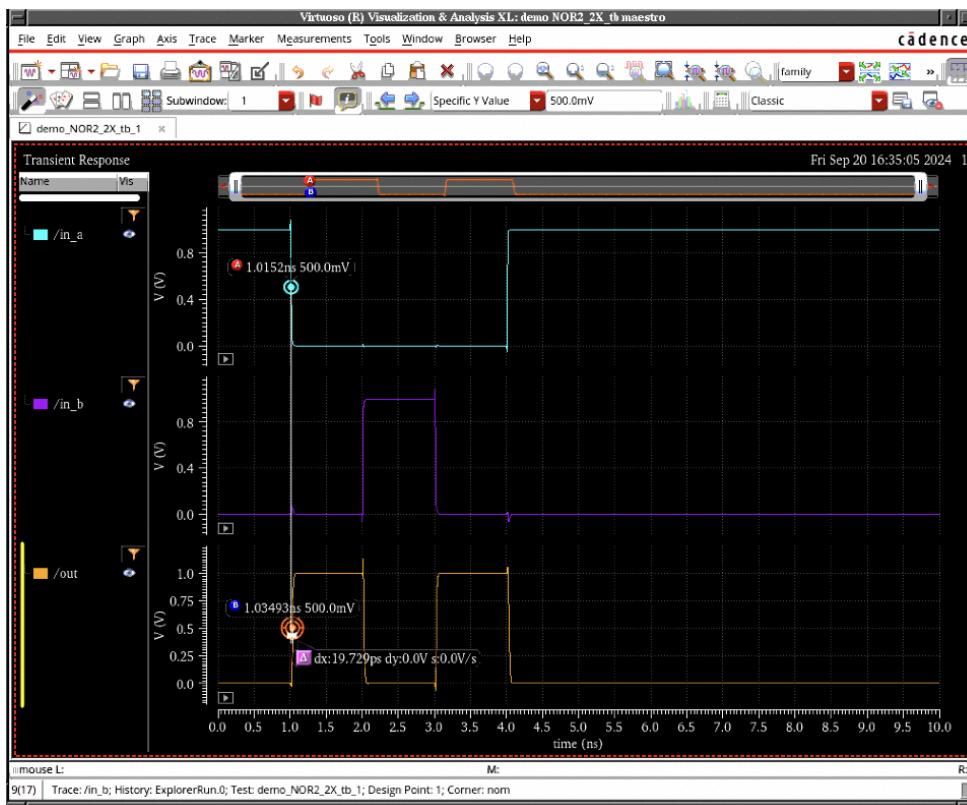
NOR2_2X testbench schematic:



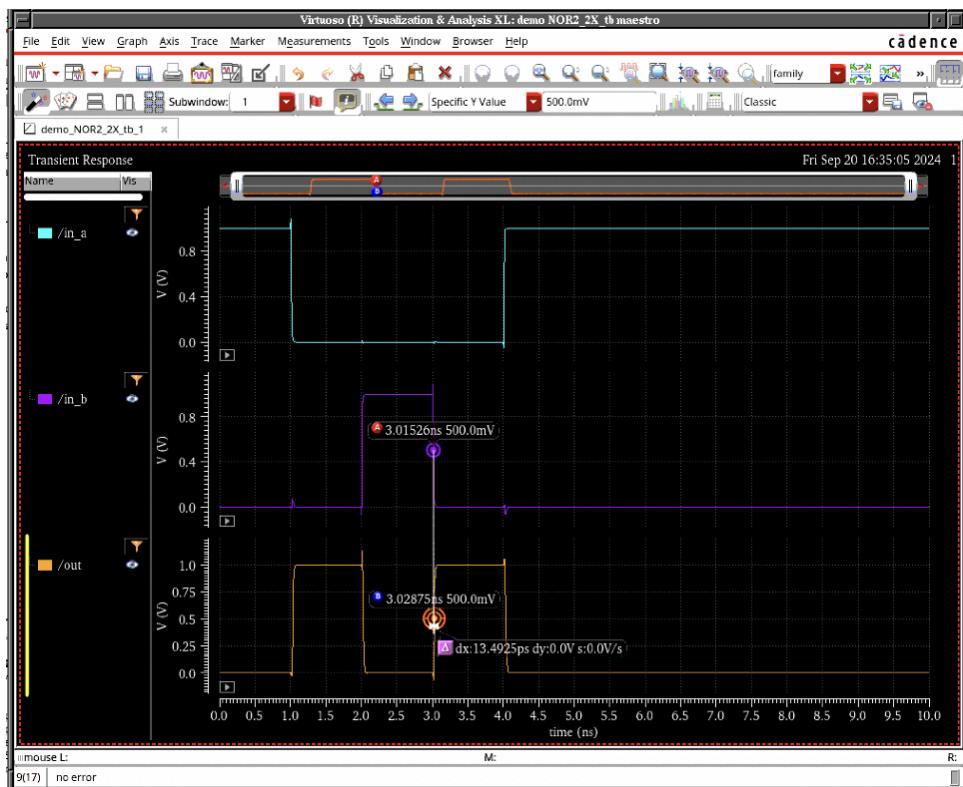
input-output waveforms (function verification) :



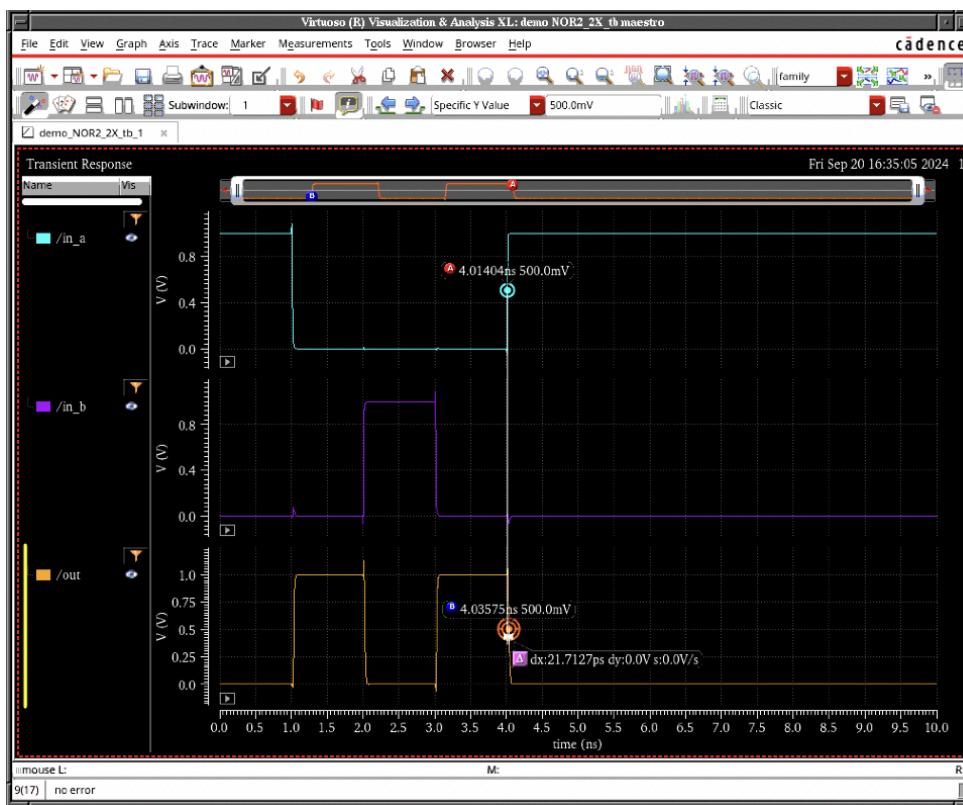
NOR2_2X (1,0) -> (0,0) Rising Delay: 19.729ps



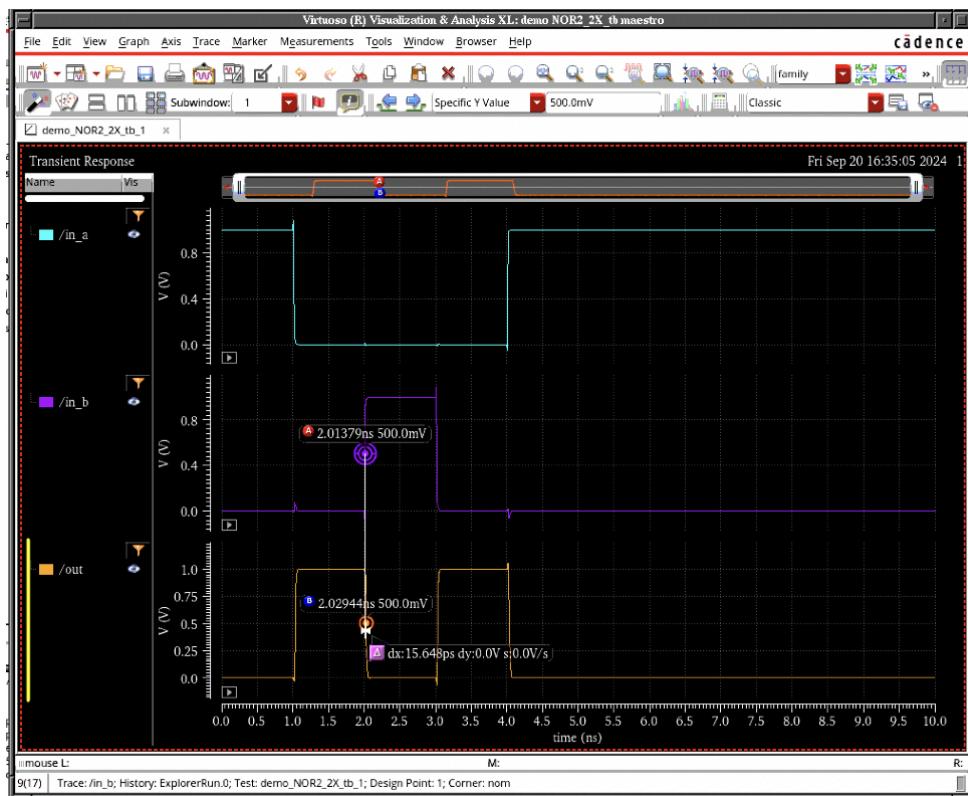
NOR2_2X (0,1) -> (0,0) Rising Delay: 13.493ps



NOR2_2X (0,0) -> (1,0) Falling Delay: 21.713ps



NOR2_2X (0,0) -> (0,1) Falling Delay: 15.648ps



Worst case delays NOR2_2X(input = (A,B))

Rising delay(ps)		Falling delay(ps)	
(A,B) = (1,0) -> (0,0)	19.729	(A,B) = (0,0) -> (1,0)	21.713
(A,B) = (0,1) -> (0,0)	13.493	(A,B) = (0,0) -> (0,1)	15.648

I'm not sure which is the USER ID for Cadence Virtuoso, So I took screenshot of my VNCviewer window and my whole demo library

