6502C	
GND	RST
RDY	Φ2
Φ1	S0
IRQ	BΦ0/Φ0
NC	R/W
NMI	HALT
SYNC	NC
+5V	D0
A0	D1
A1	D2
A2	D3
A3	D4
A4	D5
A5	D6
A6	D7
A7	A15
A8	A14
A9	A13
A10	A12
A11	GND

ANTIC	
GND	D4
AN0	D5
AN1	D6
LP	D7
AN2	RST
RNMI	F00
NMI	Φ0
REF	D3
HALT	D2
A3	D1
A2	D0
A1	BΦ2
A0	A4
R/W	+5V
RDY	A6
A10	A7
A12	A8
A13	A9
A14	A11
A15	+5V

GTIA	
A1	A2
A0	A3
GND	A4
D3	D4
D2	D5
D1	D6
D0	D7
T0	R/W
T1	CS
T2	LUM0
T3	BΦ2
S0	F00
S1	OSC
S2	+5V
S3	HALT
PAL	CSYNC
CADJ	LUM2
AN0	LUM2
AN1	LUM1
AN2	COLOR

POKEY	
GND	D2
D3	D1
D4	D0
D5	AUDIO
D6	A0
D7	A1
BΦ2	A2
P6	A3
P7	R/W
P4	CS1
P5	CS0
P2	IRQ
P3	SOD
P0	ACLK
P1	BCLK
KR2	KR1
+5V	SID
K5	K0
K4	K1
K3	K2

PIA	
GND	CA1
PA0	CA2
PA1	IRQA
PA2	IRQB
PA3	A1
PA4	A0
PA5	RST
PA6	D0
PA7	D1
PB0	D2
PB1	D3
PB2	D4
PB3	D5
PB4	D6
PB5	D7
PB6	BΦ2
PB7	CS1
CB1	CS2
CB2	CS0
+5V	R/W

FREDDIE	
CLKout	+5V
CLKin	RST
EXTSEL	R/W
CASINH	OSC
Φ2	CAS16K
LE	CAS
OE	WRT
A0	RAS
A1	RA0
A2	RA1
A3	RA2
A4	RA3
A5	RA4
A6	RA5
A7	RA6
A8	RA7
A9	FA15
A10	FA14
A11	A13
GND	A12

Supplementary Information on Φ0 and Φ2 Signals

1. Φ2 is the clock signal generated by the 6502C Sally.
   Most chips use the Buffered Φ2 signal (BΦ2), while Freddie is the only chip that directly uses Φ2.

2. The 65XE (without ECI) and XEGS have Φ0 directly connected from Antic to Sally.
   In contrast, the 130XE board has Sally clocked by the Buffered Φ0 (BΦ0) signal.