ADS127L21 512-kSPS, Programmable Filter, 24-Bit, Wideband Delta-Sigma ADC

1 Features

- Programmable FIR filter
- Programmable IIR filter
- Wideband or low-latency filter modes
- Programmable data rates:
  - Wideband filter: 512 kSPS
  - Low-latency filter: 1.365 MSPS
- Conversion latency (low-latency filter): 3 µs
- AC accuracy with dc precision:
  - Dynamic range (200 kSPS): 111.5 dB (typical)
  - THD: –125 dB (typical)
  - INL: 0.4 ppm of FS (typical)
  - Offset drift: 50 nV/°C (typical)
  - Gain drift: 0.5 ppm/°C (typical)
- Power-scalable speed ranges:
  - Max speed: 512 kSPS, 33 mW (typical)
  - High speed: 400 kSPS, 26 mW (typical)
  - Mid speed: 200 kSPS, 14 mW (typical)
  - Low speed: 50 kSPS, 4.3 mW (typical)
- Input range: $\pm V_{REF}$ or $\pm 2\ V_{REF}$
- Buffered inputs
- Internal or external clock operation
- Functional Safety-Capable
  - Documentation available to aid functional safety system design

2 Applications

- Test and measurement:
  - Data acquisition (DAQ)
  - Acoustics and dynamic strain gauges
- Factory automation and control:
  - Vibration, condition monitoring
- Medical:
  - Doppler ultrasound
- Grid infrastructure:
  - Power quality analyzers

3 Description

The ADS127L21 is a 24-bit, delta-sigma (ΔΣ), analog-to-digital converter (ADC) featuring a programmable digital filter with data rates up to 512 kSPS using the wideband filter and up to 1365 kSPS using the low-latency filter. The device offers an excellent combination of ac performance and dc precision with low power consumption.

Programmable infinite and finite impulse response (IIR and FIR) digital filters allow custom filter profiles, such as A-weighting compensation and frequency notch filters. The wideband or low-latency filter option optimize ac-signal performance or data throughput of dc signals, all in one device.

The low-drift modulator achieves excellent dc precision with low wideband noise for outstanding ac performance. The power-scalable architecture features four speed modes to optimize data rate, resolution, and power consumption. Signal and reference input buffers reduce driver loading for increased accuracy.

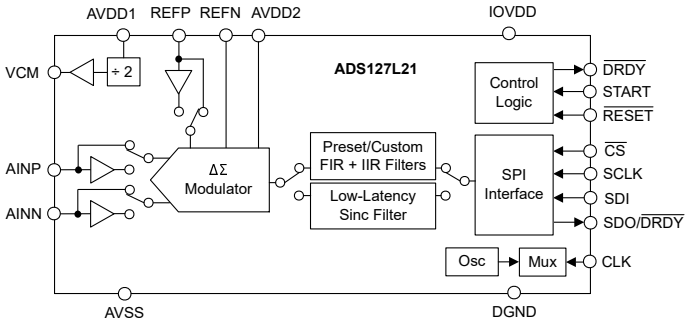
The serial interface features daisy-chain capability to reduce the number of signal lines over an isolation barrier. SPI input data and register memory contents are validated by cyclic-redundancy check (CRC) to enhance operational reliability.

The small 3-mm × 3-mm WQFN package is designed for space-limited applications. The device is fully specified for operation over the –40°C to +125°C temperature range.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
ADS127L21	RUK (WQFN, 20)	3 mm × 3 mm

(1) See the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (March 2023) to Revision A (June 2023)	Page
• Changed document status from *Advance Information* to *Production Data*	1

5 Pin Configuration and Functions

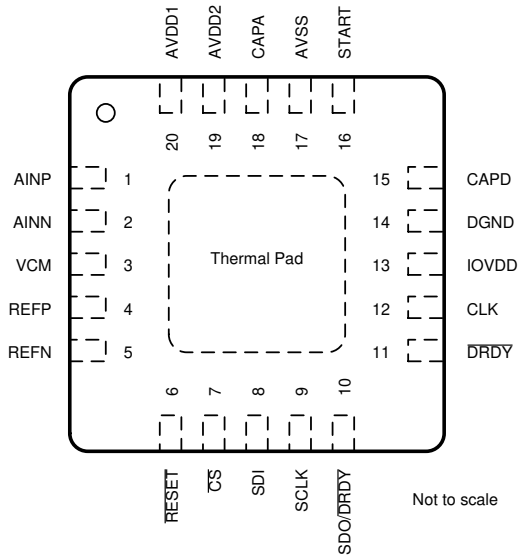


Figure 5-1. RUK Package, 20-Pin WQFN (Top View)

Table 5-1. Pin Functions

NAME	PIN NO.	TYPE	DESCRIPTION
AINN	2	Analog input	Negative analog input; see the *Analog Input* section for details.
AINP	1	Analog input	Positive analog input; see the *Analog Input* section for details.
AVDD1	20	Analog Supply	Positive analog supply 1; see the *Power Supplies* section for details.
AVDD2	19	Analog Supply	Positive analog supply 2; see the *Power Supplies* section for details.
AVSS	17	Analog Supply	Negative analog supply; see the *Power Supplies* section for details.
CAPA	18	Analog output	Analog voltage regulator output capacitor bypass.
CAPD	15	Analog output	Digital voltage regulator output capacitor bypass.
CLK	12	Digital input	Clock input; see the *Clock Operation* section for details.
$\overline{CS}$	7	Digital input	Chip select, active low; see the *Chip Select* section for details.
DGND	14	Ground	Digital ground.
$\overline{DRDY}$	11	Digital output	Data ready, active low; see the *Data Ready* section for details.
IOVDD	13	Digital Supply	I/O supply voltage; see the *Power Supplies* section for details.
REFN	5	Analog input	Negative reference input; see the *Reference Voltage* section for details.
REFP	4	Analog input	Positive reference input; see the *Reference Voltage* section for details.
$\overline{RESET}$	6	Digital input	Reset, active low; see the *Reset* section for details.
SCLK	9	Digital input	Serial data clock; see the *Serial Clock* section for details.
SDI	8	Digital input	Serial data input; see the *Serial Data Input* section for details.
SDO/$\overline{DRDY}$	10	Digital output	Serial data output and data ready (optional); see the *SDO/$\overline{DRDY}$* section for details.
START	16	Digital input	Conversion start; see the *Synchronization* section for details.
VCM	3	Analog output	Common-mode voltage output; see the *VCM Output Voltage* section for details.
Thermal Pad	Pad	—	Thermal power pad; connect to AVSS.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD1 to AVSS	–0.3	6.5	V
	AVDD2 to AVSS	–0.3	6.5	
	AVSS to DGND	–3	0.3	
	IOVDD to DGND	–0.3	6.5	
	IOVDD to AVSS		8.5	
LDO output pins	CAPD, CAPA	DGND – 0.3	1.65	V
Digital input/output voltage	SDO/$\overline{\text{DRDY}}$, $\overline{\text{DRDY}}$, START	DGND – 0.3	1.65	V
	$\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{RESET}}$, CLK	DGND – 0.3	6.5	
Input current	Continuous, any pin except power-supply pins(2)	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional – this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Analog input pins AINP, AINN, REFP, and REFN are diode-clamped to AVDD1 and AVSS. Limit the input current to 10 mA in the event the analog input voltage exceeds AVDD1 + 0.3 V or AVSS – 0.3 V. Digital input pin START and digital output pins SDO/$\overline{\text{DRDY}}$ and $\overline{\text{DRDY}}$ are diode-clamped to IOVDD and DGND. Digital input pins $\overline{\text{CS}}$, SCLK, SDI, $\overline{\text{RESET}}$ and CLK are diode-clamped to DGND. Limit the input current to 10 mA in the event the digital input voltage exceeds IOVDD + 0.3 V (for effected pins) or exceeds DGND – 0.3 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1500	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

				MIN	NOM	MAX	UNIT
POWER SUPPLY							
	Analog power supply	AVDD1 to AVSS	Max-speed mode	4.5		5.5	V
			High-speed mode	4.5		5.5	
			Mid-speed mode	3		5.5	
			Low-speed mode	2.85		5.5	
		AVDD1 to DGND		1.65			V
		Absolute ratio of AVSS / AVDD1 to DGND				1.2	V/V
		AVDD2 to AVSS		1.74		5.5	V
		AVSS to DGND		–2.75		0	
	Digital power supply	IOVDD to DGND		1.65		5.5	V
ANALOG INPUTS							
V_{AINP}, V_{AINN}	Absolute input voltage	Precharge buffer off		AVSS – 0.05		AVDD1 + 0.05	V
		Precharge buffer on		AVSS + 0.1		AVDD1 – 0.1	
V_{IN}	Differential input voltage $V_{IN} = V_{AINP} – V_{AINN}$	1x input range		$–V_{REF}$		V_{REF}	V
		2x input range		$–2·V_{REF}$		$2·V_{REF}$	
VOLTAGE REFERENCE INPUTS							
V_{REF}	Differential reference voltage $V_{REF} = V_{REFP} – V_{REFN}$	Low-reference range		0.5	2.5	2.75	V
		High-reference range		1	4.096	AVDD1 – AVSS	
V_{REFN}	Negative reference voltage			AVSS – 0.05			V
V_{REFP}	Positive reference voltage	Precharge buffer off				AVDD1 + 0.05	V
		Precharge buffer on				AVDD1 – 0.7	
CLOCK SIGNAL							
f_{CLK}	Frequency	Max-speed mode		0.5	32.768	33.6	MHz
		High-speed mode		0.5	25.6	26.2	
		Mid-speed mode		0.5	12.8	13.1	
		Low-speed mode		0.5	3.2	3.28	
DIGITAL INPUTS							
	Input voltage			DGND		IOVDD	V
TEMPERATURE RANGE							
T_A	Ambient temperature	Operational		–45		125	°C
		Specification		–40		125	

6.4 Thermal Information

THERMAL METRIC (1)		ADS127L21 WQFN (RUK) 20 PINS	UNIT
$R_{θJA}$	Junction-to-ambient thermal resistance	58.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	39.9	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	29.2	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	0.8	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	29.1	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	25.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, all speed modes, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS, MAX-SPEED MODE						
	Input current, differential input voltage	Precharge buffers off		125		µA/V
		Precharge buffers off, 2x input range		60		
		Precharge buffers on		±4		µA
	Input current drift, differential input voltage	Precharge buffers off		5		nA/V/°C
		Precharge buffers off, 2x input range		2		
		Precharge buffers on		5		nA/°C
	Input current, common-mode input voltage	Precharge buffers off		6.5		µA/V
		Precharge buffers off, 2x input range		3		
		Precharge buffers on		±4		µA
ANALOG INPUTS, HIGH-SPEED MODE						
	Input current, differential input voltage	Precharge buffers off		95		µA/V
		Precharge buffers off, 2x input range		47		
		Precharge buffers on		±3		µA
	Input current drift, differential input voltage	Precharge buffers off		3		nA/V/°C
		Precharge buffers off, 2x input range		1.5		
		Precharge buffers on		5		nA/°C
	Input current, common-mode input voltage	Precharge buffers off		5		µA/V
		Precharge buffers off, 2x input range		2.5		
		Precharge buffers on		±3		µA
ANALOG INPUTS, MID-SPEED MODE						
	Input current, differential input voltage	Precharge buffers off		47		µA/V
		Precharge buffers off, 2x input range		25		
		Precharge buffers on		±1.5		µA
	Input current drift, differential input voltage	Precharge buffers off		2		nA/V/°C
		Precharge buffers off, 2x input range		1		
		Precharge buffers on		5		nA/°C
	Input current, common-mode input voltage	Precharge buffers off		2.5		µA/V
		Precharge buffers off, 2x input range		1.3		
		Precharge buffers on		±1.5		µA
ANALOG INPUTS, LOW-SPEED MODE						
	Input current, differential input voltage	Precharge buffers off		12		µA/V
		Precharge buffers off, 2x input range		6		
		Precharge buffers on		±0.4		µA
	Input current drift, differential input voltage	Precharge buffers off		1		nA/V/°C
		Precharge buffers off, 2x input range		0.5		
		Precharge buffers on		0.2		nA/°C
	Input current, common-mode input voltage	Precharge buffers off		0.6		µA/V
		Precharge buffers off, 2x input range		0.3		
		Precharge buffers on		±0.4		µA

6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, all speed modes, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC PERFORMANCE							
	Resolution	OSR ≥ 32			24		Bits
	Noise				See the *Noise Performance* section for details		
INL	Integral nonlinearity (1)	T_A = 25°C ± 5°C			0.4	2.1	ppm of FSR
		T_A = 0°C to 70°C			0.4	2.5	
		T_A = –40°C to 125°C			0.4	2.9	
		Max-speed mode			1.5		
	Offset error	T_A = 25°C		–250	±30	250	µV
	Offset drift				50	200	nV/°C
	Offset long-term drift	1000 hr			0.5		µV
	Gain error	T_A = 25°C		–2500	±200	2500	ppm of FSR
	Gain drift				0.5	1	ppm of FSR/°C
	Gain long-term drift	1000 hr			10		ppm
NMRR	Normal-mode rejection ratio	f_{IN} = 50 Hz (±1 Hz), f_{DATA} = 50 SPS, sinc4 filter		100			dB
		f_{IN} = 60 Hz (±1 Hz), f_{DATA} = 60 SPS, sinc4 filter		100			
CMRR	Common-mode rejection ratio	At dc		110	130		dB
		Up to 10 kHz			115		
		At dc, 2x input range			95		
PSRR	Power-supply rejection ratio	AVDD1, dc		100	120		dB
		AVDD2, dc		115	130		
		IOVDD, dc		115	130		
AC PERFORMANCE, MAX-SPEED MODE (f_{CLK} = 32.768 MHz)							
f_{DATA}	Data rate	Full wideband filter		4		512	kSPS
		FIR2 wideband filter		8		1024	
		FIR1 wideband filter		16		2048	
		Low-latency filter		0.1024		1365.3	
DR	Dynamic range	Inputs shorted, OSR = 64, f_{DATA} = 256 kSPS	Wideband filter	109	111.5		dB
			Wideband filter, V_{REF} = 2.5 V		107.5		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		108.5		
			Sinc4 filter	112	114		
			Sinc4 filter, V_{REF} = 2.5 V		110.5		
			Sinc4 filter, V_{REF} = 2.5 V, 2x input range		111		

6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, all speed modes, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 256 kSPS	Wideband filter		110		dB
			Wideband filter, V_{REF} = 2.5 V		106		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		107		
			Sinc4 filter		112		
			Sinc4 filter, V_{REF} = 2.5 V		108.5		
			Sinc4 filter V_{REF} = 2.5 V, 2x input range		110		
THD	Total harmonic distortion	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS OSR = 64, f_{DATA} = 256 kSPS	V_{REF} = 2.5 V		–119	–108	dB
			V_{REF} = 4.096 V		–110	–103	
IMD	Intermodulation distortion	f_{IN} = 9.7 and 10.3 kHz, V_{IN} = –6.5 dBFS	Second-order terms		–125		dB
			Third-order terms		–125		
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64			125		dB
AC PERFORMANCE, HIGH-SPEED MODE (f_{CLK} = 25.6 MHz)							
f_{DATA}	Data rate	Full wideband filter		3.125		400	kSPS
		FIR2 wideband filter		6.25		800	
		FIR1 wideband filter		12.5		1600	
		Low-latency filter		0.08		1067	
DR	Dynamic range	Inputs shorted, OSR = 64, f_{DATA} = 200 kSPS	Wideband filter	109	111.5		dB
			Wideband filter, V_{REF} = 2.5 V		107.5		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		108.5		
			Sinc4 filter	112	114.5		
			Sinc4 filter, V_{REF} = 2.5 V		110.5		
			Sinc4 filter, V_{REF} = 2.5 V, 2x input range		111		
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 200 kSPS	Wideband filter		110		dB
			Wideband filter, V_{REF} = 2.5 V		106		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		107		
			Sinc4 filter		112		
			Sinc4 filter, V_{REF} = 2.5 V		108.5		
			Sinc4 filter, V_{REF} = 2.5 V, 2x input range		110		
THD	Total harmonic distortion	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 200 kSPS	V_{REF} = 2.5 V		–125	-113	dB
			V_{REF} = 4.096 V		–125	-106	
IMD	Intermodulation distortion	f_{IN} = 9.7 and 10.3 kHz, V_{IN} = –6.5 dBFS	Second-order terms		–125		dB
			Third-order terms		–125		dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64			125		dB

6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, all speed modes, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE, MID-SPEED MODE (f_{CLK} = 12.8 MHz)							
f_{DATA}	Data rate	Full wideband filter		1.5625		200	kSPS
		FIR2 wideband filter		3.125		400	
		FIR1 wideband filter		6.25		800	
		Low-latency filter		0.08		533.3	
DR	Dynamic range	Inputs shorted, OSR = 64, f_{DATA} = 100 kSPS	Wideband filter	109	112		dB
			Wideband filter, V_{REF} = 2.5 V		107.5		
			Wideband filter, V_{REF} = 2.5 V 2x input range		108.5		
			Sinc4 filter	112	114.5		
			Sinc4 filter, V_{REF} = 2.5 V		110.5		
			Sinc4 filter, V_{REF} = 2.5 V, 2x input range		111		
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 100 kSPS	Wideband filter		110		dB
			Wideband filter, V_{REF} = 2.5 V		106		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		107		
			Sinc4 filter		112		
			Sinc4 filter, V_{REF} = 2.5 V		108.5		
			Sinc4 filter, V_{REF} = 2.5 V, 2x input range		110		
THD	Total harmonic distortion	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 100 kSPS	V_{REF} = 2.5 V		–125	–117	dB
			V_{REF} = 4.096 V		–125	–115	
IMD	Intermodulation distortion	f_{IN} = 9.7 and 10.3 kHz, V_{IN} = –6.5 dBFS	Second-order terms		–125		dB
			Third-order terms		–125		
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64			125		dB
AC PERFORMANCE, LOW-SPEED MODE (f_{CLK} = 3.2 MHz)							
f_{DATA}	Data rate	Full wideband filter		0.390625		50	kSPS
		FIR2 wideband filter		0.78125		100	
		FIR1 wideband filter		1.5625		200	
		Low-latency filter		0.01		133.3	
DR	Dynamic range	Inputs shorted, OSR = 64, f_{DATA} = 25 kSPS	Wideband filter	109	112		dB
			Wideband filter, V_{REF} = 2.5 V		107.5		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		108.5		
			Sinc4 filter	112	114.5		
			Sinc4 filter, V_{REF} = 2.5 V		110.5		
			Sinc4 filter, V_{REF} = 2.5 V, 2x input range		111.5		

6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, all speed modes, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 25 kSPS	Wideband filter		110		dB
			Wideband filter, V_{REF} = 2.5 V		106		
			Wideband filter, V_{REF} = 2.5 V, 2x input range		108		
			Sinc4 filter		112		
			Sinc4 filter, V_{REF} = 2.5 V		108		
			Sinc4 filter, V_{REF} = 2.5 V, 2x input range		110		
THD	Total harmonic distortion	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64, f_{DATA} = 25 kSPS	V_{REF} = 2.5 V		–125	–114	dB
			V_{REF} = 4.096 V		–125	–113	
IMD	Intermodulation distortion	f_{IN} = 9.7 and 10.3 kHz, V_{IN} = –6.5 dBFS	Second-order terms		–125		dB
			Third-order terms		–125		dB
SFDR	Spurious-free dynamic range	f_{IN} = 1 kHz, V_{IN} = –0.2 dBFS, OSR = 64			125		dB
DEFAULT FIR FILTER							
	Pass-band frequency	Within envelope of pass-band ripple			0.4 · f_{DATA}		Hz
		–0.1-dB frequency			0.4125 · f_{DATA}		
		–3-dB frequency			0.4374 · f_{DATA}		
	Pass-band ripple			–0.0004		0.0004	dB
	Stop-band frequency	At stop-band attenuation			0.5 · f_{DATA}		Hz
	Stop-band attenuation(1)				106		dB
	Group delay				34 / f_{DATA}		s
	Settling time				68 / f_{DATA}		s
	Overall decimation ratio			8		4096	
PROGRAMMABLE FIR3 FILTER							
	Number of taps				128		
	Coefficient resolution				32		bits
	Coefficient format				1.31		
	Decimal range			–1		$1 – 1/2^{31}$	
	Decimation ratio				2		
PROGRAMMABLE IIR FILTER							
	Implementation				Four biquads, direct form 1		
	Scale factors				5		
	Coefficient resolution				32		bits
	Coefficient format				2.30		
	Decimal range			–2		$2 – 2/2^{31}$	
	Decimation ratio				1		
VOLTAGE REFERENCE INPUTS							
	REFP and REFN input current	REFP precharge buffer off	Max-speed mode		225		µA/V
			High-speed mode		190		
			Mid-speed mode		130		
			Low-speed mode		80		
	REFP input current	REFP precharge buffer on			±2		µA

6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, all speed modes, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	REFP and REFN input current drift	REFP precharge buffer off	Max-speed mode		10		nA/°C
			High-speed mode		10		
			Mid-speed mode		10		
			Low-speed mode		10		
	REFP input current drift	REFP precharge buffer on			5		nA/°C
INTERNAL OSCILLATOR							
	Frequency			25.4	25.6	25.8	MHz
VCM OUTPUT VOLTAGE							
	Output voltage				(AVDD1 + AVSS) / 2		V
	Accuracy			–1%	±0.1%	1%	
	Voltage noise	1-kHz bandwidth			25		μV_{RMS}
	Start-up time	C_L = 100 nF			1		ms
	Capacitive load					100	nF
	Resistive load			2			kΩ
	Short-circuit current limit				10		mA
DIGITAL INPUTS/OUTPUTS							
V_{IL}	Logic-low input threshold					0.3 IOVDD	V
V_{IH}	Logic-high input threshold			0.7 IOVDD			V
	Input hysteresis				150		mV
	Input current	Excluding $\overline{RESET}$ pin		–1		1	µA
	$\overline{RESET}$ pin pullup resistor				20		kΩ
V_{OL}	Logic-low output voltage	OUT_DRV = 0b, I_{OL} = 2 mA				0.2 · IOVDD	V
		OUT_DRV = 1b, I_{OL} = 1 mA				0.2 · IOVDD	
V_{OH}	Logic-high output voltage	OUT_DRV = 0b, I_{OH} = –2 mA		0.8 · IOVDD			V
		OUT_DRV = 1b, I_{OH} = –1 mA		0.8 · IOVDD			
ANALOG SUPPLY CURRENT							
I_{AVDD1}, I_{AVSS}	AVDD1 and AVSS current (buffers off)	Max-speed mode			2.1	2.2	mA
		High-speed mode			1.7	1.8	
		Mid-speed mode			0.9	1.0	
		Low-speed mode			0.25	0.3	
		Standby mode			35		µA
		Power-down mode			5		
	AVDD1 and AVSS additional current (per buffer function)	Input precharge buffer	Max-speed mode		1.75	2.3	mA
			High-speed mode		1.35	1.9	
			Mid-speed mode		0.7	1.0	
			Low-speed mode		0.2	0.3	
		REFP precharge buffer	Max-speed mode		1.8	1.95	mA
			High-speed mode		1.5	1.6	
			Mid-speed mode		0.9	1.0	
			Low-speed mode		0.4	0.5	
		VCM buffer			0.1		mA

6.5 Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C; typical specifications are at T_A = 25°C; all specifications are at AVDD1 = 5 V, AVDD2 = 1.8 V to 5 V, AVSS = 0 V, IOVDD = 1.8 V, V_{IN} = 0 V, V_{CM} = 2.5 V, V_{REFP} = 4.096 V, V_{REFN} = 0 V, high-reference range, 1x input range, all speed modes, input precharge buffers on, and reference precharge buffer on (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{AVDD2}, I_{AVSS}	AVDD2 and AVSS current	Max-speed mode			4.5	4.9	mA
		High-speed mode			3.5	3.8	
		Mid-speed mode			2.2	2.5	
		Low-speed mode			0.85	0.95	
		Standby mode			60		µA
		Power-down mode			1		
DIGITAL SUPPLY CURRENT							
I_{IOVDD}	IOVDD current	Wideband filter, OSR = 32, IIR filter off	Max-speed mode		7.2	8.5	mA
			High-speed mode		5.7	6.8	
			Mid-speed mode		2.8	3.4	
			Low-speed mode		0.75	0.9	
		Low-latency filter, OSR = 32	Max-speed mode		1.1	1.3	mA
			High-speed mode		0.85	1.0	
			Mid-speed mode		0.45	0.55	
			Low-speed mode		0.15	0.18	
		Standby mode	External clock		10		µA
			Internal oscillator		40		
		Power-down mode			10		µA
	IOVDD additional current	IIR filter on, OSR = 32, High-speed mode	FIR/IIR sequence		0.3		mA
			IIR/FIR sequence		0.6		
POWER DISSIPATION							
P_D	Power dissipation	AVDD2 = 1.8 V, Precharge buffers off, IIR and FIR filters, OSR = 32	Max-speed mode		32.8		mW
			High-speed mode		26		
			Mid-speed mode		14		
			Low-speed mode		4.3		
		AVDD2 = 1.8 V, Precharge buffers off, Low-latency filter, OSR = 32	Max-speed mode		20.6		mW
			High-speed mode		16.3		
			Mid-speed mode		9.3		
			Low-speed mode		3.1		

(1) Best-fit method
(2) Stop-band attenuation as provided by the digital filter. Input frequencies in the stop band intermodulate with multiples of the chop frequency beginning at f_{MOD} / 32, which results in stop-band attenuation exceeding 106 dB. See the Stop-Band Attenuation figure for details.

6.6 Timing Requirements (1.65 V ≤ IOVDD ≤ 2 V)

over operating ambient temperature range, unless otherwise noted

		MIN	MAX	UNIT
CLK PIN				
$t_{c(CLK)}$	CLK period, max-speed mode	29.7	2000	ns
	CLK period, high-speed mode	38.2	2000	
	CLK period, mid-speed mode	76.4	2000	
	CLK period, low-speed mode	305	2000	
$t_{w(CLKL)}$	Pulse duration, CLK low, max-speed mode	13.2		ns
	Pulse duration, CLK low, high-speed mode	17		
	Pulse duration, CLK low, mid-speed mode	34		
	Pulse duration, CLK low, low-speed mode	128		
$t_{w(CLKH)}$	Pulse duration, CLK high, max-speed mode	13.2		ns
	Pulse duration, CLK high, high-speed mode	17		
	Pulse duration, CLK high, mid-speed mode	34		
	Pulse duration, CLK high, low-speed mode	128		
SPI SERIAL INTERFACE				
$t_{c(SC)}$	SCLK period	25	$1/(4 \cdot f_{DATA})$	ns
$t_{w(SCL)}$	Pulse duration, SCLK low	10		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	10		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	4		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	6		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
$t_{d(FF)}$	Delay time, between SPI frames during filter coefficient read/write operations	10		t_{CLK}
RESET PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t_{CLK}
$t_{d(RSSC)}$	Delay time, communication start after $\overline{RESET}$ rising edge or after SPI RESET pattern	10000		t_{CLK}
START PIN				
$t_{w(STL)}$	Pulse duration, START low	4		t_{CLK}
$t_{w(STH)}$	Pulse duration, START high	4		t_{CLK}
$t_{su(STCLK)}$	Setup time, START high before CLK rising edge (1)	9		ns
$t_{h(STCLK)}$	Hold time, START high after CLK rising edge (1)	9		ns
$t_{su(STDR)}$	Setup time, START falling edge or STOP bit before $\overline{DRDY}$ falling edge to stop next conversion (start/stop conversion mode)	8		t_{CLK}

(1) Do not apply START rising edge between the setup and hold times of CLK rising edge.

6.7 Switching Characteristics (1.65 V ≤ IOVDD ≤ 2 V)

over operating ambient temperature range, OUT_DRV = 0b, C_{LOAD} = 20 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI SERIAL INTERFACE						
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		2			t_{CLK}
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO/$\overline{DRDY}$ driven state				20	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO/$\overline{DRDY}$ high impedance state				20	ns
$t_{h(SCDO)}$	Hold time, SCLK rising edge to invalid SDO/$\overline{DRDY}$		3			ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid SDO/$\overline{DRDY}$				23	ns
$t_{p(SCDR)}$	Propagation delay time, 8th SCLK falling edge to $\overline{DRDY}$ return high				5	t_{CLK}
$t_{p(DODR)}$	Propagation delay time, last SCLK falling edge of read operation for SDO/$\overline{DRDY}$ transition from SDO to $\overline{DRDY}$ mode	Dual function SDO/$\overline{DRDY}$ mode			50	ns

6.8 Timing Requirements (2 V < IOVDD ≤ 5.5 V)

over operating ambient temperature range, unless otherwise noted

		MIN	MAX	UNIT
CLK PIN				
$t_{c(CLK)}$	CLK period, max-speed mode	29.7	2000	ns
	CLK period, high-speed mode	38.2	2000	
	CLK period, mid-speed mode	76.4	2000	
	CLK period, low-speed mode	305	2000	
$t_{w(CLKL)}$	Pulse duration, CLK low, max-speed mode	13.2		ns
	Pulse duration, CLK low, high-speed mode	17		
	Pulse duration, CLK low, mid-speed mode	34		
	Pulse duration, CLK low, low-speed mode	128		
$t_{w(CLKH)}$	Pulse duration, CLK high, max-speed mode	13.2		ns
	Pulse duration, CLK high, high-speed mode	17		
	Pulse duration, CLK high, mid-speed mode	34		
	Pulse duration, CLK high, low-speed mode	128		
SPI SERIAL INTERFACE				
$t_{c(SC)}$	SCLK period	19.5	$1/(4 \cdot f_{DATA})$	ns
$t_{w(SCL)}$	Pulse duration, SCLK low	8		ns
$t_{w(SCH)}$	Pulse duration, SCLK high	8		ns
$t_{d(CSSC)}$	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10		ns
$t_{su(DI)}$	Setup time, SDI valid before SCLK falling edge	4		ns
$t_{h(DI)}$	Hold time, SDI valid after SCLK falling edge	6		ns
$t_{d(SCCS)}$	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	10		ns
$t_{w(CSH)}$	Pulse duration, $\overline{CS}$ high	20		ns
$t_{d(FF)}$	Delay time, between SPI frames during filter coefficient read/write operations	10		t_{CLK}
RESET PIN				
$t_{w(RSL)}$	Pulse duration, $\overline{RESET}$ low	4		t_{CLK}
$t_{d(RSSC)}$	Delay time, communication start after $\overline{RESET}$ rising edge or after SPI RESET pattern	10000		t_{CLK}
START PIN				
$t_{w(STL)}$	Pulse duration, START low	4		t_{CLK}
$t_{w(STH)}$	Pulse duration, START high	4		t_{CLK}
$t_{su(STCLK)}$	Setup time, START high before CLK rising edge (1)	9		ns
$t_{h(STCLK)}$	Hold time, START high after CLK rising edge (1)	9		ns
$t_{su(STDR)}$	Setup time, START falling edge or STOP bit before $\overline{DRDY}$ falling edge to stop next conversion (start/stop conversion mode)	8		t_{CLK}

(1) Do not apply START rising edge between the setup and hold times of CLK rising edge.

6.9 Switching Characteristics (2 V < IOVDD ≤ 5.5 V)

over operating ambient temperature range, OUT_DRV = 0b, C_{LOAD} = 20 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPI SERIAL INTERFACE						
$t_{w(DRH)}$	Pulse duration, $\overline{DRDY}$ high		2			t_{CLK}
$t_{p(CSDO)}$	Propagation delay time, $\overline{CS}$ falling edge to SDO/$\overline{DRDY}$ driven				17	ns
$t_{p(CSDOZ)}$	Propagation delay time, $\overline{CS}$ rising edge to SDO/$\overline{DRDY}$ high impedance state				17	ns
$t_{h(SCDO)}$	Hold time, SCLK rising edge to invalid SDO/$\overline{DRDY}$		3			ns
$t_{p(SCDO)}$	Propagation delay time, SCLK rising edge to valid SDO/$\overline{DRDY}$				19	ns
$t_{p(SCDR)}$	Propagation delay time, 8th SCLK falling edge to $\overline{DRDY}$ return high				5	t_{CLK}
$t_{p(DODR)}$	Propagation delay time, last SCLK falling edge of read operation for SDO/$\overline{DRDY}$ transition from SDO to $\overline{DRDY}$ mode	Dual function SDO/$\overline{DRDY}$ mode			50	ns

6.10 Timing Diagrams

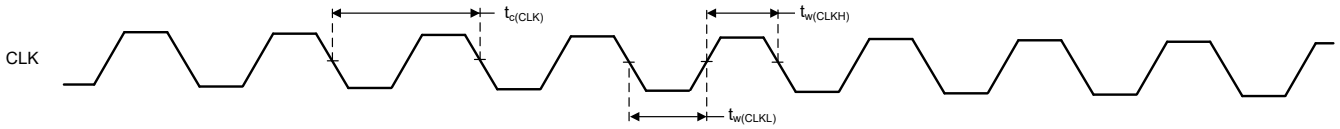


Figure 6-1. Clock Timing Requirements

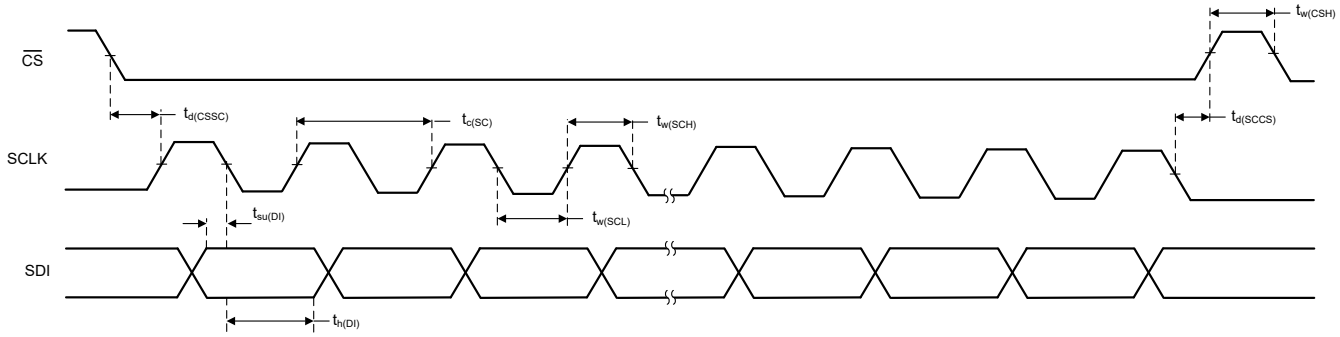


Figure 6-2. Serial Interface Timing Requirements

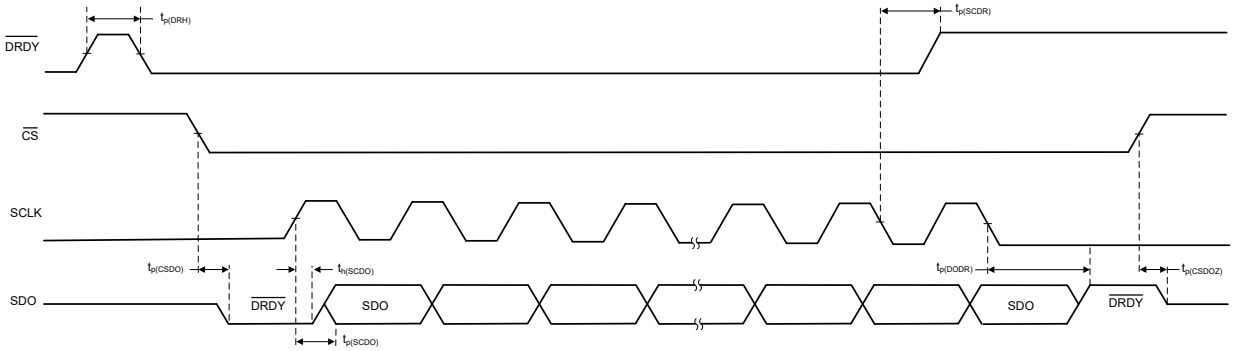


Figure 6-3. Serial Interface Switching Characteristics

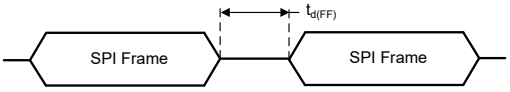


Figure 6-4. SPI Frame Timing Requirement

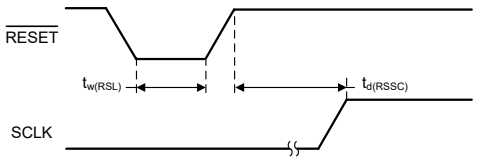


Figure 6-5. $\overline{RESET}$ Pin Timing

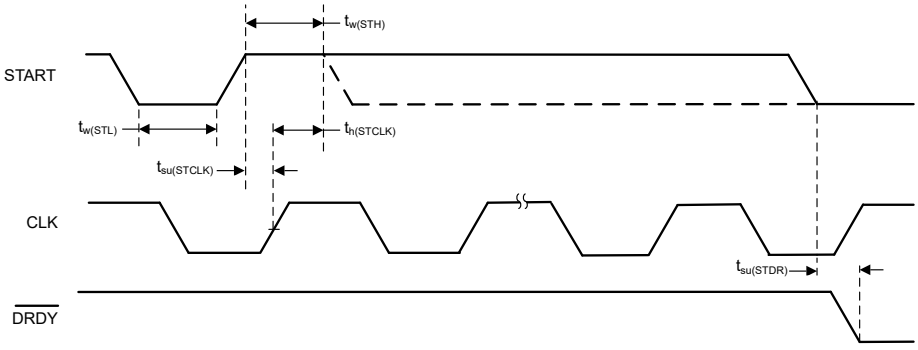
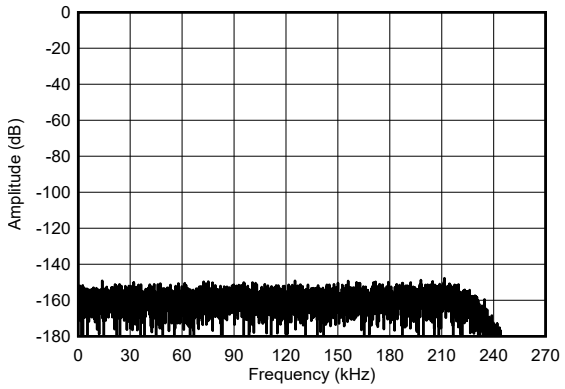


Figure 6-6. START Pin Timing

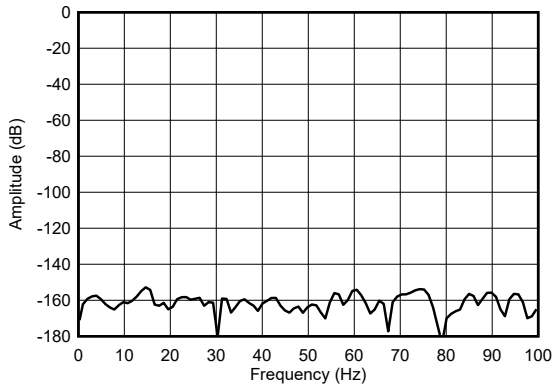
6.11 Typical Characteristics

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



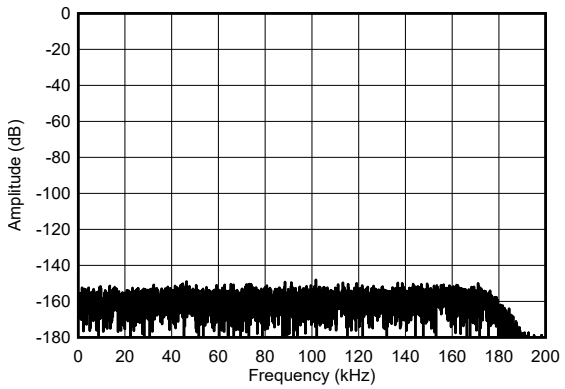
Wideband filter

Figure 6-7. Maximum-Speed Mode, Shorted-Input FFT



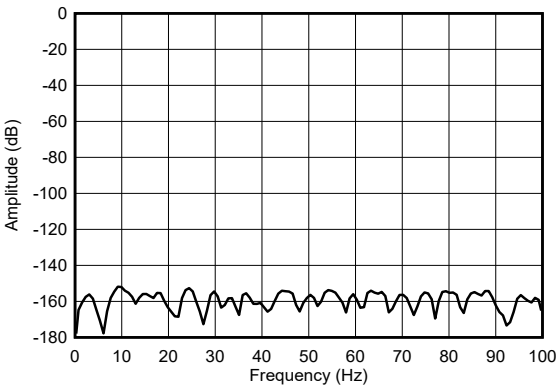
0 Hz–100 Hz

Figure 6-8. Maximum-Speed Mode, Shorted-Input FFT



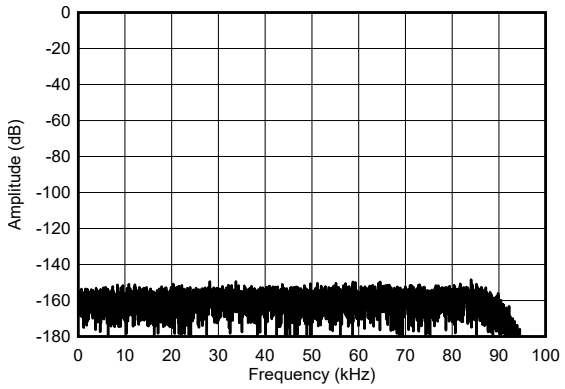
Wideband filter

Figure 6-9. High-Speed Mode, Shorted-Input FFT



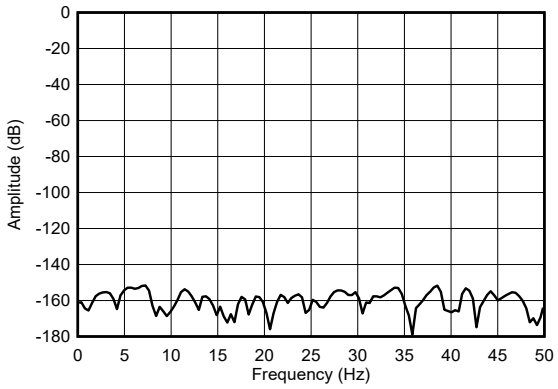
0 Hz–100 Hz

Figure 6-10. High-Speed Mode, Shorted-Input FFT



Wideband filter

Figure 6-11. Mid-Speed Mode, Shorted-Input FFT

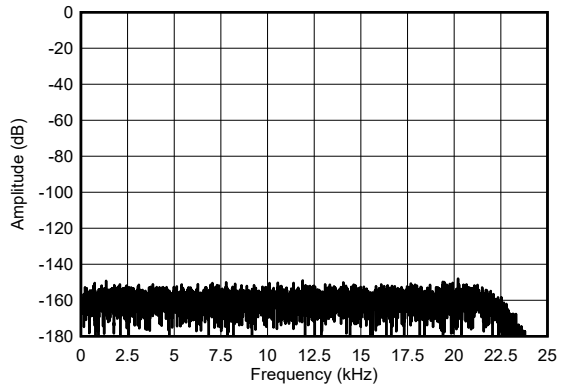


0 Hz–50 Hz

Figure 6-12. Mid-Speed Mode, Shorted-Input FFT

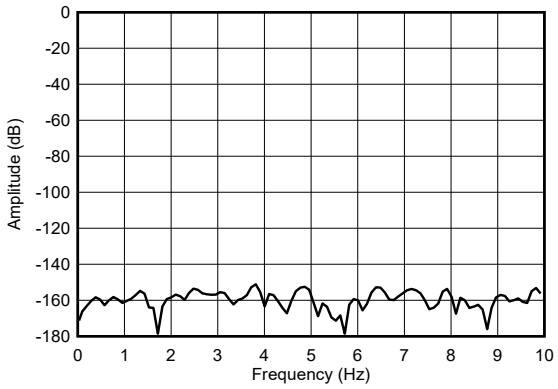
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



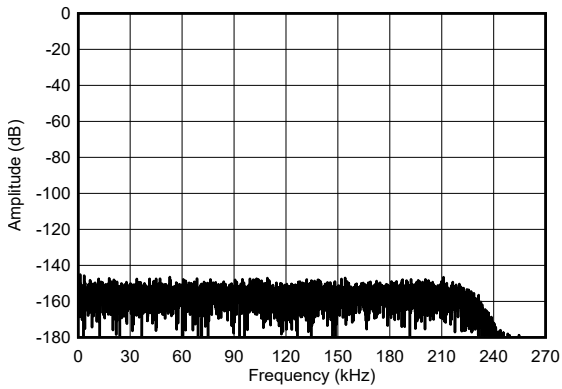
Wideband filter

Figure 6-13. Low-Speed Mode, Shorted-Input FFT



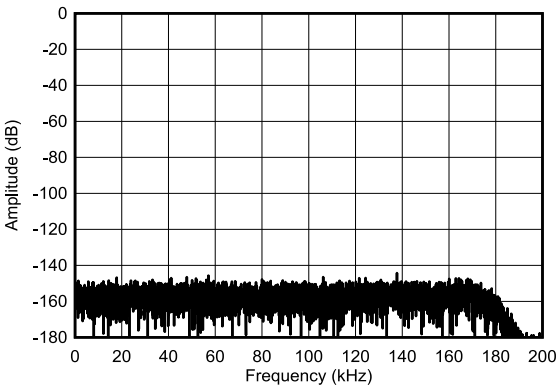
0 Hz–50 Hz

Figure 6-14. Low-Speed Mode, Shorted-Input FFT



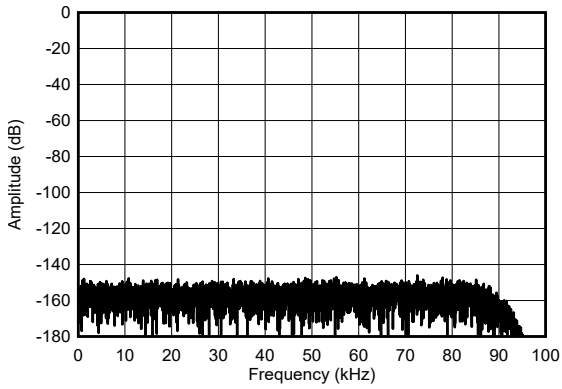
V_{REF} = 2.5 V, wideband filter, 2x range

Figure 6-15. Maximum-Speed Mode, Shorted-Input FFT



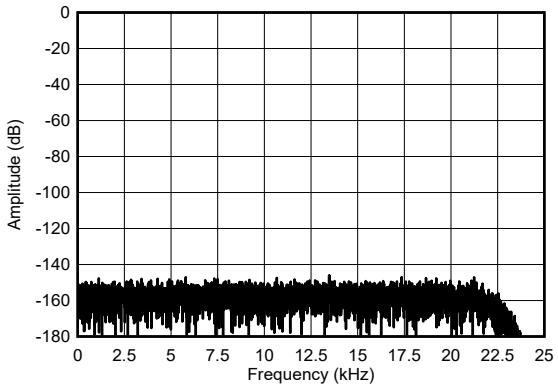
V_{REF} = 2.5 V, wideband filter, 2x range

Figure 6-16. High-Speed Mode, Shorted-Input FFT



V_{REF} = 2.5 V, wideband filter, 2x range

Figure 6-17. Mid-Speed Mode, Shorted-Input FFT

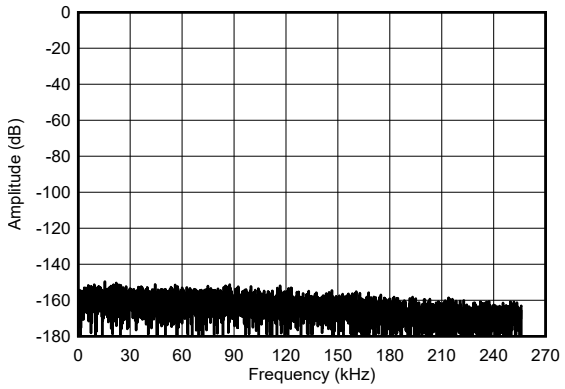


V_{REF} = 2.5 V, wideband filter, 2x range

Figure 6-18. Low-Speed Mode, Shorted-Input FFT

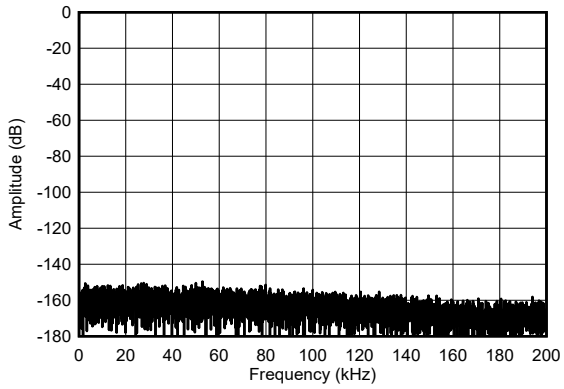
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



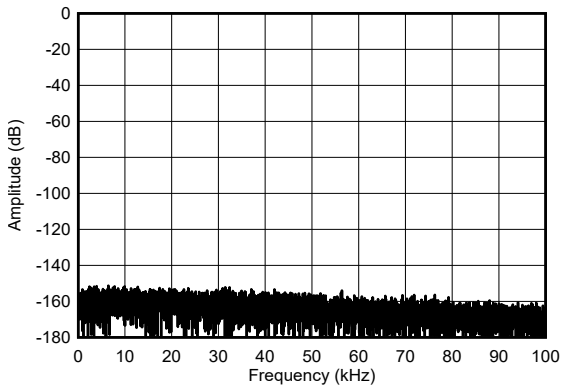
Sinc4 filter

Figure 6-19. Maximum-Speed Mode, Shorted-Input FFT



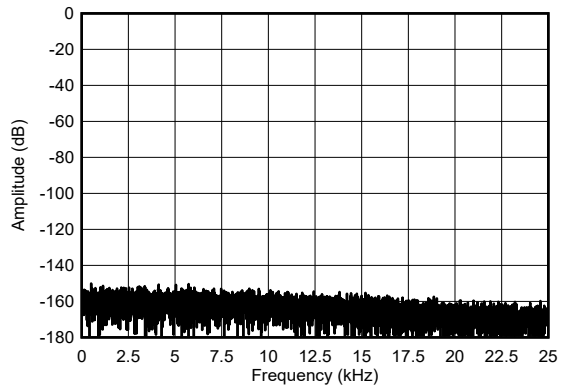
Sinc4 filter

Figure 6-20. High-Speed Mode, Shorted-Input FFT



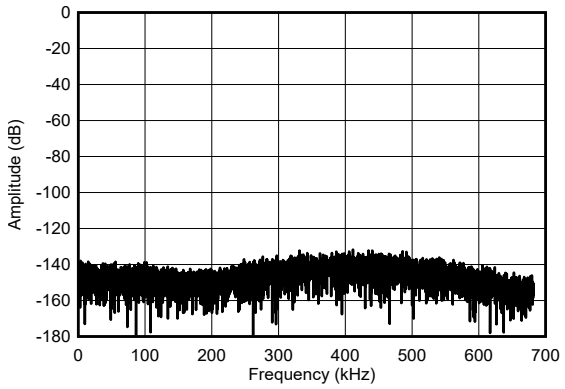
Sinc4 filter

Figure 6-21. Mid-Speed Mode, Shorted-Input FFT



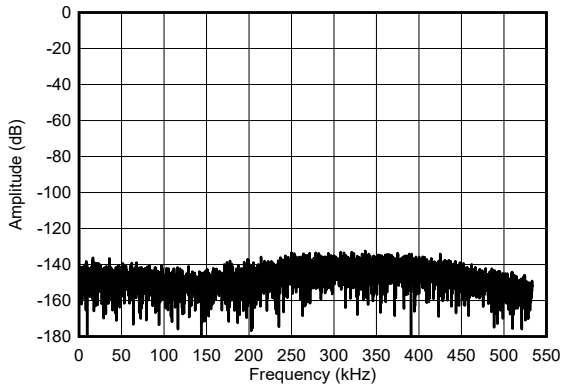
Sinc4 filter

Figure 6-22. Low-Speed Mode, Shorted-Input FFT



Sinc4 filter, OSR = 12

Figure 6-23. Maximum-Speed Mode, Shorted-Input FFT

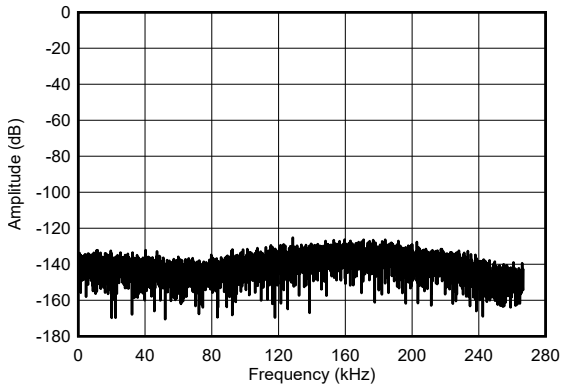


Sinc4 filter, OSR = 12

Figure 6-24. High-Speed Mode, Shorted-Input FFT

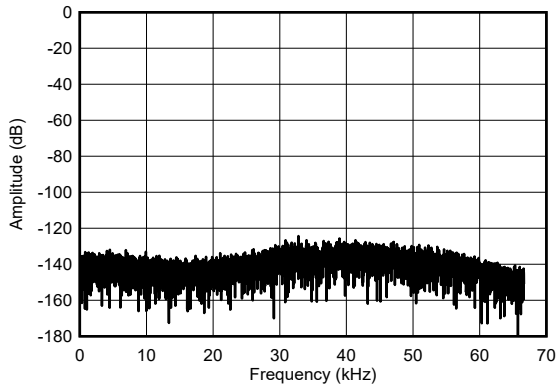
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



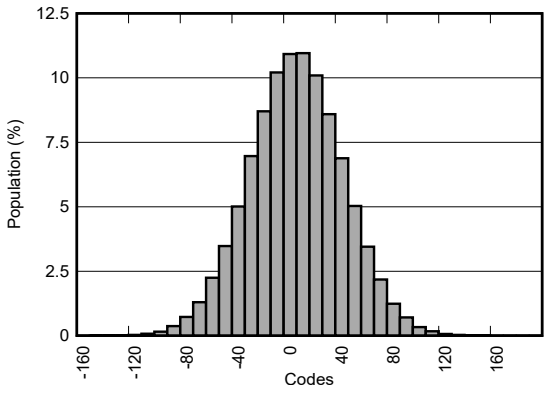
Sinc4 filter, OSR = 12

Figure 6-25. Mid-Speed Mode, Shorted-Input FFT



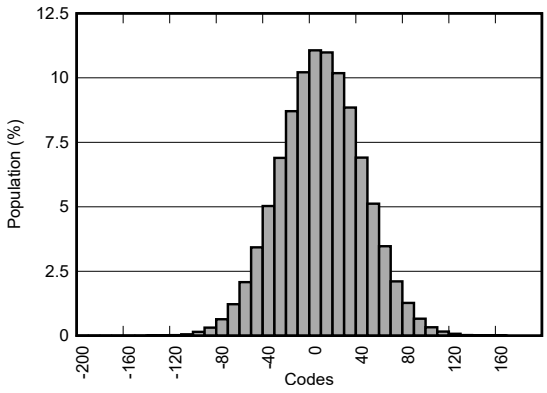
Sinc4 filter, OSR = 12

Figure 6-26. Low-Speed Mode, Shorted-Input FFT



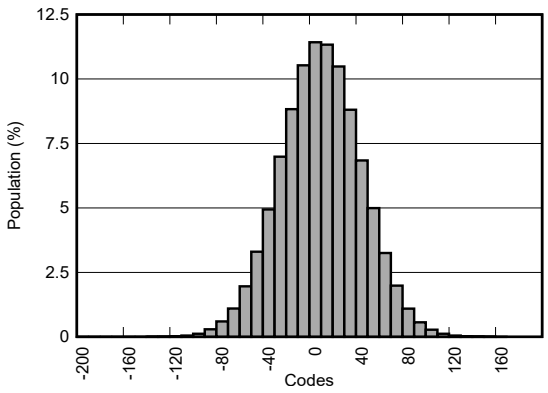
262144 samples

Figure 6-27. Maximum-Speed Mode Code Distributions



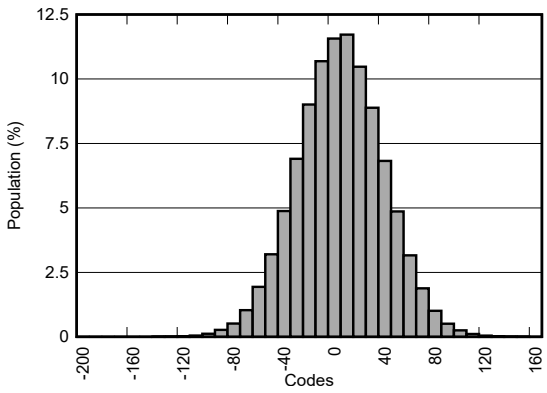
262144 samples

Figure 6-28. High-Speed Mode Code Distributions



262144 samples

Figure 6-29. Mid-Speed Mode Code Distributions

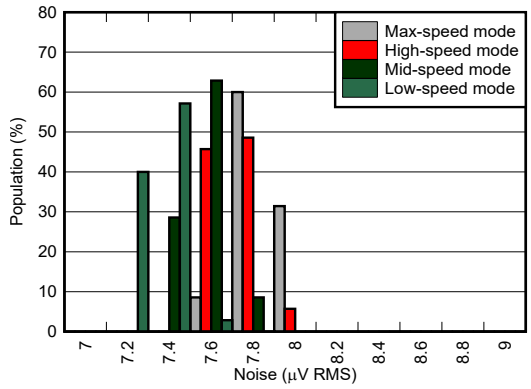


262144 samples

Figure 6-30. Low-Speed Mode Code Distributions

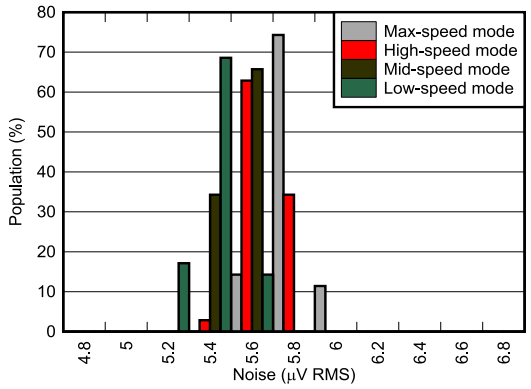
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



Wideband filter, OSR = 64, 30 units

Figure 6-31. Noise Performance Distributions



Sinc4 filter, OSR = 64, 30 units

Figure 6-32. Noise Performance Distributions

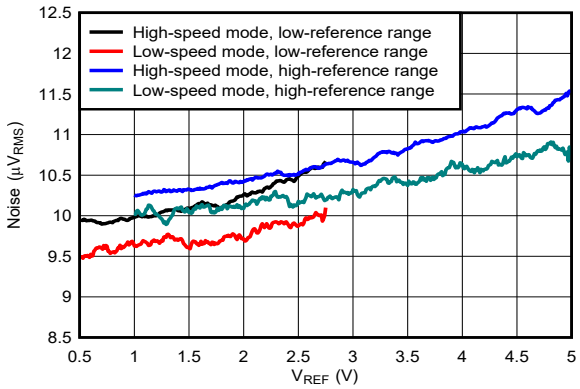
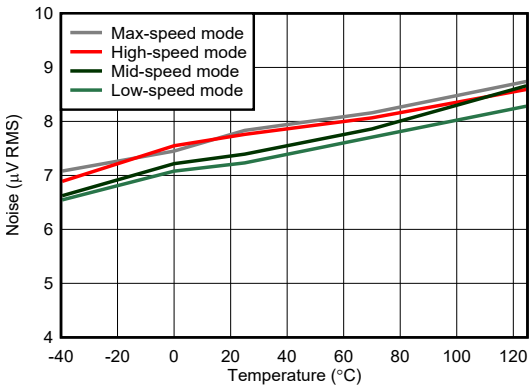
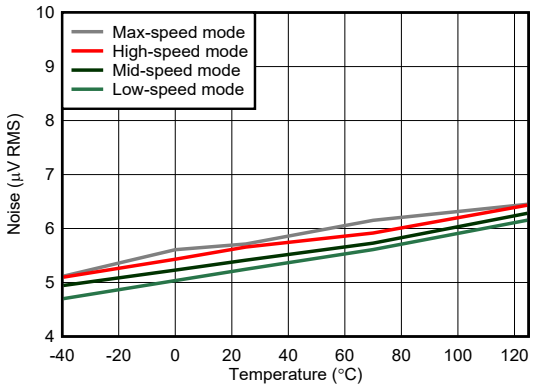


Figure 6-33. Noise Performance vs Reference Voltage



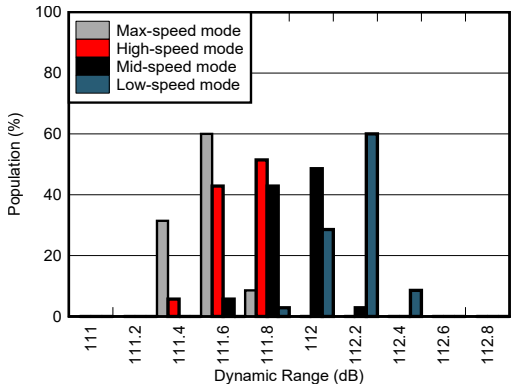
Wideband filter, OSR = 64

Figure 6-34. Noise Performance vs Temperature



Sinc4 filter, OSR = 64

Figure 6-35. Noise Performance vs Temperature

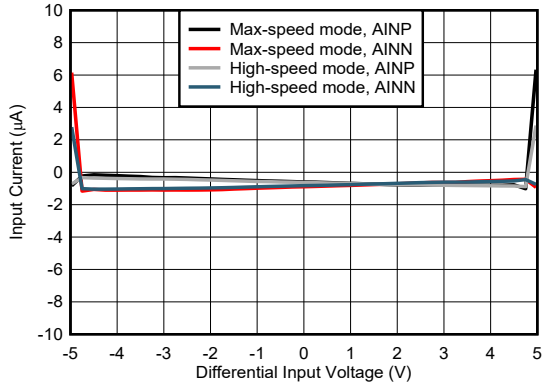


Wideband filter, OSR = 64, 30 units

Figure 6-36. Dynamic Range Distributions

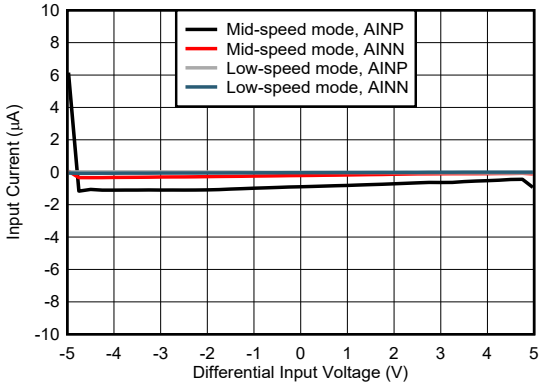
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



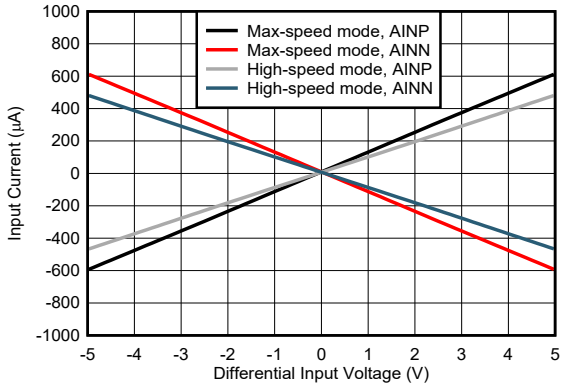
Precharge buffers on

Figure 6-37. Input Current vs Differential Voltage



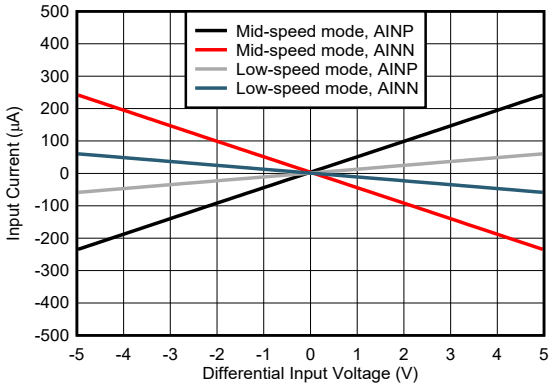
Precharge buffers on

Figure 6-38. Input Current vs Differential Voltage



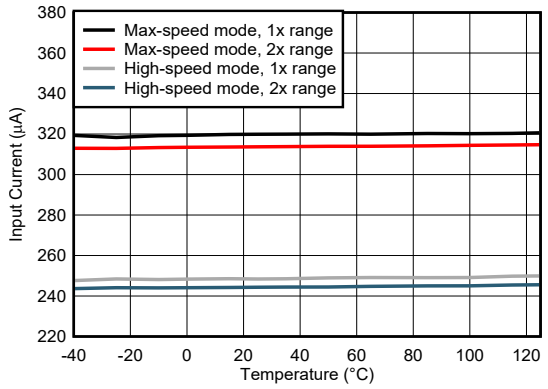
Precharge buffers off

Figure 6-39. Input Current vs Differential Voltage



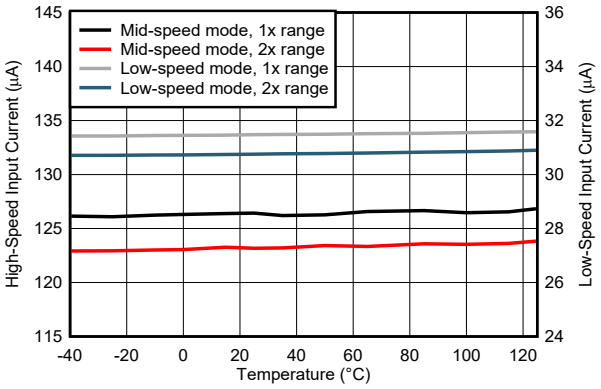
Precharge buffers off

Figure 6-40. Input Current vs Differential Voltage



Precharge buffers off, V_{IN} = full scale, V_{REF} = 2.5 V

Figure 6-41. Input Current vs Temperature

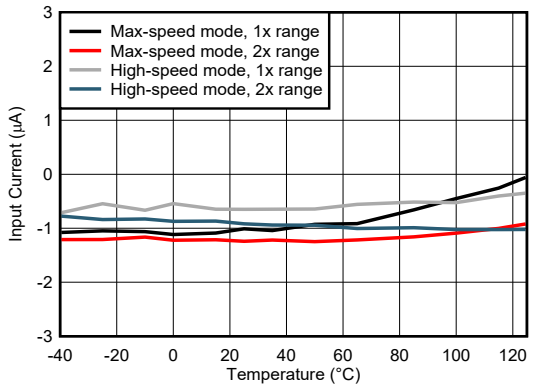


Precharge buffers off, V_{IN} = full scale, V_{REF} = 2.5 V

Figure 6-42. Input Current vs Temperature

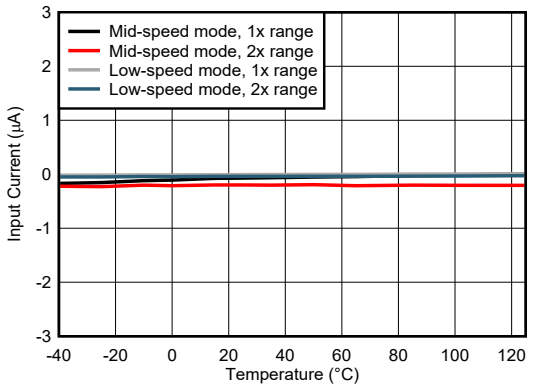
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



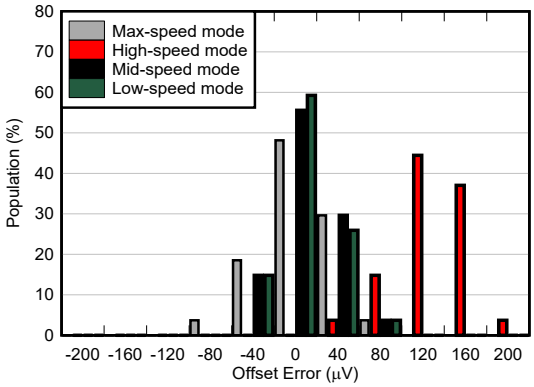
Precharge buffers on, V_{IN} = full scale, V_{REF} = 2.5 V

Figure 6-43. Input Current vs Temperature



Precharge buffers on, V_{IN} = full scale, V_{REF} = 2.5 V

Figure 6-44. Input Current vs Temperature



30 units

Figure 6-45. Offset Error Distribution

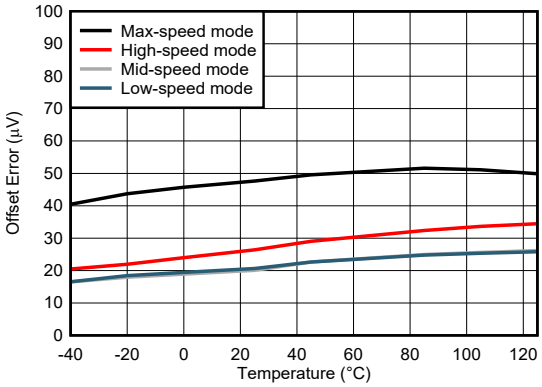
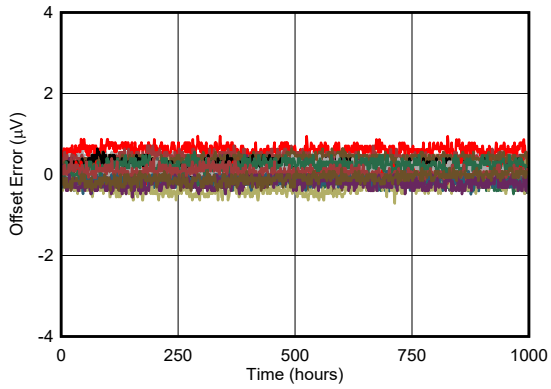
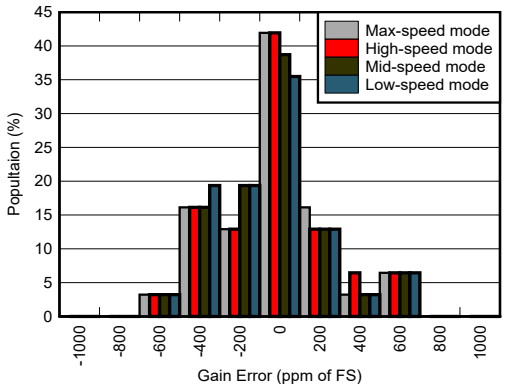


Figure 6-46. Offset Error vs Temperature



30 units, offset calibrated at t = 0

Figure 6-47. Long-Term Offset Drift

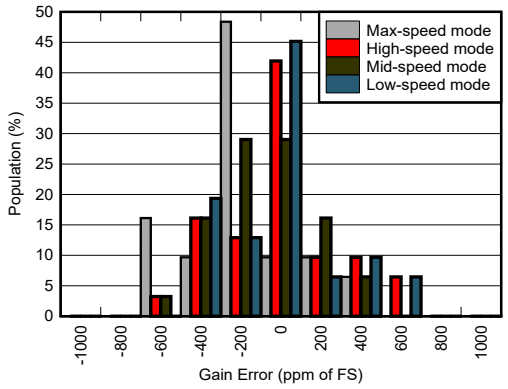


Buffers on, 30 units

Figure 6-48. Gain Error Distribution

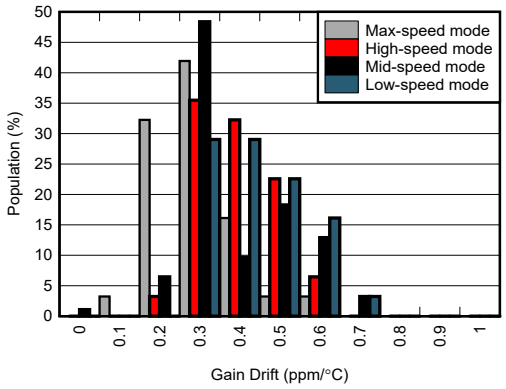
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



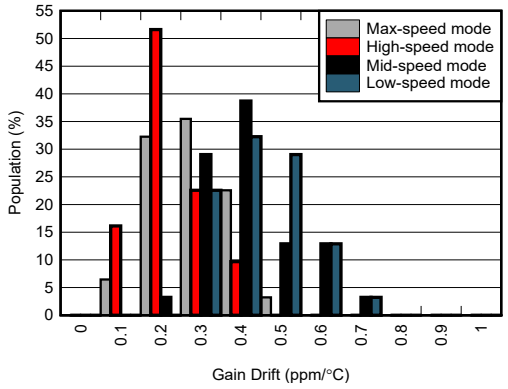
Buffers off, 30 units

Figure 6-49. Gain Error Distribution



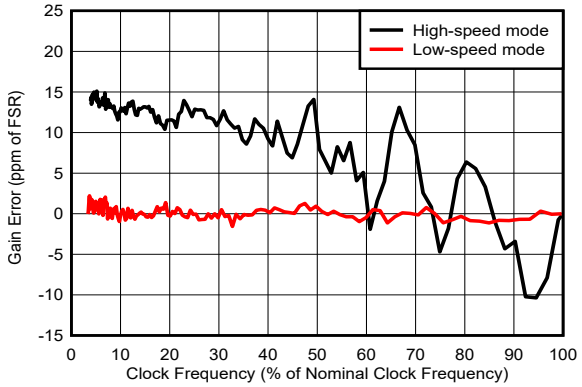
Precharge buffers on, 30 units

Figure 6-50. Gain Drift Distribution



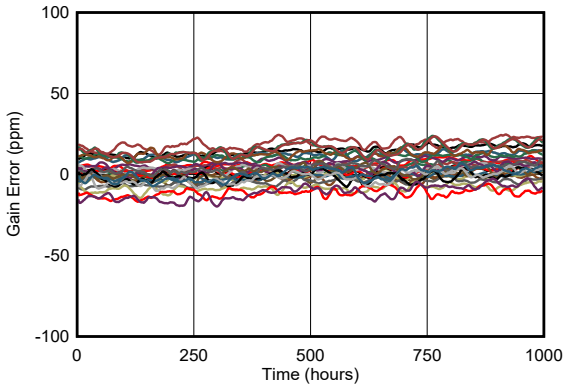
Precharge buffers off, 30 units

Figure 6-51. Gain Drift Distribution



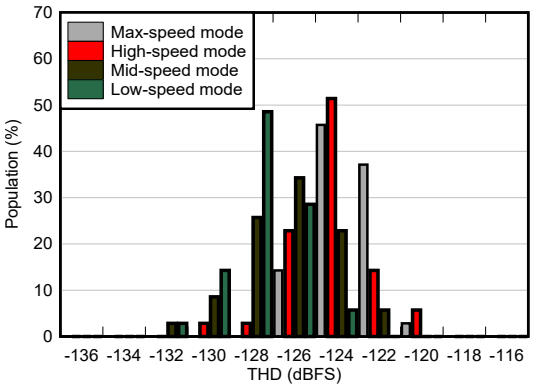
Gain error calibrated at nominal clock frequency

Figure 6-52. Gain Error vs Clock Frequency



30 units, gain calibrated at t = 0

Figure 6-53. Long-Term Gain Drift

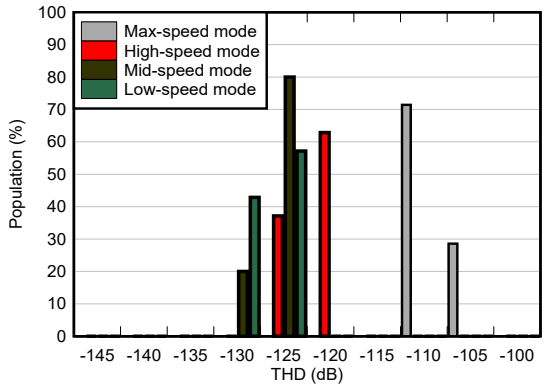


V_{REF} = 2.5 V, 30 units

Figure 6-54. THD Distribution

6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



V_{REF} = 4.096 V, 30 units

Figure 6-55. THD Distribution

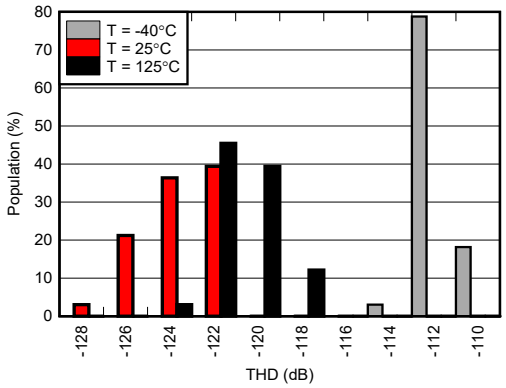


Figure 6-56. THD Over-Temperature Distributions

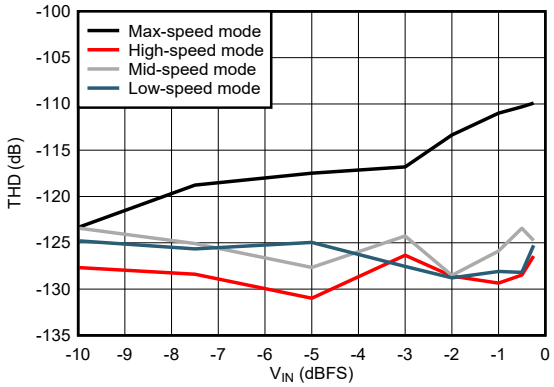
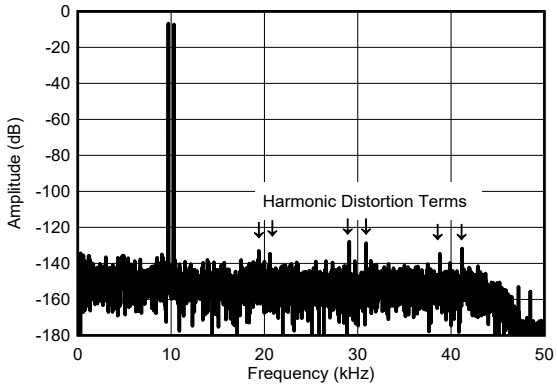


Figure 6-57. THD vs Input Amplitude



f_1 = 9.7 kHz, f_2 = 10.3 kHz, V_{IN} = -6.5 dBFS

Figure 6-58. Intermodulation Distortion FFT

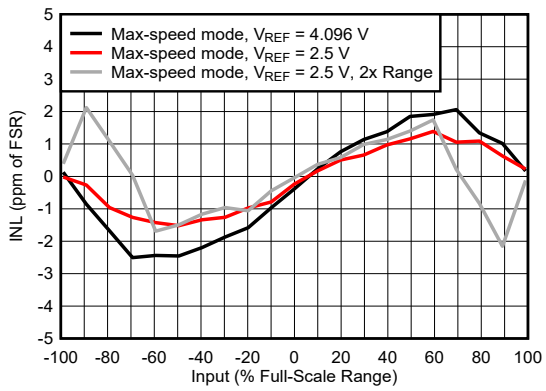


Figure 6-59. INL Error vs Input Voltage

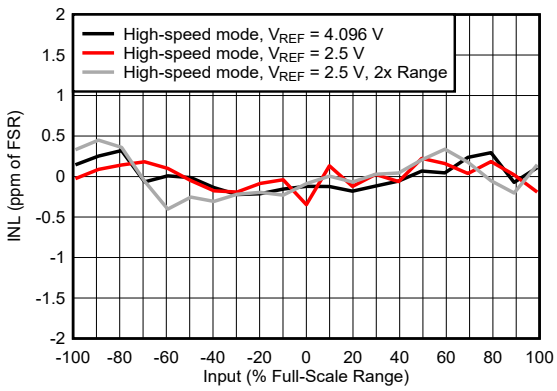


Figure 6-60. INL Error vs Input Voltage

6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)

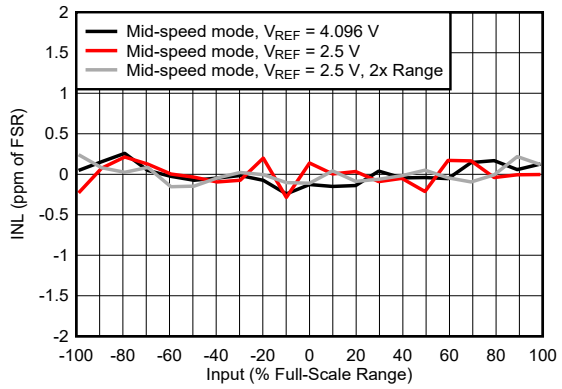


Figure 6-61. INL Error vs Input Voltage

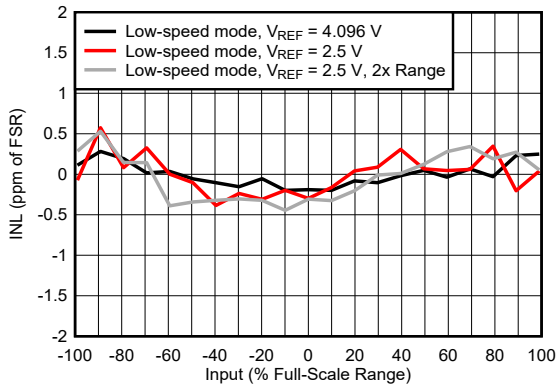


Figure 6-62. INL Error vs Input Voltage

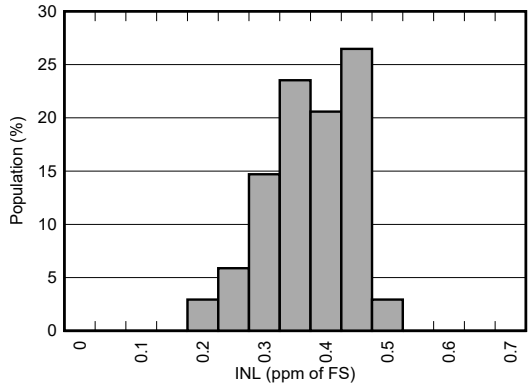


Figure 6-63. INL Distributions

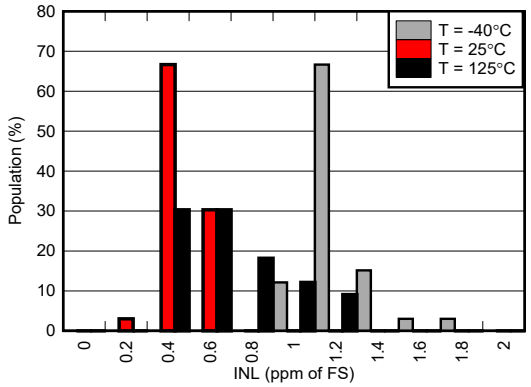


Figure 6-64. INL Over-Temperature Distributions

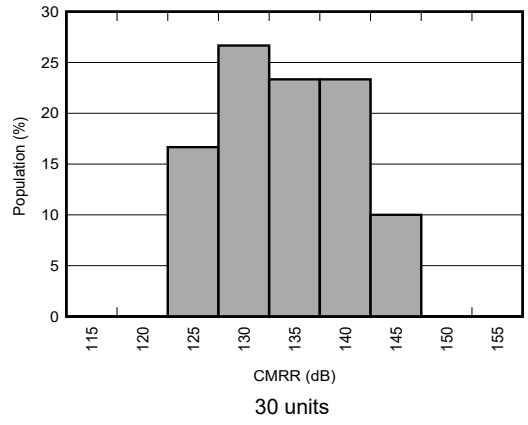


Figure 6-65. DC CMRR Distribution

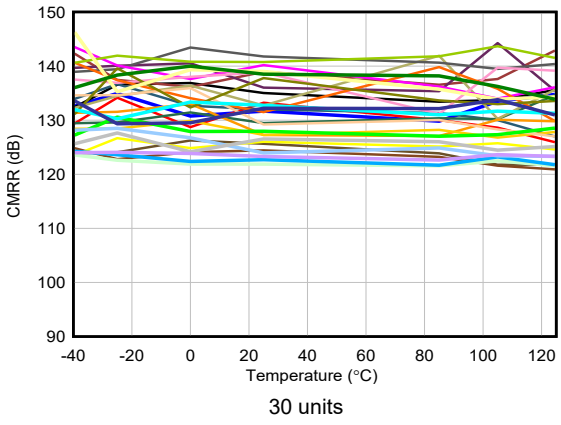
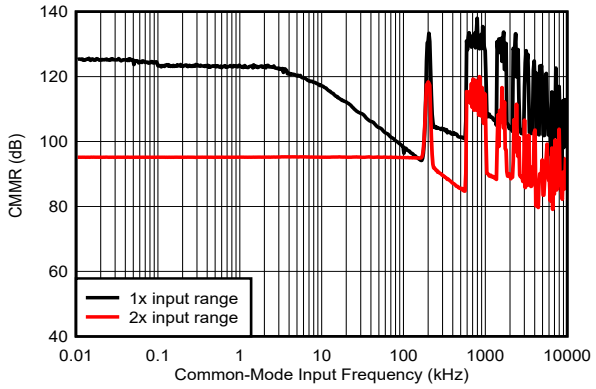


Figure 6-66. DC CMRR vs Temperature

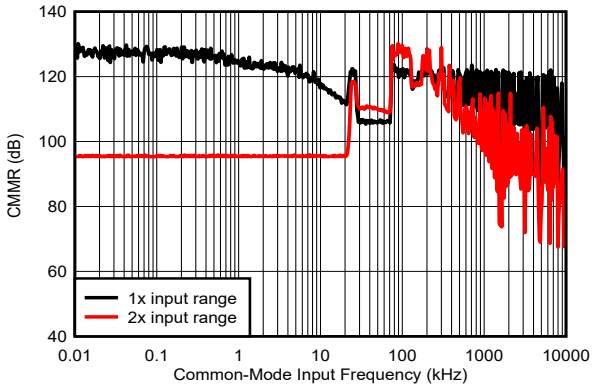
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



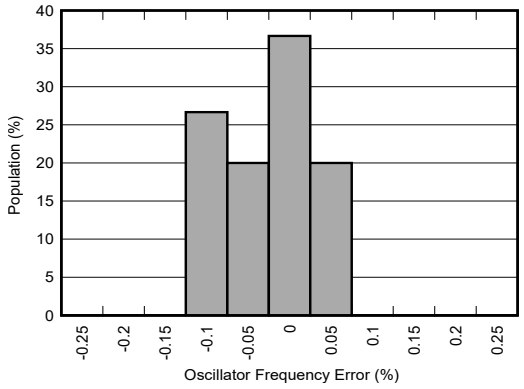
High-speed mode

Figure 6-67. CMRR vs Frequency



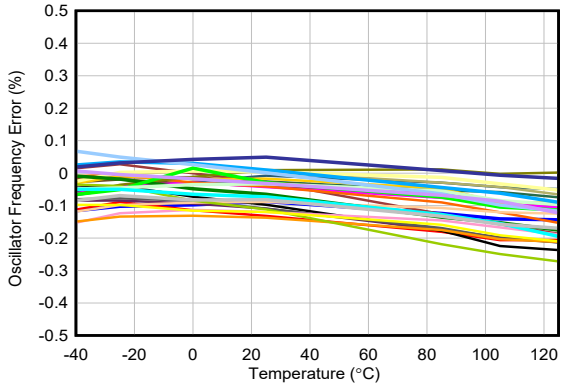
Low-speed mode

Figure 6-68. CMRR vs Frequency



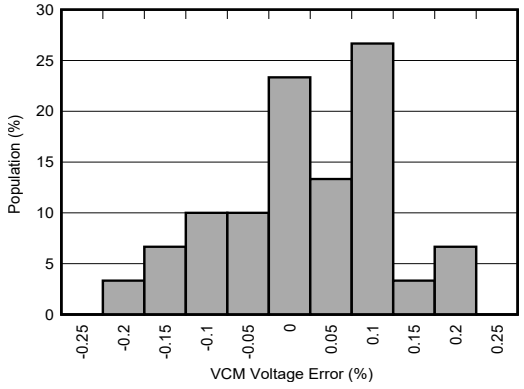
30 units

Figure 6-69. Oscillator Frequency Distribution



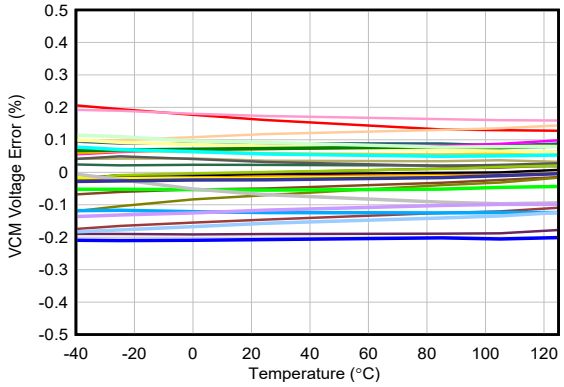
30 units

Figure 6-70. Oscillator Frequency vs Temperature



30 units

Figure 6-71. VCM Voltage Distribution

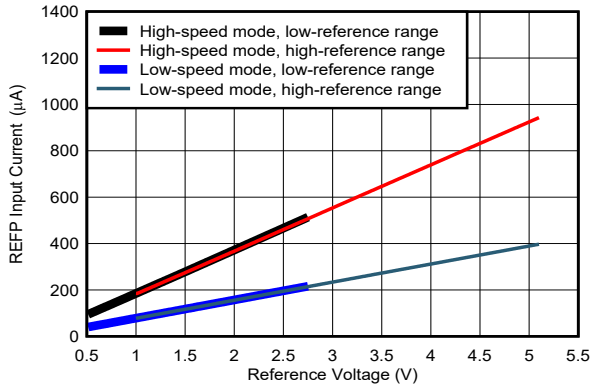


30 units

Figure 6-72. VCM Voltage vs Temperature

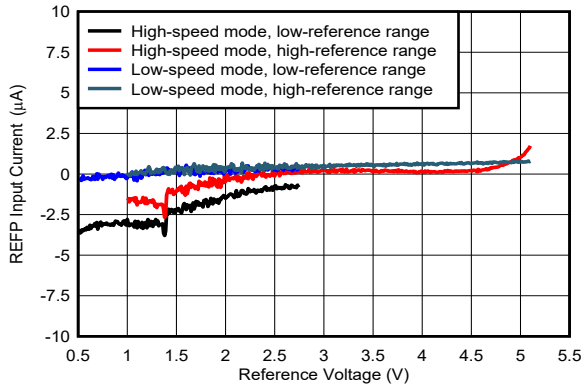
6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)



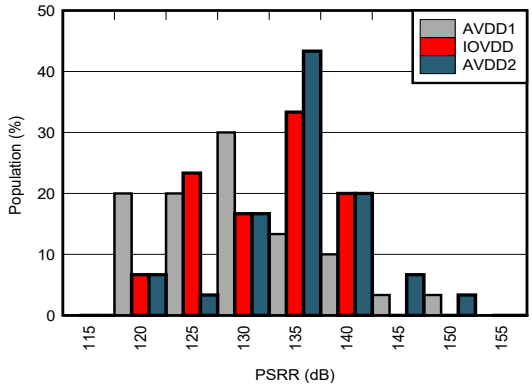
REFP precharge buffer off

Figure 6-73. REFP Input Current vs Reference Voltage



REFP precharge buffer on

Figure 6-74. REFP Input Current vs Reference Voltage



30 units

Figure 6-75. DC PSRR Distribution

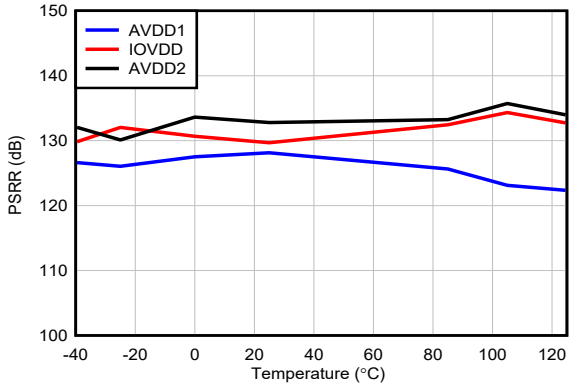


Figure 6-76. DC PSRR vs Temperature

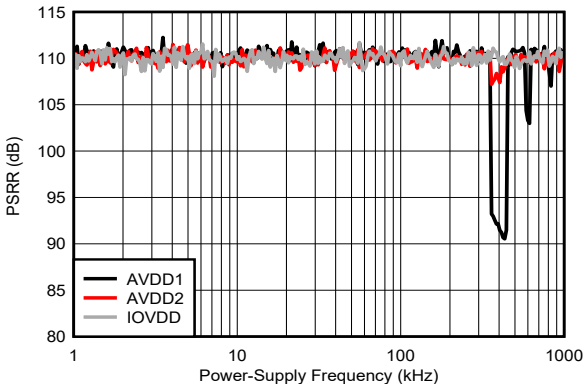
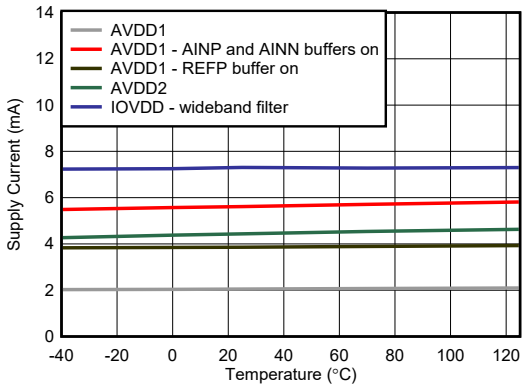


Figure 6-77. PSRR vs Power-Supply Frequency



Maximum-speed mode

Figure 6-78. Power-Supply Current vs Temperature

6.11 Typical Characteristics (continued)

AVDD1 = 5 V, AVDD2 = 1.8 V, AVSS = 0 V, IOVDD = 1.8 V, V_{REF} = 4.096 V, high-reference range, high-speed mode, wideband filter, OSR = 32, 1x input range, input precharge buffers on, reference precharge buffer off, and T_A = 25°C (unless otherwise noted)

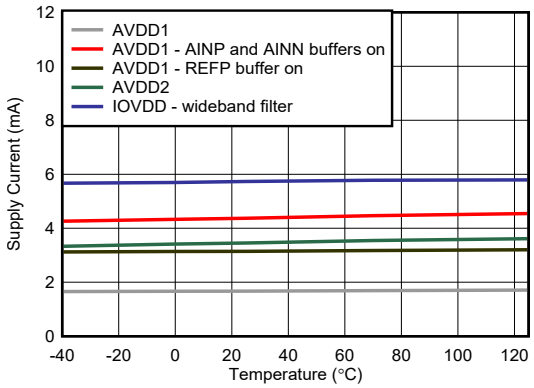


Figure 6-79. Power-Supply Current vs Temperature

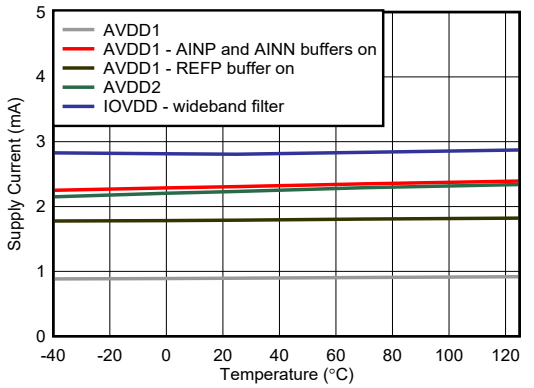


Figure 6-80. Power-Supply Current vs Temperature

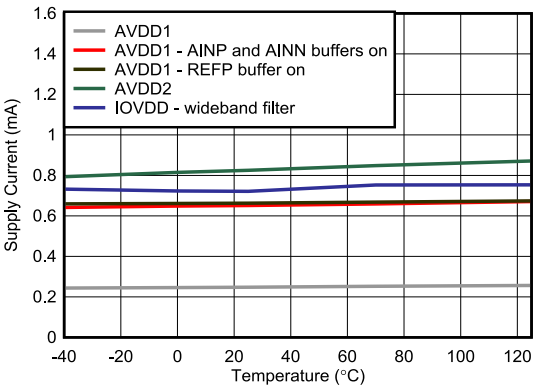


Figure 6-81. Power-Supply Current vs Temperature

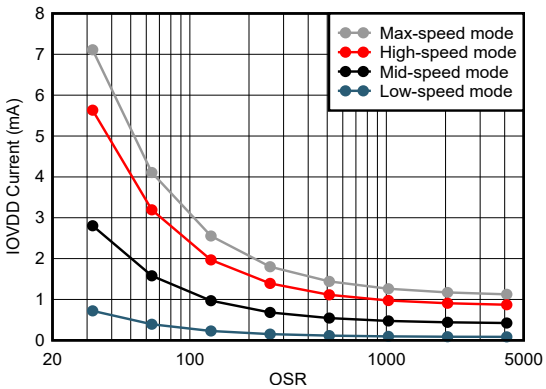


Figure 6-82. IOVDD Current vs Oversampling Ratio

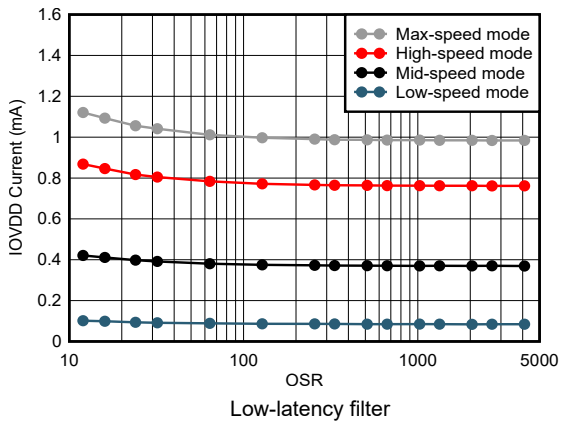


Figure 6-83. IOVDD Current vs Oversampling Ratio

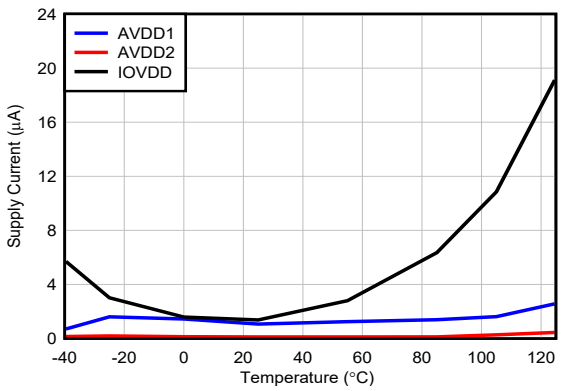


Figure 6-84. Power-Down Mode Supply Current vs Temperature

7 Parameter Measurement Information

7.1 Offset Error Measurement

Offset error is measured with the ADC inputs externally shorted together. The input common-mode voltage is fixed to the midpoint of the AVDD1 and AVSS power-supply range. Offset error is specified at T_A = 25°C.

7.2 Offset Drift Measurement

Offset drift is defined as the change in offset voltage measured at multiple points over the specified temperature range. Offset drift is calculated using the *box method*, in which a box is formed over the maximum and minimum offset voltages and over the specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test.

Equation 1 shows the offset drift calculation using the box method:

$$\text{Offset Drift (nV/°C)} = 10^9 \cdot (V_{OFSMAX} - V_{OFSMIN}) / (T_{MAX} - T_{MIN}) \quad (1)$$

where:

- V_{OFSMAX} and V_{OFSMIN} = Maximum and minimum offset voltages over the specified temperature range
- T_{MAX} and T_{MIN} = Maximum and minimum temperatures

7.3 Gain Error Measurement

Gain error is defined as the difference between the actual and the ideal slopes of the ADC transfer function. Gain error is measured by applying dc test voltages at –95% and 95% of FSR. The error is calculated by subtracting the difference of the dc test voltages (ideal slope) from the difference in the ADC output voltages (actual slope). The difference in the slopes is divided by the ideal slope and multiplied by 10^6 to convert the error to ppm of FSR. Error resulting from the ADC reference voltage is excluded from the gain error measurement. The gain error is specified at T_A = 25°C. Equation 2 shows the calculation of gain error:

$$\text{Gain Error (ppm of FSR)} = 10^6 \cdot (\Delta V_{OUT} - \Delta V_{IN}) / \Delta V_{IN} \quad (2)$$

where:

- ΔV_{OUT} = Difference of two ADC output voltages
- ΔV_{IN} = Difference of two input test voltages

7.4 Gain Drift Measurement

Gain drift is defined as the change of gain error measured at multiple points over the specified temperature range. The box method is used in which a box is formed over the maximum and minimum gain errors over the specified temperature range. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Equation 3 describes gain drift using the box method.

$$\text{Gain Drift (ppm/°C)} = (GE_{MAX} - GE_{MIN}) / (T_{MAX} - T_{MIN}) \quad (3)$$

where:

- GE_{MAX} and GE_{MIN} = Maximum and minimum gain errors over the specified temperature range
- T_{MAX} and T_{MIN} = Maximum and minimum temperatures

7.5 NMRR Measurement

Normal-mode rejection ratio (NMRR) specifies the ability of the ADC to reject normal-mode input signals at specific frequencies, usually expressed at 50-Hz and 60-Hz input frequencies. Normal-mode rejection is uniquely determined by the frequency response of the digital filter. In this case, the nulls in the frequency response of the low-latency sinc3 and sinc4 filters located at 50 Hz and 60 Hz provide rejection at these frequencies.

7.6 CMRR Measurement

Common-mode rejection ratio (CMRR) specifies the ability of the ADC to reject common-mode input signals. CMRR is expressed as dc and ac parameters. For measurement of CMRR (dc), three common-mode test voltages equal to AVSS + 50 mV, (AVDD1 + AVSS) / 2, and AVDD1 – 50 mV are applied with the inputs externally shorted together. The maximum change of the ADC offset voltage is recorded versus the change in common-mode test voltage. Equation 4 shows how CMRR (dc) is computed.

$$\text{CMRR (dc) (dB)} = 20 \cdot \log(\Delta V_{CM} / \Delta V_{OS}) \quad (4)$$

where:

- ΔV_{CM} = Change of dc common-mode test voltage
- ΔV_{OS} = Change of corresponding offset voltage

For the measurement of CMRR (ac), an ac common-mode signal is applied at various test frequencies at 95% full-scale range. A fast Fourier transform (FFT) plot is computed from the ADC data with the common-mode signal applied. As shown in Equation 5, the nine largest amplitude spurious frequencies in the frequency spectrum are summed as powers and related to the amplitude of the common-mode test signal.

$$\text{PSRR (ac) (dB)} = 20 \cdot \log(V_{CM} / V_O) \quad (5)$$

where:

- V_{CM} (RMS) = Common-mode input signal amplitude
- V_O (RMS) = Root-sum-square amplitude of spurious frequencies = $\sqrt{(V_0{}^2 + V_1{}^2 + ...V_8{}^2)}$

7.7 PSRR Measurement

Power-supply rejection ratio (PSRR) specifies the ability of the ADC to reject power-supply interference. PSRR is expressed as ac and dc parameters. For measurement of PSRR (dc), the power-supply voltage is changed over the range of minimum, nominal, and maximum specified voltages with the inputs externally shorted together. The maximum change of ADC offset voltage is recorded versus the change in power-supply voltage. PSRR (dc) is computed as shown in Equation 6 as the ratio of change of the power-supply voltage step to the change of offset voltage.

$$\text{PSRR (dc) (dB)} = 20 \cdot \log(\Delta V_{PS} / \Delta V_{OS}) \quad (6)$$

where:

- ΔV_{PS} = Change of power-supply voltage
- ΔV_{OS} = Change of offset voltage

For the measurement of PSRR (ac), the power-supply voltage is modulated by a 100-mV_{PP} (35-mV_{RMS}) signal at various test frequencies. An FFT of the ADC data with power-supply modulation is performed. As shown in Equation 7, the nine largest amplitude spurious frequencies in the frequency spectrum are summed as powers and related to the amplitude of the power-supply modulation signal.

$$\text{PSRR (ac) (dB)} = 20 \cdot \log(V_{PS} / V_O) \quad (7)$$

where:

- V_{PS} (RMS) = 100-mV ac power-supply modulation signal
- V_O (RMS) = Root-sum-square amplitude of spurious frequencies = $\sqrt{(V_0{}^2 + V_1{}^2 + ...V_8{}^2)}$

7.8 SNR Measurement

Signal-to-noise ratio (SNR) is a measure of noise performance with a full-scale ac input signal. For the SNR measurement, a –0.2-dBFS, 1-kHz test signal is used with V_{CM} equal to the mid-supply voltage. As shown in Equation 8, SNR is the ratio of the rms value of the input signal to the root-sum-square of all other frequency components derived from the FFT result of the ADC output samples. DC and harmonics of the original signal are excluded from the SNR calculation. In a test case where an FFT window function is used because of non-coherent sampling, the spectral leakage of adjacent frequency bins surrounding dc, the original signal and signal harmonics are removed to calculate SNR.

$$\text{SNR (dB)} = 20 \cdot \log(V_{IN} / e_n) \quad (8)$$

where:

- V_{IN} = Input test signal
- e_n = Root-sum-square of frequency components excluding dc and signal harmonics

7.9 INL Error Measurement

Integral nonlinearity (INL) error specifies the linearity of the ADC dc transfer function. INL is measured by applying a series of dc test voltages along a straight line computed from the slope and offset transfer function of the ADC. INL is the difference between a set of dc test voltages [$V_{IN(N)}$] to the corresponding set of output voltages [$V_{OUT(N)}$]. Equation 9 shows the *end-point method* of calculating INL error.

$$\text{INL (ppm of FSR)} = \text{maximum absolute value of INL test series } [10^6 \cdot (V_{IN(N)} - V_{OUT(N)}) / \text{FSR}] \quad (9)$$

where:

- N = Index of dc test voltage
- [$V_{IN(N)}$] = Set of test voltages over the range –95% to 95% of FSR
- [$V_{OUT(N)}$] = Set of corresponding ADC output voltages
- FSR (full-scale range) = 2 · V_{REF} (1x input range) or 4 · V_{REF} (2x input range)

The INL *best-fit method* uses a least-squared error (LSE) calculation to determine a new straight line to minimize the root-sum-square of the INL errors above and below the original end-point line.

7.10 THD Measurement

Total harmonic distortion (THD) specifies the dynamic linearity of the ADC with an ac input signal. For the THD measurement, a –0.2-dBFS, 1-kHz differential input signal with V_{CM} equal to the mid-supply voltage is applied. A sufficient number of data points are collected to yield an FFT result with frequency bin widths of 5 Hz or less. The 5-Hz bin width reduces the noise in the harmonic bins for consistent THD measurements. As shown in Equation 10, THD is calculated as the ratio of the root-sum-square amplitude of harmonics to the input signal amplitude.

$$\text{THD (dB)} = 20 \cdot \log(V_H / V_{IN}) \quad (10)$$

where:

- V_H = Root-sum-square of harmonics: $\sqrt{(V_2{}^2 + V_3{}^2 + \ldots V_n{}^2)}$, where V_n = Ninth harmonic voltage
- V_{IN} = Input signal fundamental

7.11 IMD Measurement

Intermodulation distortion (IMD) specifies the mixing effect of two input frequencies. Frequency mixing is caused by ADC nonlinearity resulting in sum and difference frequencies not within the original signal. The IMD second-order terms are ($f_1 + f_2$) and ($f_1 – f_2$), and the IMD third-order terms are ($2f_1 + f_2$), ($2f_1 – f_2$), ($f_1 + 2f_2$), and ($f_1 – 2f_2$). Test signals f_1 = 9.7 kHz and f_2 = 10.3 kHz are at –6.5 dBFS. As shown in Equation 11, IMD_2 and IMD_3 are specified as the ratio of the root-sum-square second-order and third-order terms to the sum of the original test frequencies.

$$IMD_2\,(dB) = 20 \cdot \log(V_2 / V_{IN})$$
$$IMD_3\,(dB) = 20 \cdot \log(V_3 / V_{IN}) \quad (11)$$

where:

- IMD_2 = Second-order IMD
- IMD_3 = Third-order IMD
- V_2 = Root-sum-square of second-order terms
- V_3 = Root-sum-square of third-order terms
- V_{IN} = Sum amplitude of two test signals

7.12 SFDR Measurement

Spurious-free dynamic range (SFDR) is the ratio of the rms value of a single-tone ac input to the highest spurious signal in the ADC frequency spectrum. SFDR measurement includes harmonics of the original signal. For the SFDR measurement, a –0.2-dBFS, 1-kHz input signal with V_{CM} equal to the mid-supply voltage is applied. As shown in Equation 12, SFDR is the ratio of the rms values of the input signal to the single highest spurious signal, including harmonics of the original signal.

$$SFDR\,(dB) = 20 \cdot \log(V_{IN} / V_{SPUR}) \quad (12)$$

where:

- V_{IN} = Input test signal
- V_{SPUR} = Single highest spurious level

7.13 Noise Performance

The ADC provides four operational speed modes that allow trade-offs between ADC resolution, power consumption, and signal bandwidth. The modes are max speed, high speed, mid speed, and low speed, with decreasing orders of device power consumption. The wideband filter offers data rates up to 512 kSPS in max-speed mode, up to 400 kSPS in high-speed mode, up to 200 kSPS in mid-speed mode, and up to 50 kSPS in low-speed mode. Data are also accessible from the partial filters of the intermediate FIR1 or FIR2 stages for reduced filter time latency.

The low-latency sinc4 filter offers data rates up to 1.365 MSPS in max-speed mode, up to 1.066 MSPS in high-speed mode, up to 533 kSPS in mid-speed mode, and up to 133 kSPS in low-speed mode.

The programmable oversampling ratio (OSR) determines the output data rate and signal bandwidth, therefore affecting total noise performance. Increasing the OSR lowers the signal bandwidth and total noise by averaging more samples from the modulator to yield one conversion result.

Table 7-1 through Table 7-5 summarize the noise performance of the filters. Noise performance is specified for the 1x input range and a 4.096-V reference voltage. In comparison, decreasing the reference voltage to 2.5 V decreases dynamic range by 4 dB (typical). Operation in 2x input range and a 2.5-V reference voltage decreases dynamic range by 3 dB (typical) compared to 1x input range and 4.096-V reference voltage operation.

The noise data are the result of the standard deviation (rms) of the conversion data with inputs shorted and biased to the mid-supply voltage and are representative of typical performance at T_A = 25°C. A minimum of 1,000 or 10 seconds of consecutive conversions (whichever occurs first) are used to measure RMS noise (e_n). Because of the statistical nature of noise, repeated noise measurements can yield higher or lower noise results.

Equation 13 converts RMS noise to dynamic range. Equation 14 converts RMS noise to effective resolution.

$$\text{Dynamic Range (dB)} = 20 \cdot \log_{10}[\text{FSR} / (2 \cdot \sqrt{2} \cdot e_n)] \quad (13)$$

$$\text{Effective Resolution (bits)} = \log_2(\text{FSR} / e_n) \quad (14)$$

where:

- FSR = 2 · V_{REF} (1x input range)
- FSR = 4 · V_{REF} (2x input range)
- e_n = Noise voltage (RMS)

When evaluating ADC noise performance, consider the effect of the external buffer and amplifier noise to the total noise performance. The noise performance of the ADC is evaluated in isolation of the amplifiers by selecting the input short test connection of the input multiplexer.

Table 7-1. Wideband Filter Noise Performance (V_{REF} = 4.096 V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
Max speed	32.768	32	512	11.1	108.3	19.5
High speed	25.6		400	10.9	108.5	19.5
Mid speed	12.8		200	10.6	108.7	19.6
Low speed	3.2		50	10.4	108.9	19.6
Max speed	32.768	64	256	7.64	111.6	20.0
High speed	25.6		200	7.50	111.7	20.1
Mid speed	12.8		100	7.30	112.0	20.1
Low speed	3.2		25	7.14	112.2	20.1
Max speed	32.768	128	128	5.34	114.7	20.5
High speed	25.6		100	5.25	114.8	20.6
Mid speed	12.8		50	5.07	115.1	20.6
Low speed	3.2		12.5	4.97	115.3	20.7

Table 7-1. Wideband Filter Noise Performance (V_{REF} = 4.096 V, 1x Input Range) (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
Max speed	32.768	256	64	3.79	117.7	21.0
High speed	25.6		50	3.72	117.8	21.1
Mid speed	12.8		25	3.58	118.2	21.1
Low speed	3.2		6.25	3.53	118.3	21.1
Max speed	32.768	512	32	2.71	120.6	21.5
High speed	25.6		25	2.67	120.7	21.5
Mid speed	12.8		12.5	2.54	121.2	21.6
Low speed	3.2		3.125	2.47	121.4	21.7
Max speed	32.768	1024	16	1.88	123.8	22.1
High speed	25.6		12.5	1.87	123.8	22.1
Mid speed	12.8		6.25	1.82	124.0	22.1
Low speed	3.2		1.5625	1.76	124.3	22.2
Max speed	32.768	2048	8	1.34	126.7	22.5
High speed	25.6		6.25	1.32	126.8	22.5
Mid speed	12.8		3.125	1.29	127.0	22.6
Low speed	3.2		0.78125	1.25	127.3	22.6
Max speed	32.768	4096	4	0.96	129.6	23.0
High speed	25.6		3.125	0.95	129.7	23.0
Mid speed	12.8		1.5625	0.93	129.9	23.1
Low speed	3.2		0.390625	0.89	130.3	23.1

Table 7-2. Sinc3 and Sinc4 Filter Noise Performance (V_{REF} = 4.096 V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})[1]		DYNAMIC RANGE (dB)		EFFECTIVE RESOLUTION (Bits)	
				SINC3	SINC4	SINC3	SINC4	SINC3	SINC4
Max speed	32.768	12	1365.3	239	66.8	81.7	92.7	15.1	16.9
High speed	25.6		1066.6	235	66.6	81.8	92.8	15.1	16.9
Mid speed	12.8		533.3	235	63.8	81.8	93.1	15.1	17.0
Low speed	3.2		133.33	232	63.1	81.9	93.2	15.1	17.0
Max speed	32.768	16	1024	99.9	24.8	89.2	101.3	16.3	18.3
High speed	25.6		800	99.6	24.5	89.3	101.5	16.3	18.4
Mid speed	12.8		400	98.9	24.5	89.3	101.5	16.3	18.4
Low speed	3.2		100	96.0	24.3	89.6	101.5	16.4	18.4
Max speed	32.768	24	682.67	31.1	10.8	99.4	108.6	18.0	19.5
High speed	25.6		533.3	31.0	10.3	99.4	108.9	18.0	19.6
Mid speed	12.8		266.67	30.8	10.1	99.5	109.2	18.0	19.6
Low speed	3.2		66.67	30.7	9.96	99.5	109.3	18.0	19.6
Max speed	32.768	32	512	15.2	8.24	105.6	110.9	19.0	19.9
High speed	25.6		400	15.0	8.07	105.7	111.1	19.1	20.0
Mid speed	12.8		200	14.8	7.88	105.8	111.3	19.1	20.0
Low speed	3.2		50	14.7	7.76	105.9	111.4	19.1	20.0
Max speed	32.768	64	256	6.20	5.71	113.4	114.1	20.3	20.5
High speed	25.6		200	6.15	5.53	113.5	114.4	20.3	20.5
Mid speed	12.8		100	5.98	5.42	113.7	114.6	20.4	20.5
Low speed	3.2		25	5.78	5.24	114.0	114.9	20.4	20.6

Table 7-2. Sinc3 and Sinc4 Filter Noise Performance (V_{REF} = 4.096 V, 1x Input Range) (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})(1)		DYNAMIC RANGE (dB)		EFFECTIVE RESOLUTION (Bits)	
				SINC3	SINC4	SINC3	SINC4	SINC3	SINC4
Max speed	32.768	128	128	4.21	3.98	116.8	117.2	20.9	21.0
High speed	25.6		100	4.16	3.89	116.9	117.4	20.9	21.0
Mid speed	12.8		50	4.10	3.75	117.0	117.8	20.9	21.1
Low speed	3.2		12.5	3.99	3.72	117.2	117.8	21.0	21.1
Mid speed	12.8	167	38.323	3.56	3.39	118.2	118.6	21.1	21.2
Max speed	32.768	256	64	2.99	2.78	119.7	120.4	21.4	21.5
High speed	25.6		50	2.95	2.74	119.8	120.5	21.4	21.5
Mid speed	12.8		25	2.87	2.69	120.1	120.6	21.4	21.5
Low speed	3.2		6.25	2.81	2.61	120.3	120.9	21.5	21.6
Max speed	32.768	333	49.201	2.67	2.50	120.7	121.3	21.5	21.6
High speed	25.6		38.438	2.59	2.46	121.0	121.4	21.6	21.7
Mid speed	12.8		19.219	2.53	2.43	121.2	121.5	21.6	21.7
Low speed	3.2		4.804	2.46	2.33	121.4	121.9	21.7	21.7
Max speed	32.768	512	32	2.11	1.98	122.8	123.3	21.9	22.0
High speed	25.6		25	2.09	1.93	122.8	123.5	21.9	22.0
Mid speed	12.8		12.5	2.01	1.88	123.2	123.8	22.0	22.1
Low speed	3.2		3.125	1.96	1.67	123.4	124.8	22.0	22.2
Max speed	32.768	667	24.564	1.90	1.77	123.7	124.3	22.0	22.1
High speed	25.6		19.19	1.86	1.75	123.8	124.4	22.1	22.2
Mid speed	12.8		9.595	1.82	1.67	124.0	124.8	22.1	22.2
Low speed	3.2		2.39	1.77	1.65	124.3	124.9	22.1	22.2
Max speed	32.768	1024	16	1.50	1.41	125.7	126.3	22.4	22.5
High speed	25.6		12.5	1.47	1.40	125.9	126.3	22.4	22.5
Mid speed	12.8		6.25	1.43	1.34	126.1	126.7	22.4	22.5
Low speed	3.2		1.56	1.42	1.31	126.2	126.9	22.5	22.6
Max speed	32.768	1333	12.291	1.36	1.25	126.6	127.3	22.5	22.6
High speed	25.6		9.602	1.34	1.23	126.7	127.4	22.5	22.7
Mid speed	12.8		4.801	1.29	1.19	127.0	127.7	22.6	22.7
Low speed	3.2		1.2	1.24	1.17	127.4	127.9	22.7	22.7
Max speed	32.768	2048	8	1.06	1.00	128.7	129.2	22.9	23.0
High speed	25.6		6.25	1.05	0.995	128.8	129.3	22.9	23.0
Mid speed	12.8		3.125	1.02	0.952	129.1	129.7	22.9	23.0
Low speed	3.2		0.78	0.969	0.935	129.5	129.8	23.0	23.1
Max speed	32.768	2667	6.143	0.967	0.890	129.5	130.3	23.0	23.1
High speed	25.6		4.799	0.949	0.858	129.7	130.6	23.0	23.2
Mid speed	12.8		2.4	0.913	0.867	130.0	130.5	23.1	23.2
Low speed	3.2		0.6	0.914	0.844	130.0	130.7	23.1	23.2
Max speed	32.768	4096	4	0.751	0.710	131.7	132.2	23.4	23.5
High speed	25.6		3.125	0.752	0.709	131.7	132.2	23.4	23.5
Mid speed	12.8		1.563	0.725	0.681	132.0	132.6	23.4	23.5
Low speed	3.2		0.39	0.709	0.649	132.2	133.0	23.5	23.6
Max speed	32.768	5333	3.072	0.697	0.630	132.4	133.3	23.5	23.6
High speed	25.6		2.4	0.676	0.626	132.6	133.3	23.5	23.6
Low speed	3.2		0.3	0.661	0.604	132.8	133.6	23.6	23.7

Table 7-2. Sinc3 and Sinc4 Filter Noise Performance (V_{REF} = 4.096 V, 1x Input Range) (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})(1)		DYNAMIC RANGE (dB)		EFFECTIVE RESOLUTION (Bits)	
				SINC3	SINC4	SINC3	SINC4	SINC3	SINC4
Mid speed	12.8	13333	0.437	0.410	0.60	136.3	137.0	24.2	24.3
Mid speed	12.8	16000	0.400	0.392	0.356	137.4	138.2	24.3	24.5
Max speed	32.768	26667	0.614	0.335	0.320	138.7	139.4	24.5	24.6
High speed	25.6		0.480	0.330	0.311	138.9	139.1	24.6	24.7
Low speed	3.2		0.06	0.316	0.290	139.2	140.0	24.7	24.8
Max speed	32.768	32000	0.512	0.309	0.303	139.4	139.6	24.7	24.7
High speed	25.6		0.4	0.306	0.294	139.5	139.9	24.7	24.7
Low speed	3.2		0.05	0.290	0.275	140.0	140.5	24.8	24.8
Mid speed	12.8	48000	0.133	0.251	0.274	141.2	140.5	25.0	24.8
Mid speed	12.8	80000	0.08	0.233	0.208	141.9	142.9	25.1	25.2
Max speed	32.768	96000	0.17067	0.238	0.202	141.7	143.1	25.0	25.3
High speed	25.6		0.133	0.186	0.250	143.8	141.3	25.4	25.0
Low speed	3.2		0.0167	0.245	0.207	141.5	142.9	25.0	25.2
Max speed	32.768	160000	0.102	0.243	0.243	141.5	141.5	25.0	25.0
High speed	25.6		0.08	0.232	0.242	141.9	141.6	25.1	25.0
Low speed	3.2		0.01	0.243	0.177	141.5	144.3	25.0	25.5

(1) High OSR values can yield varying noise results because of the limits of 24-bit quantization: 4.096 V / 2^{23} = 0.488 µV / code.

Table 7-3. Sinc3 + Sinc1 and Sinc4 + Sinc1 Filter Noise Performance (V_{REF} = 4.096 V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (SPS)	NOISE (e_n, μV_{RMS})(1)	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
Mid speed	12.8	13333	480	0.573	134.1	23.8
Mid speed	12.8	16000	400	0.533	134.7	23.9
Max speed	32.768	26656	614	0.419	136.8	24.2
High speed	25.6		480	0.416	136.9	24.2
Low speed	3.2		60	0.413	136.9	24.2
Max speed	32.768	32000	512	0.409	137.0	24.3
High speed	25.6		400	0.387	137.5	24.3
Low speed	3.2		50	0.362	138.1	24.4
Mid speed	12.8	48000	133	0.321	139.1	24.6
Mid speed	12.8	80000	80	0.274	140.5	24.8
Max speed	32.768	96000	170.6	0.254	141.1	24.9
High speed	25.6		133	0.256	141.1	24.9
Low speed	3.2		16.7	0.251	141.2	25.0
Max speed	32.768	160000	102.44	0.202	143.1	25.3
High speed	25.6		80	0.187	143.8	25.4
Low speed	3.2		10	0.201	143.2	25.3

(1) High OSR values can yield varying noise results because of the limits of 24-bit quantization: 4.096 V / 2^{23} = 0.488 µV / code. Sinc3 + sinc1 and sinc4 + sinc1 filters yield equal noise performance.

Table 7-4. FIR1 Filter Noise Performance (V_{REF} = 4.096 V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
Max speed	32.768	8	2048	641	73.1	13.6
High speed	25.6		1600	648	73.0	13.6
Mid speed	12.8		800	662	72.8	13.6
Low speed	3.2		200	681	72.6	13.6
Max speed	32.768	16	1024	93.0	89.9	16.4
High speed	25.6		800	94.8	89.7	16.4
Mid speed	12.8		400	99.9	89.2	16.3
Low speed	3.2		100	105	88.8	16.2
Max speed	32.768	32	512	11.0	108.4	19.5
High speed	25.6		400	10.8	108.6	19.5
Mid speed	12.8		200	10.5	108.8	19.6
Low speed	3.2		50	10.3	109.0	19.6
Max speed	32.768	64	256	7.44	111.8	20.1
High speed	25.6		200	7.30	112.0	20.1
Mid speed	12.8		100	7.09	112.2	20.1
Low speed	3.2		25	6.93	112.4	20.2
Max speed	32.768	128	128	5.20	114.9	20.6
High speed	25.6		100	5.10	115.1	20.6
Mid speed	12.8		50	4.93	115.4	20.7
Low speed	3.2		12.5	4.82	115.6	20.7
Max speed	32.768	256	64	3.69	117.9	21.1
High speed	25.6		50	3.63	118.0	21.1
Mid speed	12.8		25	3.48	118.4	21.2
Low speed	3.2		6.25	3.39	118.6	21.2
Max speed	32.768	512	32	2.64	120.8	21.6
High speed	25.6		25	2.62	120.9	21.6
Mid speed	12.8		12.5	2.47	121.4	21.7
Low speed	3.2		3.125	1.27	127.1	22.6
Max speed	32.768	1024	16	1.94	123.5	22.0
High speed	25.6		12.5	1.90	123.6	22.0
Mid speed	12.8		6.25	1.76	124.3	22.2
Low speed	3.2		1.5625	0.886	130.3	23.1

Table 7-5. FIR2 Filter Performance (V_{REF} = 4.096 V, 1x Input Range)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
Max speed	32.768	16	1024	51.0	95.1	17.3
High speed	25.6		800	51.0	95.1	17.3
Mid speed	12.8		400	50.3	95.2	17.3
Low speed	3.2		100	50.0	95.3	17.3
Max speed	32.768	32	512	11.6	108.0	19.4
High speed	25.6		400	11.4	108.1	19.5
Mid speed	12.8		200	11.1	108.3	19.5
Low speed	3.2		50	10.9	108.5	19.5

Table 7-5. FIR2 Filter Performance (V_{REF} = 4.096 V, 1x Input Range) (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	NOISE (e_n, μV_{RMS})	DYNAMIC RANGE (dB)	EFFECTIVE RESOLUTION (Bits)
Max speed	32.768	64	256	7.85	111.3	20.0
High speed	25.6		200	7.69	111.5	20.0
Mid speed	12.8		100	7.47	111.8	21.1
Low speed	3.2		25	7.33	111.9	21.1
Max speed	32.768	128	128	5.47	114.5	20.5
High speed	25.6		100	5.36	114.7	20.5
Mid speed	12.8		50	5.18	114.9	20.6
Low speed	3.2		12.5	5.07	115.1	20.6
Max speed	32.768	256	64	3.86	117.5	21.0
High speed	25.6		50	3.80	117.6	21.0
Mid speed	12.8		25	3.66	118.0	21.1
Low speed	3.2		6.25	3.58	118.2	21.1
Max speed	32.768	512	32	2.79	120.3	21.5
High speed	25.6		25	2.73	120.5	21.5
Mid speed	12.8		12.5	2.59	121.0	21.6
Low speed	3.2		3.125	1.76	124.3	22.2
Max speed	32.768	1024	16	2.01	123.2	22.0
High speed	25.6		12.5	1.99	123.3	22.0
Mid speed	12.8		6.25	1.83	124.0	22.1
Low speed	3.2		1.5625	1.26	127.2	22.6
Max speed	32.768	2048	8	1.51	125.6	22.4
High speed	25.6		6.25	1.48	125.8	22.4
Mid speed	12.8		3.125	0.928	129.9	23.1
Low speed	3.2		0.78125	0.927	129.9	23.1

8 Detailed Description

8.1 Overview

The ADS127L21 is a high-performance, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with data rates up to 512 kSPS in the wideband filter mode and 1.365 MHz in the low-latency filter mode. The ADC features a programmable digital filter to customized the filter response and offers an excellent combination of dc accuracy and ac precision with trade-offs between resolution, bandwidth and power consumption.

The *Functional Block Diagram* shows the features of the ADS127L21. Input and positive-reference precharge buffers increase the input impedance for reduced system errors. The VCM output provides a mid-supply voltage to drive the common-mode voltage of an external input driver.

The delta-sigma modulator is a multibit design that measures the differential input signal, $V_{IN} = (V_{AINP} – V_{AINN})$, against the differential reference, $V_{REF} = (V_{REFP} – V_{REFN})$. The modulator shapes the quantization noise to an out-of-band frequency range where the noise is removed by the digital filter. The noise remaining within the signal band is constant-density white noise. The digital filter decimates and filters the modulator data to provide the high-resolution output data.

The digital filter has two operating modes: low-latency and wideband. The low-latency mode consists of a programmable sinc3 or sinc4 filter, with the option of a sinc1 filter in cascade operation. The low-latency filter minimizes latency time for dc signal measurements.

The wideband filter consists of a preset or programmable coefficient FIR filter with a four biquad IIR filter operating in series. The IIR filter allows customized filters such as high pass, band pass, band reject, low pass, and so on.

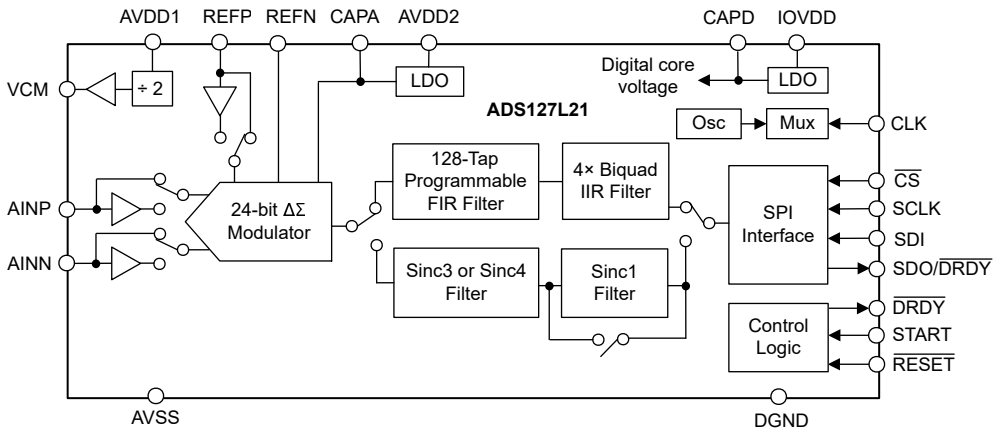
The programmable oversampling ratio (OSR) combined with four speed modes allows optimization of signal bandwidth, resolution, and power consumption.

The SPI-compatible serial interface is used to configure the device and read conversion data. The interface features daisy-chaining capability for simplified SPI routing in multichannel, simultaneous-sampled systems. Integrated cyclic redundancy check (CRC) error monitoring improves system-level reliability. The $\overline{DRDY}$ pin indicates when conversion data are ready. The $\overline{DRDY}$ function can be combined with the SDO/$\overline{DRDY}$ pin to reduce the number of SPI lines.

The device supports external clock operation for ac or dc signal applications and an internal oscillator for dc signal applications. The START pin synchronizes the digital filter process. The $\overline{RESET}$ pin resets the ADC.

Supply voltage AVDD1 powers the precharge buffers and the input sampling switches. AVDD2 powers the modulator via an internal voltage regulator. Supply voltage IOVDD is the digital I/O voltage that also powers the digital core with a digital voltage regulator. The internal regulators minimize power consumption while providing consistent levels of performance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input (AINP, AINN)

The analog input of the ADC is differential, with the input defined as a difference voltage: $V_{IN} = V_{AINP} – V_{AINN}$. For best performance, drive the input with a differential signal with the common-mode voltage centered to mid-supply (AVDD1 + AVSS) / 2.

The ADC accepts either unipolar or bipolar input signals by configuring the AVDD1 and AVSS power supplies accordingly. Figure 8-1 shows an example of a differential signal with the supplies configured to unipolar operation. Symmetric input voltage headroom is available when the common-mode voltage is at mid-supply (AVDD1 / 2). Use AVDD1 = 5 V and AVSS = 0 V for unipolar operation (see specifications for reduced AVDD1 operation).

Figure 8-2 shows an example of a differential signal in bipolar operation. The common-mode voltage of the signal (V_{CM}) is normally at 0 V. Use AVDD1 = 2.5 V and AVSS = –2.5 V for bipolar operation.

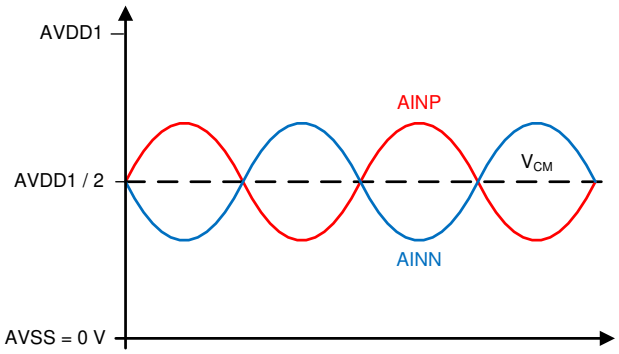


Figure 8-1. Unipolar Differential Input Signal

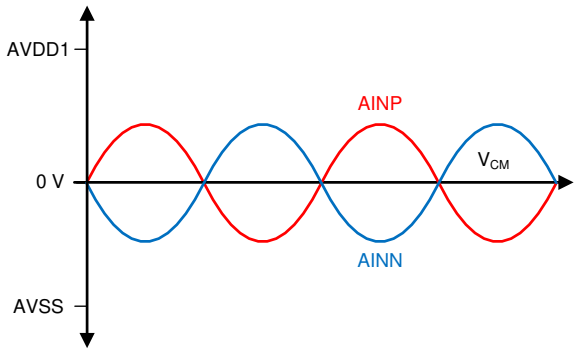


Figure 8-2. Bipolar Differential Input Signal

In either bipolar or unipolar power-supply configuration, the ADC accepts single-ended input signals by tying the AINN input to AVSS, ground, or mid-supply. However, because AINN is now fixed, the voltage range of the ADC is limited by the input voltage swing of AINP (±2.5 V for bipolar operation or 0 V to 5 V for a 5-V unipolar operation).

The simplified circuit shown in Figure 8-3 represents the analog input structure.

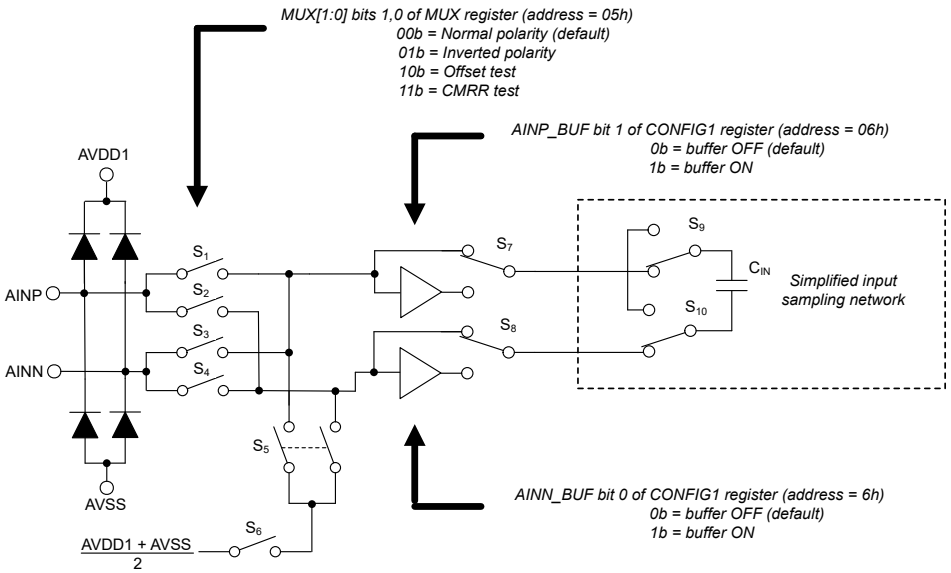


Figure 8-3. Analog Input Circuit

Diodes protect the ADC inputs from electrostatic discharge (ESD) events that occur during the manufacturing process and during printed circuit board (PCB) assembly when manufactured in an ESD-controlled environment. If the inputs are driven below AVSS – 0.3 V, or above AVDD1 + 0.3 V, the protection diodes can conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

The input multiplexer offers the option of normal or reverse input signal polarities. The multiplexer also provides two internal test modes to help verify ADC performance. The offset test mode verifies noise and offset error by providing a short to the ADC inputs. The resulting noise and offset voltage data are evaluated by the user. CMRR performance is tested using the CMRR test mode by applying a CMRR test signal to the AINP input. The resulting CMRR test data are also evaluated by the user. Table 8-1 shows the switch configurations of the input multiplexer circuit of Figure 8-3.

Table 8-1. Input Multiplexer Configurations

MUX[1:0] BITS	CLOSED SWITCHES	DESCRIPTION
00b	S_1, S_4	Normal polarity input ($V_{IN} = V_{AINP} - V_{AINN}$)
01b	S_2, S_3	Reverse polarity input ($V_{IN} = V_{AINN} - V_{AINP}$)
10b	S_5, S_6	Internal noise and offset error test
11b	S_1, S_5	CMRR test using a signal applied to AINP

The ADC samples the input voltage at the modulator frequency (f_{MOD}) by storing the voltage on the C_{IN} capacitor. The capacitor is discharged on the opposite clock phase of the modulator, at which time the sample process repeats. The instantaneous charge demand of C_{IN} requires the signal to settle within a half cycle at the modulator frequency $t = 1 / (2 \cdot f_{MOD})$. To satisfy this requirement, the external driver bandwidth is typically required to be much larger than the original signal frequency. The bandwidth of the driver is determined sufficient when the desired THD, SNR, and gain error performance are achieved. In mid- and low-speed modes of operation, the modulator frequency is reduced, therefore more time is available for the driver to settle.

The input charge required by the sampling capacitor is modeled as a peak current and an average current flowing into the ADC inputs. As given in Equation 15 and Equation 16, the average input current is comprised of differential and absolute components.

$$\text{Input Current (Differential Input Voltage)} = f_{MOD} \cdot C_{IN} \cdot 10^6 \ (\mu A/V) \quad (15)$$

where:

- $f_{MOD} = f_{CLK} / 2$
- C_{IN} = 7.4 pF (1x input range), 3.6 pF (2x input range)

$$\text{Input Current (Absolute Input Voltage)} = f_{MOD} \cdot C_{CM} \cdot 10^6 \ (\mu A/V) \quad (16)$$

where:

- $f_{MOD} = f_{CLK} / 2$
- C_{CM} = 0.35 pF (1x input range), 0.17 pF (2x input range)

For f_{MOD} = 12.8 MHz (high-speed mode), C_{IN} = 7.4 pF, and C_{CM} = 0.35 pF, the average current resulting from the differential voltage is 95 µA/V and the average current resulting from the absolute voltage is 4.5 µA/V. For example, if AINP = 4.5 V and AINN = 0.5 V, then V_{IN} = 4 V. The total AINP average current = (4 V · 95 µA/V) + (4.5 V · 4.5 µA/V) = 400 µA, and the total AINN average current is (–4 V · 95 µA/V) + (0.5 V · 4.5 µA/V) = –378 µA.

The device incorporates input precharge buffers to significantly reduce the charge demand from the C_{IN} capacitor. When enabled, the buffers are initially in-circuit during the sampling phase. When C_{IN} is nearly fully charged, the buffers are bypassed (S_7 and S_8 of Figure 8-3 in up positions). The external signal then provides the fine charge to the capacitor. At the completion of the sample phase, the sampling capacitor is discharged by the modulator to complete the conversion cycle. The buffers reduce the input current required to charge C_{IN}, therefore improving the input impedance and relaxing external driver requirements. The input buffers are

enabled by the AINP_BUF and AINN_BUF bits of the CONFIG1 register. If AINN is tied to ground or to a low-impedance fixed potential, disable the AINN buffer to reduce power consumption.

8.3.1.1 Input Range

The ADC has two input ranges: 1x and 2x, where the 1x range is defined by $V_{IN} = \pm V_{REF}$ and the 2x range is defined by $V_{IN} = \pm 2 \cdot V_{REF}$. The 2x input range doubles the available range when using a reference voltage of 2.5 V or less. The 2x input range typically improves SNR by 1 dB when using a 2.5-V reference, but also requires driving the inputs to the 5-V supply rails to achieve full dynamic range. The best available dynamic range (4-dB improvement, typical) is through the use a 4.096-V or 5-V reference voltage (program the ADC to the high-reference range mode). The 2x range operation is internally forced to the 1x range mode when the high-reference range is selected. See the CONFIG1 register to program the input range. Table 8-2 summarizes the ADC input range options.

Table 8-2. ADC Input Range

INP_RNG BIT(1)	INPUT RANGE (V)
0	$\pm V_{REF}$
1	$\pm 2 \cdot V_{REF}$

(1) The input range is forced to 1x when the high-reference range is selected.

In some cases, the full available input range is limited by the power-supply voltage and cannot be measured. For example, the input range exceeds the power-supply voltage when using a 3-V AVDD1 power supply with a 2.5-V reference voltage in the 2x range mode.

The ADC also provides the option of extending the input range beyond the standard full-scale range. In this mode, the input range is extended by 25% to provide signal headroom before clipping of the signal occurs. Output data are scaled such that the positive and negative full-scale output codes (7FFFFFh and 800000h) are at $\pm 1.25 \cdot k \cdot V_{REF}$, where k is the 1x or 2x input range option.

Because of modulator saturation, the SNR performance degrades when the signal exceeds 110% of the standard full-scale range. The MOD_FLAG bit of the STATUS1 register indicates modulator saturation. Figure 8-4 shows SNR performance when operating in the extended range. See the CONFIG1 register to program the extended range mode.

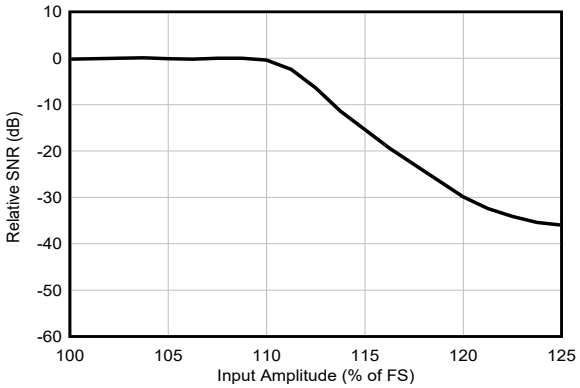


Figure 8-4. Extended Range SNR Performance

8.3.2 Reference Voltage (REFP, REFN)

A reference voltage is required for operation. The reference voltage input is differential, defined as: $V_{REF} = V_{REFP} – V_{REFN}$, and is applied to the REFP and REFN pins. See the *Reference Voltage Range* section for details of the reference voltage operating range.

As shown in Figure 8-5, the reference inputs have an input structure similar to the analog inputs. ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AVSS by more than 0.3 V, or above AVDD1 by 0.3 V. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified value.

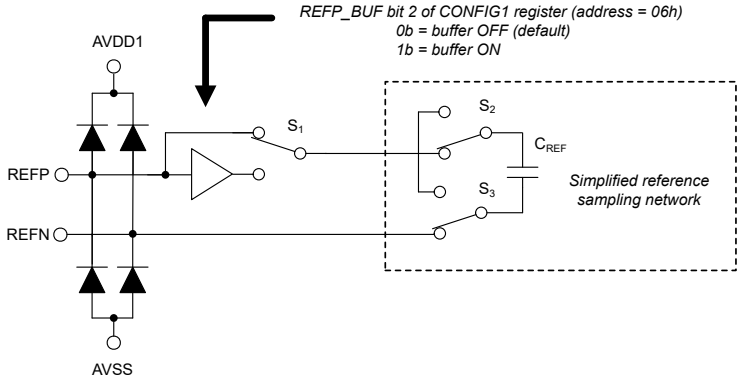


Figure 8-5. Reference Input Circuit

The reference voltage is sampled by a sampling capacitor, C_{REF}. In unbuffered mode, current flows through the reference inputs to charge the sampling capacitor. The current consists of a dc component and an ac component that varies with the frequency of the modulator sampling clock. See the *Electrical Characteristics* table for the reference input current specification.

Charging the reference sampling capacitor requires the reference voltage to settle at the end of the sample phase $t = 1 / (2 \cdot f_{MOD})$. Incomplete settling of the reference voltage can increase gain error and gain error drift. Operation in the lower-speed modes reduces the modulator sampling clock frequency, therefore allowing more time for the reference driver to settle.

The ADC provides a precharge buffer option for the REFP input to reduce the charge drawn by the sampling capacitor. The precharge buffer provides the coarse charge for the reference sampling capacitor, C_{REF}. Halfway through the sample phase, the precharge buffer is bypassed (S_1 is in an up position as demonstrated in Figure 8-5), at which time the external driver provides the fine charge to the sampling capacitor. Because the buffer reduces the charge demand of the sampling capacitor, the reference input impedance increases.

Many applications ground REFN, therefore a precharge buffer for REFN is not necessary for these cases. For applications when REFN is not a low-impedance source, consider buffering the REFN input.

8.3.2.1 Reference Voltage Range

The reference voltage is divided into two ranges: low-reference range and high-reference range. The voltage range must be programmed to match the applied reference voltage, such as 2.5 V or 4.096 V. The low-reference operating range is 0.5 V to 2.75 V, and the high-reference operating range is 1 V to the AVDD1 – AVSS power supplies. For best noise performance where the ranges overlap, such as 2.5 V, use the low-reference range. Program the REF_RNG bit of the CONFIG1 register to the appropriate reference voltage. When the high-reference range is selected, the input range is internally forced to 1x range.

8.3.3 Clock Operation

Figure 8-6 shows the block diagram of the ADC clock circuit. The ADC is operated by an external clock signal applied to the CLK pin or by the internal oscillator. Clock operation is made by the CLK_SEL bit of the CONFIG3 register. The output of the clock divider produces the ADC system clock (f_{CLK}). The system clock is further divided by two to derive the modulator clock (f_{MOD}).

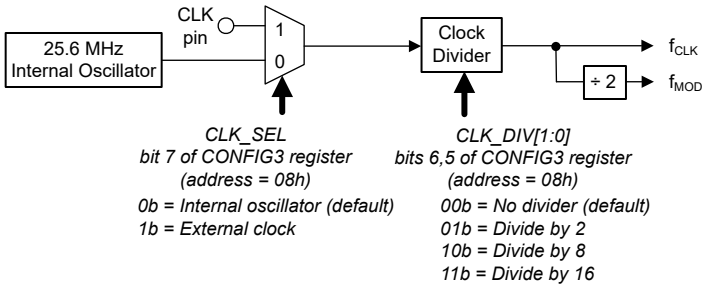


Figure 8-6. Clock Block Diagram

If necessary, use the clock divider to program the appropriate frequency for the selected speed mode. Table 8-3 shows the nominal clock frequencies for the respective speed modes and the corresponding data rates at the minimum OSR setting. Clock division factors of divide-by-2 or divide-by-16 force the low-latency filter OSR values of all speed modes to those of the mid-speed mode. See Table 8-30 for a list of OSR values of the speed modes.

Table 8-3. ADC Clock Frequency

SPEED MODE	CLOCK FREQUENCY (MHz)	MAXIMUM RATED DATA RATE (kSPS)	
		WIDEBAND FILTER	LOW-LATENCY FILTER
Max	32.768	512	1365.3
High	25.6	400	1066.6
Mid	12.8	200	533.3
Low	3.2	50	133.333

8.3.3.1 Internal Oscillator

At power-up and device reset, the ADC defaults to internal oscillator mode (CLK_SEL bit = 0b). Because the internal oscillator frequency is fixed to 25.6 MHz, use the clock divider when using the mid- and low-speed modes. The internal oscillator is not available for the maximum-speed mode. Because of the clock jitter of the internal oscillator, only use the internal oscillator for dc signal measurements. The internal oscillator is not recommended when measuring ac signals.

When changing the clock mode from an external clock to the internal oscillator, maintain the external clock for at least four clock cycles after completing the SPI register write command used to change the clock mode. After the clock mode changes, the ADC ignores control inputs (the START and RESET pins) for a period of 150 µs to allow time for the internal oscillator to stabilize.

8.3.3.2 External Clock

For external clock operation, program the CLK_SEL bit to 1b. Apply the clock signal to the CLK pin before programming the bit. the clock divider is available to divide the clock frequency. For example, a 25.6-MHz clock signal can be divided by 8 to produce 3.2 MHz for the low-speed mode. The clock frequency can be decreased from the nominal value to yield specific data rates between OSR values. However, when reducing the clock frequency, the conversion noise is the same as the nominal clock frequency. Reducing the conversion noise is only possible by increasing the OSR value or changing the filter mode.

Clock jitter results in timing variations when the signal is sampled, leading to degraded SNR performance. A low-jitter clock is essential to meet data sheet SNR performance. For example, with a 200-kHz signal frequency, an external clock with <10-ps (rms) jitter is required. For lower signal frequencies, the clock jitter requirement is relaxed by –20 dB per decade of signal frequency. For example, with f_{IN} = 20 kHz, 100-ps clock jitter

is acceptable. Many types of RC oscillators exhibit high levels of jitter and must be avoided for ac signal measurement. Instead, use crystal or bulk acoustic wave type oscillators. Avoid ringing on the clock input. A series resistor placed at the output of the clock buffer often helps reduce ringing.

8.3.4 Modulator

The modulator is a switched-capacitor, third-order architecture achieving excellent noise and linearity performance while maintaining low power consumption. As with most modulators, when driven by high amplitude or by out-of-band signals, modulator saturation can occur. When saturated, the in-band signal still converts, however the noise floor increases. Figure 8-7 shows the amplitude limit versus frequency to avoid modulator saturation. The amplitude limit for in-band signals is 1 dBFS.

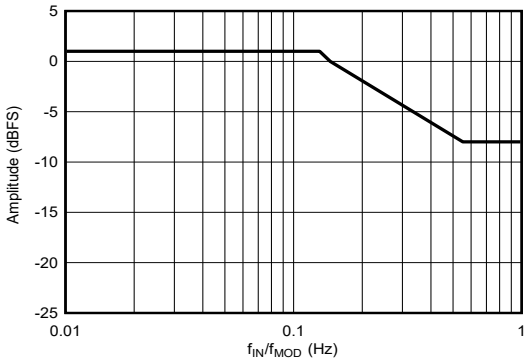


Figure 8-7. Amplitude Limit to Avoid Modulator Saturation

Modulator saturation is indicated by the MOD_FLAG bit of the STATUS1 register. The modulator saturation status is latched during the conversion period and is refreshed at completion of the conversion. Modulator saturation as a result of out-of-band signals is avoided by using an antialias filter at the ADC inputs. The *THS4551 Antialias Filter Design* section shows an example of a fourth-order antialias filter, however a low-order filter is acceptable, provided the input amplitude is below the saturation limit.

8.3.5 Digital Filter

The digital filter performs low-pass filtering and decimation to the low-resolution data of the modulator to produce high-resolution, lower speed conversion data. The oversampling ratio (OSR) determines the amount of filtering and decimation that, in turn, affects signal bandwidth, conversion noise, and the final data rate. The output data rate is defined as: $f_{DATA} = f_{MOD} / OSR$.

As shown in Figure 8-8, the ADC provides two filter modes: wideband and low latency. The filters optimize between frequency response characteristics (wideband filter mode) or time-domain characteristics (low-latency filter mode). The wideband filter features an IIR filter for emulation of analog-type filters. The coefficients of the wideband FIR and IIR filters are user programmable.

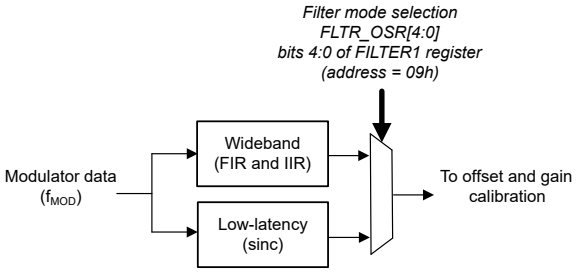


Figure 8-8. Digital Filter Diagram

8.3.5.1 Wideband Filter

The pass-band, transition-band, and stop-band characteristics of the wideband filter make this filter suitable for ac signal measurement. The wideband filter supports a 211-kHz input signal bandwidth in the maximum-speed mode operation. The wideband filter is operated using default coefficients, with characteristics described in the

Specifications section, or operated using user-programmed coefficients. The wideband filter also includes an IIR filter consisting of four biquads for digital filter emulation of analog filters.

Figure 8-9 shows the wideband filter block diagram.

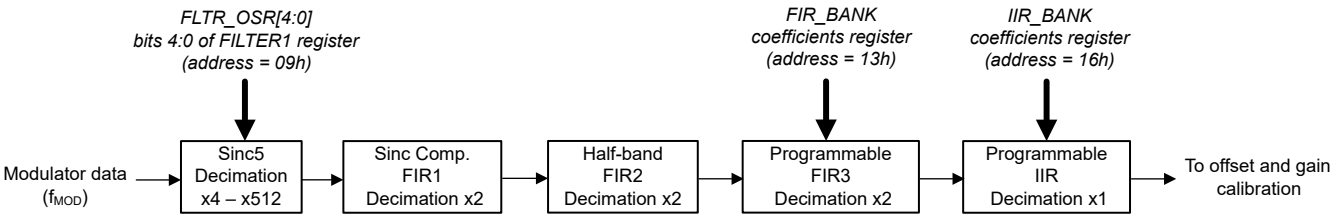


Figure 8-9. Wideband Filter Diagram

8.3.5.1.1 Wideband Filter Options

The wideband filter provides inter-stage bypassing and the option of reversing the FIR3-IIR filter sequence. Figure 8-10 shows the wideband filter options. Disabling a filter stage bypasses the filter function and associated decimation. For example, with the FIR2, FIR3, and IIR filter stages disabled, FIR1 filter data are output at 4 times the normal data rate. There are no restrictions to the number of filter options. However, if FIR2 is disabled then the FIR3 and IIR filters must also be disabled at an overall OSR of 16.

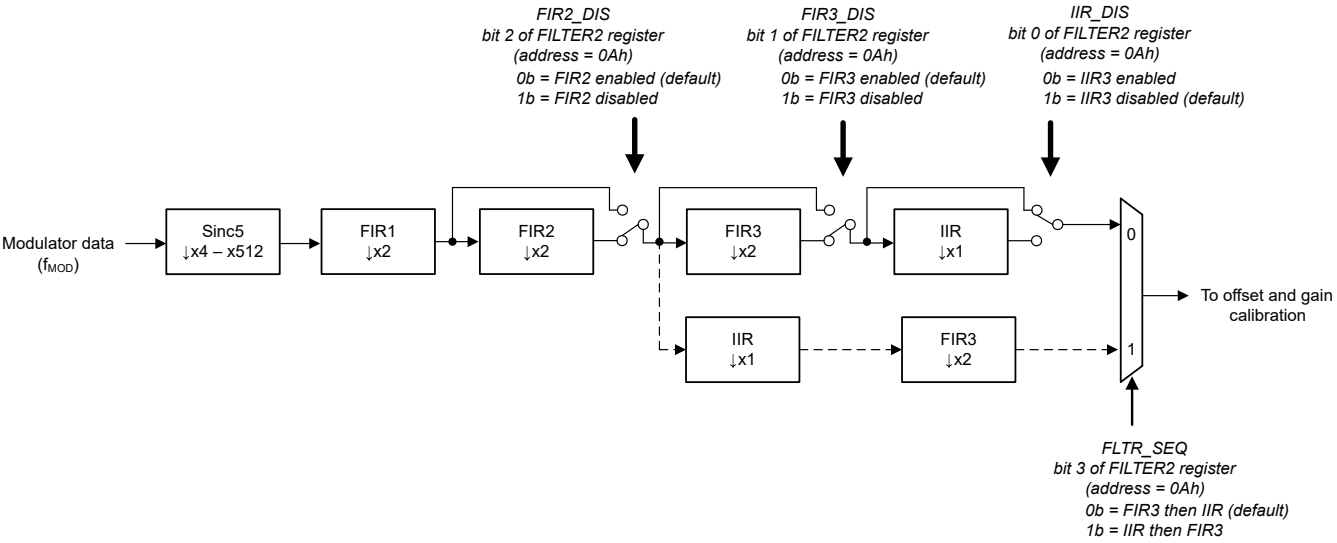


Figure 8-10. Wideband Filter Options

8.3.5.1.2 Sinc5 Filter Stage

The sinc5 filter prefilters the modulator data through averaging and decimation. The variable OSR of the sinc5 filter determines the range of final data rates. The sinc5 filter OSR is programmable from 4 to 512 by the FLTR_OSR[4:0] bits of the FILTER1 register, which results in the final range of OSR 32 to 4096.

8.3.5.1.3 FIR1 Filter Stage

The FIR1 filter stage follows the sinc5 filter. The FIR1 filter band-limits and decimates the data while compensating the sinc5 filter roll-off. The coefficients of the FIR1 filter are fixed with divide-by-2 decimation. FIR1 filter data are routed directly to the output by disabling the FIR2, FIR3, and IIR filters. Figure 8-11 illustrates the frequency response of the FIR1 filter output.

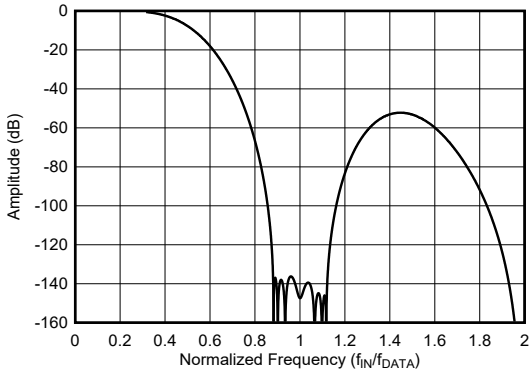


Figure 8-11. FIR1 Filter Frequency Response (OSR = 32)

See Table 7-4 for the FIR1 filter noise performance. Table 8-4 lists the filter latency time values

Table 8-4. FIR1 Filter Latency Time

MODE	f_{CLK} (MHz)	OSR[1]	DATA RATE (kSPS)	LATENCY TIME[2] (µs)
Max speed	32.768	8	2048	5.9
High speed	25.6		1600	7.5
Mid speed	12.8		800	15.0
Low speed	3.2		200	59.8
Max speed	32.768	16	1024	11.0
High speed	25.6		800	14.1
Mid speed	12.8		400	28.1
Low speed	3.2		100	112.3
Max speed	32.768	32	512	21.3
High speed	25.6		400	27.2
Mid speed	12.8		200	54.4
Low speed	3.2		50	217.2
Max speed	32.768	64	256	41.8
High speed	25.6		200	53.4
Mid speed	12.8		100	106.9
Low speed	3.2		25	427.4
Max speed	32.768	128	128	82.8
High speed	25.6		100	105.9
Mid speed	12.8		50	211.8
Low speed	3.2		12.5	847.2
Max speed	32.768	256	64	164.8
High speed	25.6		50	210.9
Mid speed	12.8		25	421.9
Low speed	3.2		6.25	1687.3
Max speed	32.768	512	32	328.9
High speed	25.6		25	420.9
Mid speed	12.8		12.5	841.9
Low speed	3.2		3.125	3367.4
Max speed	32.768	1024	16	657.0
High speed	25.6		12.5	840.9
Mid speed	12.8		6.25	1681.9
Low speed	3.2		1.5625	6727.3

(1) The FIR1 OSR is the FILT_OSR[4:0] setting of the FILTER1 register divided by 4.
(2) Latency time increases by 8 / f_{CLK} (µs) when analog input buffers are enabled.

8.3.5.1.4 FIR2 Filter Stage

The FIR2 filter is an intermediate stage *half-band* low-pass filter that reduces the data rate by divide-by-2 decimation. FIR2 filter data are supplied directly to the output by disabling the FIR3 and IIR filter stages. Figure 8-12 shows the frequency response of the FIR2 filter output.

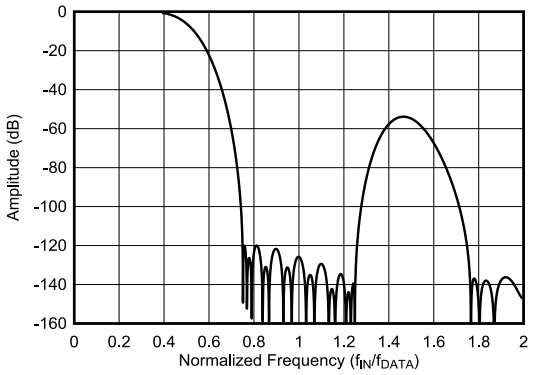


Figure 8-12. FIR2 Filter Frequency Response (OSR = 32)

Table 8-5 and Table 7-5 illustrate the FIR2 filter latency time and noise performance.

Table 8-5. FIR2 Filter Latency Time

MODE	f_{CLK} (MHz)	OSR[1]	DATA RATE (kSPS)	LATENCY TIME[2] (µs)
Max speed	32.768	16	1024	19.8
High speed	25.6		800	25.3
Mid speed	12.8		400	50.6
Low speed	3.2		100	202.3
Max speed	32.768	32	512	38.9
High speed	25.6		400	49.7
Mid speed	12.8		200	99.4
Low speed	3.2		50	397.2
Max speed	32.768	64	256	76.9
High speed	25.6		200	98.4
Mid speed	12.8		100	196.9
Low speed	3.2		25	787.4
Max speed	32.768	128	128	153.1
High speed	25.6		100	195.9
Mid speed	12.8		50	391.9
Low speed	3.2		12.5	1567.5
Max speed	32.768	256	64	305.5
High speed	25.6		50	390.9
Mid speed	12.8		25	781.8
Low speed	3.2		6.25	3127.4
Max speed	32.768	512	32	610.1
High speed	25.6		25	780.9
Mid speed	12.8		12.5	1561.8
Low speed	3.2		3.125	6247.5
Max speed	32.768	1024	16	1219.5
High speed	25.6		12.5	1560.9
Mid speed	12.8		6.25	3121.8
Low speed	3.2		1.5625	12487

Table 8-5. FIR2 Filter Latency Time (continued)

MODE	f_{CLK} (MHz)	OSR(1)	DATA RATE (kSPS)	LATENCY TIME(2) (µs)
Max speed	32.768	2048	8	2438.3
High speed	25.6		6.25	3120.9
Mid speed	12.8		3.125	6241.9
Low speed	3.2		0.78125	24.968

(1) The FIR2 OSR is the FILT_OSR[4:0] setting of the FILTER1 register divided by 2.
(2) Latency time increases by 8 / f_{CLK} (µs) when analog input buffers are enabled.

8.3.5.1.5 FIR3 Filter Stage

The FIR3 filter is operated by either preset or programmable coefficients. The FIR3 filter, and the associated divide-by-2 decimation, can be bypassed from the wideband filter path. Figure 8-13 shows the structure of the FIR3 filter.

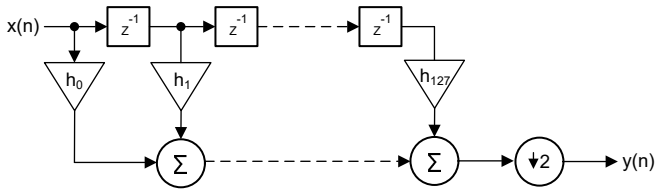


Figure 8-13. FIR3 Filter Structure

The FIR3 filter consists of 128 taps using fixed divide-by-2 decimation to perform the final data rate reduction. The coefficients are 32-bit integer values in signed 1.31 format with the MSB as the sign bit, representing the decimal range of –1 (80000000h) to 1 – $1/2^{31}$ (7FFFFFFFh). The coefficients are typically designed to sum to unity for 0-dB gain in the pass band. Pad the end coefficients with zero values if fewer taps are used.

Because the ADC uses 128 taps, the latency time of the first conversion is 75 / f_{DATA} + 16 / f_{CLK}, compared to 68 / f_{DATA} + 16 / f_{CLK} for the preset coefficients. The *group delay* of the filter, however, is determined by the design of the filter coefficients.

The FLTR_OSR[4:0] register bits program the overall OSR and final data rate of the wideband filter. FLTR_SEL[2:0] register bits = 000b selects the default coefficient operation and 111b selects the programmable coefficient operation. See the FILTER1 register for details.

The programmable coefficients of the FIR3 filter are written to the FIR_BANK register. The register is a single address (address 13h) that stores 512 bytes of the 128 coefficient values. To read or write the coefficients, repeat the read or write operation to the same register address. The device automatically increments a memory pointer to the next internal memory location after completion of each read or write operation. As given in Table 8-6, the first byte of the operation is the MSB of the 127th coefficient (h_{127}), followed by MSB-1, MSB-2, and LSB bytes. The next byte is the MSB of the 126th coefficient, and so on. The last byte (byte 512) of the read/write operation is the LSB of coefficient h_0. Any register address change during the read or write operation to another address resets the coefficient pointer to the first memory location (MSB of h_{127}). If an SPI CRC error occurs during the write operation, clear the SPI_ERR bit of the STATUS1 register, which restarts the coefficient read or write operation at the beginning.

A minimum 10 × t_{CLK} delay time is required between SPI frames when reading or writing filter coefficients. Synchronize the ADC after writing the filter coefficients.

Table 8-6. FIR3 Coefficient Upload Byte Sequence (Register Address = 13h)

FIR3 COEFFICIENT	BYTE SEQUENCE	BYTES
h_{127}	1, 2, 3, 4	MSB, MSB-1, MSB-2, LSB
h_{126}	5, 6, 7, 8	MSB, MSB-1, MSB-2, LSB
…	…	…
h_0	509, 510, 511, 512	MSB, MSB-1, MSB-2, LSB

8.3.5.1.6 FIR3 Default Coefficients

FIR3 coefficients are available without the need to supply custom coefficients. The default coefficients are selected by the FLTR_SEL[2:0] bits = 000b of the FILTER1 register. The default coefficients feature linear phase response, low pass-band ripple, narrow transition band, and high stop-band attenuation.

Figure 8-14 through Figure 8-18 illustrate the default wideband filter frequency response. Figure 8-14 shows the pass-band ripple. Figure 8-15 shows the frequency response at the transition band.

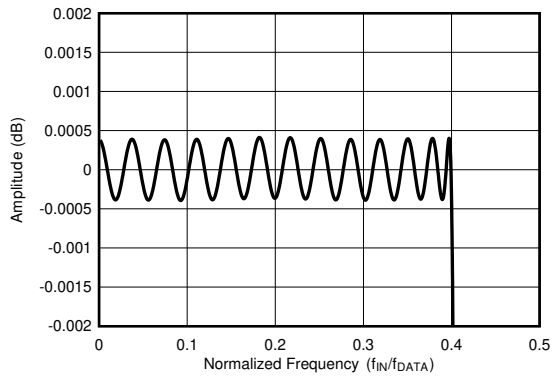


Figure 8-14. Wideband Filter Pass-Band Ripple

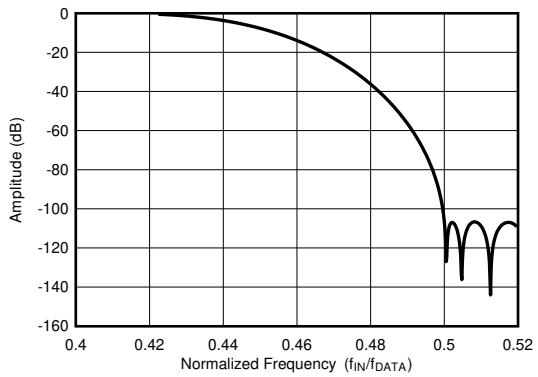
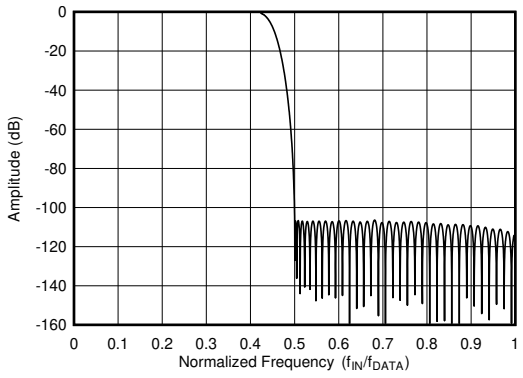


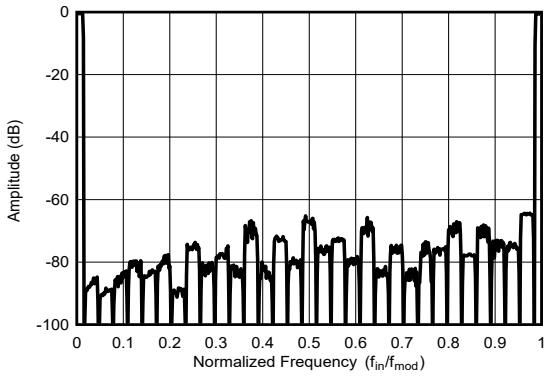
Figure 8-15. Wideband Filter Transition Band

Figure 8-16 shows the filter response up to f_{DATA} for OSR ≥ 64. The stop band begins at f_{DATA} / 2 to reduce signal aliasing. Figure 8-17 shows the filter to f_{MOD}. In the stop-band region, signal frequencies intermodulate with multiples of the chop frequency at f_{MOD} / 32, creating a series of response peaks that exceed the attenuation provided by the digital filter. The width of the response peaks is twice the filter bandwidth. Stop-band attenuation is improved when the ADC input is filtered by an analog antialias filter. See the *THS4551 Antialias Filter Design* section for details of a fourth-order antialias filter at the ADC input.



OSR ≥ 64

Figure 8-16. Wideband Filter Frequency Response



OSR = 32

Figure 8-17. Wideband Filter Stop-Band Attenuation

Figure 8-18 shows the filter response at f_{MOD}. As shown, the filter response repeats for input signals at f_{MOD}. If not removed by an antialias filter, signal frequencies at f_{MOD} appear as aliased frequencies in the pass band.

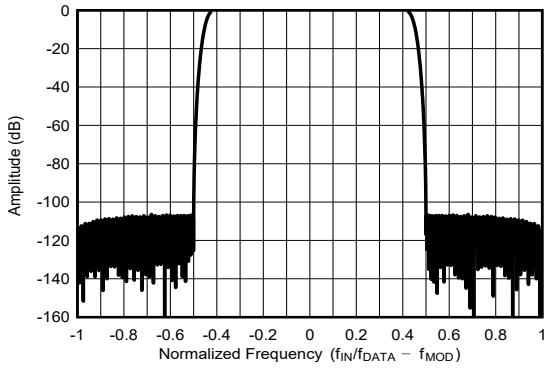


Figure 8-18. Wideband Filter Frequency Response at f_{MOD}

Aliasing also occurs with input frequencies occurring at multiples of f_{MOD}. These frequency bands are defined by:

$$\text{Alias frequency bands: } (N \cdot f_{MOD}) \pm f_{BW} \quad (17)$$

where:

- N = 1, 2, 3, and so on
- f_{MOD} = Modulator sampling frequency
- f_{BW} = Filter bandwidth

The group delay of the filter is the propagation time for an input signal to appear at the output of the filter. Because the filter is a linear-phase design, the envelope of a complex input signal is undistorted by the filter. The group delay (expressed in units of time) is constant versus frequency, equal to 34 / f_{DATA}. After a step input is applied, fully settled data occur 68 data periods later. Figure 8-19 shows the filter group delay (34 / f_{DATA}) and the settling time to a step input (68 / f_{DATA}).

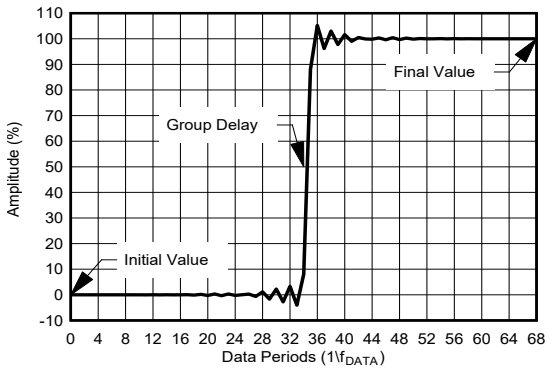


Figure 8-19. Wideband Filter Step Response

The digital filter is restarted when the ADC is synchronized. The ADC suppresses the first 68 conversion periods until the filter is fully settled. There is no need to discard data after synchronization. The time of data suppression is the conversion latency time as listed in the *latency time* column of Table 8-7. 16 f_{CLK} cycles of overhead time is incurred for all data rates. If a step input is applied randomly to the conversion period without synchronizing, the next 69 conversions are unsettled data. The –0.1-dB frequency of the amplitude response is 0.4125 × f_{DATA} and the –3-dB frequency is 0.4374 × f_{DATA} for all data rates.

Table 8-7. Wideband Default Filter Characteristics

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	–0.1-dB FREQUENCY (kHz)	–3-dB FREQUENCY (kHz)	LATENCY TIME(1) (µs)
Max speed	32.768	32	512	211.2	223.9	135.5
High speed	25.6		400	165	174.96	173.4
Mid speed	12.8		200	82.5	87.48	346.9
Low speed	3.2		50	20.63	21.87	1387.8
Max speed	32.768	64	256	105.6	112.0	270.4
High speed	25.6		200	82.5	87.48	346.1
Mid speed	12.8		100	41.25	43.74	692.2
Low speed	3.2		25	10.31	10.94	2768.7
Max speed	32.768	128	128	52.8	55.99	540.0
High speed	25.6		100	41.25	43.74	691.2
Mid speed	12.8		50	20.63	21.87	1382.3
Low speed	3.2		12.5	5.1562	5.468	5529.2
Max speed	32.768	256	64	26.4	28.00	1079.2
High speed	25.6		50	20.625	21.87	1381.3
Mid speed	12.8		25	10.31	10.93	2762.6
Low speed	3.2		6.25	2.578	2.734	11051
Max speed	32.768	512	32	13.2	14.00	2157.6
High speed	25.6		25	10.312	10.935	2761.6
Mid speed	12.8		12.5	5.156	5.467	5523.3
Low speed	3.2		3.125	1.289	1.367	22093
Max speed	32.768	1024	16	6.6	7.998	4314.2
High speed	25.6		12.5	5.156	5.467	5522.3
Mid speed	12.8		6.25	2.578	2.734	11045
Low speed	3.2		1.5625	0.645	0.6834	44178
Max speed	32.768	2048	8	3.3	3.499	8627.8
High speed	25.6		6.25	2.578	2.734	11044
Mid speed	12.8		3.125	1.289	1.367	22087
Low speed	3.2		0.78125	0.322	0.3417	88348
Max speed	32.768	4096	4	1.65	1.750	17254
High speed	25.6		3.125	1.289	1.367	22086
Mid speed	12.8		1.5625	0.645	0.6834	44172
Low speed	3.2		0.390625	0.161	0.1709	176690

(1) IIR filter bypassed. Latency time increases by 8 / f_{CLK} (µs) when analog input buffers are enabled.

8.3.5.1.7 IIR Filter Stage

The wideband filter has an IIR filter option. As shown in Figure 8-20, the IIR filter is composed of four biquad filters with five scaling factors (g_1 through g_5). The IIR filter block is enabled by the IIR_DIS bit of the FILTER2 register (default is disabled). The IIR filter can operate before or after the FIR3 filter.

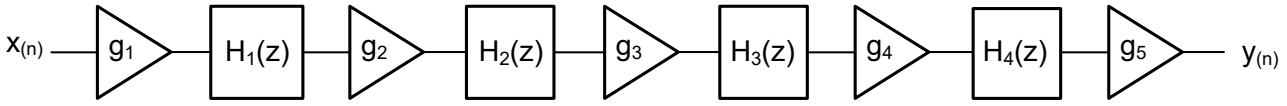


Figure 8-20. IIR Filter Block Diagram

As shown in Figure 8-21, the biquad filter sections are implemented in direct form 1. Equation 18 shows the biquad transfer function.

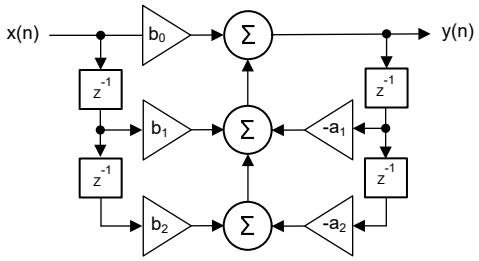


Figure 8-21. IIR H(z)

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \quad (18)$$

The biquad coefficients are 32-bit signed integers, in 2.30 format with the MSB as the sign bit, representing the decimal range of –2 (80000000h) to 2 – $2/2^{31}$ (7FFFFFFFh). The coefficients are uploaded to the IIR_BANK register. The register is a single address (address 16h) that stores the 100-byte set of the IIR coefficients, comprised of 80 coefficient bytes and 20 scaling factor bytes.

To read and write the coefficients, perform sequential read and write operations to the same register address (address 16h). An internal pointer automatically increments to the next memory location after each read or write operation. As given in Table 8-8, the first byte of the operation is the MSB of coefficient g_5, followed by MSB-1, MSB-2, and LSB bytes; followed next by the MSB of a_{42}, and so on. Coefficient a_{42} signifies the a_2 coefficient of the fourth biquad $H_4(z)$. The last byte (byte 100) is the LSB of g_1. Any change of address to another register during the sequence of read or write operations resets the pointer to the first memory location. If an SPI CRC error occurs during the write operation, clear the SPI_ERR bit of the STATUS1 register, which resets the coefficient write operation to the beginning. A minimum 10 × t_{CLK} delay time is required between SPI frames when reading or writing filter coefficients.

Synchronize the ADC after writing the filter coefficients.

The default configuration of the IIR filter is a unity-gain, all-pass filter. That is, g_1 through g_5 = 1, b_{x0} = 1, and b_{x1}, b_{x2}, a_{x1}, a_{x2} = 0, where x is the biquadratic number.

Table 8-8. IIR Coefficient Upload Byte Sequence (Register Address = 16h)

IIR COEFFICIENT	BYTE SEQUENCE	BYTES	DEFAULT VALUE	
			HEX	DECIMAL
g_5	1, 2, 3, 4	MSB, MSB-1, MSB-2, LSB	40000000h	1.0
a_{42}	5, 6, 7, 8	MSB, MSB-1, MSB-2, LSB	00000000h	0
a_{41}	9, 10, 11, 12	MSB, MSB-1, MSB-2, LSB	00000000h	0
b_{42}	13, 14, 15, 16	MSB, MSB-1, MSB-2, LSB	00000000h	0
b_{41}	17, 18, 19, 20	MSB, MSB-1, MSB-2, LSB	00000000h	0
b_{40}	21, 22, 23, 24	MSB, MSB-1, MSB-2, LSB	40000000h	1.0
g_4	25, 26, 27, 28	MSB, MSB-1, MSB-2, LSB	40000000h	1.0
...	...	...	...	...
b_{10}	93, 94, 95, 96	MSB, MSB-1, MSB-2, LSB	40000000h	1.0
g_1	97, 98, 99, 100	MSB, MSB-1, MSB-2, LSB	40000000h	1.0

8.3.5.1.7.1 IIR Filter Stability

An IIR filter designed for stable operation requires the pole radius of the polynomial H(z) denominator to be on or within the unit circle (that is, the pole radius r must be ≤ 1). However, resulting from the finite resolution of the ADS127L21 IIR filter, the IIR filter can exhibit artifacts such as dead-band effects at zero signal input and rounding noise not contained in the original signal when the pole radius of H(z) is > 0.98. Figure 8-22 shows the unit circle in the z-plane and the IIR filter 0.98 pole radius.

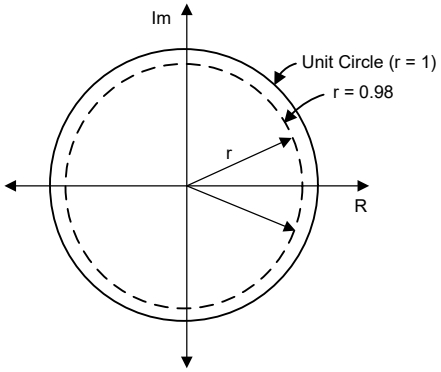


Figure 8-22. Z-Plane

The pole radius of the H(z) prototype filter design is computing by $\sqrt{a_2}$, where a_2 is the coefficient of the $1 + a_1z^{-1} + a_2z^{-2}$ polynomial in the H(z) denominator. The pole radius is reduced by decreasing the ratio of the data rate to the filter frequency. Evaluate the suitability of the prototype IIR filter design by testing the filter in the ADC.

8.3.5.2 Low-Latency Filter (Sinc)

The low-latency filter is a cascaded-integrator-comb (CIC) topology that minimizes the delay (latency) when conversion data propagates through the filter. The CIC filter is otherwise known as a sinc filter because of the characteristic sinx/x (sinc) frequency response. The latency time is shorter than the wideband filter, making the sinc filter suitable for fast acquisition of dc signals or for use in control loops. As shown in Figure 8-23, the device offers programmable OSR and several sinc filter configurations: sinc3, sinc4, followed by the option of a cascaded sinc1 stage. The configurations of the sinc filter allow trade-offs between acquisition time, noise performance, and line-cycle rejection.

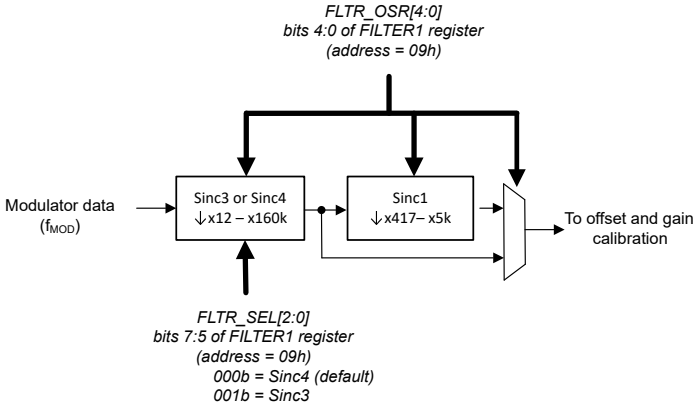


Figure 8-23. Sinc Filter Bock Diagram

Equation 19 describes the general expression of the sinc-filter frequency response. For the single-stage sinc filter mode, the second stage is not used.

$$\left|H_{(f)}\right| = \left| \frac{\sin\left[\frac{A\pi f}{f_{MOD}}\right]}{A\sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^{n} \cdot \left| \frac{\sin\left[\frac{AB\pi f}{f_{MOD}}\right]}{B\sin\left[\frac{A\pi f}{f_{MOD}}\right]} \right| \quad (19)$$

where:

- n = Filter order of stage 1 (3 or 4)
- A = Sinc3 or sinc4 stage OSR
- B = Sinc1 stage OSR
- f = Input signal frequency
- $f_{MOD} = f_{CLK} / 2$

Latency is defined as the time from the start of the first conversion to the falling edge of $\overline{DRDY}$, at which time fully settled data are available. There is no need to discard data because unsettled data are suppressed by the ADC. Detailed latency data for each sinc filter mode are given in Table 8-9 and Table 8-12.

If the input signal is changed while actively converting (without synchronizing to the START pin or to the START bit), then the next conversion data are partially settled. The required number of conversions for fully settled data is found by rounding the latency time value listed in the sinc filter tables to the next whole number of conversion periods.

8.3.5.2.1 Sinc3 and Sinc4 Filters

The sinc filter averages and decimates the high-speed modulator data to produce high-resolution output data at reduced data rate. Increasing the OSR value decreases the data rate and simultaneously reduces signal bandwidth and conversion noise resulting from increased decimation and data averaging. Table 8-9 lists the sinc3 and sinc4 filter –3-dB frequency and latency time.

Table 8-9. Sinc3 and Sinc4 Filter Characteristics

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)		LATENCY TIME[1] (µs)	
				SINC3	SINC4	SINC3	SINC4
Max speed	32.768	12	1365.3	357.0	310.2	2.97	3.66
High speed	25.6		1066.6	278.9	242.3	3.73	4.69
Mid speed	12.8		533.3	139.5	121.2	7.46	9.36
Low speed	3.2		133.33	34.9	30.3	29.8	37.4
Max speed	32.768	16	1024	267.8	232.7	3.66	4.63
High speed	25.6		800	209.2	181.8	4.67	5.95
Mid speed	12.8		400	104.6	90.9	9.33	11.9
Low speed	3.2		100	26.2	22.7	37.4	47.3
Max speed	32.768	24	682.67	178.5	155.1	5.12	6.64
High speed	25.6		533.3	139.5	121.2	6.57	8.43
Mid speed	12.8		266.67	69.7	60.6	13.1	16.9
Low speed	3.2		66.67	17.4	15.1	52.3	67.4
Max speed	32.768	32	512	133.9	116.3	6.59	8.55
High speed	25.6		400	104.6	90.9	8.42	10.9
Mid speed	12.8		200	52.3	45.4	16.9	21.8
Low speed	3.2		50	13.1	11.4	67.3	87.2
Max speed	32.768	64	256	66.9	58.2	12.4	16.4
High speed	25.6		200	52.3	45.4	16.0	21.0
Mid speed	12.8		100	26.2	22.7	31.8	41.9
Low speed	3.2		25	6.54	5.68	127	167

Table 8-9. Sinc3 and Sinc4 Filter Characteristics (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)		LATENCY TIME[1] (µs)	
				SINC3	SINC4	SINC3	SINC4
Max speed	32.768	128	128	33.5	29.1	24.2	32.0
High speed	25.6		100	26.2	22.7	31.0	41.0
Mid speed	12.8		50	13.1	11.4	61.9	81.9
Low speed	3.2		12.5	3.27	2.84	247	327
Mid speed	12.8	167	38.323	10.0	8.71	80.2	106
Max speed	32.768	256	64	16.7	14.5	47.6	63.2
High speed	25.6		50	13.1	11.4	60.9	80.9
Mid speed	12.8		25	6.54	5.68	121.9	162
Low speed	3.2		6.25	1.63	1.42	487	648
Max speed	32.768	333	49.201	12.9	11.2	61.7	82.0
High speed	25.6		38.438	10.1	8.73	79.0	105
Mid speed	12.8		19.219	5.03	4.37	158	210
Low speed	3.2		4.804	1.26	1.09	631	840
Max speed	32.768	512	32	8.37	7.27	94.5	126
High speed	25.6		25	6.54	5.68	121	161
Mid speed	12.8		12.5	3.27	2.84	242	322
Low speed	3.2		3.125	0.817	0.710	967	1287
Max speed	32.768	667	24.564	6.42	5.58	123	164
High speed	25.6		19.19	5.02	4.36	157	209
Mid speed	12.8		9.595	2.51	2.18	314	419
Low speed	3.2		2.39	0.627	0.545	1258	1675
Max speed	32.768	1024	16	4.18	3.64	188	251
High speed	25.6		12.5	3.27	2.84	241	321
Mid speed	12.8		6.25	1.63	1.42	482	642
Low speed	3.2		1.5625	0.409	0.355	1927	2567
Max speed	32.768	1333	12.291	3.21	2.79	245	326
High speed	25.6		9.602	2.51	2.18	313	417
Mid speed	12.8		4.801	1.26	1.09	627	835
Low speed	3.2		1.2	0.314	0.273	2507	3340
Max speed	32.768	2048	8	2.09	1.82	376	501
High speed	25.6		6.25	1.63	1.42	481	641
Mid speed	12.8		3.125	0.817	0.710	962	1282
Low speed	3.2		0.7813	0.204	0.178	3847	5127
Max speed	32.768	2667	6.143	1.61	1.40	489	652
High speed	25.6		4.799	1.26	1.09	626	834
Mid speed	12.8		2.4	0.628	0.545	1252	1669
Low speed	3.2		0.6	0.157	0.136	5008	6675
Max speed	32.768	4096	4	1.046	0.909	751	1001
High speed	25.6		3.125	0.817	0.710	961	1281
Mid speed	12.8		1.563	0.409	0.355	1922	2562
Low speed	3.2		0.391	0.102	0.089	7687	10247
Max speed	32.768	5333	3.072	0.803	0.698	977	1303
High speed	25.6		2.4	0.628	0.545	1251	1667
Low speed	3.2		0.3	0.078	0.068	10006	13340

Table 8-9. Sinc3 and Sinc4 Filter Characteristics (continued)

MODE	f_{CLK} (MHz)	OSR	DATA RATE (kSPS)	–3-dB FREQUENCY (kHz)		LATENCY TIME(1) (µs)	
				SINC3	SINC4	SINC3	SINC4
Mid speed	12.8	13333	0.480	0.126	0.109	6251	8335
Mid speed	12.8	16000	0.400	0.105	0.0909	7501	10002
Max speed	32.768	26667	0.614	0.161	0.140	4884	6511
High speed	25.6		0.480	0.126	0.109	6251	8334
Low speed	3.2		0.06	0.0157	0.0136	50008	66675
Max speed	32.768	32000	0.512	0.134	0.116	5860	7813
High speed	25.6		0.4	0.105	0.091	7501	10001
Low speed	3.2		0.05	0.0131	0.0114	60007	80007
Mid speed	12.8	48000	0.133	0.0349	0.0303	22502	30002
Mid speed	12.8	80000	0.08	0.0209	0.0182	37502	50002
Max speed	32.768	96000	0.17067	0.0446	0.0388	17579	23438
High speed	25.6		0.133	0.0349	0.0303	22501	30001
Low speed	3.2		$0.016\overline{6}$	0.0044	0.0038	180007	240007
Max speed	32.768	160000	0.102	0.0268	0.0233	29298	39063
High speed	25.6		0.08	0.0209	0.0182	37501	50001
Low speed	3.2		0.01	0.0026	0.0023	300005	400004

(1) Latency time increases by 8 / f_{CLK} (µs) when analog input buffers are enabled.

Because of the reduction of data averaging performed in the filtering process, the full 24 bits of output data are reduced for OSR ≤ 24. Table 8-10 summarizes output resolution for OSR values ≤ 24.

Table 8-10. Sinc3 and Sinc4 Data Resolution

OSR	RESOLUTION (Bits)
12	19
16	20.5
24	23

Figure 8-24 and Figure 8-25 show the sinc filter frequency response. The frequency response consists of a series of response nulls occurring at f_{DATA} and multiples thereof. At the null frequencies, the filter has zero gain. Figure 8-25 shows the folding of the frequency response starting at the f_{MOD} / 2 frequency. No attenuation is provided by the filter at input frequencies near n · f_{MOD} (n = 1, 2, 3, and so on).

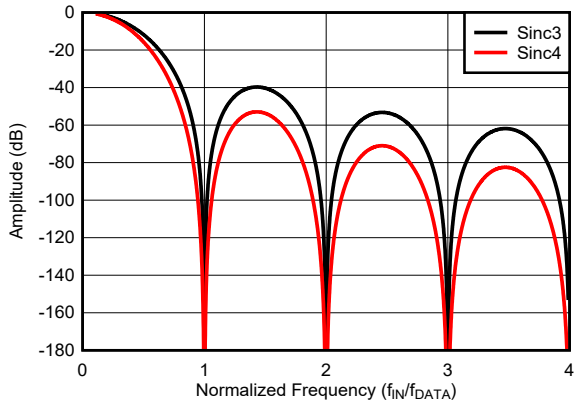


Figure 8-24. Sinc3 and Sinc4 Frequency Response (OSR = 32)

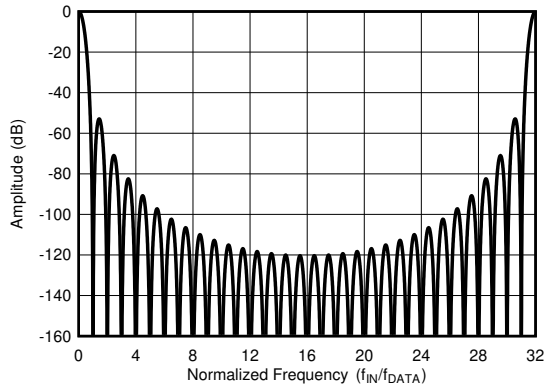


Figure 8-25. Sinc4 Frequency Response to f_{MOD} (OSR = 32)

Table 8-11 shows the normal-mode rejection of the filter for data rates equal to common line-cycle frequencies.

Table 8-11. Normal-Mode Rejection

MODE	OSR	f_{DATA} (SPS)	2% CLOCK VARIATION		6% CLOCK VARIATION	
			SINC3 FILTER	SINC4 FILTER	SINC3 FILTER	SINC4 FILTER
Low-speed	96000	$16.\overline{6}$	100 dB	135 dB	72 dB	95 dB
Low-speed	32000	50				
Low-speed	26667	60				
High-speed	32000	400				

8.3.5.2.2 Sinc3 + Sinc1 and Sinc4 + Sinc1 Cascade Filter

For selected data rates, the sinc3 and sinc4 filters offer the option of a cascade sinc1 filter section. Compared to a single-stage sinc3 or sinc4 filter, cascading the sinc1 filter shortens latency time when operated at the same data rate. However, the sinc3 and sinc4 filters provide greater rejection of 50-Hz and 60-Hz interference signals because of the wide frequency-rejection range at the data rate frequency. When operated in cascade mode, the OSR of the sinc3 or sinc4 stage is fixed at 32 (OSR = A) and the decimation of the sinc1 stage (OSR = B) determines the output data rate. The first stage of the cascade filter is programmable to sinc3 or sinc4. Table 8-12 summarizes the cascade filter characteristics.

Table 8-12. Sinc3 + Sinc1 and Sinc4 + Sinc1 Cascade Filter Characteristics

MODE	f_{CLK} (MHz)	OSR (A × B)(1)	DATA RATE (SPS)	–3-dB FREQUENCY (Hz)	LATENCY TIME (µs)	
					SINC3 + SINC1	SINC4 + SINC1
Mid speed	12.8	13334 (32 × 417)	480	212	2097	2102
Mid speed	12.8	16000 (32 × 500)	400	177	2512	2517
Max speed	32.768	26656 (32 × 833)	614	271	1632	1634
High speed	25.6		480	212	2089	2091
Low speed	3.2		60	26.5	16708	16728
Max speed	32.768	32000 (32 × 1000)	512	226	1958	1960
High speed	25.6		400	177	2506	2509
Low speed	3.2		50	22.1	20048	20068
Mid speed	12.8	48000 (32 × 1500)	133	58.9	7512	7517
Mid speed	12.8	80000 (32 × 2500)	80	35.4	12512	12517
Max speed	32.768	96000 (32 × 3000)	170.6	75.4	5864	5866
High speed	25.6		133.3	58.9	7506	7508
Low speed	3.2		16.7	7.37	60048	60068
Max speed	32.768	160000 (32 × 5000)	102.4	45.3	9770	9772
High speed	25.6		80	35.4	12506	12508
Low speed	3.2		10	4.42	100047	100067

(1) A = OSR of the first stage sinc3 or sinc4, B = OSR of the sinc1 second stage.

Figure 8-26 illustrates the frequency response of the sinc1 cascade mode filter with the first stage in sinc4 mode for OSR = 26656 and 32000, representing f_{DATA} = 50 SPS and 60 SPS in low-speed mode operation. Nulls in the frequency response occur at n · f_{DATA}, n = 1, 2, 3, and so on. At the null frequencies, the filter has zero gain. Assuming no ADC clock frequency error, the normal-mode rejection is 34 dB (typical) over a ±2% signal frequency variation at the null frequencies.

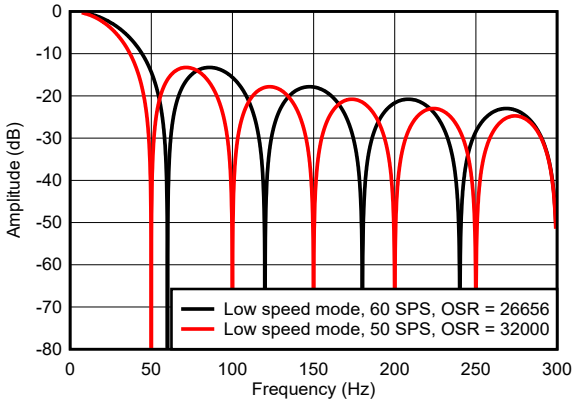


Figure 8-26. Sinc1 Cascaded Filter Frequency Response

8.3.6 Power Supplies

The device has three analog power supplies (AVDD1, AVSS, and AVDD2) and one digital power supply (IOVDD).

8.3.6.1 AVDD1 and AVSS

AVDD1 and AVSS are analog power supplies that power the input and voltage reference precharge buffers and sampling switches. The ADC can be configured for bipolar supply operation (such as AVDD1 = 2.5 V and AVSS = –2.5 V), or for unipolar supply operation (such as AVDD1 = 5 V and AVSS = DGND).

8.3.6.2 AVDD2

AVDD2 is an analog power supply with respect to AVSS and is used to power the modulator core. In unipolar supply operation, connect AVDD2 to AVDD1 to reduce the required number of power-supply voltages, or connect AVDD2 to a lower voltage supply to reduce device power consumption.

8.3.6.3 IOVDD

IOVDD is the digital I/O power-supply voltage of the device. IOVDD is internally regulated to 1.35 V to power the digital core. The voltage level of IOVDD is independent of the analog power-supply voltage levels.

8.3.6.4 Power-On Reset (POR)

The ADC uses power-supply monitors to detect power-up and supply brownout events. Power-up or power-cycling of the IOVDD digital supply results in device reset. Power-up or power-cycling of the analog power supplies does not reset the ADC.

Figure 8-27 illustrates the digital power-on thresholds of the IOVDD and the internal CAPD voltages. When the voltages are above the respective thresholds, the ADC is released from reset. $\overline{\text{DRDY}}$ transitions high when the SPI is ready for communication. If the START pin is high, the ADC immediately begins conversions with the $\overline{\text{DRDY}}$ pin pulsing for each conversion. However, valid conversion data only occur after the power supplies and reference voltage are stabilized. The POR_FLAG bit of the STATUS register indicates the device POR. Write 1b to clear the bit in order to detect the next POR event.

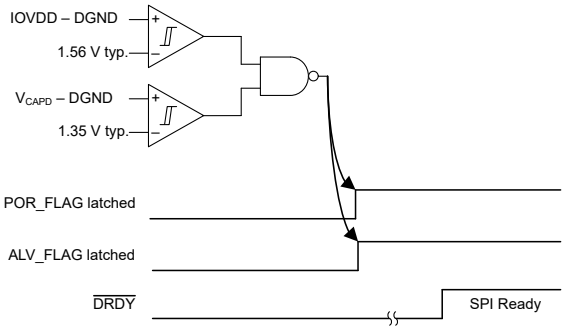


Figure 8-27. Digital Supply Threshold

Figure 8-28 shows the power-on thresholds of the analog power supplies. Four monitors are used for four analog supply voltage conditions (AVDD1 – AVSS), (AVDD1 – DGND), (AVDD2 – AVSS), and (CAPA – AVSS). Valid conversion data are available after all power supplies and the reference voltage are stabilized after power on. The ALV_FLAG bit of the STATUS register sets when any analog power voltage falls below the respective threshold. Write 1b to clear the bit to detect the next analog supply low-voltage condition. Power cycling the analog power supplies does not reset the ADC. Because a low voltage on the IOVDD supply resets the internal analog LDO (CAPA), the analog low-voltage flag (ALV_FLAG) is set when the POR_FLAG sets.

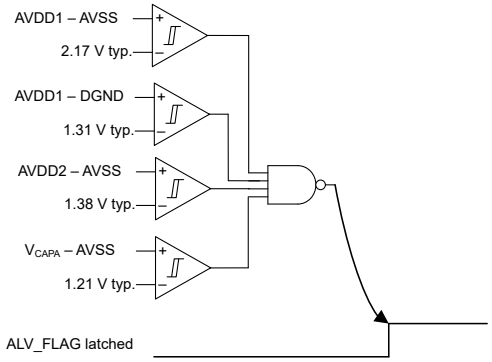


Figure 8-28. Analog Supply Threshold

8.3.6.5 CAPA and CAPD

CAPA and CAPD are the output voltages of the internal analog and digital voltage regulators. The regulators are used to reduce the supply voltage to operate internal sub-circuits at reduced power consumption. These regulators are not designed to drive external loads. CAPA is the analog regulator voltage output and is powered from AVDD2. The output voltage is 1.6 V with respect to AVSS. Bypass CAPA with a 1-µF capacitor to AVSS.

CAPD is the digital regulator voltage output, powered from IOVDD. The regulator output is 1.35 V with respect to DGND. Bypass CAPD with a 1-µF capacitor to DGND.

8.3.7 VCM Output Voltage

The VCM output is a bias voltage for the control input of the output common-mode of a fully differential amplifier (FDA). The bias voltage establishes the common-mode voltage for the ADC input signal. The VCM voltage is regulated to the mid-point of the AVDD1 – AVSS power supply. With many types of FDAs, the same common-mode voltage is provided when the common-mode control input is floated when the FDA and ADC use the same power supply. However, if the FDA and ADC power supplies have different values, bias the FDA common-mode voltage with the VCM voltage. If the VCM voltage is not used, leave the pin unconnected. The VCM output is enabled by the VCM bit of the CONFIG1 register.

8.4 Device Functional Modes

8.4.1 Speed Modes

The ADC offers power-scalable speed modes that allow optimization of signal bandwidth, data rate, and power consumption. For overlapping data rate values among the speed modes, using a higher value of OSR improves the dynamic range performance. Max-speed mode provides the highest data rate and signal bandwidth, and low-speed mode minimizes power consumption for applications not requiring large signal bandwidths. The ADC clock frequency must be adapted by the user according to the speed mode. See the *Clock Operation* section for the clock frequencies and clock divider options. The speed mode is selected by the SPEED_MODE[1:0] bits of the CONFIG2 register.

8.4.2 Idle Mode

When conversions are stopped, the ADC offers the option to remain in a full-powered idle mode or to enter a low-power standby mode. In idle mode, the analog circuit remains fully operational, including sampling of the signal and voltage reference inputs. Only the digital filter is inactive. When conversions are restarted, the digital filter begins the conversion process. Idle mode (default) is programmed by the STBY_MODE bit of the CONFIG2 register.

8.4.3 Standby Mode

The ADC has the option of a low-power standby mode when conversions are stopped. The standby mode function is engaged automatically when enabled by the STBY_MODE bit of the CONFIG2 register. During standby, sampling of the signal and reference voltages are stopped. When conversions are restarted, sampling of the signal and reference voltages resume. When standby mode is exited, the latency time for the first conversion increases 24 f_{CLK} cycles.

8.4.4 Power-Down Mode

Power-down mode is engaged by setting the PWDN bit of the CONFIG2 register. In power-down mode, the analog and digital sections are powered off, except for a small bias current required to maintain SPI operation needed to exit power-down mode by clearing the PWDN bit. The digital LDO also remains active to maintain user register settings. Sampling of the signal and voltage reference is stopped during power-down mode. Exit power-down mode by writing 0b to the PWDN bit or by resetting the device.

8.4.5 Reset

The ADC performs an automatic reset at power-on and is also reset manually by the $\overline{\text{RESET}}$ pin or SPI operation. At reset, the control logic, digital filter, and SPI restart and the user registers reset to the default values. See Figure 6-5 for details when the ADC is available for operation after reset.

8.4.5.1 $\overline{\text{RESET}}$ Pin

The $\overline{\text{RESET}}$ pin is an active-low input. The ADC is reset by taking $\overline{\text{RESET}}$ low then back high. Because the $\overline{\text{RESET}}$ pin has an internal 20-kΩ pullup resistor, $\overline{\text{RESET}}$ can be left unconnected if not used. The $\overline{\text{RESET}}$ pin is a Schmitt-triggered input designed to reduce noise sensitivity. See Figure 6-5 for $\overline{\text{RESET}}$ pin timing and when SPI communications are available after reset. Because the ADC performs an automatic reset at power-on, manual reset is not required.

8.4.5.2 Reset by SPI Register Write

The device is reset through SPI operation by writing 01011000b to the CONTROL register. Writing any other value to this register does not result in a reset. In 4-wire SPI mode, reset takes effect at the end of the frame at the time $\overline{\text{CS}}$ is taken high. In 3-wire SPI mode, reset takes effect on the last falling edge of SCLK of the register write operation. Reset in 3-wire SPI mode requires that the SPI communication is synchronized to the host. If SPI synchronization is lost, use the pattern described in the *Reset by SPI Input Pattern* section to reset the device. Reset is validated by checking the POR_FLAG of the STATUS register.

8.4.5.3 Reset by SPI Input Pattern

The device is also reset through SPI operation by inputting a long bit pattern. The input pattern is not part of the regular command format. $\overline{CS}$ must remain low for the entire bit sequence. There are two input patterns that can reset the ADC: pattern 1 and pattern 2. Pattern 1 consists of a *minimum* 1023 consecutive ones followed by one zero. The device resets on the falling edge of SCLK when the final zero is shifted in. This pattern is used for either 3- or 4-wire SPI modes. Figure 8-29 shows a pattern 1 reset example.

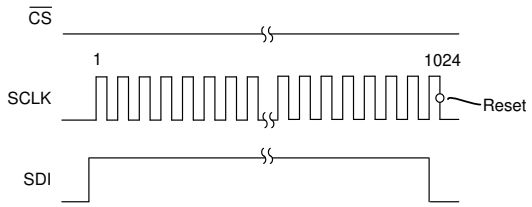


Figure 8-29. Reset Pattern 1 (3-Wire or 4-Wire SPI Mode)

Reset pattern 2 is only used with the 4-wire SPI mode. To reset, input a *minimum* of 1024 consecutive ones (no ending zero value), followed by taking $\overline{CS}$ high, at which time reset occurs. Use pattern 2 when the devices are connected in daisy-chain mode. Figure 8-30 shows a pattern 2 reset example.

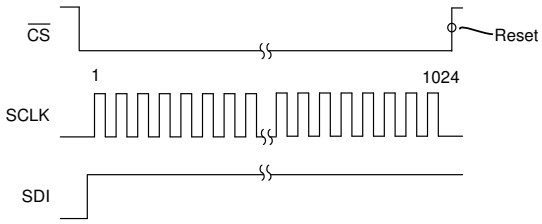


Figure 8-30. Reset Pattern 2 (4-Wire SPI Mode)

8.4.6 Synchronization

Conversions are synchronized and controlled by the START pin or, optionally, through SPI operation. If controlling conversions through SPI operation, keep the START pin low to avoid contention with the pin. Writing to any register from 04h through 0Eh causes an ongoing conversion to restart, thus resulting in loss of synchronization. Resynchronization of the ADC can be necessary in this case.

The ADC has three modes to synchronize and control conversions: *synchronized, start/stop, and one-shot* modes, each with specific functional differences. Program the desired synchronization mode with the START_MODE[1:0] bits of the CONFIG2 register. Only the start/stop and one-shot modes offer control through SPI operation.

After the ADC is synchronized, the first conversion provides fully settled data but incurs a delay (latency time) compared to the normal data period. This latency is needed to account for full settling of the digital filter and depends on the specific data rate and the filter mode (see the *Digital Filter* section for filter latency details).

8.4.6.1 Synchronized Control Mode

In synchronized control mode, the ADC converts continuously regardless if the START pin is high or low. The ADC is synchronized on the rising edge of START. When synchronized, the first $\overline{DRDY}$ falling edge is delayed to account for the filter settling time (latency time). Both a single-pulse input and a continuous-clock input equal to data rate multiples can be applied to the START pin in this mode.

The ADC synchronizes at the rising edge of START. If the time to the next rising edge of START is an *n* multiple of the conversion period, within a ±1 / f_{CLK} window, the ADC does not resynchronize (*n* = 1, 2, 3, and so on). Synchronization does not occur because the ADC conversion period is already synchronized to the period of the START signal. If the period of the applied START signal is *not* an *n* multiple of the conversion period, the ADC resynchronizes. As a result of the propagation delay of the digital filter, a phase difference exists between

the START signal and the $\overline{\text{DRDY}}$ output. Figure 8-31 shows the synchronization to the START signal when the period of START pulses is not equal to an *n* multiple of the conversion period.

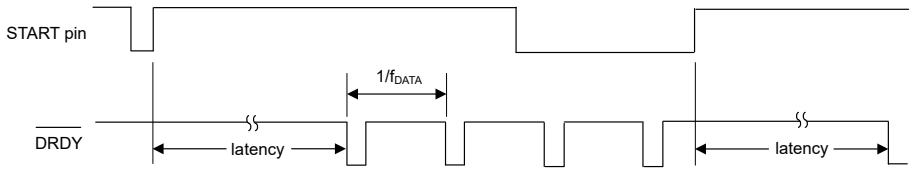


Figure 8-31. Synchronized Control Mode

8.4.6.2 Start/Stop Control Mode

Start/stop control mode is a gate-control mode used to start and stop conversions. Conversions are started by taking the START pin high or, if conversions are controlled through SPI operation, by writing 1b to the START bit of the CONTROL register.

Conversions continue until stopped by taking the START pin low, or by writing 1b to the STOP bit through SPI operation. $\overline{\text{DRDY}}$ is driven high at conversion start and is driven low when each conversion data are ready. If START is taken low or 1b is written to the STOP bit while conversions are in progress, the ongoing conversion runs to completion and then stops. (See Figure 6-6 for detailed START timing).

To restart an ongoing conversion, pulse START low to high, or write 1b to the START bit a second time. Figure 8-32 shows the START and $\overline{\text{DRDY}}$ operation. If conversions are stopped when standby mode is enabled, $\overline{\text{DRDY}}$ returns high three clock cycles after falling low, otherwise when not in standby mode $\overline{\text{DRDY}}$ remains low until being forced high at the eighth SCLK edge during conversion data readout. If data are not read, $\overline{\text{DRDY}}$ remains low and pulses high just before the next $\overline{\text{DRDY}}$ falling edge.

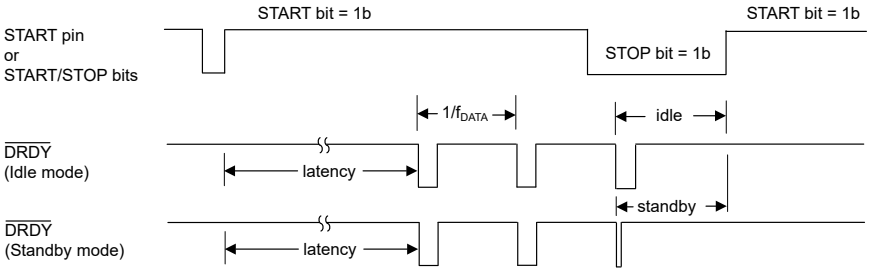


Figure 8-32. Start/Stop Control Mode

8.4.6.3 One-Shot Control Mode

One-shot control mode initiates a single conversion when START is taken high or, through SPI operation, when the START bit of the CONTROL register is set to 1b. $\overline{\text{DRDY}}$ drives high to indicate the conversion is started and drives low when the conversion is complete. Data are available for readback at that time.

Taking START low, or writing 1b to the STOP bit, does not interrupt the ongoing conversion. The STOP bit has no effect. To restart the conversion, pulse START low to high, or write 1b to the START bit a second time. Figure 8-33 illustrates the one-shot control mode operation. When standby mode is enabled, $\overline{\text{DRDY}}$ returns high three clock cycles after transitioning low, otherwise $\overline{\text{DRDY}}$ remains low until forced high at the next rising edge of START.

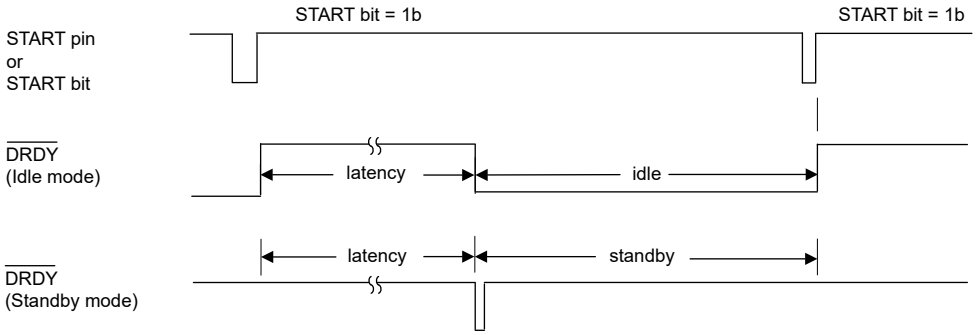


Figure 8-33. One-Shot Control Mode

8.4.7 Conversion-Start Delay Time

A programmable delay time is available to delay the start of the first conversion cycle when the START pin or START bit are asserted. This delay time allows for settling of external components, such as the voltage reference after exiting standby mode, or for additional settling time when switching the signal through an external multiplexer. After the initial delay time, subsequent conversions are not delayed. The programmable delay value adds time to the latency time value of the digital filter. See the DELAY[2:0] bits of the FILTER2 register for details.

8.4.8 Calibration

The ADS127L21 offers offset and gain calibration by the user offset and gain calibration registers. As shown in Figure 8-34, the 24-bit offset calibration value is subtracted from the conversion data before being multiplied by the 24-bit gain calibration value. Output data are rounded to the final resolution (16- or 24-bit) and clipped to +FS and –FS code values after the scaling operation.

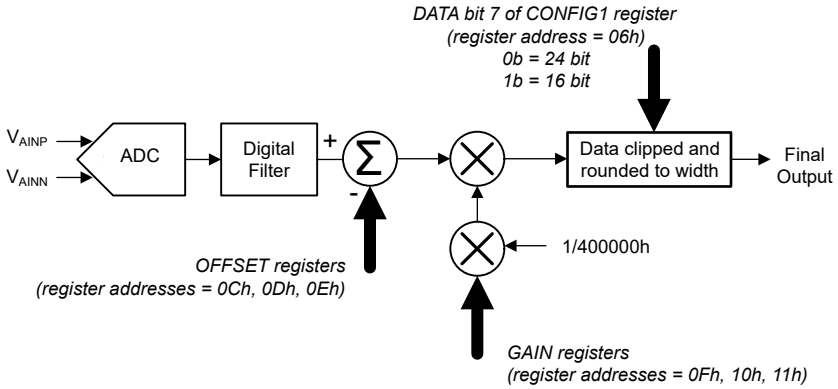


Figure 8-34. Calibration Block Diagram

Equation 20 shows how conversion data are calibrated:

$$\text{Final Output Data} = (\text{Data} - \text{OFFSET}) \times \text{GAIN} / 400000\text{h} \quad (20)$$

8.4.8.1 OFFSET2, OFFSET1, OFFSET0 Calibration Registers (Addresses 0Ch, 0Dh, 0Eh)

The offset calibration value is a 24-bit value consisting of three 8-bit registers coded in two's-complement format. The offset value is subtracted from the conversion data. Register 0Ch is the most-significant byte, register 0Dh is the middle byte, and register 0Eh is the least-significant byte. If the ADC is programmed to provide 16-bit resolution, the least-significant offset byte provides sub-LSB offset accuracy. Table 8-13 shows example offset calibration values.

Table 8-13. OFFSET Register Values

OFFSET REGISTER VALUE	OFFSET APPLIED
000010h	–16 LSB
000001h	–1 LSB
FFFFFFh	1 LSB
FFFFF0h	16 LSB

8.4.8.2 GAIN2, GAIN1, GAIN0 Calibration Registers (Addresses 0Fh, 10h, 11h)

The gain calibration value is a 24-bit value consisting of three 8-bit registers coded in straight-binary format and normalized to unity gain at 400000h. For example, to correct a gain error greater than 1, the gain calibration value is less than 400000h. Register 0Fh is the most-significant byte, register 10h is the middle byte, and register 11h is the least-significant byte. Table 8-14 shows example gain calibration values.

Table 8-14. GAIN Register Values

GAIN REGISTER VALUE	GAIN APPLIED
433333h	1.05
400000h	1
3CCCCCh	0.95

8.4.8.3 Calibration Procedure

The recommended calibration procedure is as follows:

1. Preset the offset and gain calibration registers to 000000h and 400000h, respectively.
2. Perform offset calibration by shorting the ADC inputs, or short the inputs at the system level to include the offset error of the external amplifier stages. Acquire conversion data and write the average value of the data to the offset calibration registers. Averaging the data reduces conversion noise to improve calibration accuracy.
3. Perform gain calibration by applying a calibration signal to the ADC input or at the system level to include the gain error of the external buffer stages. For the standard input range mode, choose the calibration voltage to be less than the full-scale input range to avoid clipping the output code. Clipped output codes result in inaccurate calibration. For example, use a 3.9-V calibration signal with V_{REF} = 4.096 V. When operating in the extended range mode, the calibration signal can be equal to V_{REF} without causing clipped output codes. Acquire conversion data and average the results. Use Equation 21 to calculate the gain calibration value.

$$\text{Gain Calibration Value} = (\text{expected output code} / \text{actual output code}) \cdot 400000\text{h} \quad (21)$$

For example, the expected output code of a 3.9-V calibration voltage using a 4.096-V reference voltage is: (3.9 V / 4.096 V) · 7FFFFFh = 79E000h.

8.5 Programming

8.5.1 Serial Interface (SPI)

The serial interface reads conversion data, configures device registers, and controls ADC conversions. The optional CRC mode validates error-free data transmission between the host and ADC. Additional CRCs validate the register map contents after the register data are loaded.

The serial interface consists of four signals: $\overline{CS}$, SCLK, SDI, and SDO/$\overline{DRDY}$. The interface operates in peripheral mode (passive) where SCLK is driven by the host. The interface is compatible to SPI mode 1 (CPOL = 0 and CPHA = 1). In SPI mode 1, SCLK idles low and data are updated on SCLK rising edges and are read on SCLK falling edges. The interface supports full-duplex operation, meaning input data and output data can be transmitted simultaneously. The interface also supports daisy-chain connection of multiple ADCs to simplify the SPI connection.

8.5.1.1 Chip Select ($\overline{CS}$)

$\overline{CS}$ is an active-low input that enables the interface for communication. The communication frame is started by taking $\overline{CS}$ low and is ended by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device ends the frame by interpreting the last 16 bits of input data (24 bits in CRC mode) regardless of the total number of bits shifted in. When $\overline{CS}$ is high, the SPI interface resets, commands are blocked, and SDO/$\overline{DRDY}$ enters a high-impedance state. $\overline{DRDY}$ is an active output regardless of the state of $\overline{CS}$. Tie $\overline{CS}$ low to operate the interface in 3-wire SPI mode.

8.5.1.2 Serial Clock (SCLK)

SCLK is the serial clock input used to shift data into and out of the ADC. Output data are updated on the rising edge of SCLK and input data are latched on the falling edge of SCLK. SCLK is a Schmitt-triggered input designed to increase noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. A series-termination resistor at the SCLK driver often reduces ringing.

8.5.1.3 Serial Data Input (SDI)

SDI is the serial interface data input. SDI is used to input data to the device. Input data are latched on the falling edge of SCLK. SDI can be idled high or low when not active.

8.5.1.4 Serial Data Output/Data Ready (SDO/$\overline{DRDY}$)

SDO/$\overline{DRDY}$ is a dual-function output pin. This pin is programmable to provide output data only, or to provide output data and the data-ready indication. The dual-function mode multiplexes output data and data-ready operations on a single pin. Output data are updated on the rising edge of SCLK. The SDO/$\overline{DRDY}$ pin is in a high-Z state when $\overline{CS}$ is high. See the *SDO/$\overline{DRDY}$* section for details of dual-function operation. The DATA_MODE[1:0] bits of the FILTER3 register programs the mode.

8.5.1.5 SPI Frame

Communication through the serial interface is based on the concept of frames. A frame consists of a prescribed number of SCLKs required to shift in or shift out data. A frame is started by taking $\overline{CS}$ low and is ended by taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the device interprets the last 16 bits (or 24 bits in CRC mode) of input data regardless of the amount of data shifted into the device. In typical use, the input frame is sized to match the output frame by padding the frame with leading zeros if needed. However, if not transmitting and receiving data in full-duplex mode, the input data frame can be the minimum size of 16 bits (or 24 bits in CRC mode). The output frame size, as given in Table 8-15, depends on the programmed data resolution (16 or 24 bits) and the optional STATUS header and CRC bytes. After the ADC is powered up or reset, the default output frame size is 24 bits. In 3-wire SPI mode, the input frame must match the size of the output frame for the SPI to remain synchronized.

Table 8-15. Output Frame Size

RESOLUTION (Bits)	STATUS BYTE	CRC BYTE	FRAME SIZE (Bits)
24	No	No	24
24	No	Yes	32
24	Yes	No	32
24	Yes	Yes	40
16	No	No	16
16	No	Yes	24
16	Yes	No	24
16	Yes	Yes	32

8.5.1.6 Full-Duplex Operation

The serial interface supports full-duplex operation. Full-duplex operation allows the simultaneous transmission and reception of data in one frame. For example, the register read command for the next register can be input at the same time that data of the previously addressed register are output, which doubles the throughput for reading registers. An example of full-duplex operation is illustrated in Figure 8-36.

8.5.1.7 Device Commands

Commands are used to read and write register data. The register map of Table 8-19 consists of a series of one-byte registers, accessible by read and write operations. The minimum frame length of the input command sequence is two bytes (three bytes in CRC mode). If desired, pad the input command sequence with leading zeros to match the length of the output data frame. In CRC mode, the device interprets the two bytes immediately preceding the CRC byte at the end of the frame. Table 8-16 shows the ADS127L21 device commands.

Table 8-16. SPI Commands

DESCRIPTION	BYTE1	BYTE2	BYTE 3 (Optional CRC Byte)
No operation	00h	00h	D7h
Read register command	40h + address [3:0]	Don't care	CRC of byte 1 and byte 2
Write register command	80h + address [3:0]	Register data	CRC of byte 1 and byte 2

There are extended-length bit patterns that are different from the standard command length. These patterns reset the ADC and the SPI frame in three-wire SPI operation. These patterns are explained in the *Reset by SPI Input Pattern* and *3-Wire SPI Mode* sections.

8.5.1.7.1 No-Operation

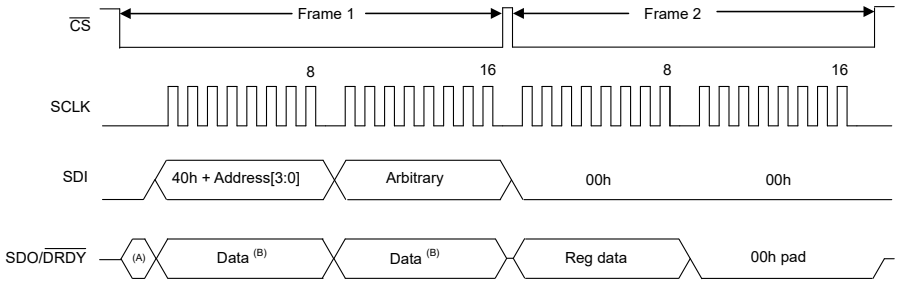
The no-operation command bytes are <00h 00h>. Use these bytes when no command is desired, such as reading conversion data. If the SPI CRC is enabled, the CRC byte is required (byte 3), which is always D7h for bytes <00h 00h>. SDI can be held low during data readback, but in CRC mode the SPI_ERR flag is set, which blocks future register write operations. The SPI_ERR flag can be ignored while reading conversion data until a register write operation is desired. At that point, clear the SPI_ERR flag of the STATUS register by writing 1b.

8.5.1.7.2 Read Register Command

The read register command reads register data. The command follows an off-frame protocol where the read command is sent in one frame and the ADC responds with register data in the next frame. The first byte of the command is the base command value (40h) added to the 4-bit register address. The value of the second command byte is arbitrary, but is used together with the first byte for the CRC. The response to registers outside the valid address range is 00h. The register data format is most-significant-bit first.

Figure 8-35 illustrates an example of reading register data using the 16-bit output frame size. Frame 1 is the command frame and frame 2 is the data response frame. The frames are delimited by taking $\overline{CS}$ high. The data response frame is padded with 00h after the register data byte to fill the 16-bit frame. If desired, shorten the data response frame after the data byte by taking $\overline{CS}$ high.

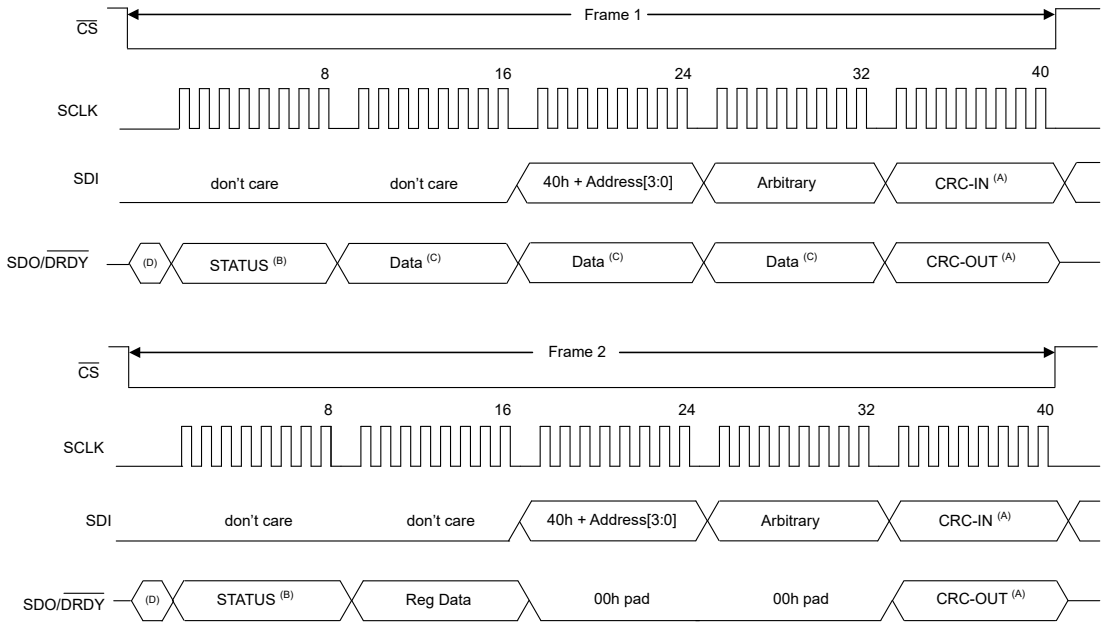
If operating in full-duplex mode (such as a simultaneous read of 24-bit conversion data during the input of the register read command), pad the command frame with a leading 00h value to match the length of the data response frame. When configuring multiple registers, full-duplex operation is optional to double the throughput of the read register operations by inputting the next read register command during the data response frame of the previous register.



A. Previous state of SDO/DRDY before the first SCLK.
B. Data are either 16 bits of conversion data, or if register data, the data field is the register data byte + 00h.

Figure 8-35. Read Register Data, Minimum 16-Bit Frame Size

Figure 8-36 shows an example of the read register operation using the maximum 40-bit frame size in full-duplex operation. In frame 1, conversion data are output simultaneous with the input of the read register command (if the previous frame was not a read register command). The input command is padded with two don't care bytes in order to match the length of the output data frame. The padded input bytes are excluded from the CRC-IN code calculation. Frame 2 shows the input of the next read register command concurrent with the output of the previous register data. Zeros are padded after the register data to place CRC-OUT in the same location as in the conversion data output frame. The CRC-OUT code includes all preceding bytes within the data output frame. The SPI_ERR bit of the STATUS header indicates if an SPI CRC error occurred and whether the read register command is accepted.



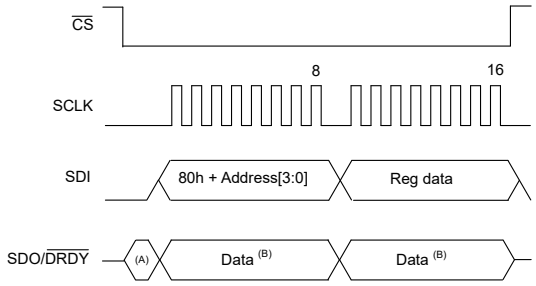
A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS byte. If STATUS is disabled, the frame shortens by one byte.
C. Depending on the previous operation, the data field is either conversion data or register data + two 00h pad bytes.
D. Previous state of SDO/DRDY before the first SCLK.

Figure 8-36. Read Register Data, Maximum 40-Bit Frame Size

8.5.1.7.3 Write Register Command

The write register command writes register data. The write register operation is performed in a single frame. The first byte of the command is the base value (80h) added to the 4-bit register address. The second byte of the command is the register data. Writing to registers outside the valid address range is ignored.

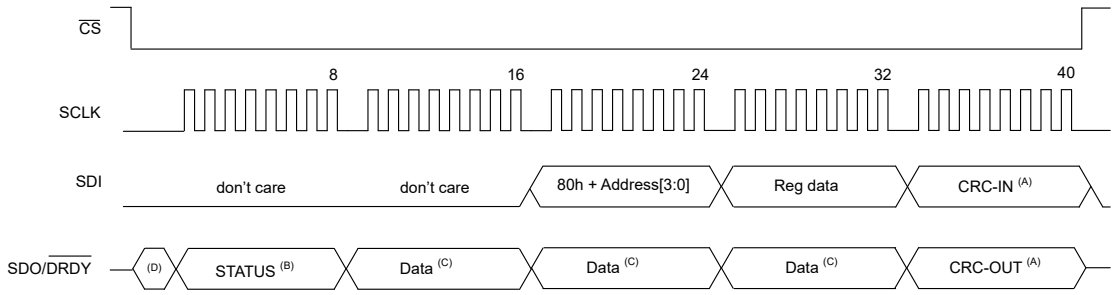
Figure 8-37 shows an example of a register write operation using the 16-bit frame size. If operating in full-duplex mode (simultaneous reading of 24-bit conversion data during the input of the register write command), include one or more leading pad bytes to the input data to match the length of the output frame. When configuring a series of registers (when conversion data are ignored), the minimum 16-bit frame size improves throughput.



A. Previous state of SDO/DRDY before the first SCLK.
B. Data are either conversion data, or if register data, the field is register data byte + one 00h pad byte.

Figure 8-37. Write Register Data, Minimum 16-Bit Frame Size

Figure 8-38 shows an example of a write register operation using the maximum 40-bit frame size. Full-duplex operation is also illustrated to show simultaneous input of the command and output of conversion data. The input frame is prefixed with two *don't care* bytes to match the output frame so all conversion data bytes are transmitted. Successful write operations are verified by reading back the register data, or by checking the SPI_ERR bit of the STATUS byte for input byte CRC errors. If an input SPI CRC error occurred, the SPI_ERR is set and further register write operations are blocked (except for the STATUS register) until reset by writing 1b to the same SPI_ERR bit.



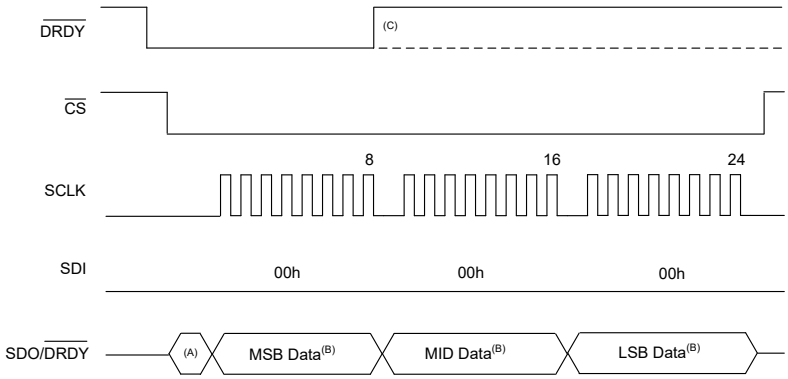
A. Optional CRC byte. If CRC is disabled, the frame shortens by one byte.
B. Optional STATUS byte. If STATUS is disabled, the frame shortens by one byte.
C. The data field is either 24 bits of conversion data, or if the read register command was sent in the prior frame, register data byte + two 00h pad bytes.
D. Previous state of SDO/DRDY before the first SCLK.

Figure 8-38. Write Register Data, Maximum 40-Bit Frame Size

8.5.1.8 Read Conversion Data

Conversion data are read by taking $\overline{CS}$ low and by applying SCLK to shift out the data directly (no command is used). Conversion data are buffered, which allows data to be read up to one f_{MOD} clock cycle before the next $\overline{DRDY}$ falling edge. Conversion data can be read multiple times until the next conversion data are ready. If the register read command was sent in the previous frame then register data replaces the conversion data.

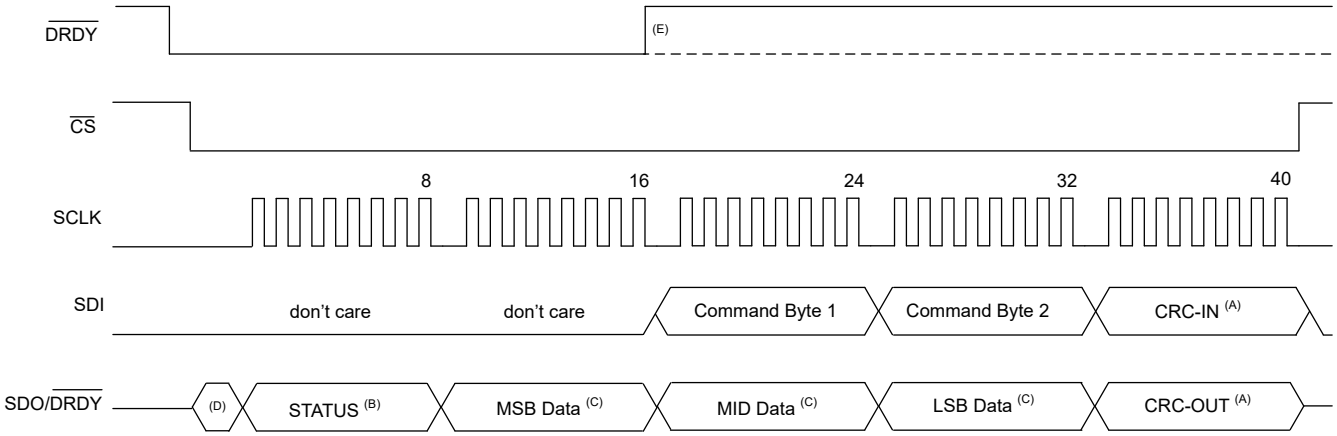
Figure 8-39 shows an example of reading 24-bit conversion data with the STATUS and CRC bytes disabled.



A. Before the first SCLK, SDO/DRDY is the previous state when SDO_MODE = 0b. Otherwise, SDO/DRDY follows DRDY.
B. The data field is two bytes (16-bit resolution) or three bytes (24-bit resolution).
C. In synchronized and start/stop control modes, DRDY returns high at the eighth SCLK falling edge. In one-shot control mode, DRDY remains low until a new conversion is started.

Figure 8-39. Conversion Data Read, Short Format

Figure 8-40 is an example of the long-format read data operation, which includes the STATUS byte and the CRC byte. This example also shows the optional use of a full-duplex transmission when a register command is input at the same time the conversion data are output. If no input command is desired, the input bytes are 00h, 00h, and D7h. The output CRC (CRC-OUT) code computation includes the STATUS byte. If the conversion data readback is stopped after the eighth SCLK of the MSB data, DRDY returns high and the DRDY bit of the STATUS byte goes low to indicate a data-read attempt.



A. Optional CRC byte. If the CRC is disabled, the frame shortens by one byte.
B. Optional STATUS header. If STATUS is disabled, the frame shortens by one byte.
C. Data are two bytes (16-bit resolution) or three bytes (24-bit resolution).
D. If the SDO_MODE bit = 0, the previous state of SDO/DRDY remains until SCLK begins. Otherwise, SDO/DRDY follows DRDY.
E. In synchronized and start/stop control modes, DRDY returns high at the 16th SCLK falling edge (eighth bit of the MS data byte). In one-shot control mode, DRDY stays low until a new conversion is started.

Figure 8-40. Conversion Data Read, Long Format

In normal operation, reading of conversion data ready is synchronized to the DRDY signal, but data can be read asynchronously to DRDY. However, when conversion data are read close to the DRDY falling edge, there is uncertainty whether previous data or new data are output. If the SCLK shift operation starts at least one f_{MOD} clock cycle before the DRDY falling edge, then old data are provided. If the shift operation starts at least one f_{MOD} clock cycle *after the* DRDY falling edge, then new data are output. The DRDY bit of the STATUS byte indicates if the data are old (previously read data) or new.

8.5.1.8.1 Conversion Data

Conversion data are coded in two's-complement format, MSB first (sign bit), with resolution programmable to 24 bits or 16 bits. The 24-bit or 16-bit resolution is programmed by the DATA bit of the CONFIG1 register. The SNR of 16-bit data is limited to 98.1 dB as a result of 16-bit quantization noise. Table 8-17 shows the output code for standard and extended input ranges for 24-bit resolution mode. The conversion data clips to positive and negative full-scale code values when the input signal exceeds the respective positive and negative full-scale values.

Table 8-17. 24-Bit Output Data Format

DIFFERENTIAL INPUT VOLTAGE (V)(1)	24-BIT OUTPUT DATA(2)	
	STANDARD RANGE	EXTENDED RANGE
$1.25 \cdot k \cdot V_{REF} \cdot (2^{23} - 1) / 2^{23}$	7FFFFFh	7FFFFFh
$k \cdot V_{REF} \cdot (2^{23} - 1) / 2^{23}$	7FFFFFh	666666h
$k \cdot V_{REF} / 2^{23}$	000001h	000001h
0	000000h	000000h
$-k \cdot V_{REF} / 2^{23}$	FFFFFFh	FFFFFFh
$-k \cdot V_{REF}$	800000h	99999Ah
$-1.25 \cdot k \cdot V_{REF}$	800000h	800000h

(1) k = 1x or 2x input range option.
(2) Ideal output data excluding offset and gain errors, and reduced resolution for OSR values < 32.

8.5.1.8.2 Data Ready

There are several methods available to determine when conversion data are ready for readback.

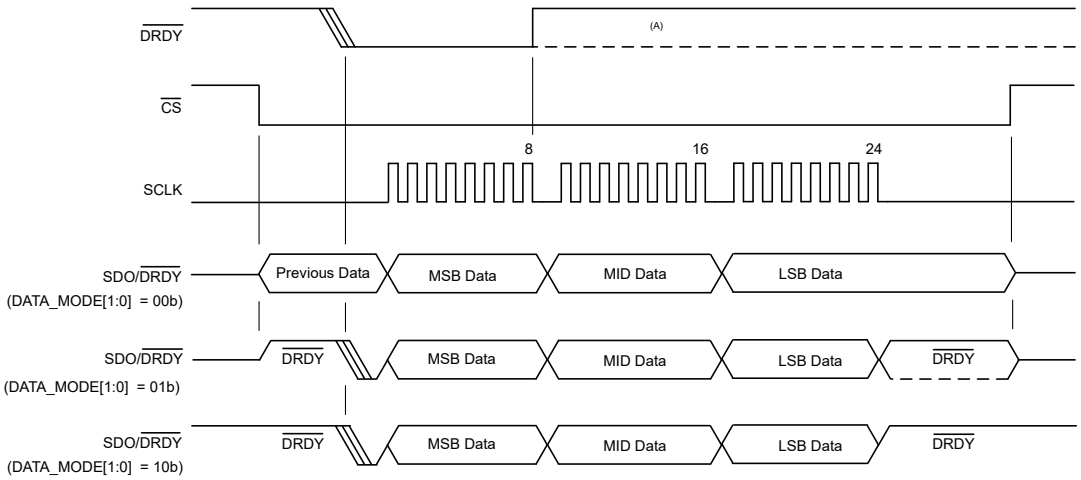
1. Hardware: Monitor the $\overline{\text{DRDY}}$ or the SDO/$\overline{\text{DRDY}}$ pin
2. Software: Monitor the DRDY bit of the STATUS byte
3. Clock count: Count the number of ADC clocks to predict when data are ready

8.5.1.8.2.1 $\overline{\text{DRDY}}$

$\overline{\text{DRDY}}$ is the data-ready output signal. $\overline{\text{DRDY}}$ drives high when conversions are started or resynchronized, and drives low when conversion data are ready. $\overline{\text{DRDY}}$ is driven back high at the eighth SCLK during conversion data read. This behavior applies to the synchronized and the start/stop control modes. In one-shot control mode, $\overline{\text{DRDY}}$ stays low during conversion data read. If the ADC is programmed to enter standby mode (STBY_MODE bit = 1b), $\overline{\text{DRDY}}$ is driven back high three f_{CLK} cycles after transitioning low. If conversion data are not read, $\overline{\text{DRDY}}$ pulses high just prior to the next falling edge. See the *Synchronization* section for details of the $\overline{\text{DRDY}}$ operation for each of the conversion control modes. $\overline{\text{DRDY}}$ is an active output whether $\overline{\text{CS}}$ is high or low.

8.5.1.8.2.2 SDO/$\overline{\text{DRDY}}$

SDO/$\overline{\text{DRDY}}$ is a dual-function output pin that can be programmed to automatically change modes from data ready (when not reading data) to data output mode (when reading data). In this mode, the pin replaces the function of the $\overline{\text{DRDY}}$ pin to conserve the number of SPI I/O lines. When programmed to the dual-function mode and when $\overline{\text{CS}}$ is low, SDO/$\overline{\text{DRDY}}$ mirrors the $\overline{\text{DRDY}}$ pin until the first rising edge of SCLK, at which time the pin changes mode to provide data output. When the data-read operation is complete (24th falling edge of SCLK, or 40th edge if the CRC and STATUS bytes are included), the pin reverts back to mirroring $\overline{\text{DRDY}}$. The DATA_MODE[1:0] bits = 01b programs the dual-function mode. The 10b setting also operates the dual-function mode, but maintains SDO/$\overline{\text{DRDY}}$ as an active output when $\overline{\text{CS}}$ is high. Figure 8-41 illustrates the SDO/$\overline{\text{DRDY}}$ operation.



A. In synchronized and start/stop control modes, $\overline{DRDY}$ returns high at the eighth SCLK falling edge (eighth bit of MSB data). In one-shot control mode, $\overline{DRDY}$ stays low until a new conversion is started.

Figure 8-41. SDO/$\overline{DRDY}$ and $\overline{DRDY}$ Function

8.5.1.8.2.3 DRDY Bit

The software method of determining data ready is by polling the DRDY bit (bit 0 of the STATUS byte). When DRDY = 1b, the data are new from the last data read operation, otherwise the data supplied are the previous data. After data are read, the bit stays cleared until the next conversion data are ready. To avoid missing data, poll the bit at least as often as the output data rate.

8.5.1.8.2.4 Clock Counting

Another method to determine if data are ready is to count clock cycles. This method is only possible when using an external clock because the internal clock oscillator is not observable. After synchronization or conversion start, the number of clock cycles for the first conversion is larger compared to the normal conversion period. The clock cycles of the first conversion is equivalent to the latency time, as listed in the *Digital Filter* section.

8.5.1.8.3 STATUS Byte

STATUS is an optional byte prefixed to the conversion data. See Table 8-23 for the STATUS byte field descriptions. The STATUS byte is enabled by setting the STATUS bit of the CONFIG3 register. The STATUS byte sent with conversion data has the same content as the STATUS register.

8.5.1.9 Daisy-Chain Operation

In simultaneous-sampling systems with multiple ADCs, a daisy-chain string connection reduces the number of SPI I/Os to the host controller. A daisy-chain connection links the SPI output of one device to the SPI input of the next device, resulting in the chained devices appearing as a single logical device to the host controller. There is no special programming required for daisy-chain operation, simply apply additional shift clocks to access all devices in the chain. For simplified operation, program the same SPI frame size for each device (for example, when enabling the CRC option of all devices, thus producing a 32-bit frame size).

Figure 8-42 illustrates four devices connected in a daisy-chain configuration. The SDI of ADS127L21 (1) connects to the host SPI data out, and SDO/$\overline{DRDY}$ of ADS127L21 (4) connects to the host SPI data input. The shift operation is simultaneous for all devices in the chain. After each ADC completes the conversion data shifting, the shifted-in data of SDI appears on SDO/$\overline{DRDY}$ to drive the SDI of the next device in the chain. The shift operation continues until the last device in the chain is reached. The SPI frame ends when $\overline{CS}$ is taken high, at which time the data shifted into each device is interpreted. The SDO/$\overline{DRDY}$ pin must be programmed to data-output-only mode.

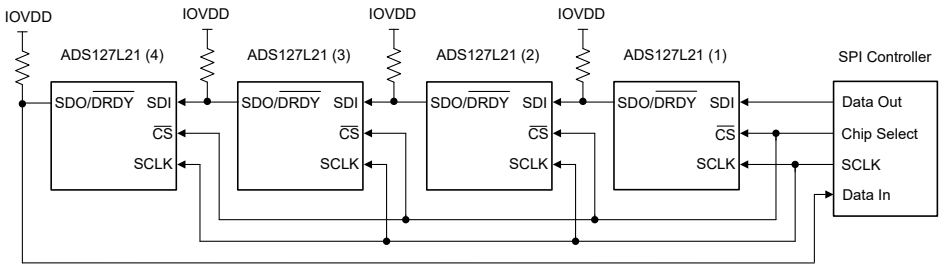


Figure 8-42. Daisy-Chain Connection

Figure 8-43 shows the 24-bit frame size of each device used at initial communication after device power up.

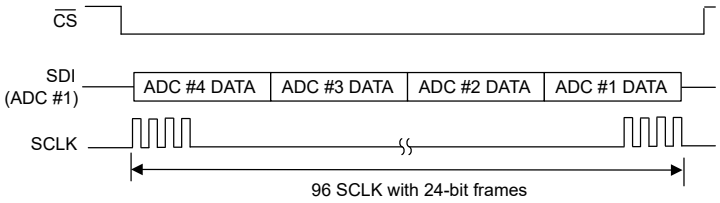
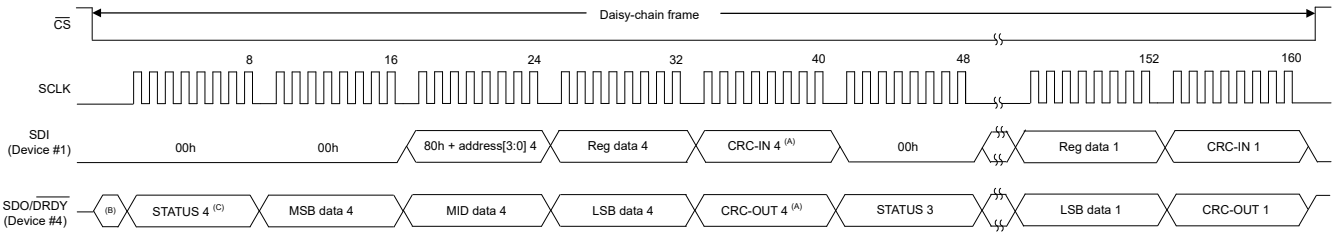


Figure 8-43. 24-Bit Data Input Sequence

To input data, the host first shifts in the data intended for the last device in the chain. The number of input bytes for each ADC is sized to match the output frame size. The default frame size is 24 bits, so initially each ADC requires three bytes by prefixing a pad byte in front of the two command bytes. The input data of ADC (4) is first, followed by the input data of ADC (3), and so forth.

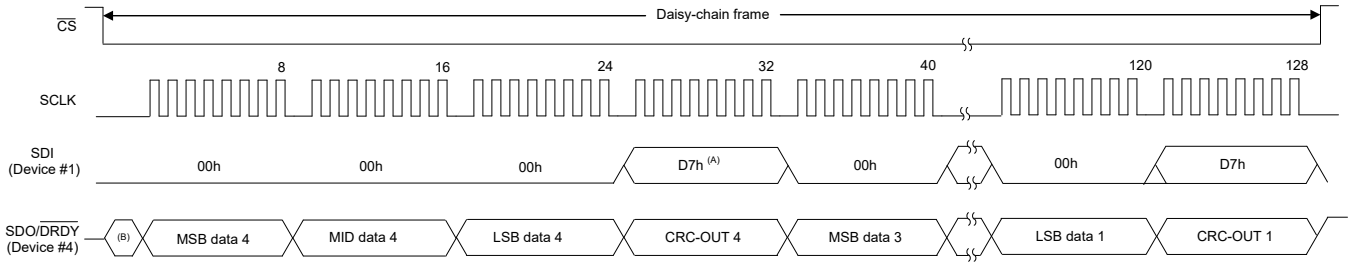
Figure 8-44 shows the detailed input data sequence for the daisy-chain write register operation of Figure 8-42. 40-bit frames for each ADC are shown (24-bits of data, with the STATUS and CRC bytes enabled). Command operations can be different for each ADC. The read register operation requires a second frame operation to read out register data.



A. Optional CRC byte. If CRC is disabled, the individual frames shorten by one byte.
B. Previous state of SDO/DRDY before SCLK is applied.
C. Optional STATUS byte. If STATUS is disabled, the individual frames shorten by one byte.

Figure 8-44. Write Register Data in Daisy-Chain Connection

Figure 8-45 illustrates the clock sequence to read conversion data from the device connection provided in Figure 8-42. This example illustrates a 32-bit output frame (24-bits of data, with the CRC byte enabled). The output data of ADC (4) is first in the sequence, followed by the data of ADC (3), and so on. The total number of clocks required to shift out the data is given by the number of bits per frame multiplied by the number of devices in the chain. In this example, 32-bit output frames × four devices result in 128 total clocks.



A. Optional CRC byte. If CRC is disabled, the individual frames shorten by one byte.
B. Previous state of SDO/$\overline{DRDY}$ before SCLK is applied.

Figure 8-45. Read Conversion Data in Daisy-Chain Connection

As shown in Equation 22, the maximum number of devices connected in daisy-chain configuration is limited by the SCLK signal frequency, data rate, and number of bits per frame. The same limitation applies to parallel-connected SPI because the data from each ADC is also read in series.

$$\text{Maximum devices in a chain} = \lfloor f_{SCLK} / (f_{DATA} \cdot \text{bits per frame}) \rfloor \quad (22)$$

For example, if f_{SCLK} = 20 MHz, f_{DATA} = 100 kSPS, and 32-bit frames are used, the maximum number of daisy-chain connected devices is the floor of: $\lfloor 20\ \text{MHz} / (100\ \text{kHz} \cdot 32) \rfloor = 6$.

8.5.1.10 3-Wire SPI Mode

The ADC has the option of 3-wire SPI operation by grounding $\overline{CS}$. 3-wire mode is engaged by grounding $\overline{CS}$ at power up or after reset. 3-wire SPI mode is indicated by bit 7 (CS_MODE) of the STATUS register. The device changes to 4-wire SPI mode when $\overline{CS}$ is taken high.

Because $\overline{CS}$ no longer controls the frame timing in 3-wire mode, SCLKs are counted by the ADC to determine the beginning and ending of a frame. The number of SCLK bits must be controlled by the host and must match the size of the output frame. The number of bits per frame depends on the device configuration. The size of the output frame is given in Table 8-15. Because frame timing is determined by the number of SCLKs, avoid inadvertent SCLK transitions, such as those occurring at power up.

3-wire SPI mode supports the same command format and clocking as 4-wire mode, except there is no $\overline{CS}$ toggling. Except for read/write operations of the programmable filter coefficients, where 10 f_{CLK} cycle delay is required between frames, no wait time between frames is required for the remaining registers.

8.5.1.10.1 3-Wire SPI Mode Frame Reset

In 3-wire SPI mode, an unintended SCLK transition can misalign the frame, resulting in loss of SPI synchronization. As shown in Figure 8-46, the SPI is resynchronized by sending an SPI reset pattern. The reset pattern is a minimum of 63 consecutive 1s followed by one 0 at the 64th SCLK. The 65th SCLK starts a new SPI frame. Optionally, the ADC can be completely reset by toggling $\overline{RESET}$ or by the reset pattern described in the *Reset by SPI Input Pattern* section.

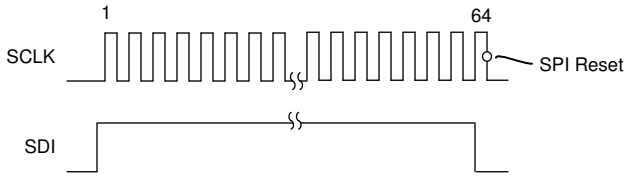


Figure 8-46. 3-Wire Mode SPI Reset Pattern

8.5.1.11 SPI CRC

The SPI cyclic redundancy check (CRC) is an SPI check code used to detect transmission errors to and from the host controller. An input CRC byte is transmitted with the input data on SDI by the host and a CRC byte is transmitted with the output data on SDO/$\overline{\text{DRDY}}$ by the ADC. The SPI CRC error check is enabled by the SPI_CRC bit of the CONFIG3 register.

The CRC code is calculated by the host on the two command bytes. Any input bytes padded to the start of the frame are not included in the CRC calculation. The ADC checks the input command CRC code against an internal code calculated over the two input command bytes. If the CRC codes do not match, the command is not executed and the SPI_ERR bit is set in the STATUS byte. Register write operations are blocked except to the STATUS register to allow clearing the SPI CRC error by writing 1b to the SPI_ERR bit. Register read operations are not blocked unless an SPI_CRC error is detected in the SPI frame of a register read command.

The number of bytes used to calculate the output CRC code depends on the amount of data bytes transmitted in the frame. All data bytes that precede the output CRC code are used in the CRC calculation. Table 8-18 shows the number of bytes used for the output CRC calculation.

Table 8-18. Byte Count of Output CRC Code

BYTE COUNT	BYTE FIELD DESCRIPTION
2	16 bits of conversion data
2	One byte of register data + 00h pad byte
3	16 bits of conversion data + STATUS byte
3	24 bits of conversion data
3	One byte of register data + two 00h pad bytes
4	24 bits of conversion data + STATUS byte
4	One byte of register data + three 00h pad bytes

The CRC value is the 8-bit or 16-bit remainder of a bitwise exclusive-OR (XOR) operation of the variable length argument with the CRC polynomial. The ADS127L21 uses 8-bit and 16-bit CRC lengths depending on the CRC function. An 8-bit CRC is used for SPI, main program memory, and IIR filter coefficients. The 8-bit CRC is based on the CRC-8-ATM (HEC) polynomial: $X^8 + X^2 + X^1 + 1$. The nine coefficients of the polynomial are: 1 00000111.

A 16-bit CRC is used exclusively for the 128 FIR filter coefficients. The 16-bit CRC is based on the CRC-16-IBM polynomial: $X^{16} + X^{15} + X^2 + 1$. The 17 coefficients are 1 10000000 00000101.

The following procedure computes the CRC value:

1. Left shift the initial data value by eight bits (16 bits for the 16-bit CRC) by appending 0s in the LSB, creating a new data value.
2. Perform an initial XOR to the MSB of the new data value from step 1 with FFh (FFFFh for the 16-bit CRC).
3. Align the MSB of the CRC polynomial to the left-most, logic 1 of the data.
4. The bits of the data value that are not in alignment with the CRC polynomial drop down and append to the right of the new XOR result. XOR the data value with the aligned CRC polynomial. The XOR operation creates a new, shorter-length value.
5. If the XOR result is less than or equal to the 8-bit or 16-bit CRC length, the procedure ends, yielding an 8-bit or 16-bit CRC code result. Otherwise, continue with the XOR operation at step 3 using the current XOR result. The number of loop iterations depend on the value of the initial data.

8.5.2 Register Memory CRC

CRCs are used to detect unintended changes in the user register memory. The register memory consists of three spaces with corresponding CRC values: the main program memory, the FIR filter coefficient memory, and the IIR filter coefficient memory. Error flags indicate CRC errors in the three spaces (see the STATUS2 register). The flags are ORed to set the global register map CRC error flag (CRC_ERR) of the STATUS1 register. The CRC function is enabled by the REG_CRC bit of the CONFIG3 register.

8.5.2.1 Main Program Memory CRC

The main program memory CRC is calculated over register addresses 00h to 11h, excluding addresses 02h, 03h, and 04h (STATUS1, STATUS2, and CONTROL registers) using the 8-bit CRC polynomial shown in the *SPI CRC* section. Write the CRC value to the MAIN_CRC register whenever the program memory is changed. The ADC compares the value to an internal calculation. If the values do not match, the M_CRC_ERR bit in the STATUS2 register is set. This error is ORed with the other CRC memory errors and is shown in the global CRC_ERR of the STATUS1 register. If the M_CRC_ERR is set, check the memory contents and update the CRC value. Allow a delay for the ADC to compute the internal CRC then write 1b to the bit to clear. The CRC error check is enabled by the REG_CRC bit of the CONFIG3 register.

Because the REV_ID can change during device production without notice, read the contents of the REV_ID register when calculating the CRC value.

8.5.2.2 FIR Filter Coefficient CRC

The FIR filter coefficient CRC is used to validate FIR coefficient memory. The FIR CRC value is calculated over the 128, 32-bit FIR coefficients, including zero-valued ending coefficients. A 16-bit CRC polynomial is used for the FIR memory (see the *SPI CRC* section for details). After the FIR coefficients are loaded to the ADC, write the 16-bit CRC value to the two, eight-bit FIR CRC registers (see the FIR_CRC1 and FIR_CRC0 registers). The ADC compares the CRC value to an internal calculation. If the values do not match, the F_CRC_ERR bit in the STATUS2 register is set. The bit is ORed with the other CRC error flags to set the global CRC_ERR bit of the STATUS1 register. If the error flag is set, check the FIR coefficient contents and update the CRC value then disable and re-enable the REG_CRC bit to clear the bit. The FIR coefficient CRC is disabled if the FIR3 filter is disabled by the FIR3_DIS bit of the FILTER2 register.

8.5.2.3 IIR Filter Coefficient CRC

The IIR filter coefficient CRC validates the IIR coefficient memory. The IIR CRC value is calculated over the 25, 32-bit IIR coefficients, using the 8-bit CRC polynomial; see the *SPI CRC* section. After the IIR coefficients are loaded to the ADC, write the 8-bit CRC value to the IIR_CRC register. The ADC compares the CRC value to an internal calculation. If the values do not match, the I_CRC_ERR bit of the STATUS2 register is set, which is logically ORed with the other CRC error flags to set the global CRC_ERR bit of the STATUS1 register. If the error bit is set, check the IIR coefficient contents and update the CRC value then disable and re-enable the REG_CRC bit to clear the bit. The IIR coefficient CRC is disabled if the IIR filter is disabled by the IIR_DIS bit of the FILTER2 register.

8.6 Registers

Table 8-19 shows the ADS127L21 register map. Register data are read or written one register byte at a time for each SPI operation. The FIR_BANK and IIR_BANK registers use a single address to read or write filter coefficients. Writing to any register address greater than the CONTROL register (address = 04h) results in a conversion restart and loss of synchronization. If conversions are stopped (START pin low or STOP bit written), conversions are not restarted after register writes.

Table 8-19. ADS127L21 Register Map Overview

ADDRESS	REGISTER	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	DEV_ID	02h	DEV_ID[7:0]							
01h	REV_ID	xxh	REV_ID[7:0]							
02h	STATUS1	x1100xxxb	CS_MODE	ALV_FLAG	POR_FLAG	SPI_ERR	CRC_ERR	ADC_ERR	MOD_FLAG	DRDY
03h	STATUS2	00h	RESERVED					I_CRC_ERR	F_CRC_ERR	M_CRC_ERR
04h	CONTROL	00h	RESET[5:0]						START	STOP
05h	MUX	00h	RESERVED						MUX[1:0]	
06h	CONFIG1	00h	DATA	EXT_RNG	REF_RNG	INP_RNG	VCM	REFP_BUF	AINP_BUF	AINN_BUF
07h	CONFIG2	08h	RESERVED		START_MODE[1:0]		SPEED_MODE[1:0]		STBY_MODE	PWDN
08h	CONFIG3	00h	CLK_SEL	CLK_DIV[1:0]		OUT_DRV	RESERVED	SPI_CRC	REG_CRC	STATUS
09h	FILTER1	00h	FLTR_SEL[2:0]			FLTR_OSR[4:0]				
0Ah	FILTER2	01h	RESERVED	DELAY[2:0]			FLTR_SEQ	FIR2_DIS	FIR3_DIS	IIR_DIS
0Bh	FILTER3	01h	RESERVED						DATA_MODE[1:0]	
0Ch	OFFSET2	00h	OFFSET[23:16]							
0Dh	OFFSET1	00h	OFFSET[15:8]							
0Eh	OFFSET0	00h	OFFSET[7:0]							
0Fh	GAIN2	40h	GAIN[23:16]							
10h	GAIN1	00h	GAIN[15:8]							
11h	GAIN0	00h	GAIN[7:0]							
12h	MAIN_CRC	00h	MAIN_CRC[7:0]							
13h	FIR_BANK	xxh	FIR_BANK[7:0]							
14h	FIR_CRC1	xxh	FIR_CRC[15:8]							
15h	FIR_CRC0	xxh	FIR_CRC[7:0]							
16h	IIR_BANK	xxh	IIR_BANK[7:0]							
17h	IIR_CRC	xxh	IIR_CRC[7:0]							

Table 8-20 lists the access codes of the registers.

Table 8-20. Register Access Codes

Access Type	Code	Description
Read	R	Read only
Write	W	Write only
Read and write	R/W	Read and write
Reset or default value	*-n*	Value after reset or the default value

8.6.1 DEV_ID Register (Address = 00h) [reset = 02h]

Return to the Register Map Overview.

Figure 8-47. DEV_ID Register

7	6	5	4	3	2	1	0
DEV_ID[7:0]							
R-02h							

Table 8-21. DEV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DEV_ID[7:0]	R	02h	Device ID. 02h = ADS127L21

8.6.2 REV_ID Register (Address = 01h) [reset = xxh]

Return to the Register Map Overview.

Figure 8-48. REV_ID Register

7	6	5	4	3	2	1	0
REVID[7:0]							
R-xxxxxxxxb							

Table 8-22. REV_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	REV_ID[7:0]	R	xxxxxxxxb	Die revision ID. The die revision ID can change during device production without notice.

8.6.3 STATUS1 Register (Address = 02h) [reset = x1100xxxb]

Return to the Register Map Overview.

Figure 8-49. STATUS1 Register

7	6	5	4	3	2	1	0
CS_MODE	ALV_FLAG	POR_FLAG	SPI_ERR	CRC_ERR	ADC_ERR	MOD_FLAG	DRDY
R-xb	R/W-1b	R/W-1b	R/W-0b	R-0b	R-xb	R-xb	R-xb

Table 8-23. STATUS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CS_MODE	R	xb	$\overline{CS}$ mode. This bit indicates 4-wire or 3-wire SPI mode. The mode is determined by the state of $\overline{CS}$ at power up or after reset. 0b = 4-wire SPI operation ($\overline{CS}$ is active) 1b = 3-wire SPI operation ($\overline{CS}$ is tied low)
6	ALV_FLAG	R/W	1b	Analog supply low-voltage flag. This bit indicates a low-voltage was detected on the analog power supplies. Write 1b to clear the flag to detect the next low-voltage condition. 0b = No low-voltage detection from when the flag was last cleared 1b = Low-voltage detected

Table 8-23. STATUS1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	POR_FLAG	R/W	1b	Power-on reset (POR) flag. This bit indicates a reset at device power-on, by a brownout of the IOVDD supply, or by a user-initiated reset. Write 1b to clear the flag to detect the next reset. 0b = No reset from when the flag was last cleared 1b = Device reset occurred
4	SPI_ERR	R/W	0b	SPI communication CRC error. This bit indicates an SPI CRC error. If set, register write operations are blocked, except for the STATUS register that allows clearing the error (write 1b to clear the error). Register read operations remain functional. The SPI CRC error detection is enabled by the SPI_CRC bit of the CONFIG4 register. 0b = No SPI CRC error 1b = SPI CRC error
3	CRC_ERR	R	0b	Global memory CRC error. This bit is an OR of the main memory, the FIR coefficients, and the IIR coefficients CRC errors. If the values written to the associated CRC registers do not match the ADC calculation, individual error bits are set in the I_CRC_ERR, F_CRC_ERR, and M_CRC_ERR bits of the STATUS2 register. This flag auto-clears when the individual CRC errors are cleared. Set the REG_CRC bit of the CONFIG3 register to enable memory CRC error check. 0b = No global memory CRC error 1b = Global memory CRC error
2	ADC_ERR	R	xb	Internal ADC error. ADC_ERR indicates an internal error. Perform a power cycle or reset the device. 0b = No ADC error 1b = ADC error
1	MOD_FLAG	R	xb	Modulator saturation flag. This bit indicates modulator saturation occurred during the conversion cycle. The flag is valid at the end of the conversion cycle. 0b = No modulator saturation 1b = Modulator saturation during the conversion cycle
0	DRDY	R	xb	Data-ready bit. This bit asserts when new conversion data are ready. The bit is the inverse of the $\overline{\text{DRDY}}$ pin. Poll this bit in lieu of the $\overline{\text{DRDY}}$ pin to determine if conversion data are new or are repeated data from the last read operation. In one-shot control mode, this bit remains at 1b until a new conversion is started. 0b = Data are not new 1b = Data are new

8.6.4 STATUS2 Register (Address = 03h) [reset = 00h]

Return to the Register Map Overview.

Figure 8-50. STATUS2 Register

7	6	5	4	3	2	1	0
RESERVED					I_CRC_ERR	F_CRC_ERR	M_CRC_ERR
R-00000b					R-0b	R-0b	R/W-0b

Table 8-24. STATUS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R	00000b	Reserved
2	I_CRC_ERR	R	0b	IIR coefficient memory CRC error. If the value written to the IIR memory CRC register (register address 17h) does not match the internal calculation, the error is flagged to this bit and to the global CRC_ERR bit of the STATUS1 register. Clear the error by correcting the IIR_CRC register value and disable and re-enable the register CRC check (REG_CRC bit of the CONFIG3 register). Set the REG_CRC bit (CONFIG3 register) to enable the IIR memory error check. 0b = No IIR coefficient memory CRC error 1b = IIR coefficient memory CRC error
1	F_CRC_ERR	R	0b	FIR coefficient memory CRC error. If the value written to the FIR memory CRC register (register addresses 14h and 15h) do not match the internal calculation, the error is flagged to this bit and to the global CRC_ERR bit of the STATUS1 register. Clear the error by correcting the FIR_CRC register values and disable and re-enable the register CRC check (REG_CRC bit of the CONFIG3 register). Set the REG_CRC bit (CONFIG3 register) to enable the register bank error check. 0b = No FIR coefficient memory CRC error 1b = FIR coefficient memory CRC error
0	M_CRC_ERR	R/W	0b	Main memory CRC error. If the value written to the main register memory CRC register (register address 12h) does not match the internal calculation, the error is flagged to this bit and to the global CRC_ERR bit of the STATUS1 register. Clear the error by correcting the MAIN_CRC register value, then write 1b to this bit. Set the REG_CRC bit (CONFIG3 register) to enable the register bank error check. 0b = No main memory CRC error 1b = Main memory CRC error

8.6.5 CONTROL Register (Address = 04h) [reset = 00h]

Return to the Register Map Overview.

Figure 8-51. CONTROL Register

7	6	5	4	3	2	1	0
RESET[5:0]						START	STOP
W-000000b						W-0b	W-0b

Table 8-25. CONTROL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESET[5:0]	W	000000b	Device reset. Write 010110b to reset the ADC. The adjacent START and STOP bits must be set to 00b in the same write operation to reset the ADC. These bits always read 000000b.
1	START	W	0b	Start conversion. Conversions are started or restarted by writing 1b. In one-shot control mode, one conversion is started. In start/stop control mode, conversions are started and continue until stopped by the STOP bit. Writing 1b to the START bit while a conversion is ongoing restarts the conversion. This bit has no effect in synchronized control mode. Writing 1b to both the START and STOP bits has no effect. The START bit is self-clearing and always reads 0b. 0b = No operation 1b = Start or restart conversion
0	STOP	W	0b	Stop conversion. This bit stops conversions after the current conversion completes. This bit has no effect in synchronized control mode. Writing 1b to both the START and STOP has no effect. STOP is self-clearing and always reads 0b. 0b = No operation 1b = Stop conversion after the current conversion completes

8.6.6 MUX Register (Address = 05h) [reset = 00h]

Return to the Register Map Overview.

Figure 8-52. MUX Register

7	6	5	4	3	2	1	0
RESERVED						MUX[1:0]	
R-000000b						R/W-00b	

Table 8-26. MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R	000000b	Reserved
1:0	MUX[1:0]	R/W	00b	Input multiplexer selection. These bits select the polarity of the analog input and select the test modes. See the *Analog Input* section for details. 00b = Normal input polarity 01b = Inverted input polarity 10b = Offset and noise test: AINP and AINN disconnected, ADC inputs internally shorted to (AVDD1 + AVSS) / 2 11b = Common-mode test: ADC inputs internally shorted and connected to AINP

8.6.7 CONFIG1 Register (Address = 06h) [reset = 00h]

Return to the Register Map Overview.

Figure 8-53. CONFIG1 Register

7	6	5	4	3	2	1	0
DATA	EXT_RNG	REF_RNG	INP_RNG	VCM	REFP_BUF	AINP_BUF	AINN_BUF
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-27. CONFIG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DATA	R/W	0b	Data resolution selection. This bit selects the output data resolution. 0b = 24-bit resolution 1b = 16-bit resolution
6	EXT_RNG	R/W	0b	Extended input range selection. This bit extends the input range by 25%. See the *Input Range* section for more details. 0b = Standard input range 1b = 25% extended input range
5	REF_RNG	R/W	0b	Voltage reference range selection. Program this bit to select the low- or high-reference voltage range to match the applied reference voltage. See the *Recommended Operating Conditions* table for the range of reference voltages. When the high-reference range is selected, the INP_RNG bit is internally overridden to the 1x input range. 0b = Low-reference range 1b = High-reference range
4	INP_RNG	R/W	0b	Input range selection. This bit selects the 1x or 2x input range. See the *Input Range* section for more details. 0b = 1x input range 1b = 2x input range
3	VCM	R/W	0b	VCM output enable. This bit enables the VCM output voltage pin. The VCM voltage is (AVDD1 + AVSS) / 2. 0b = Disabled 1b = Enabled
2	REFP_BUF	R/W	0b	Reference positive buffer enable. This bit enables the REFP reference input precharge buffer. 0b = Disabled 1b = Enabled
1	AINP_BUF	R/W	0b	Analog input positive buffer enable. This bit enables the AINP analog input precharge buffer. 0b = Disabled 1b = Enabled
0	AINN_BUF	R/W	0b	Analog input negative buffer enable. This bit enables the AINN analog input precharge buffer. 0b = Disabled 1b = Enabled

8.6.8 CONFIG2 Register (Address = 07h) [reset = 08h]

Return to the Register Map Overview.

Figure 8-54. CONFIG2 Register

7	6	5	4	3	2	1	0
RESERVED		START_MODE[1:0]		SPEED_MODE[1:0]		STBY_MODE	PWDN
R-0b		R/W-00b		R/W-10b		R/W-0b	R/W-0b

Table 8-28. CONFIG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R	00b	Reserved
5:4	START_MODE[1:0]	R/W	00b	START mode selection. These bits program the mode of the START pin. See the *Synchronization* section for more details. 00b = Start/stop control mode 01b = One-shot control mode 10b = Synchronized control mode 11b = Reserved
3:2	SPEED_MODE[1:0]	R/W	10b	Speed mode selection. These bits program the speed modes of the device. The ADC clock frequency listed corresponds to the mode. 00b = Low-speed mode (f_{CLK} = 3.2 MHz) 01b = Mid-speed mode (f_{CLK} = 12.8 MHz) 10b = High-speed mode (f_{CLK} = 25.6 MHz) 11b = Max-speed mode (f_{CLK} = 32.768 MHz, external only)
1	STBY_MODE	R/W	0b	Standby mode selection. This bit enables the automatic standby mode when conversions are stopped. 0b = Idle mode; the ADC remains fully powered when conversions stop. 1b = Standby mode; the ADC powers down when conversions stop. Standby mode is exited when conversions restart.
0	PWDN	R/W	0b	Power-down mode selection. This bit powers down the ADC. All functions are powered down except for SPI operation and the digital LDO to retain user register settings. 0b = Normal operation 1b = Power-down mode

8.6.9 CONFIG3 Register (Address = 08h) [reset = 00h]

Return to the Register Map Overview.

Figure 8-55. CONFIG3 Register

7	6	5	4	3	2	1	0
CLK_SEL	CLK_DIV[1:0]		OUT_DRV	RESERVED	SPI_CRC	REG_CRC	STATUS
R/W-0b	R/W-00b		R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b

Table 8-29. CONFIG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLK_SEL	R/W	0b	Clock selection. Selects internal or external clock operation. 0b = Internal oscillator operation 1b = External clock operation
6:5	CLK_DIV[1:0]	R/W	00b	Clock divider selection. Select the clock division factor for either internal or external clock. Selecting the divide-by-2 and divide-by-16 clock division factors force the low-latency filter OSR values of the mid-speed mode to all other speed modes. See the FILTER1 register for a list of OSR values of the speed modes. 00b = f_{CLK} / 1 01b = f_{CLK} / 2 10b = f_{CLK} / 8 11b = f_{CLK} / 16
4	OUT_DRV	R/W	0b	Digital output drive selection. Select the drive strength of the digital outputs. 0b = Full-drive strength 1b = Half-drive strength
3	RESERVED	R	0b	Reserved
2	SPI_CRC	R/W	0b	SPI CRC enable. This bit enables the SPI CRC error detection. When enabled, the device verifies the CRC input byte and appends a CRC byte to the output data. The SPI_ERR bit of the STATUS byte sets if an input SPI CRC error is detected. Write 1b to the SPI_ERR bit to clear the error. 0b = Disabled 1b = Enabled
1	REG_CRC	R/W	0b	Memory CRC enable. This bit enables the main, IIR coefficient, and FIR coefficient memory CRC error check. If the values written to the associated CRC value registers do not match the ADC calculation, individual errors are reported to the I_CRC_ERR, F_CRC_ERR, and M_CRC_ERR error bits of the STATUS2 register. If any CRC error bit is set, the global CRC error bit (CRC_ERR) is set in the STATUS1 register. Toggle the REG_CRC bit to clear the I_CRC_ERR and F_CRC_ERR flags after correcting the CRC value. 0b = Disabled 1b = Enabled

Table 8-29. CONFIG3 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	STATUS	R/W	0b	STATUS1 byte output enable. Program this bit to prefix the STATUS1 register data to the conversion data. The STATUS1 register data are also prefixed to the register data output when reading registers. 0b = Disabled 1b = Enabled

8.6.10 FILTER1 Register (Address = 09h) [reset = 00h]

Return to the Register Map Overview.

Figure 8-56. FILTER1 Register

7	6	5	4	3	2	1	0
FLTR_SEL[2:0]			FLTR_OSR[4:0]				
R/W-000b			R/W-00000b				

Table 8-30. FILTER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	FLTR_SEL[2:0]	R/W	000b	Digital filter selection. The function of these bits depend on the wideband or sinc filter mode selection made by the FLTR_OSR[4:0] bits. If the wideband filter is selected by FLTR_OSR[4:0], these bits select the preset or programmable FIR filter coefficients. 000b = Preset FIR filter coefficients 001b to 110b = Reserved 111b = Programmable FIR filter coefficients If the sinc filter is selected by FLTR_OSR[4:0], these bits select the sinc3 or sinc4 first stage filter. 000b = Sinc4 first stage filter 001b = Sinc3 first stage filter 010b to 111b = Reserved

Table 8-30. FILTER1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	FLTR_OSR[4:0]	R/W	00000b	Digital filter mode and oversampling ratio selection. These bits select the oversampling ratio and the filter mode (wideband or sinc). For sinc filter mode, sincx = sinc3 or sinc4 filter selection made by FLTR_SEL[2:0]. The wideband filter OSR values decrease by 2 if FIR2 *or* FIR3 is disabled, and decrease by 4 if FIR2 *and* FIR3 are disabled. The output data rate is equal to f_{MOD} / OSR. 00000b = Wideband, OSR = 32 00001b = Wideband, OSR = 64 00010b = Wideband, OSR = 128 00011b = Wideband, OSR = 256 00100b = Wideband, OSR = 512 00101b = Wideband, OSR = 1024 00110b = Wideband, OSR = 2048 00111b = Wideband, OSR = 4096 01000b = Sincx, OSR = 12 01001b = Sincx, OSR = 16 01010b = Sincx, OSR = 24 01011b = Sincx, OSR = 32 01100b = Sincx, OSR = 64 01101b = Sincx, OSR = 128 01110b = Sincx, OSR = 256 (167 mid-speed mode) 01111b = Sincx, OSR = 333 (256 mid-speed mode) 10000b = Sincx, OSR = 512 (333 mid-speed mode) 10001b = Sincx, OSR = 667 (512 mid-speed mode) 10010b = Sincx, OSR = 1024 (667 mid-speed mode) 10011b = Sincx, OSR = 1333 (1024 mid-speed mode) 10100b = Sincx, OSR = 2048 (1333 mid-speed mode) 10101b = Sincx, OSR = 2667 (2048 mid-speed mode) 10110b = Sincx, OSR = 4096 (2667 mid-speed mode) 10111b = Sincx, OSR = 5333 (4096 mid-speed mode) 11000b = Sincx, OSR = 26667 (13333 mid-speed mode) 11001b = Sincx, OSR = 32000 (16000 mid-speed mode) 11010b = Sincx, OSR = 96000 (48000 mid-speed mode) 11011b = Sincx, OSR = 160000 (80000 mid-speed mode) 11100b = Sincx + sinc1, OSR = 26656 (13334 mid-speed mode) 11101b = Sincx + sinc1, OSR = 32000 (16000 mid-speed mode) 11110b = Sincx + sinc1, OSR = 96000 (48000 mid-speed mode 11111b = Sincx + sinc1, OSR = 160000 (80000 mid-speed mode)

8.6.11 FILTER2 Register (Address = 0Ah) [reset = 01h]

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Figure 8-57. FILTER2 Register

7	6	5	4	3	2	1	0
RESERVED	DELAY[2:0]			FLTR_SEQ	FIR2_DIS	FIR3_DIS	IIR_DIS
R/W-0b	R/W-000b			R/W-0b	R/W-0b	R/W-0b	R/W-1b

Table 8-31. FILTER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved
6:4	DELAY[2:0]	R/W	000b	Conversion-start delay time selection. These bits program a delay time between when the START pin is high or when writing to the START bit to the start of the first conversion (f_{MOD} = f_{CLK} / 2). 000b = 0 001b = 4 / f_{MOD} 010b = 8 / f_{MOD} 011b = 16 / f_{MOD} 100b = 32 / f_{MOD} 101b = 128 / f_{MOD} 110b = 512 / f_{MOD} 111b = 1024 / f_{MOD}
3	FLTR_SEQ	R/W	0b	Wideband filter computation sequence. This bit programs the computational sequence of the IIR and FIR3 wideband filter sections. 0b = FIR3 then IIR 1b = IIR then FIR3
2	FIR2_DIS	R/W	0b	Wideband filter, FIR2 section disable. This bit disables the FIR2 section of the wideband filter. 0b = Enabled 1b = Disabled
1	FIR3_DIS	R/W	0b	Wideband filter, FIR3 section disable. This bit disables the FIR3 section of the wideband filter. 0b = Enabled 1b = Disabled
0	IIR_DIS	R/W	1b	Wideband filter, IIR section disable. This bit disables the IIR section of the wideband filter. 0b = Enabled 1b = Disabled

8.6.12 FILTER3 Register (Address = 0Bh) [reset = 01h]

Return to the Register Map Overview.

Figure 8-58. FILTER3 Register

7	6	5	4	3	2	1	0
RESERVED						DATA_MODE[1:0]	
R-000000b						R/W-01b	

Table 8-32. FILTER3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	Reserved[5:0]	R	000000b	Reserved
1:0	DATA_MODE[1:0]	R/W	01b	Data output pin function selection. These bits program the function of the SDO/$\overline{\text{DRDY}}$ pin. For SPI daisy-chain connection, use the data-output only mode. 00b = SDO/$\overline{\text{DRDY}}$ pin is data-output only mode 01b = SDO/$\overline{\text{DRDY}}$ is a dual mode: Data output and data ready 10b = Same as mode 01b, except SDO/$\overline{\text{DRDY}}$ is active when $\overline{\text{CS}}$ is high 11b = Reserved

8.6.13 OFFSET2, OFFSET1, OFFSET0 Registers (Addresses = 0Ch, 0Dh, 0Eh) [reset = 00h, 00h, 00h]

Return to the Register Map Overview.

Figure 8-59. OFFSET2, OFFSET1, OFFSET0 Registers

7	6	5	4	3	2	1	0
OFFSET[23:16]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OFFSET[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
OFFSET[7:0]							
R/W-00000000b							

Table 8-33. OFFSET Registers Field Description

Bit	Field	Type	Reset	Description
23:0	OFFSET[23:0]	R/W	000000h	User offset calibration value. Three registers form the 24-bit offset calibration word. OFFSET[23:0] is in two's-complement representation and is subtracted from the conversion result. The offset operation precedes the gain operation.

8.6.14 GAIN2, GAIN1, GAIN0 Registers (Addresses = 0Fh, 10h, 11h) [reset = 40h, 00h, 00h]

Return to the Register Map Overview.

Figure 8-60. GAIN2, GAIN1, GAIN0 Registers

7	6	5	4	3	2	1	0
GAIN[23:16]							
R/W-01000000b							
7	6	5	4	3	2	1	0
GAIN[15:8]							
R/W-00000000b							
7	6	5	4	3	2	1	0
GAIN[7:0]							
R/W-00000000b							

Table 8-34. GAIN Registers Field Description

Bit	Field	Type	Reset	Description
23:0	GAIN[23:0]	R/W	400000h	User gain calibration value. Three registers form the 24-bit gain calibration word. GAIN[23:0] is a straight binary representation and normalized to 400000h for gain = 1. The conversion data are multiplied by GAIN[23:0] / 400000h after the offset operation.

8.6.15 MAIN_CRC Register (Address = 12h) [reset = 00h]

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Figure 8-61. MAIN_CRC Register

7	6	5	4	3	2	1	0
MAIN_CRC[7:0]							
R/W-00000000b							

Table 8-35. MAIN_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	MAIN_CRC[7:0]	R/W	00h	Main memory CRC value. The main memory CRC is computed over registers 0h and 1h, skipping registers 2h, 3h, and 4h, and continuing with registers 5h through 11h. Write the computed CRC value to this register. If the value does not match the internal calculation, the M_REG_ERR bit is set in the STATUS2 register. The global CRC_ERR bit is also set in the STATUS1 register. Set the REG_CRC bit of the CONFIG3 register to enable all three types of memory CRC.

8.6.16 FIR_BANK Register (Address = 13h) [reset = xxh]

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Figure 8-62. FIR_BANK Register

7	6	5	4	3	2	1	0
FIR_BANK[7:0]							
R/W-xxh							

Table 8-36. FIR_BANK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FIR_BANK[7:0]	R/W	xxh	FIR programmable filter coefficient register memory bank This register is a single address space that stores the 128 coefficients of the programmable FIR filter memory. Perform sequential read and write operations to the same register address to increment an internal pointer to the next memory location. Any change of address to another register in a read or write operation resets the internal pointer to the first memory space. The reset values of the programmable coefficients are undefined. See the *FIR3 Filter Stage* section for the FIR coefficient byte sequence.

8.6.17 FIR_CRC1, FIR_CRC0 Registers (Addresses = 14h, 15h) [reset = xxh, xxh]

Return to the Register Map Overview.

Figure 8-63. FIR_CRC1, FIR_CRC0 Registers

7	6	5	4	3	2	1	0
FIR_CRC1[15:8]							
R/W-xxh							
7	6	5	4	3	2	1	0
FIR_CRC0[7:0]							
R/W-xxh							

Table 8-37. FIR_CRC1, FIR_CRC0 Registers Field Description

Bit	Field	Type	Reset	Description
23:0	FIR_CRC[23:0]	R/W	xxxxh	Programmable FIR filter coefficients CRC value. The programmable FIR filter coefficients CRC is a user-computed value for the 128, 32-bit FIR filter coefficients. A 16-bit polynomial is used for the FIR coefficient CRC ($x^{16} + x^{15} + x^2 + 1$). FIR_CRC1 is the high byte value. If the value written does not match an internal calculation, the F_REG_ERR bit is set in the STATUS2 register. The global CRC_ERR bit is also set in the STATUS1 register. Set the REG_CRC bit of the CONFIG3 register to enable all three types of memory bank CRC. See the *FIR Filter Coefficient CRC* section for more details.

8.6.18 IIR_BANK Register (Address = 16h) [reset = xxh]

Return to the Register Map Overview.

Figure 8-64. IIR_BANK Register

7	6	5	4	3	2	1	0
IIR_BANK[7:0]							
R/W-xxh							

Table 8-38. IIR_BANK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IIR_BANK[7:0]	R/W	xxh	IIR programmable filter coefficients register bank. This register is a single address space that stores the programmable coefficients for the IIR filter. Successive read and write operations to this register increment an internal pointer to the next memory byte location. See Table 8-8 for the byte sequence of the IIR filter coefficients. Any change of address to another resister during a read or write operation resets the operation to the first IIR coefficient memory location.

8.6.19 IIR_CRC Register (Address = 17h) [reset = xxh]

Return to the Register Map Overview.

Figure 8-65. IIR_CRC Register

7	6	5	4	3	2	1	0
IIR_CRC[7:0]							
R/W-xxh							

Table 8-39. IIR_CRC Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	IIR_CRC[7:0]	R/W	xxh	IIR filter coefficients memory CRC value. The IIR filter coefficients memory CRC is a user-computed value of the entire IIR filter memory. If the value written does not match an internal calculation, the I_REG_ERR bit is set in the STATUS2 register. The global CRC_ERR bit is also set in the STATUS1 register. Set the REG_CRC bit of the CONFIG3 register to enable all three types of memory bank CRC. See the *IIR Filter Coefficient CRC* section for more details.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The high-performance characteristics of the ADS127L21 are achieved when familiar with the requirements of the input driver, antialias filter, reference voltage, SPI clocking, and PCB layout. The following sections provide design guidelines.

9.1.1 SPI Operation

Although the ADC provides flexible SPI clock options and the wide IOVDD voltage range, the following guidelines help achieve full data sheet performance.

1. If possible, use an SCLK signal that is phase coherent to the CLK signal (that is, ratios of 2:1, 1:1, 1:2, 1:4, and so on)
2. Minimize phase skew between SCLK and CLK (< 5 ns)
3. Operate IOVDD at the lowest voltage possible to reduce digital noise coupling
4. If IOVDD ≥ 3.3 V, consider operating SCLK continuously over the full conversion period to spread the effects of noise coupling over the full conversion period
5. Keep the trace capacitance of SDO/$\overline{\text{DRDY}}$ ≤ 20 pF to limit the peak currents associated with the digital code transitions

The ADC updates data on the SCLK rising edge for latching the data on the SCLK falling edge. Considering the data propagation delay time after the SCLK rising edge, the practical limit of the SCLK signal frequency is 22 MHz using an IOVDD supply of 3.3 V. Reading 24-bit data at f_{DATA} = 512 kSPS with a 40-bit payload is possible assuming there are no other delays in the SDO/$\overline{\text{DRDY}}$ signal path.

The FIR1 filter output mode provides data at up to 2.048 MSPS, requiring a 49.152-MHz SCLK signal to read the 24-bit data. Reading data at an SCLK of 49.152 MHz requires non-standard SPI clocking by latching the data on the same rising edge that the data updates. The ADC data hold time specification holds the old data briefly before updating the new data. Additional hold time is provided by delaying the SDO/$\overline{\text{DRDY}}$ signal by adding a discrete buffer leading to the external controller.

9.1.2 Input Driver

The ADC incorporates precharge buffers that reduce the settling and bandwidth requirement of the analog input driver. If a 10-MHz or less bandwidth driver is used, or if there is a long distance between the driver and the ADC inputs (such as a cable connection), enable the input precharge buffers. For higher gain-bandwidth drivers, the precharge buffers can be disabled to reduce power consumption, but in any case, full-rated THD and SNR data sheet performance is realized with the input precharge buffers active. The lower speed modes operate the modulator at a slower rate, and therefore the driver has more time to settle between the modulator sampling transients. Using a low bandwidth input driver and disabling the precharge buffers can be possible for the lower speed modes.

9.1.3 Antialias Filter

Input signals occurring near the modulator sampling rate (f_{MOD} = f_{CLK} / 2) fold back (or alias) to the pass band, resulting in data errors. When aliased, the frequency errors cannot be removed by post processing. An analog antialias filter at the ADC inputs removes out-of-band frequencies from the input signal before being aliased by the ADC. The required order of the antialias filter is dependent on the selected OSR and the target value of signal attenuation at f_{MOD}. A large value of OSR means more frequency range between the f_{DATA} Nyquist frequency and f_{MOD} for the filter to provide the desired attenuation. For example, for OSR = 128, more than two

decades of frequency separates f_{DATA} and f_{MOD}. With a corner frequency = f_{DATA}, a third-order, 60-dB per decade filter provides a 120-dB alias rejection at f_{MOD}.

9.1.4 Reference Voltage

For data sheet performance, the ADC requires a reference voltage with low noise and good drive strength to charge the sampled reference input. Because the modulator continuously samples the reference voltage whether conversions are ongoing or not (except for standby and power-down modes), the reference loading is constant. Therefore, incomplete settling of the reference voltage appears as a gain error to the system. The system gain error can be calibrated. A 22-µF decoupling capacitor at the reference output and 1-µF and 0.1-µF capacitors directly across the reference input pins filters the reference kickback voltage caused by capacitor sampling. The ADC incorporates an optional reference precharge buffer that greatly reduces the kickback voltage and gain error.

9.1.5 Simultaneous-Sampling Systems

When using the ADC in a multichannel system, the same design principles apply with additional considerations for clock routing, synchronization, shared reference voltage, and SPI clocking. The *ADS127L11 in Simultaneous-Sampling Systems* application brief discusses a similar ADC (ADS127L11) and provides details for use in simultaneous-sampling systems.

9.2 Typical Applications

9.2.1 A-Weighting Filter Design

Figure 9-1 shows the ADS127L21 IIR filter performing A-weighting frequency compensation from a microphone signal. A-weighting shapes the original input frequency spectrum to account for the frequency-dependent sensitivity of the human ear to the perceived sound pressure level (SPL). As such, occupational health and safety standards specify SPL exposure limits in high noise environments using A-weighted compensated instrumentation. Figure 9-2 shows the A-weighting compensating curve.

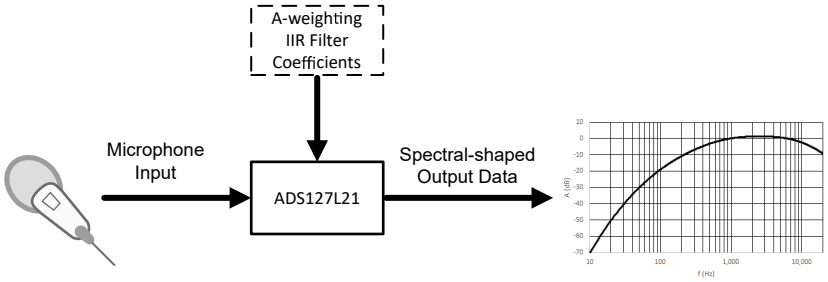

Figure 9-1. ADS127L21 A-Weighting Compensation

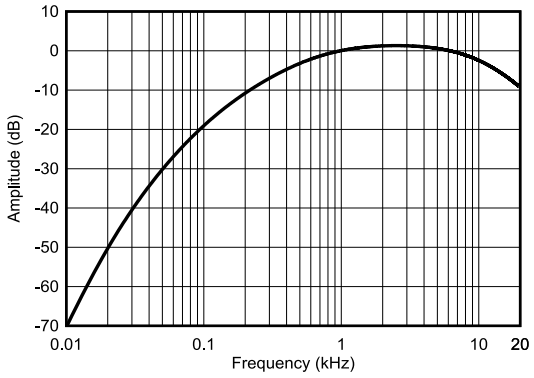

Figure 9-2. A-weighting Frequency Response

A-weighting compensation is specified by poles in the continuous-time domain by ANSI S1.43 and IEC 616672-1. The continuous-time poles cannot be used directly as Z-domain poles for a digital filter design. This application summarizes the transformation steps of the continuous-time poles to the Z-domain poles for use in the ADS127L21 IIR digital filter.

9.2.1.1 Design Requirements

The ANSI A-weighting standard specifies three classes of accuracy depending on the application requirements. Table 9-1 shows the instrumentation class accuracy levels at ±22.5° microphone angles of incident. As such, less than a 0.3-dB filter compliance error can be achieved in this design.

Table 9-1. ANSI A-weighting Instrumentation Class Accuracy (±22.5° Microphone Angle of Incident)

FREQUENCY RANGE (Hz)	TYPE 0 (dB)	TYPE 1 (dB)	TYPE 2 (dB)
31.5 to 2000	±0.5	±1	±2
2000 to 4000	±1	+1.5, –1	±2.5
4000 to 5000	±1	+2, –1.5	±3
5000 to 6300	±1.5	+2.5, –2	±3.5
6300 to 8000	±2	+3, –2.5	±4.5
8000 to 10000	±2	+3.5, –3.5	None specified
10000 to 12500	±3	+4, –6.5	None specified

As shown in Table 9-2, the target error of the IIR filter design is < ±0.3 dB over the 10-Hz to 20-kHz bandwidth. The 50-kSPS sample rate supporting a 20.6-kHz, –0.1-dB bandwidth is selected for compliance over the full 20-kHz audio band.

Table 9-2. Design Requirements

PARAMETER	VALUE
Frequency range	10 Hz to 20 kHz
Compensation accuracy	< ±0.3 dB
Sample rate	50 kHz

9.2.1.2 Detailed Design Procedure

The bilinear transform converts the continuous time function H_A (s) to the discrete time function H_A (z). From an analytical perspective, the bilinear transform involves substituting a function of z for s in H_A (s) to produce H_A (z).

Equation 23 shows the A-weighting transfer function given in the ANSI standard. The denominator pole frequencies are in Hz.

$$H_A(f) = 20 \times \text{Log}\left[\frac{12194^2 \times f^4}{(f^2 + 20.6^2) \times \sqrt{(f^2 + 107.7^2) \times (f^2 + 737.9^2)} \times (f^2 + 12194^2)}\right] + 2 \quad (23)$$

Equation 24 shows the S-plane result of converting the frequency equation of Equation 23 by multiplying the frequency terms by 2 × Pi to convert to angular frequency. The pole frequencies of the denominator are radians/s.

$$H_A(s) = \frac{7.39014 \times 10^9 \times s^4}{(s + 129.4)^2 \times (s + 767.4) \times (s + 4636) \times (s + 76818)^2} \quad (24)$$

The bilinear transform substitutes the s-function of *z* of Equation 25, for *s* in the H_A (s) to produce H_A (z) in each term of the denominator.

$$s = \frac{2}{T} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \tag{25}$$

where:

- T = 1 / 50 kSPS

After substituting s, H_A (z) is found by collecting like powers of *z* then multiplying through by z^{-1} / z^{-1} to yield the H_A (z) function in the form of Equation 26.

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \tag{26}$$

In the z-plane transformation, pole frequency error occurs when the system poles are located close to the Nyquist frequency (f_{DATA} / 2). As such, the pole located at 12194 Hz (closest to the Nyquist frequency) is compensated for the error by scaling the pole frequency.

Table 9-3 shows the biquad coefficient values in decimal and 2.30 hex format for the IIR filter design. The gain coefficients including g_5 are 1.0 (40000000h). The coefficient upload procedure is described in the *IIR Filter Stage* section.

Table 9-3. A-Weighting IIR Filter Coefficients (Decimal, 2.30 Hex Format)

COEFFICIENT(1)	BIQUAD 1	BIQUAD 2	BIQUAD 3	BIQUAD 4
b_{x0}	0.997417013 3FD5AE2Bh	0.993278382 3F91DF7Eh	0.955663664 3D2997EEh	0.481661428 1ED38A74h
b_{x1}	–1.994834026 8054A3AAh	–0.99327838 C06E2082h	–0.955663664 C2D66812h	0.161859553 0A5BE82Ch
b_{x2}	0.997417013 3FD5AE2Bh	0.00000000 00000000h	0.00000000 00000000h	0.00000000 00000000h
a_{x1}	–1.99483069 8054B1ACh	–0.986556766 C0DC4103h	–0.911327329 C5ACD023h	–0.395604811 E6AE6929h
a_{x2}	0.994837367 3FAB6A59h	0.00000000 00000000	0.00000000 00000000h	0.039125792 02810977h
g_x	1.00000000 40000000h	1.00000000 40000000h	1.00000000 40000000h1	1.00000000 40000000h

1. *x* = biquad number.

9.2.1.3 Application Curve

Figure 9-3 shows the ADS127L21 A-weighting IIR filter error with a swept sine-wave signal over the 10-Hz to 20-kHz frequency band. The filter conformity error is less than the design target of ±0.3 dB. The filter conformity error is for the ADC alone and does not include microphone errors. The filter is scaled to provide a –1-dB full-scale ADC output at a 2-kHz full-scale signal input. Additional signal headroom for overload conditions is achieved by reducing the gain of the ADC input amplifier stage.

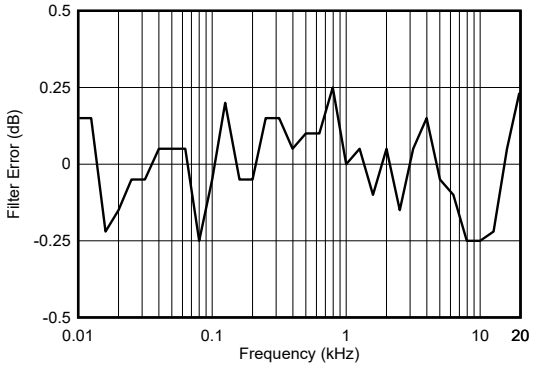

Figure 9-3. A-Weighting IIR Filter Error

9.2.2 PGA855 Programmable Gain Amplifier

Figure 9-4 shows the PGA855 programmable gain amplifier driving the ADS127L21 inputs. The PGA855 features differential inputs and differential outputs with 24-V input capability using ±15-V power supplies The PGA accepts single-ended signals by converting the signal to differential for driving the ADC differential inputs. Pin-controlled gains scale the signal to the ADC input range. The PGA855 operates by independent input and output power supplies. For example, ±15-V power supplies are used for the input section and a 5-V power supply for the output section. The 5-V output operation prevents overloading the ADC inputs during PGA overdrive conditions. The VCM output of the ADC drives the common mode voltage of the PGA outputs.

The goal of the application is to implement a two-pole PGA855 antialias filter and to show SNR and THD performance data of the PGA and ADC combination across PGA gain settings.

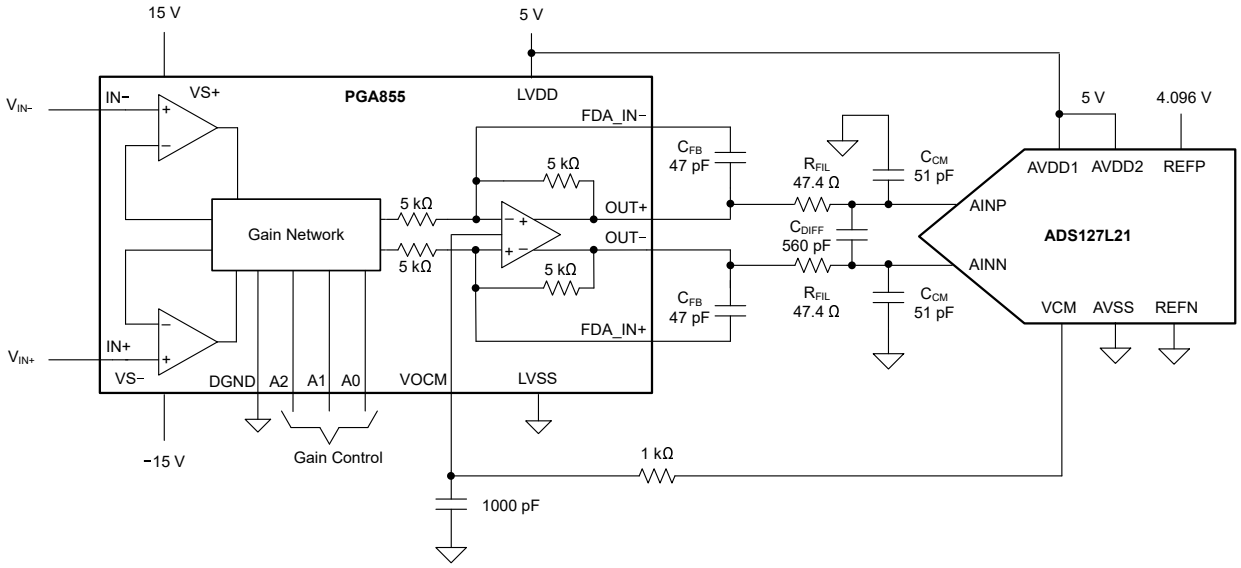

Figure 9-4. PGA855 Driver Circuit

9.2.2.1 Design Requirements

Table 9-4 lists the design parameters of the PGA855 application.

Table 9-4. Design Parameters

PARAMETER	VALUE
Input voltages (V_{PP}, differential)	20 V, 16 V, 8 V, 4 V, 2 V, 1 V, 0.5 V, 0.25 V
ADC reference voltage	4.096 V
Data rate	187.5 kSPS, OSR = 64
Alias rejection	–35 dB at 12-MHz f_{MOD}
Test frequency	1 kHz
THD (gain = 1)	< –120 dB
SNR (gain = 1, wideband filter)	> 107 dB
SNR (gain = 1, sinc4 filter)	> 109 dB

9.2.2.2 Detailed Design Procedure

Two first-order antialias filters are implemented with the PGA855 circuit. Referring to Figure 9-4, the first filter is provided by C_{FB} in parallel with the PGA 5-kΩ feedback resistors. The PGA resistors are ±15% absolute tolerance, as such, consider the effect of the tolerance on the filter cutoff frequency. C_{FB} = 47 pF results in a filter cutoff frequency of 675 kHz. On the high side of the resistor tolerance, the filter frequency changes to 574 kHz. At this tolerance, the filter maintains –0.1-dB flatness at the edge of the wideband filter signal band (77 kHz).

The second antialias filter is at the ADS127L21 inputs. Filter values R_{FIL} = 47.4 Ω and C_{DIFF} = 560 pF yield a filter cutoff frequency of 2.8 MHz. The ADC input precharge buffers significantly reduce the sample-phase input charge that raises the ADC input impedance to decrease gain error. Because of the buffers, R_{FIL} and C_{DIFF} can be increased in this design to improve antialias rejection.

C0G dielectric capacitors are used throughout the signal path (C_{FB}, C_{DIFF}, and C_{CM}) to provide low distortion performance.

9.2.2.3 Application Curves

A 1-kHz sine-wave test signal generates the SNR and THD data. The amplitude is adjusted to provide a –0.2-dBFS output from the ADC.

Table 9-5 summarizes the SNR, ENOB, and THD combined performance of the PGA855 driving the ADS127L21, with ADC input buffers enabled. At gain = 1, the design achieves –121.4-dB THD and 107.6-dB SNR for the wideband filter and 109.6-dB SNR for the sinc4 filter.

Table 9-5. PGA855 and ADS127L21 Performance Summary

PGA GAIN (V/V)	INPUT (V_{PP})	SNR (dB)		EFFECTIVE RESOLUTION (Bits)		THD (dB)
		WIDEBAND	SINC4	WIDEBAND	SINC4	
0.125	20	106.0	107.6	19.1	19.4	–119.6
0.25	16	107.5	109.0	19.4	19.6	–119.0
0.5	8	107.7	109.8	19.4	19.7	–121.2
1	4	107.6	109.6	19.4	19.7	–121.4
2	2	107.0	109.6	19.3	19.7	–121.4
4	1	105.4	107.4	19.0	19.3	–121.4
8	0.5	101.7	104.0	18.4	18.8	–121.4
16	0.25	96.7	99.1	17.6	17.9	–117.0

Figure 9-5 and Figure 9-6 show the respective 1-kHz, full-scale FFT plots for the wideband and sinc4 filters. Because of the frequency roll-off of the sinc4 filter, SNR performance improves by an average of 2 dB compared to the wideband filter. The filters provide identical THD results.

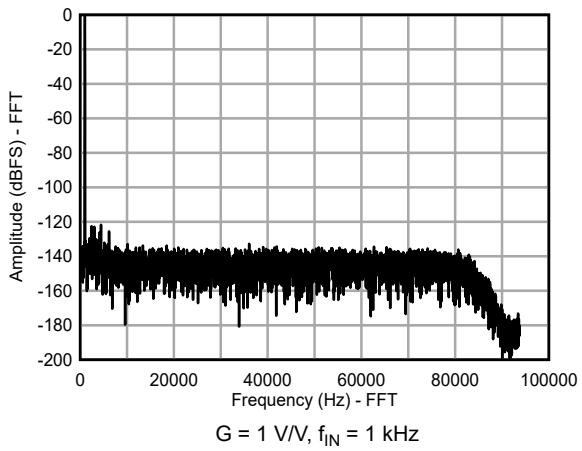

Figure 9-5. Wideband Filter Performance

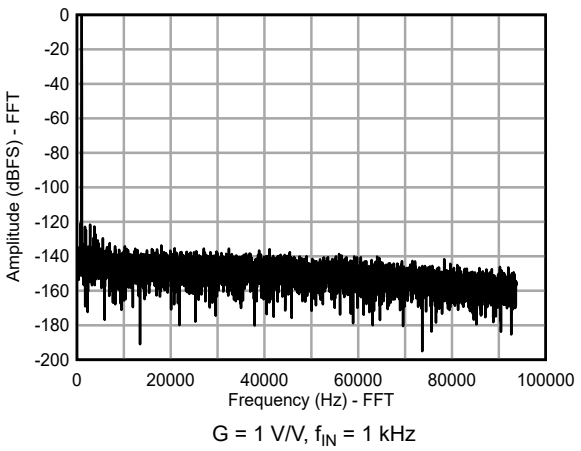

Figure 9-6. Sinc4 Filter Performance

Figure 9-7 shows the response of the two-pole antialias filter. The filter provides –38-dB antialias rejection at the 12-MHz f_{MOD} frequency.

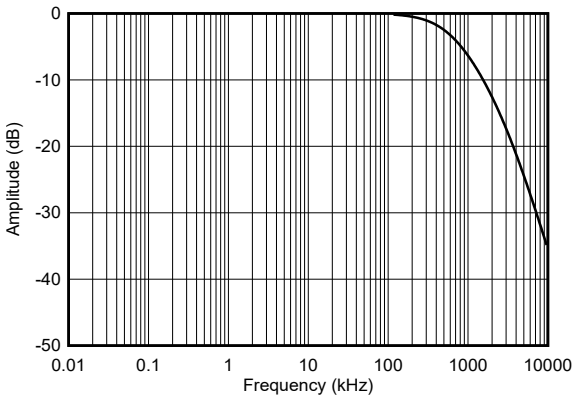

Figure 9-7. PGA855 Antialias Filter Response

9.2.3 THS4551 Antialias Filter Design

Figure 9-8 shows an application of the ADS127L21 used in a precision data acquisition system. Many sensors are limited in the amount of high-frequency signal content. For this reason, a first- or second-order filter can be sufficient to filter the high-frequency noise of the sensor and amplifier to prevent aliasing the noise to the pass band. However, in some applications the signal is unknown, requiring the use of a high-order antialiasing filter. The goal of this design is a THS4551 FDA antialias filter at the ADC input to attenuate out-of-band signals at the modulator sample rate (f_{MOD}).

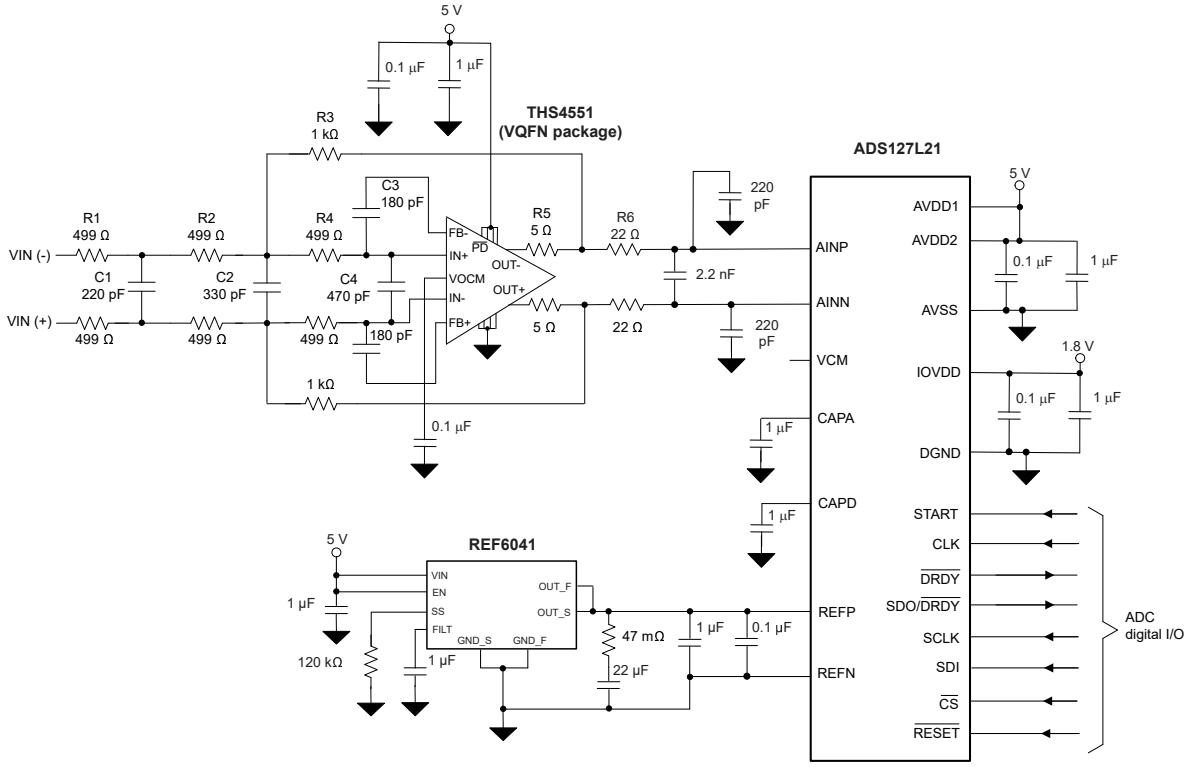

Figure 9-8. ADS127L21 Circuit Diagram

9.2.3.1 Design Requirements

The requirement of the antialias filter design is 90-dB attenuation at the critical f_{MOD} frequency (12.8 MHz in high-speed mode) using the OSR = 32 setting in wideband filter mode. The filter is designed for a flat amplitude response and low group delay error within the pass band of the signal.

Table 9-6 lists the target design values and the actual values in this design example.

Table 9-6. Antialias Filter Design Requirements

FILTER PARAMETER	TARGET VALUE	ACTUAL VALUE
Voltage gain	0 dB	0 dB
Alias rejection at 12.8 MHz	90 dB	90 dB
–0.1-dB frequency	250 kHz	260 kHz
–3-dB frequency	500 kHz	550 kHz
Amplitude peaking	20 mdB	12 mdB
Group delay linearity	0.1 µs	0.017 µs
Total noise of filter and ADC (165-kHz bandwidth)	12 µV	11.8 µV

9.2.3.2 Detailed Design Procedure

The antialias filter consists of a passive first-order input filter, an active second-order filter, and a passive first-order output filter. The filter is fourth-order overall, necessitated by the selection of a low value of OSR (32), which results in less than two decades of frequency range between the Nyquist frequency at f_{DATA} and the f_{MOD} frequency. The fourth-order filter provides 90-dB rolloff over this frequency range. The filter rolloff at f_{MOD} is the key function of the filter.

The THS4551 amplifier is selected for the active filter stage because of the 135-MHz gain-bandwidth product (GBP) and 50-ns settling time. The amplifier GBP is sufficient to maintain the filter rolloff at 12.8 MHz, even with the dc gain of 15 dB. For example, for applications where gain is desired, a 10-MHz amplifier has marginal GBP to fully support the required rolloff at the f_{MOD} frequency. The settling time specification of the THS4551 also makes the device a good choice for driving the ADC sampled inputs.

The design of the active filter section begins with an equal-R assumption to reduce the number of determined component values. The dc gain of the filter is R_3 / (R_1 + R_2). 1-kΩ resistors are selected to be low enough in value to keep resistor noise and amplifier input current noise from affecting the noise of the ADC.

The 1-kΩ input resistor is divided into two 499-Ω resistors (R_1 and R_2) to implement the first-order filter using C_1. The first-order filter is decoupled from the second-order active filter, but shares R_1 and R_2 to determine each filter stage corner frequency. The corner frequency is given by C_1 and the Thevenin resistance at the terminals of C_1 (R_{TH} = 2 × 250 Ω).

Given an arbitrary selection of R_4 (2 × 499 Ω in this case), the values of the 2 × 180 pF (C_3) feedback capacitors and the single 330-pF differential capacitor (C_2) are determined from the filter design equations given in the *Design Methodology for MFB Filters in ADC Interface Applications* application note. The design inputs are filter f_O and filter Q for the multiple-feedback active filter topology. The differential capacitor (C_4) is not part of the filter design but helps improve filter phase margin. The 5-Ω resistors (R_5) isolate the amplifier outputs from stray capacitance to further improve filter phase margin.

The final stage RC filter at the ADC inputs serves two purposes. First, the filter provides a fourth pole to the overall filter response, thereby increasing the filter rolloff slope. The other purpose of the filter is a charge reservoir to filter the capacitor sampled input of the ADC. The charge reservoir reduces the instantaneous charge demand of the amplifier, maintaining low distortion and low gain error that otherwise can degrade because of incomplete amplifier settling. The input filter values are 2 × 22 Ω and 2.2 nF. The 22-Ω resistors are outside the THS4551 filter loop to isolate the amplifier outputs from the 2.2-nF capacitor to maintain phase margin.

Low voltage-coefficient C0G capacitors are used everywhere in the signal path for the low distortion properties. The amplifier gain resistors are 0.1% tolerance to provide best possible THD performance. The ADC VCM output connection to the amplifier VOCM input pin is optional because the same function is provided by the amplifier.

See the THS4551 data sheet for additional examples of active filter designs and application.

9.2.3.3 Application Curves

The following figures are produced by the TINA-TI™, SPICE-based analog simulation program. Download the THS4551 SPICE model at the THS4551 product folder.

Figure 9-9 shows the frequency response of the antialias filter and the *total* response of the antialias filter and ADC. As shown in this image, the filter provides 90-dB stop-band attenuation from the Nyquist frequency to the 12.8-MHz f_{MOD} frequency.

Figure 9-10 shows the analog filter group delay. The 0.575-µs group delay is small in comparison to the 85-µs group delay of the ADC digital filter (34 / f_{DATA}). The analog filter group delay linearity is 0.017 µs, peaking at the edge of the 165-kHz pass-band.

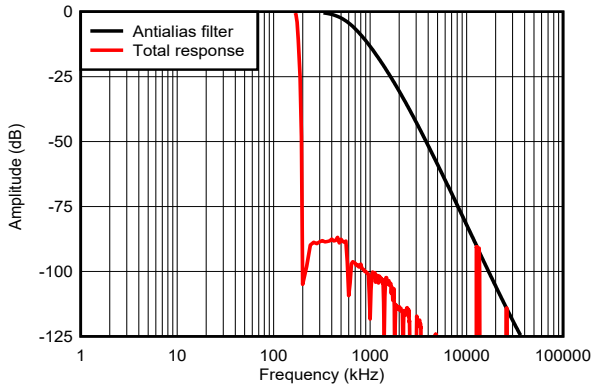

Figure 9-9. Antialias Filter Frequency Response

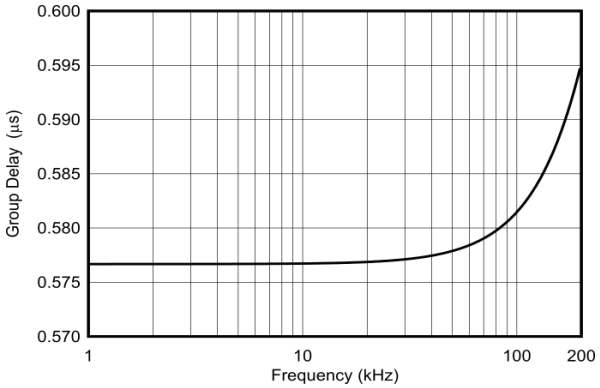

Figure 9-10. Antialias Filter Group Delay

Figure 9-11 shows the noise density of the antialias filter circuit, the noise density of the ADC, and the combined noise density of the filter and ADC. Noise density is the noise voltage per $\sqrt{Hz}$ of bandwidth plotted versus frequency.

Figure 9-12 shows the total noise from the 1-Hz start frequency up to the ADC final bandwidth. Below 200 Hz, noise is dominated by 1 / f voltage and current noise of the THS4551 amplifier. Above 200 Hz, noise is dominated by ADC noise. The combined noise of the filter and ADC over the 165-kHz bandwidth is 11.8 µV, meeting the 12-µV target value.

Improved low-frequency noise performance is possible by substituting the THP210 input driver with the THS4551. See the *THP210 and ADS127L11 Performance* application note for details.

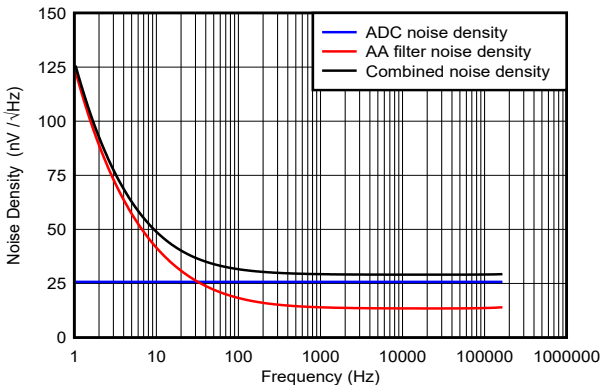

Figure 9-11. Noise Density

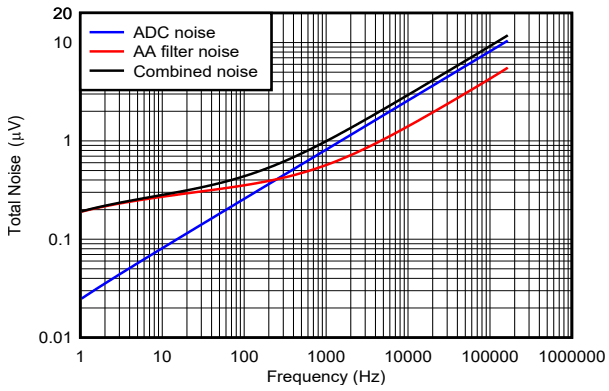

Figure 9-12. Total Noise

9.3 Power Supply Recommendations

The ADC has three analog power supplies and one digital power supply. The power supplies can be sequenced in any order and are tolerant of slow or fast power-supply voltage ramp rates. However, the analog and digital inputs must not exceed the respective AVDD1 and AVSS (analog) or IOVDD (digital) power-supply voltages under any circumstance.

Power-supply voltages AVDD1 and AVSS establish the range of the analog input. Bipolar input signals are only possible using bipolar supply voltages (such as AVDD1 = 2.5 V and AVSS = –2.5 V), and unipolar input signals are possible using unipolar supply voltages (such as AVDD1 = 5 V and AVSS = DGND). Operation in mid- and low-speed mode offer the option of operating AVDD1 at 3.3 V and 3 V (nominal) for reduced power consumption.

The AVDD2 power-supply voltage is with respect to AVSS. The IOVDD power-supply voltage is with respect to DGND. The ADC can be operated using a single 5-V voltage for all supplies (or one 3.3-V or 3-V supply voltage in mid- and low-speed mode operation) with AVSS = DGND. Table 9-7 shows the possible power-supply voltages for AVDD1, AVSS, AVDD2, and IOVDD. All voltages are nominal values.

Table 9-7. Power-Supply Configurations

MODE	ANALOG CONFIGURATION	AVDD1 – DGND	AVSS – DGND	AVDD2 – DGND	IOVDD – DGND
Max-speed	Unipolar	5 V	0 V	1.8 V to 5 V	1.8 V to 5 V
	Bipolar	2.5 V	–2.5 V	0 V to 2.5 V	1.8 V to 5 V
High-speed	Unipolar	5 V	0 V	1.8 V to 5 V	1.8 V to 5 V
	Bipolar	2.5 V	–2.5 V	0 V to 2.5 V	1.8 V to 5 V
Mid-speed	Unipolar	3.3 V to 5 V	0 V	1.8 V to 5 V	1.8 V to 5 V
	Bipolar	1.65 V to 2.5 V	–1.65 V to –2.5 V	0.15 V to 2.5 V	1.8 V to 5 V
Low-speed	Unipolar	3 V to 5 V	0 V	1.8 V to 5 V	1.8 V to 5 V
	Bipolar	1.5 V to 2.5 V	–1.5 V to –2.5 V	0.3 V to 2.5 V	1.8 V to 5 V

Power-supply bypassing at the device pins is essential to achieve data sheet performance. The ADC also requires capacitors for the CAPA and CAPD pins, and for the analog input and reference pins. Place the capacitors close to the device pins using short, direct traces with the smaller capacitor value placed closest to the device pins.

The recommended bypass components of the device pins are as follows:

1. AVDD1 to AVSS: Parallel combination of 1-µF and 0.1-µF capacitors across the pins
2. AVDD2 to AVSS: Parallel combination of 1-µF and 0.1-µF capacitors across the pins
3. IOVDD to DGND: Parallel combination of 1-µF and 0.1-µF capacitors across the pins
4. CAPA to AVSS: 1-µF capacitor placed across the pins
5. CAPD to DGND: 1-µF capacitor placed across the pins
6. REFP, REFN: Parallel combination of 1-µF and 0.1-µF capacitors across the pins
7. AINP, AINN: General recommendation 22-Ω resistors in series, followed by 2.2 nF across the pins, 220 pF from each pin to AVSS

Figure 9-13 shows the component placement for the device configured for unipolar power-supply operation.

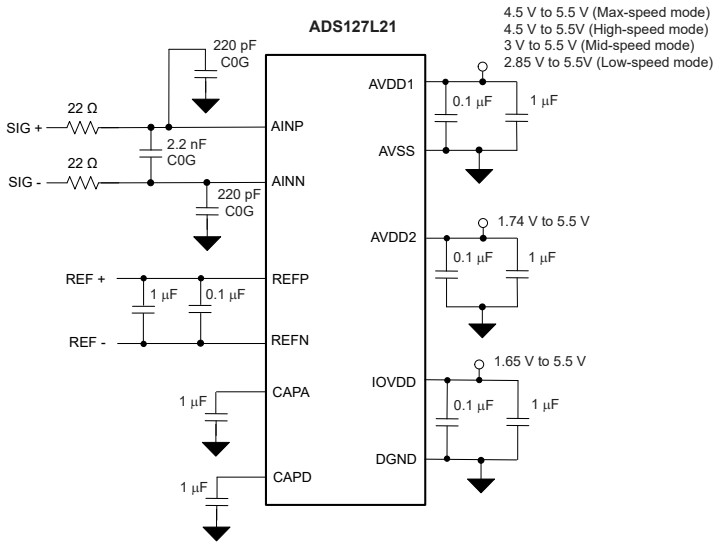

Figure 9-13. Device Capacitor Bypass Recommendation

9.4 Layout

9.4.1 Layout Guidelines

To achieve data sheet performance, use a minimum four-layer PCB board with the inner layers dedicated to ground and power planes. Best performance is achieved by combining the analog and digital grounds on a single, unbroken ground plane. In some layout geometries, however, using separate analog and digital grounds can be necessary to help direct digital currents away from the analog ground (such as pulsing LED indicators, relays, and so on). In this case, consider separate ground return paths for these loads. When separate analog and digital grounds are used, join the grounds at the ADC.

Use the power plane layer to route the power supplies to the ADC.

The top and bottom layers route the analog and digital signals. Route the input signal as a matched differential pair throughout the signal chain to reduce differential noise coupling. Avoid crossing or adjacent placement of digital signals with the analog signals. This layout is especially true for high-frequency digital signals such as the clock input, and SPI signals, SCLK, and SDO/$\overline{\text{DRDY}}$. The pin placement of the package minimizes the need to cross digital and analog signals.

Place the voltage reference close to the ADC. Orient the reference such that the reference ground pin is close to the ADC REFN pin. Place the reference input bypass capacitors directly at the ADC pins. Use reference bypass capacitors for each ADC in multichannel systems and connect the reference ground pin to the ground plane (or to AVSS in some bipolar supply systems) at one point and route REFP and REFN as paired traces to each ADC.

9.4.2 Layout Example

Figure 9-14 is a layout example based on the circuit diagram of Figure 9-8. A four-layer PCB is used, with the inner layers dedicated as ground and power planes. Cutouts are used on the plane layers under the amplifier input pins to reduce stray capacitance to increase amplifier phase margin. Thermal vias for the ADS127L21 and THS4551 WQFN package thermal pad are not used to enable bypass capacitor placement on the bottom layer underneath the devices. Place the smaller of the parallel supply bypass capacitors closest to the device supply pins.

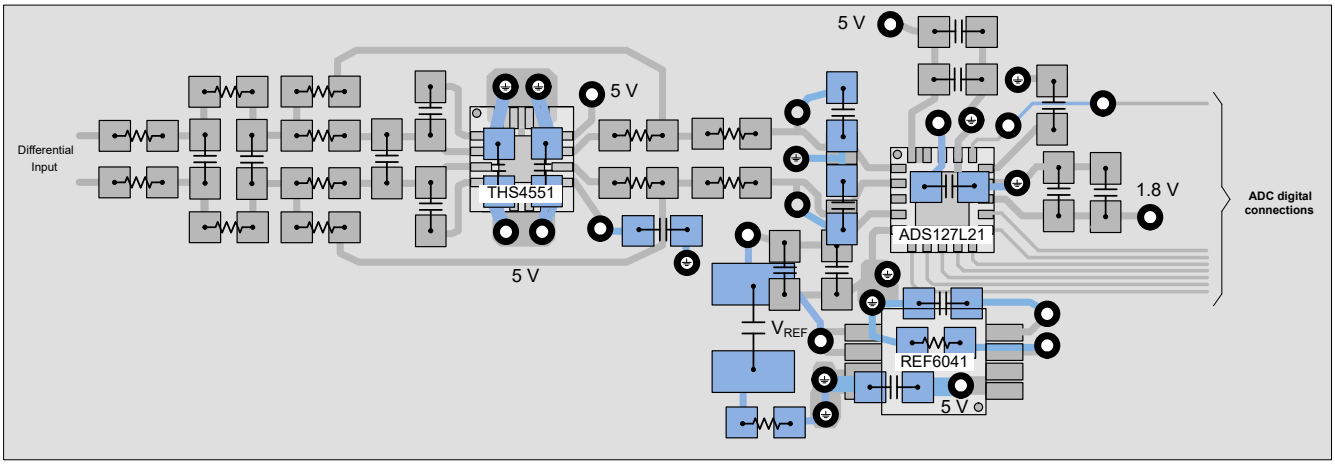

Figure 9-14. Layout Example of a Typical Application Circuit

See the *QFN and SON PCB Attachment* application note for details of attaching the WQFN package to the printed circuit board.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *THP210 and ADS127L11 Performance* application note
- Texas Instruments, *PGA855 Low-Noise, Wide-Bandwidth, Fully Differential PGA* data sheet
- Texas Instruments, *ADS127L11 in Simultaneous-Sampling Systems* application brief
- Texas Instruments, *ADS127L11 CRC Calculator*
- Texas Instruments, *Four-Channel Synchronous IEPE Vibration Sensor Interface* reference design
- Texas Instruments, *THS4551 Low-Noise, Precision, 150-MHz, Fully Differential Amplifier* data sheet
- Texas Instruments, *REF60xx High-Precision Voltage Reference with Integrated ADC Drive Buffer* data sheet
- Texas Instruments, *Design Methodology for MFB Filters in ADC Interface Applications* application note
- Texas Instruments, *QFN and SON PCB Attachment* application note

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.4 Trademarks

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS127L21IRUKR	ACTIVE	WQFN	RUK	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	127L21	Samples
ADS127L21IRUKT	ACTIVE	WQFN	RUK	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	127L21	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

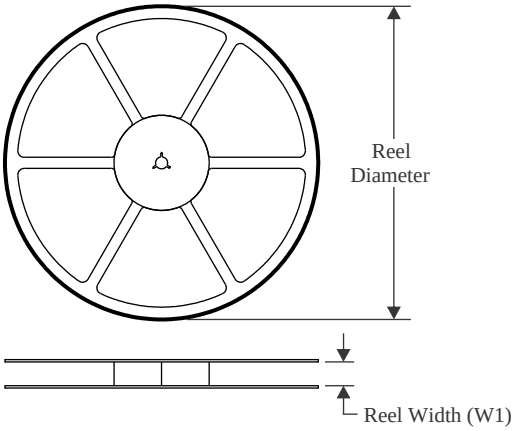
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

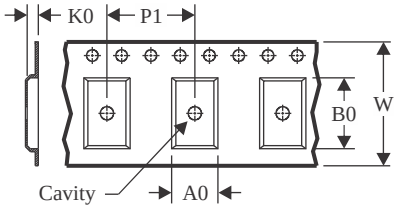
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

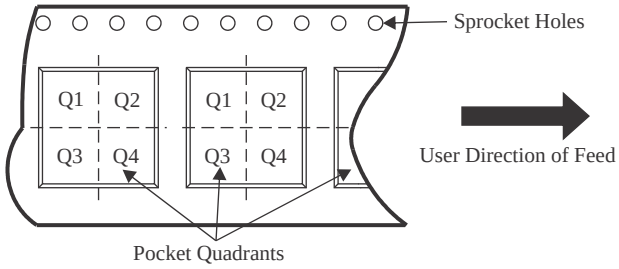


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

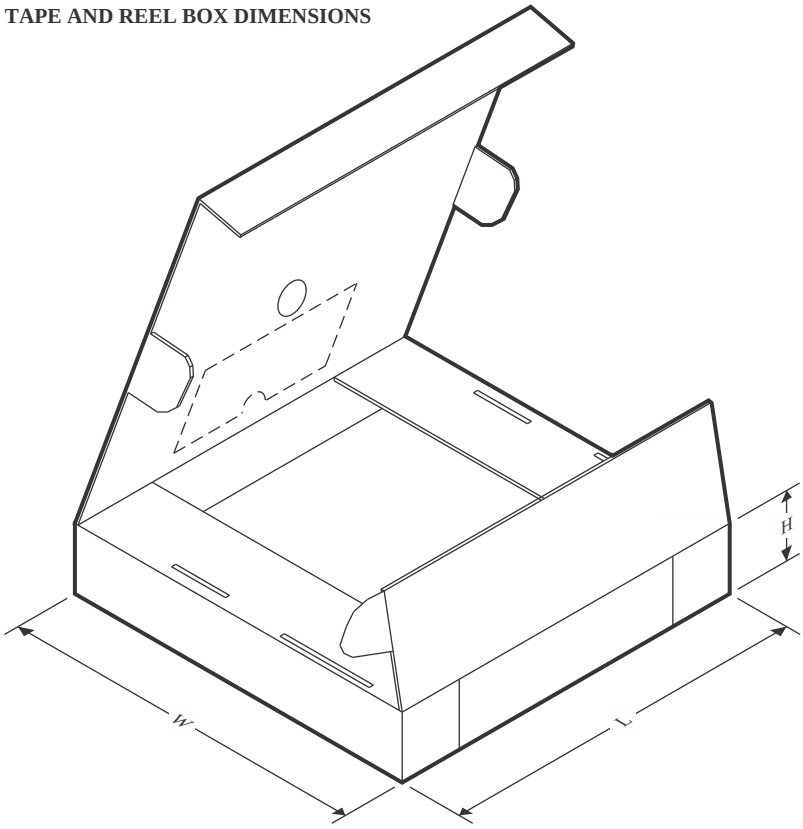
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS127L21IRUKR	WQFN	RUK	20	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS127L21IRUKT	WQFN	RUK	20	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

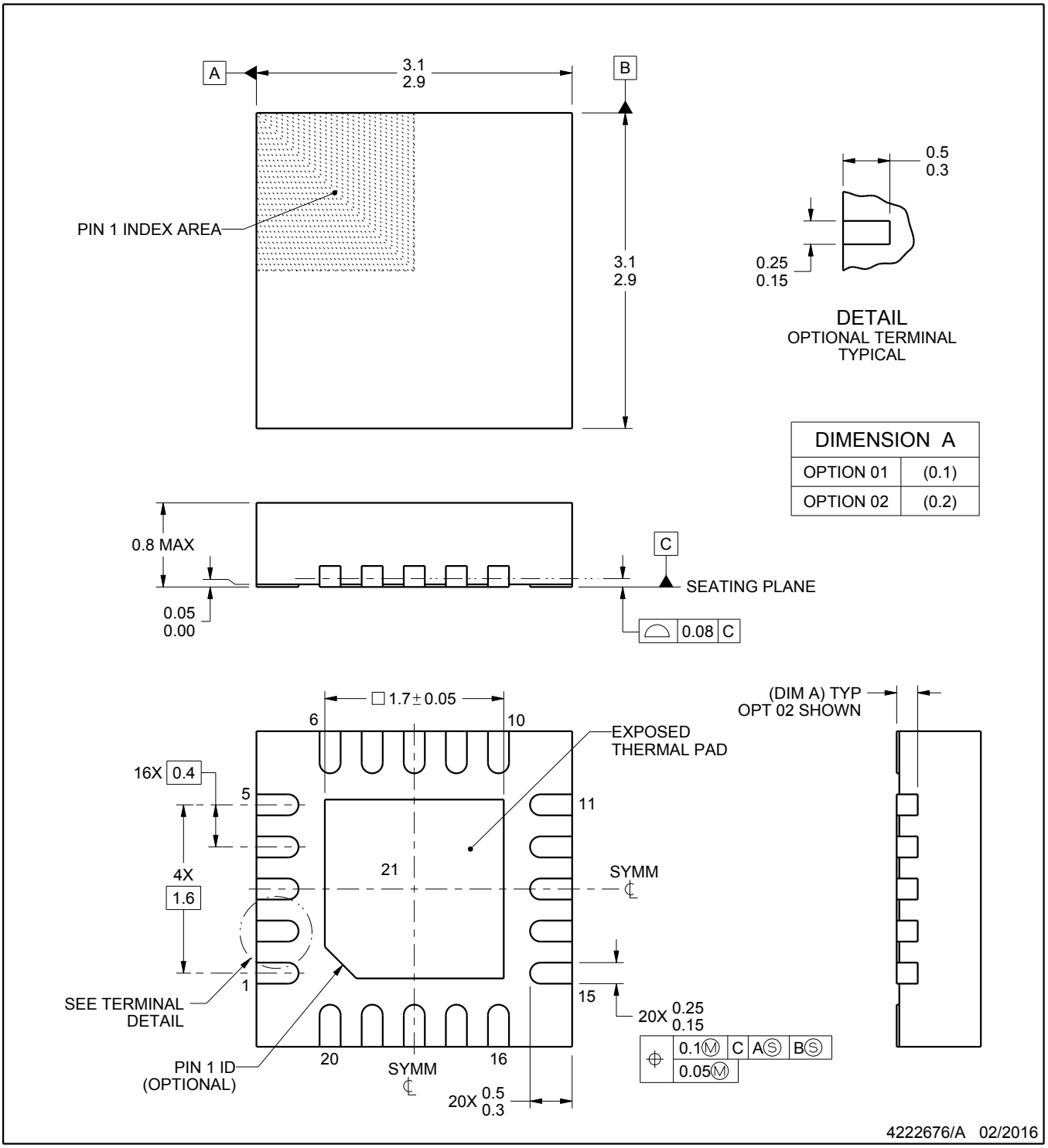
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS127L21IRUKR	WQFN	RUK	20	3000	367.0	367.0	35.0
ADS127L21IRUKT	WQFN	RUK	20	250	210.0	185.0	35.0

PACKAGE OUTLINE

RUK0020B

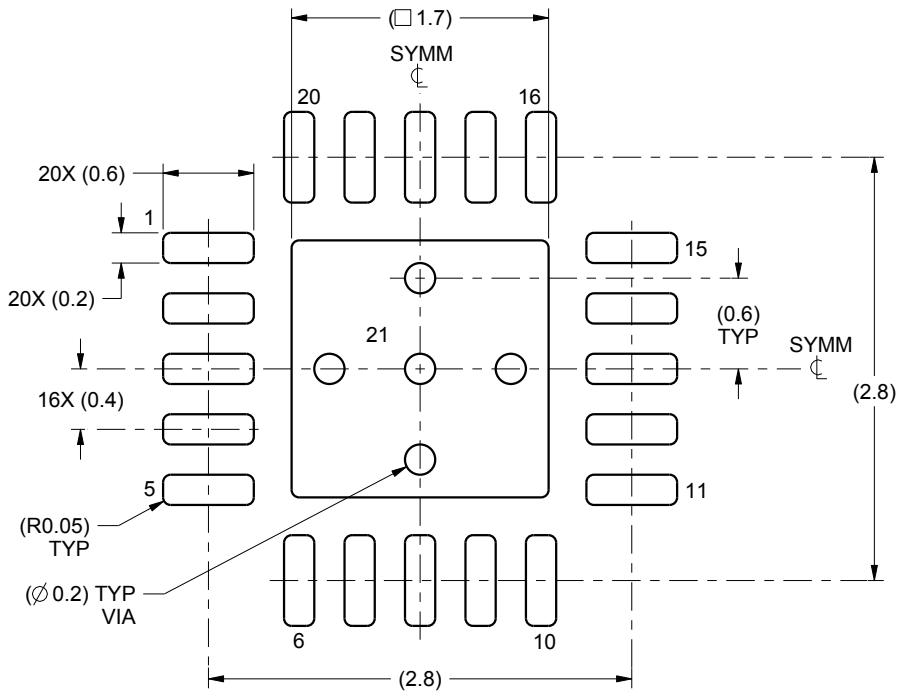
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

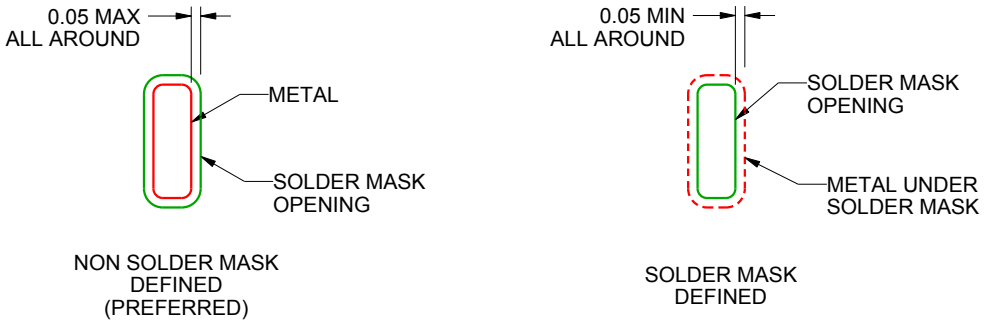


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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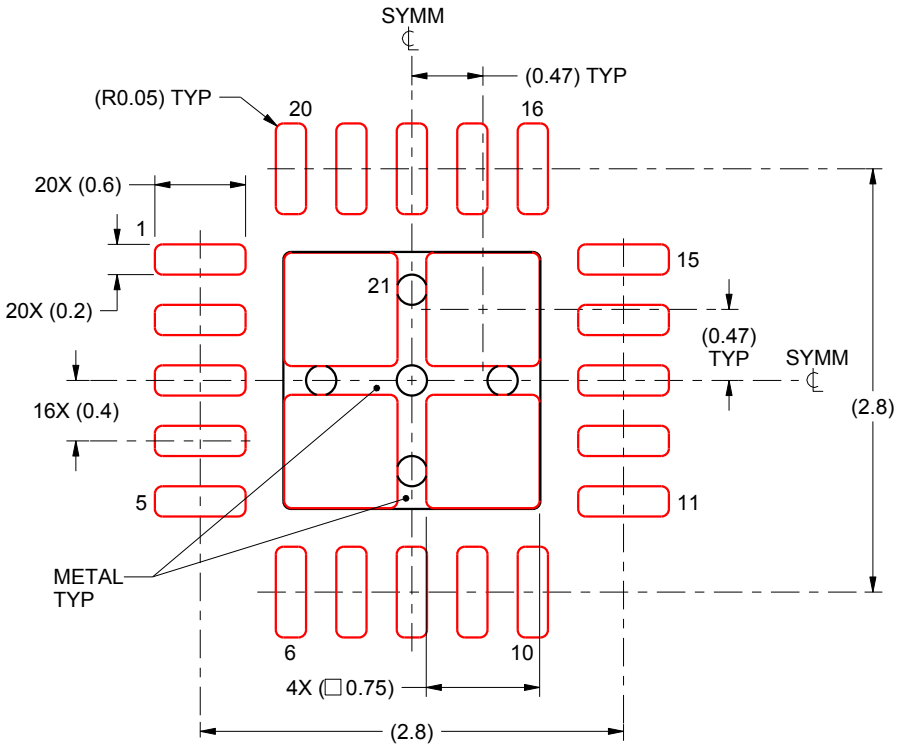
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 21:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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