D0011E - Assignment 2

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1 Part 1 - MIPS instructions

$r1 <= 1
addi $r1, $r0, 0x1
0010 0000 0000 0001 0000 0000 0000 0001

$r2 <= 2
addi $r2, $r1, 0x1
0010 0000 0010 0010 0000 0000 0000 0001

$r3 <= $r1 + $r2
add $r3, $r1, $r2
0000 0000 0010 0010 0001 1000 0010 0000

$r4 <= 1 if $r3 < 4 else 0
slti $r4, $r3, 0x4
0010 1000 0110 0100 0000 0000 0000 0100

$r5 <= 1 if $r3 < $r2 else 0
slt $r5, $r3, $r2
0000 0000 0110 0010 0010 1000 0010 1010

$r6 <= $r3 « 1
sll $r6, $r3, 1
0000 00– —0 0011 0011 0000 0100 0000

$r7 <= $r3 « $r1
sllv $r7, $r3, $r1
0000 0000 0010 0011 0011 1— –00 0100

$r8 <= $r0 –$r2
sub $r8, $r0, $r2
0000 0000 0000 0010 0100 0000 0010 0010

$r9 <= $r8 « 10
sll $r9, $r8, 0xA
0000 00– —0 1000 0101 0010 0100 0000

$r9 <= $r9 » 4
sra $r9, $r9, 0x4
0000 00– —0 1001 0100 1001 0000 001a

$r9 <= $r9 » 6
sra $r9, $r9, 0x6
0000 00– —0 1001 0100 1001 1000 0011

$r10 <= -10
-10 = 10110 (2's complement)
addi $r10, $r0, 0x15
0010 0000 0000 1010 1111 1111 1111 0110

$r11 <= 0x12340000
lui $r11, 0x1234
0011 11– —0 1011 0001 0010 0011 0100

$r11 <= $r11 | 0x5678
ori $r11, $r11, 0x5678
0011 0101 0110 1011 0101 0110 0111 1000

$r12 <= 0x1234
addi $r12, $0, 0x1234
0010 0001 1000 0000 0001 0010 0011 0100

$r12 <= $r12 « 16
sll $r12, $r12, 0x10
0000 00– —0 1100 0110 0100 0000 0000

$r12 <= $r12 | 0x5678
ori $r12, $r12, 0x5678
0011 0101 1000 1100 0101 0110 0111 1000

$r13 <= $r11 – $r12
sub $r13, $r11, $r12
0000 0001 0110 1100 0110 1000 0010 0011

$r14 <= $r11 and 0xFFFF
andi $r14, $r11, 0xFFFF
0011 0001 0110 1110 1111 1111 1111 1111

$r15 <= $r14 « $r2
srlv $r15, $r14, $r2
0000 0001 1100 0010 0111 1000 0000 0110

1.1 Contents of registers $r1 – $r15

```
$r1  = 0x00000001
$r2  = 0x00000002
$r3  = 0x00000003
$r4  = 0x00000001
$r5  = 0x00000000
$r6  = 0x00000006
$r7  = 0x00000006
$r8  = 0xFFFFFFFE
$r9  = 0xFFFFFFFE
$r10 = 0xFFFFFFF6
$r11 = 0x12345678
$r12 = 0x12345678
$r13 = 0x00000000
$r14 = 0x00005678
$r15 = 0x000159D0
```

2 Part 2 - MIPS Processor

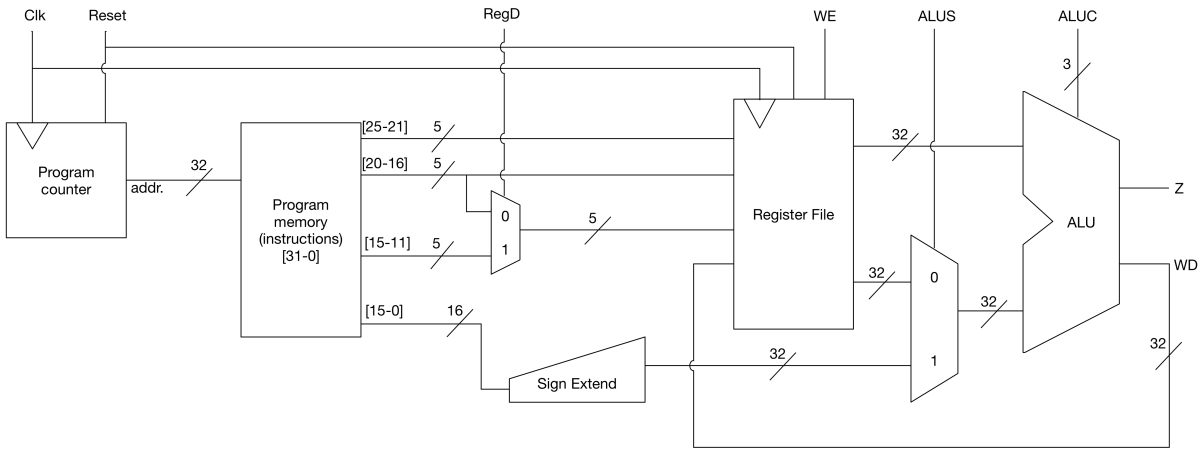

Figure 1: RTL schematic

3 Part 3 - Truth table of control signals

Instruction	opcode	funct	WE	ALUC	RegD	ALUS
ADD	0x0	0x20	1	010	1	0
ADDI	0x8	-	1	010	0	1
SUB	0x0	0x22	1	110	1	0
SLT	0x0	0x2A	1	111	1	0
SLTI	0xA	-	1	111	0	1
AND	0x0	0x24	1	000	1	0
OR	0x0	0x25	1	001	1	0

Table 1: Truth table of control signalsand instructions