Zynq-7000 All Programmable SoC Family Product Tables and Product Selection Guide







Zynq®-7000 All Programmable SoC Family

				(Cost-Optimi	zed Device	S								
		Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100			
		Part Number	XC7Z007S	XC7Z012S	XC7Z014S	XC7Z010	XC7Z015	XC7Z020	XC7Z030	XC7Z035	XC7Z045	XC7Z100			
			Single-Core		Dual-Core ARM			Dual-Core ARM							
	Processor Core			rtex™-A9 N		Cortex-A9 MPCore			Cortex-A9 MPCore						
			U	p to 766MF			Up to 866MHz			Up to 1GHz ⁽¹⁾					
bS)	Pr	ocessor Extensions	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per processor												
Processing System (PS)	L1 Cache		32KB Instruction, 32KB Data per processor												
ter	L2 Cache		512KB												
Sys		On-Chip Memory						256KB							
ng B		Memory Support ⁽²⁾	DDR3, DDR3L, DDR2, LPDDR2												
ssi	External Static	Memory Support ⁽²⁾	2x Quad-SPI, NAND, NOR												
900		DMA Channels	8 (4 dedicated to PL)												
P		Peripherals	2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO												
	Peripherals	s w/ built-in DMA ⁽²⁾	2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO												
		Security ⁽³⁾							st Stage Boot Loader,						
		AES and SHA 256b Decryption and Authentication for Secure Boot													
	Dr	ocessing System to	2x AXI 32b Master, 2x AXI 32b Slave												
	Programmable Lo	4x AXI 64b/32b Memory													
		& Interrupts Only)	AXI 64b ACP												
			16 Interrupts												
	7 S	Series PL Equivalent	Artix®-7	Artix-7	Artix-7	Artix-7	Artix-7	Artix-7	Kintex®-7	Kintex-7	Kintex-7	Kintex-7			
		Logic Cells		55K	65K	28K	74K	85K	125K	275K	350K	444K			
٦)	Loc	ok-Up Tables (LUTs)	14,400	34,400	40,600	17,600	46,200	53,200	78,600	171,900	218,600	277,400			
))		Flip-Flops	28,800	68,800	81,200	35,200	92,400	106,400	157,200	343,800	437,200	554,800			
ogo		Total Block RAM	1.8Mb	2.5Mb	3.8Mb	2.1Mb	3.3Mb	4.9Mb	9.3Mb	17.6Mb	19.1Mb	26.5Mb			
e L		(# 36Kb Blocks)	(50)	(72)	(107)	(60)	(95)	(140)	(265)	(500)	(545)	(755)			
ap		DSP Slices	66	120	170	80	160	220	400	900	900	2,020			
μL		PCI Express®	_	Gen2 x4		_	Gen2 x4		Gen2 x4	Gen2 x8	Gen2 x8	Gen2 x8			
Programmable Logic (PL)	Analog Mixed Sig	nal (AMS) / XADC ⁽²⁾		_				•	17 Differentia	•					
o g		Security ⁽³⁾			ES & SHA 25	6b Decrypt		or Secure Prog							
-α-		Commercial		-1			-1			-1		-1			
	Speed Grades	Extended Industrial		-2			-2,-3			-2,-3 -1, -2, -2L		-2			
			-1, -2			-1, -2, -1L			-1, -2, -2L						

Notes:



^{1.1} GHz processor frequency is available only for -3 speed grades for devices in flip-chip packages. See DS190, Zynq-7000 All Programmable SoC Overview for details.

^{2.} Z-7007S and Z-7010 in CLG225 have restrictions on PS peripherals, memory interfaces, and I/Os. Please refer to UG585, Zynq-7000 All Programmable SoC Technical Reference Manual for more details.

^{3.} Security block is shared by the Processing System and the Programmable Logic.

Zynq®-7000 All Programmable SoC Family HR I/O, HP I/O, PS I/O, and Transceivers (GTP or GTX)

		Cost-Optimized Devices							Mid-Range Devices				
	Device Name	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100		
Package	Dimensions			HR I/O,		HR I/O, HP I/O							
Footprint (mm) ⁽¹⁾		PS I/O ⁽²⁾ , GTP Transceivers							PS I/O ⁽²⁾ , GTX Transceivers				
CLG225	13x13	54, 0 84 ⁽³⁾ , 0			54, 0 84 ⁽³⁾ , 0								
CLG400	17x17	100, 0		125, 0	100, 0		125, 0						
CL0400	1//1/	128, 0		128, 0	128, 0		128, 0						
CLG484	19x19			200, 0			200, 0						
CLG404	13/13			128, 0			128, 0						
CLG485 ⁽⁴⁾	19x19		150, 0			150, 0							
020 103	IJAIJ		128, 4			128, 4							
SBG485 / SBV485 ⁽⁴⁾	19x19							50, 100					
								128, 4					
FBG484 / FBV484	23x23							100, 63					
,,								128, 4					
FBG676 / FBV676 ⁽¹⁾	27x27							100, 150	100, 150	100, 150			
· ·								128, 4	128, 8	128, 8			
FFG676 / FFV676 ⁽¹⁾	27x27							100, 150	100, 150	100, 150			
,								128, 4	128, 8	128, 8			
FFG900 / FFV900	31x31								212, 150	212, 150	212, 150		
									128, 16	128, 16	128, 16		
FFG1156 / FFV1156	35x35										250, 150		
•											128, 16		

Notes:

^{1.} Devices in the same package are footprint compatible. FBG676 / FBV676 and FFG676 / FFV676 are also footprint compatible.

^{2.} PS I/O count does not include dedicated DDR calibration pins.

^{3.} PS DDR and PS MIO pin count is limited by package size. See DS190, Zyng-7000 All Programmable SoC Overview for details.

CLG485 and SBG485 / SBV485 are pin-to-pin compatible. See product data sheets and user guides for more details.
 See <u>DS190</u>, Zynq-7000 All Programmable SoC Overview for package details.

Zynq®-7000 Device Footprint Compatibility

13mm-35mm

HR I/O, PS I/O, and GTP Transceivers

	Footprint Dimensions (mm)	13x13	17x17	19x19	19x19	23x23	27x27	27x27	31x31	35x35
	Unique Footprint	CLG225	CLG400	CLG484	CLG485	FBG484	FBG676	FFG676	FFG900	FFG1156
	Z-7007S	54, 84, 0	100, 128, 0							
	Z-7012S				150, 128, 4					
	Z-7014S		125, 128, 0	200, 128, 0						
	Z-7010	54, 84, 0	100, 128, 0							
	Z-7015				150, 128, 4					
	Z-7020		125, 128, 0	200, 128, 0						
HR I/O, HP I/O, PS I/O, GTX Transceivers										
	Z-7030				50, 100, 128, 4	100, 63, 128, 4	100, 150, 128, 4	100, 150, 128, 4		
	Z-7035						100, 150, 128, 8	100, 150, 128, 8	212, 150, 128, 16	

The footprint compatibility range is indicated by shading per column.



100, 150, 128, 8 | 100, 150, 128, 8 | 212, 150, 128, 16

212, 150, 128, 16 250, 150, 128, 16

Z-7045

Z-7100

Zynq®-7000 Family Speed Grades

Device Name⁽¹⁾

	Speed Grade	Z-7007S	Z-7012S	Z-7014S	Z-7010	Z-7015	Z-7020	Z-7030	Z-7035	Z-7045	Z-7100
С	-1	•	•	•	•	•	•	•	•	•	•
Е	-2	•	•	•	•	•	•	•	•	•	•
	-3	-	-	-	•	•	•	•	•	•	_
	-1	•	•	•	•	•	•	•	•	•	•
	-2	•	•	•	•	•	•	•	•	•	•
'	-1L	_	_	_	•	•	•	_	_	_	-
	-2L	-	-	_	-	-	_	•	•	•	•

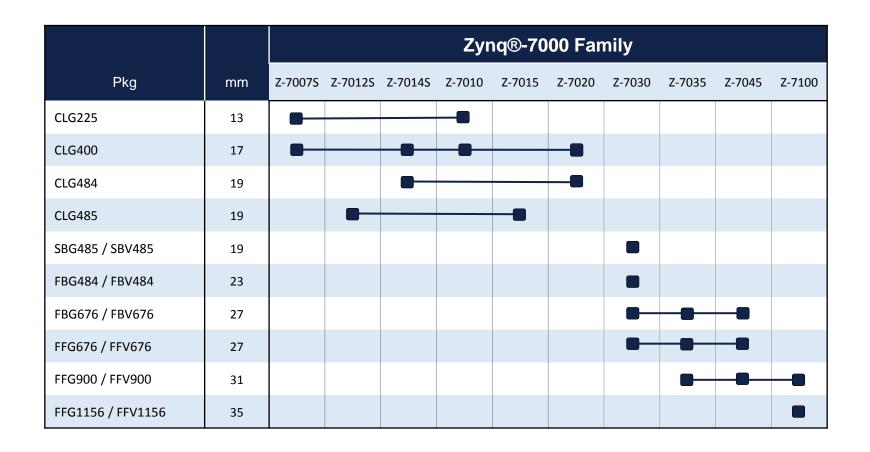
Notes

1. For full part number details, see the Ordering Information section in <u>DS190</u>, Zynq®-7000 All Programmable SoC Overview.

- Available
- Not offered

C = Commercial (Tj =
$$0^{\circ}$$
C to +85°C)
E = Extended (Tj = 0° C to +100°C)
I = Industrial (Tj = -40° C to +100°C)

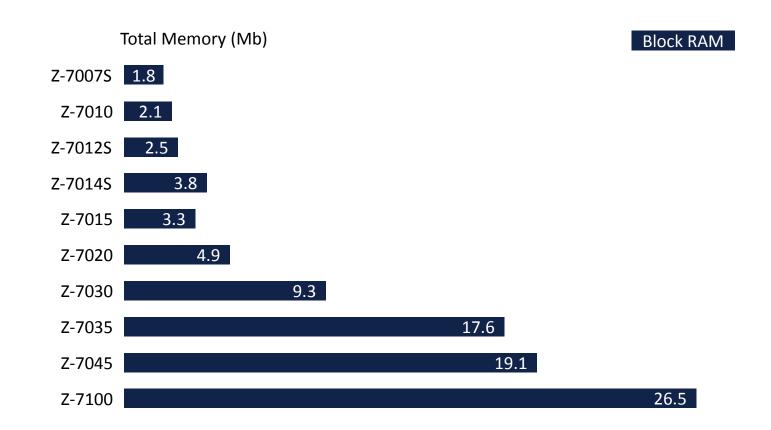
Zynq®-7000 Family Device Migration Table



Memory



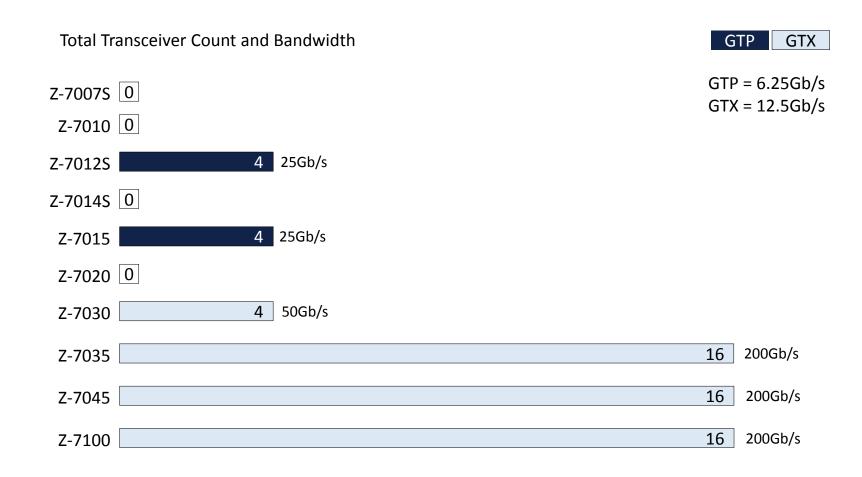
The Zynq®-7000 family has block RAM (dual-port, programmable, built-in optional error correction), which shares nothing but stored data.



Transceiver Count and Bandwidth



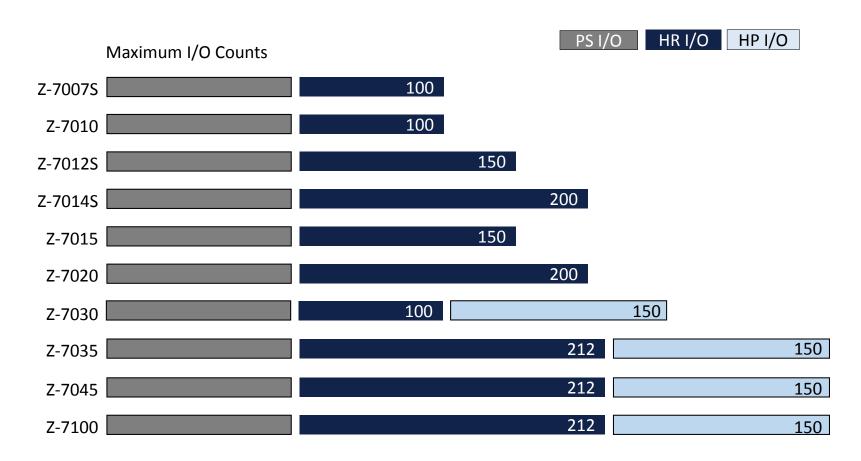
The serial transceivers in the Zynq-7000 family include the proven on-chip circuits required to provide optimal signal integrity in real-world environments, at data rates up to 6.25Gb/s (GTP) and 12.5Gb/s (GTX).



I/O Count



The I/Os are classified as PS I/O, high-range (HR) I/O, and high-performance (HP) I/O. The PS I/Os are composed of multi-use I/O (MIO), which support 1.8V to 3.3V standards. The HR I/Os are reduced-feature I/Os, providing voltage support from 1.2V to 3.3V. The HP I/Os are optimized for highest performance operation, from 1.2V to 1.8V.



Notes:

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

^{1.} The PS I/O count is composed of 54 I/Os (excluding DDR interface), which are used to communicate to external components, referred to as multiplexed I/O (MIO).

Zyng®-7000 Family Device Ordering Information



Xilinx

Commercial

Series

Zynq

Value

Index

Speed Grade -1: Slowest

(Z-7007S

Z-7012S Z-7014S only)

Single Core Indicator -L1: Low Power

-2: Mid -L2: Low Power

-3: Fastest

FF

CL: Wire-bond Molded V: RoHS 6/6

(.8mm)

SB: Flip-chip Lidless (.8mm)

FB: Flip-chip Lidless

(1mm)

FF: Flip-chip Lidded (1mm)

Footprint

G(CLG) = RoHS 6/6G (SBG, FBG, FFG) =

RoHS 6/6 with

exemption 15

Package Pin Count

###

Temperature Grade

(C, E, I)

C = Commercial (Tj = 0°C to +85°C)E = Extended (Ti = 0°C to +100°C)

I = Industrial (Ti = -40°C to +100°C)

Refer to DS190, Zynq-7000 All Programmable SoC Overview for additional information.

References

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DS190, Zyng®-7000 All Programmable SoC Overview
DS187, Zynq-7000 AP SoC (Z-7007S, Z-7012S, Z-7014S, Z-7010, Z-7015, and Z-7020): DC and AC Switching Characteristics
DS191, Zynq-7000 AP SoC (Z-7030, Z-7035, Z-7045, and Z-7100):DC and AC Switching Characteristics
DS176, Zyng-7000 AP SoC and 7 Series Devices Memory Interface Solutions (v4.0)
UG585, Zyng-7000 All Programmable SoC Technical Reference Manual
UG865, Zyng-7000 All Programmable SoC Packaging and Pinout Product Specification
UG471, 7 Series FPGAs SelectIO™ Resources User Guide
UG472, 7 Series FPGAs Clocking Resources User Guide
UG473, 7 Series FPGAs Memory Resources User Guide
UG474, 7 Series FPGAs Configurable Logic Block User Guide
UG479, 7 Series FPGAs DSP48E1 Slice User Guide
UG480, 7 Series FPGAs and Zyng-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS ADC User Guide
UG482, 7 Series FPGAs GTP Transceivers User Guide
UG821, Zyng-7000 All Programmable SoC Software Developers Guide
UG933, Zyng-7000 All Programmable SoC PCB Design Guide
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For a complete list of available documentation, go to: http://www.xilinx.com/products/silicon-devices/soc/zynq-7000.html#documentation

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

XMP097 (v1.2)

