Georgia Institute of Technology
School of Computer Science
CS 3220: Fall 2017
Project 3: Pipelining [100 + 25 Points]

Due: 11:55 PM, December 4^{th}, 2017

Project Description

In this project, you will design a five-stage pipelined processor and synthesize it on your FPGA board. The processor should be able to support the entire set of instructions described in the project-ISA-description.pdf. You can start from your own single-cycle processor. You should consider all the hazards and insert bubbles if necessary. Implementing forwarding is not mandatory but will lead to 25 points of extra credit.

To get you started, we have provided you with a project2.zip in the T-Square repository with settings, timing requirements, and some of the Verilog codes for the design. It is highly recommended to begin work on the processor design immediately.

What to hand in via T-Square?

There are two deliverables for this project:

1. A brief 1-page report (PDF). You should write this report by yourself (your partner will write his/her own report and submit it). The report should describe the approach taken, which problems were encountered and how they were fixed, and what the student's own contribution (i.e. which member of the group did what) to the project was. Note that it is fine if the two members of the group worked together (as in, sat together and got something working), and it is OK to say so in the report. If your report is missing, you will lose 50% of the points.

2. Quartus project (ZIP).

You should adhere with the following format and organization:

- Create a directory and name it PipeProc-[Student's Full Name] (*e.g.* PipeProc-AmirYazdanbakhsh)
- Create a subdirectory named report and include your report file. The report file has to be named PipeProc-[Student's Full Name].pdf (*e.g.* PipeProc-AmirYazdanbakhsh.pdf).

- Create another subdirectory name quartus and include all the Quartus project files and subdirectories.
- Archive the entire directory PipeProc-[Student's Full Name] into PipeProc-[Student's Full Name].zip (*e.g.* PipeProc-AmirYazdanbakhsh.zip) and submit this zip file to T-Square.

Note 1. You get zero points if you do not follow the naming format.

Note 2. Your Quartus project has to be synthesized on FPGA without any other modifications.

Note 3. Please use **Quartus II Web Edition 13.0sp1** from Altera. Here's a quick installation guide: `https://www.cc.gatech.edu/~hadi/teaching/cs3220/doc/quick-start/quick-start-de0.pdf`.

Note 4. This project is a **team** project. As such, you must work together with your teammate. The zip file you submit should the same as the one submitted by your teammate. However, each person has to write their own report. Identical reports in a team get **zero** points.

Note 5. Double check your submission to T-Square and make sure that all the files are correctly uploaded. We can not accept any missing files after the deadline. The best practice would be to download the zip file from T-Square and test your work again to make sure it is correct.

Note 6. Testbench is not required, but is encouraged to verify your design.