Yu-Cheng Wu

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EDUCATION

National Taiwan University Sep.2019 -- present
Bachelor of Electrical Engineering - CGPA - 3.92/4.3

COURSES

- Computer Programming
- Data Structure
- Algorithms
- Digital Circuit Lab
- Computer Architecture
- Integrated Circuit Design
- Machine Learning
- Introduction to EDA

PROJECTS

RISC-V CPU | Computer Architecture Final Project Dec.2021 -- Jan.2022

- Design a **five-stage pipeline CPU**.
- The CPU supports **single-cycle instructions defined in the RISC-V instruction set** including 'auipc', 'jal(r)', 'beq', 'lw', 'sw', 'add(i)', 'sub', 'srli', 'slli', 'slti'.
- Design a **multi-cycle instruction 'mul' for 32-bit multiplication**.

CIM-Based DNN | Access IC Lab (Prof. An-Yeu Wu) Sep.2021 -- present

- **Recommendation by Prof. An-Yeu Wu for MOST University Student Research Program**.
- **Hardware performance and accuracy analysis** for different CIM-based DNNs.
- Implement **dynamic inference** according to different conductance variations with **multi-exit architecture**.

Stochastic Neural Networks | ALCom Lab (Prof. Jie-Hong Jiang) Sep.2021 -- present

- Using **stochastic computing** for DNN inference.
- **Eliminate APCs by combining addition and activation**, which dramatically reduces latency.
- Currently working on **logic synthesis for stochastic neural newtworks**.

TECHNICAL SKILLS

Skilled: Python, C++, Verilog
Basic: RISC-V, SQL

EXTRACURRICULAR

Men's Varsity Badminton Team Sep.2019 -- present
Captain

- Schedule the training program.
- Specialized in men's single.