RTL Report

Testbench	Pass
Clock Cycle	10(ns)
Total Time	2140(ns)

Synthesis Report

Testbench	Pass
Clock Cycle	6(ns)
Cell Area	142871.853352(um^2)(**Total cell area**)
Total Time	1284(ns)
Area*$Time^2$	2.355e11(um^2 * ns^2)

APR Report

Testbench	Pass
Clock Cycle	9.13(ns)
Cell Area	178603.823(um^2)(**Total area of Core)**
Total Time	1955.96(ns)
Area*$Time^2$	6.833e11(um^2 * ns^2)

How to report area in Design Vision?

➔ report_area > autoseller_area.txt, find **Total cell area.**

How to report area in Innovus?

➔ File > Report > Summary > choose Text only, file name: **summaryReport.rpt**>OK, find **Total area of Core.**

RTL Simulation Result (截圖)

```
                                Instances  Unique
               Modules:                18       3
               Registers:             140      50
               Scalar wires:           21       -
               Vectored wires:        182       -
               Always blocks:          41      11
               Initial blocks:          8       8
               Cont. assignments:      53      10
               Pseudo assignments:    115      17
               Simulation timescale:  10ps
       Writing initial simulation snapshot: worklib.tb:v
Loading snapshot worklib.tb:v ..................... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
./dat/ref1.dat, ./dat/query1.dat and ./dat/golden1.dat were used for this simulation.


====================== The test result is ..... PASS ========================


        ************************************************
        **                                            **      /|____|\
        **             Congratulations !!             **    ((´-___-` ))
        **                                            **   ///         \\\
        **  All data have been generated successfully! **  /||           ||\
        **                                            **  w|\ m       m /|w
        ************************************************    \(o)____(o)/


================================================================================
   total cycle:         213
Simulation complete via $finish(1) at time 2140 NS + 0
```

Synthesis Simulation Result (截圖)

```
                                Instances  Unique
               Modules:            12984     529
               UDPs:                2205      12
               Primitives:         27939      10
               Timing outputs:     13680      32
               Registers:           1967     175
               Scalar wires:       15639       -
               Expanded wires:         4       2
               Always blocks:          3       3
               Initial blocks:         8       8
               Pseudo assignments:     1       1
               Timing checks:      18169    1928
               Interconnect:       33048       -
               Delayed tcheck signals:   5406    1834
               Simulation timescale:     1ps
       Writing initial simulation snapshot: worklib.tb:v
Loading snapshot worklib.tb:v ..................... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
./dat/ref1.dat, ./dat/query1.dat and ./dat/golden1.dat were used for this simulation.


====================== The test result is ..... PASS ========================


        ************************************************
        **                                            **      /|____|\
        **             Congratulations !!             **    ((´-___-` ))
        **                                            **   ///         \\\
        **  All data have been generated successfully! **  /||           ||\
        **                                            **  w|\ m       m /|w
        ************************************************    \(o)____(o)/


================================================================================
   total cycle:         213
Simulation complete via $finish(1) at time 1284 NS + 0
```

Synthesis Timing Report

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
        -sort_by group
Design : SW
Version: R-2020.09-SP5
Date   : Wed Jun 15 22:49:02 2022
****************************************

 # A fanout number of 1000 was used for high fanout net computations.

Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

  Startpoint: PEs[1].genblk1.PE_single/last_A_base_reg[1]
              (rising edge-triggered flip-flop clocked by clk)
  Endpoint: row_highest_columns_reg[2][1]
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  SW                 tsmc13_wl10           slow

  Point                                                    Incr       Path
  -----------------------------------------------------------------------------
  clock clk (rise edge)                                    0.00       0.00
  clock network delay (ideal)                              1.00       1.00
  PEs[1].genblk1.PE_single/last_A_base_reg[1]/CK (DFFRX1)
                                                           0.00 #     1.00 r
  PEs[1].genblk1.PE_single/last_A_base_reg[1]/Q (DFFRX1)
                                                           0.41       1.41 r
  U19746/Y (XNOR2X1)                                       0.18       1.59 r
  U12174/Y (CLKAND2X3)                                     0.22       1.80 r
  U19748/Y (INVX12)                                        0.11       1.92 f
  U19749/Y (NAND2X1)                                       0.12       2.03 r
  U19750/Y (OAI21X1)                                       0.14       2.17 f
  U19752/Y (OAI2BB1X2)                                     0.17       2.34 f
  U19753/Y (OAI22X1)                                       0.24       2.58 r
  U16951/Y (OAI2BB1X1)                                     0.31       2.89 r
  U19784/Y (XNOR2X1)                                       0.25       3.14 f
  U19785/Y (OR2X4)                                         0.17       3.31 f
  U19790/Y (OAI22X1)                                       0.15       3.46 r
  U19791/Y (XNOR2X1)                                       0.40       3.86 r
  U19815/Y (INVX3)                                         0.11       3.96 f
  U19848/Y (OAI22X1)                                       0.26       4.22 r
  U17131/Y (OAI22XL)                                       0.26       4.48 f
  U19850/Y (AOI21X2)                                       0.22       4.70 r
  U19853/Y (NAND3X1)                                       0.12       4.82 f
  U19856/Y (OAI21X1)                                       0.18       5.00 r
  U17211/Y (NOR3BX1)                                       0.20       5.21 r
  U12606/Y (AND2X4)                                        0.21       5.42 r
  U12782/Y (NAND2X1)                                       0.11       5.53 f
  U21359/Y (NAND3X2)                                       0.15       5.67 r
  U11792/Y (CLKINVX1)                                      0.15       5.82 f
  U22355/Y (AOI22X1)                                       0.20       6.03 r
  U13883/Y (AOI21X2)                                       0.09       6.12 f
  U14616/Y (OAI21X2)                                       0.12       6.24 r
  U22359/Y (OAI2BB1X4)                                     0.15       6.39 r
  U22360/Y (NAND2X6)                                       0.16       6.55 f
  U22637/Y (OAI22X1)                                       0.21       6.76 r
  row_highest_columns_reg[2][1]/D (DFFRX1)                 0.00       6.76 r
  data arrival time                                                   6.76

  clock clk (rise edge)                                    6.00       6.00
  clock network delay (ideal)                              1.00       7.00
  clock uncertainty                                       -0.10       6.90
  row_highest_columns_reg[2][1]/CK (DFFRX1)                0.00       6.90 r
  library setup time                                      -0.14       6.76
  data required time                                                  6.76
  -----------------------------------------------------------------------------
  data required time                                                  6.76
  data arrival time                                                  -6.76
  -----------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

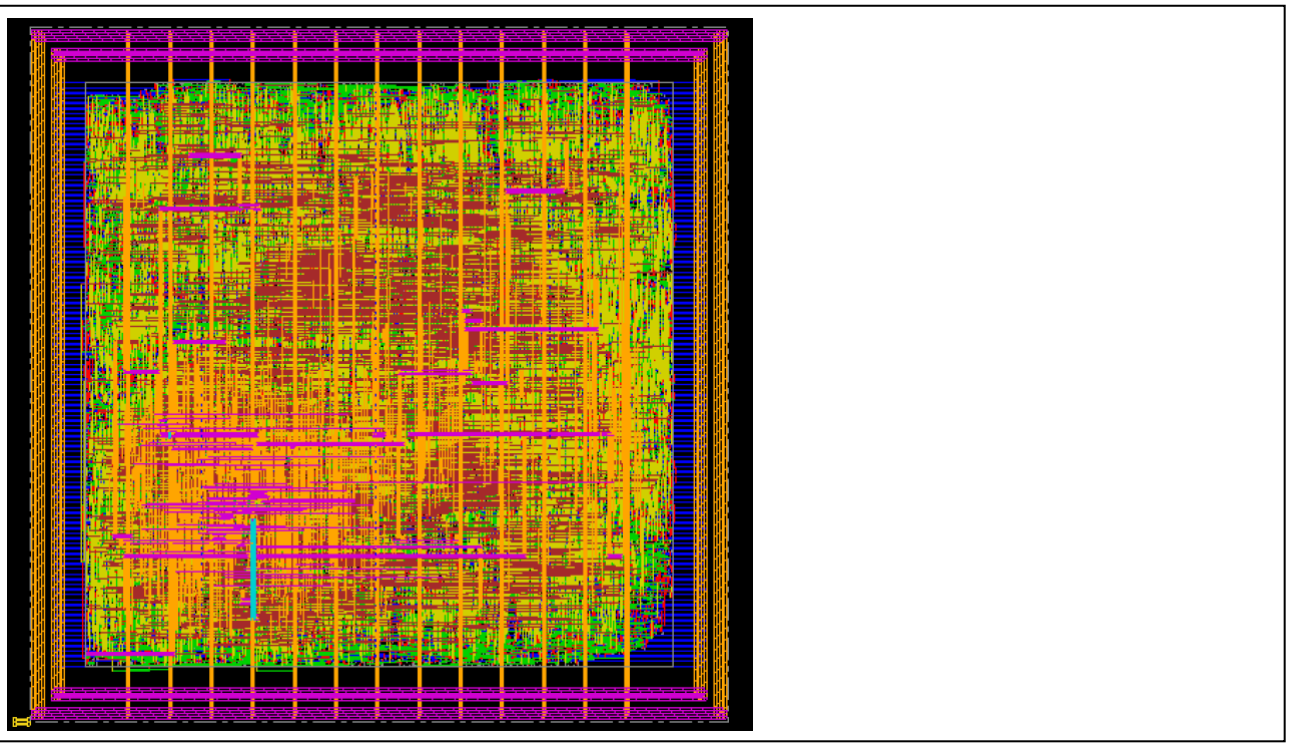
Synthesis Area Report

```
****************************************
Report : area
Design : SW
Version: R-2020.09-SP5
Date   : Wed Jun 15 22:47:58 2022
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                           29
Number of nets:                         14218
Number of cells:                        12921
Number of combinational cells:          11119
Number of sequential cells:              1802
Number of macros/black boxes:               0
Number of buf/inv:                       2100
Number of references:                     130

Combinational area:              83943.219403
Buf/Inv area:                     8982.640696
Noncombinational area:           58928.633949
Macro/Black Box area:                0.000000
Net Interconnect area:         1559981.277740

Total cell area:                142871.853352
Total area:                    1702853.131093
```

Synthesis Power Report

```
****************************************
Report : power
        -analysis_effort low
Design : SW
Version: R-2020.09-SP5
Date   : Wed Jun 15 22:48:27 2022
****************************************


Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)


Operating Conditions: slow   Library: slow
Wire Load Model Mode: top

Design        Wire Load Model            Library
------------------------------------------------
SW                    tsmc13_wl10       slow


Global Operating Voltage = 1.08
Power-specific unit information :
    Voltage Units = 1V
    Capacitance Units = 1.000000pf
    Time Units = 1ns
    Dynamic Power Units = 1mW    (derived from V,C,T units)
    Leakage Power Units = 1pW


  Cell Internal Power  =   8.8450 mW   (86%)
  Net Switching Power  =   1.3855 mW   (14%)
                         ---------
Total Dynamic Power    =  10.2305 mW  (100%)

Cell Leakage Power     =  23.5615 uW


                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000            0.0000            0.0000  (   0.00%)
memory             0.0000           0.0000            0.0000            0.0000  (   0.00%)
black_box          0.0000           0.0000            0.0000            0.0000  (   0.00%)
clock_network      0.0000           0.0000            0.0000            0.0000  (   0.00%)
register           8.5605           0.1072        1.5768e+07            8.6834  (  84.68%)
sequential         0.0000           0.0000            0.0000            0.0000  (   0.00%)
combinational      0.2845           1.2783        7.7933e+06            1.5706  (  15.32%)
--------------------------------------------------------------------------------------------------
Total              8.8450 mW        1.3855 mW     2.3561e+07 pW        10.2540 mW
```

APR NanoRoute Innovus Result (截圖)



APR Simulation Result (截圖)

```
                                  Instances  Unique
               Modules:               13385     154
               UDPs:                   1972       2
               Primitives:            27025       8
               Timing outputs:        14673      31
               Registers:              1813      17
               Scalar wires:          16480       -
               Expanded wires:            4       2
               Always blocks:             3       3
               Initial blocks:            8       8
               Pseudo assignments:        1       1
               Timing checks:         16218    2897
               Interconnect:          33917     704
               Delayed tcheck signals:   5406    2409
               Simulation timescale:      1ps
        Writing initial simulation snapshot: worklib.tb:v
Loading snapshot worklib.tb:v ..................... Done
*Verdi* Loading libsscore_ius152.so
ncsim> source /usr/cad/cadence/INCISIV/cur/tools/inca/files/ncsimrc
ncsim> run
./dat/ref1.dat, ./dat/query1.dat and ./dat/golden1.dat were used for this simulation.


====================== The test result is ..... PASS ========================


        ************************************************
        **                                            **      /|____|\
        **             Congratulations !!             **    ((´-___-` ))
        **                                            **   ///        \\\
        **  All data have been generated successfully! **  /||          ||\
        **                                            **  w|\ m      m /|w
        ************************************************    \(o)____(o)/


==============================================================================
   total cycle:         213
Simulation complete via $finish(1) at time 1955960 PS + 0
```

Report

(If you don’t pass APR, the score will be determined by the completeness of the report below)