

# YU-CHENG WU

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## EDUCATION

Dept. of Electrical Engineering, National Taiwan University (NTU)

Taipei, Taiwan

Bachelor of Science in Engineering

Sep. 2019 – Jun. 2023

- **Last-60-credit GPA: 4.19/4.3 (3.99/4.0)**, CGPA: 3.99/4.3 (3.87/4.0).
- Courses with A(+) grades: \*Machine Learning, \*Deep Learning for Computer Vision, Algorithms, Data Structure, Operating Systems, Computer Architecture, Computer Programming Lab, Intro. to Electronic Design Automation, Digital Circuit Lab, Communication System Lab, Linear Algebra, Calculus, etc. (\* for graduate-level courses.)

## PAPERS

- **Yu-Cheng Wu**, I-Ching Tseng, and Chung-Wei Lin, "Deep-Reinforcement-Learning-Based Design Space Exploration for Time-Sensitive Networking," ACM/IEEE Design Automation Conference (**DAC**), 2024. (Accepted for WIP.)
- **Yu-Cheng Wu**, Chi-Tse Huang, and An-Yeu Wu, "DEA-NIMC: Dynamic Energy-Aware Policy for Near/In-Memory Computing Hybrid Architecture," IEEE International System-on-Chip Conference (**SOCC**), 2023. 📄 (Oral Presentation.)
- I-Ching Tseng, **Yu-Cheng Wu**, Hsuan Ling, and Chung-Wei Lin, "A Contract-Based Distributed Task-Offloading Methodology for Vehicular Edge Computing," IEEE Vehicular Networking Conference (**VNC**), 2024. (Submitted.)

## RESEARCH EXPERIENCE

Cyber-Physical Systems Lab, National Taiwan University

Taipei, Taiwan

Advisor: Prof. Chung-Wei Lin | Research Assistant, Undergraduate Researcher

Sep. 2022 – Nov. 2023

- Automated design space exploration for Cyber-Physical Systems (CPSs) complying with Time-Sensitive Networking (TSN) by Graph Neural Networks and Deep Reinforcement Learning.
- **Collected at least 3.93X more solutions than any other comparative method** for schedulable data flow periods and proposed a more efficient design flow for TSN-based CPSs.

Access IC Lab, National Taiwan University

Taipei, Taiwan

Advisor: Prof. An-Yeu Wu (IEEE Fellow) | Undergraduate Researcher

Sep. 2021 – Aug. 2023

- **Outperformed prior works in accuracy by up to 8.8% and 4.6% on the CIFAR-10 and CIFAR-100 datasets** within the same energy consumption on hybrid accelerators based on In-Memory and Near-Memory Computing (IMC/NMC).
- Proposed a data-level and energy-aware policy using Deep Reinforcement Learning to dynamically adjust IMC and NMC usage in deep learning inference for image classification.

Applied Logic and Computation Lab, National Taiwan University

Taipei, Taiwan

Advisor: Prof. Jie-Hong Jiang | Undergraduate Researcher

Sep. 2020 – Aug. 2022

- Researched dimension reduction for output layers of Convolutional and Recurrent Neural Networks (CNN/RNN).
- Researched circuit synthesis methodology based on stochastic computing for CNNs and RNNs.

## HONORS

- **Finalist of the 2022 NSTC Research Grant for University Students**, the largest for undergraduates in Taiwan.
- **Regional Representative for the 2017 APMO**, one of the largest mathematical competitions for the Pacific Rim Region.

## WORK EXPERIENCE

Conformal ECO Team, Cadence

Hsinchu City, Taiwan

Intern Software Engineer

Jul. 2022 – Aug. 2022

- Optimized the Conformal ECO Designer, which enables RTL engineering change orders for pre-mask and post-mask designs.
- **Accelerated circuit error rectification by up to 32.3 times and reduced patch circuit sizes by up to 59.7%** by preliminarily fixing primary outputs with sparse error patterns.
- Implemented error pattern collection and patch circuit generation for circuits with limited error patterns based on the widely used open-source tool ABC. 📄

## PROJECTS

- **Talking to Me, Ego4D Challenge for CVPR Workshop 2023** 📄 📄 📄  
Used CNNs, a Video Vision Transformer, HuBERT, and Mel-scale Frequency Cepstral Coefficients for video and audio data processing to identify whether a specific person is talking to the camera wearer.
- **Neural Network Synthesis** 📄 📄  
Implemented a quantized neural network synthesis algorithm based on Booth encoding and partial sum sharing for a tiny CNN optimized with knowledge distillation on the MNIST dataset.
- **Digital Circuit Design** 📄  
Implemented audio recording and playing, an RSA256 decoder, Smith-Waterman algorithm for short-read mapping, a random number generator, and the Red Light, Green Light game in "Squid Game" with a motion detector on the DE2-115 FPGA.
- **RISC-V CPU** 📄  
Implemented a RISC-V CPU supporting 12 single-cycle instructions and 32-bit multiplication.