


RRNCF

< Previous instruction: [RRCE](#) | Instruction [index](#) | Next instruction: [SETF](#) >

RRNCF	Rotate Right f (no carry)								
Syntax:	[<i>label</i>] RRNCF f [,d [,a]								
Operands:	$0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$								
Operation:	$(f<n>) \rightarrow \text{dest}<n-1>$, $(f<0>) \rightarrow \text{dest}<7>$								
Status Affected:	N, Z								
Encoding:	<table><tr><td>0100</td><td>00da</td><td>ffff</td><td>ffff</td></tr></table>	0100	00da	ffff	ffff				
0100	00da	ffff	ffff						
Description:	<p>The contents of register 'f' are rotated one bit to the right. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).</p> 								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table><tr><th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr><tr><td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr></table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example 1: RRNCF REG, 1, 0

Before Instruction

REG = 1101 0111

After Instruction

REG = 1110 1011

Example 2: RRNCF REG, 0, 0

Before Instruction

W = ?

REG = 1101 0111

After Instruction

W = 1110 1011

REG = 1101 0111

< Previous instruction: [RRCE](#) | Instruction [index](#) | Next instruction: [SETF](#) >