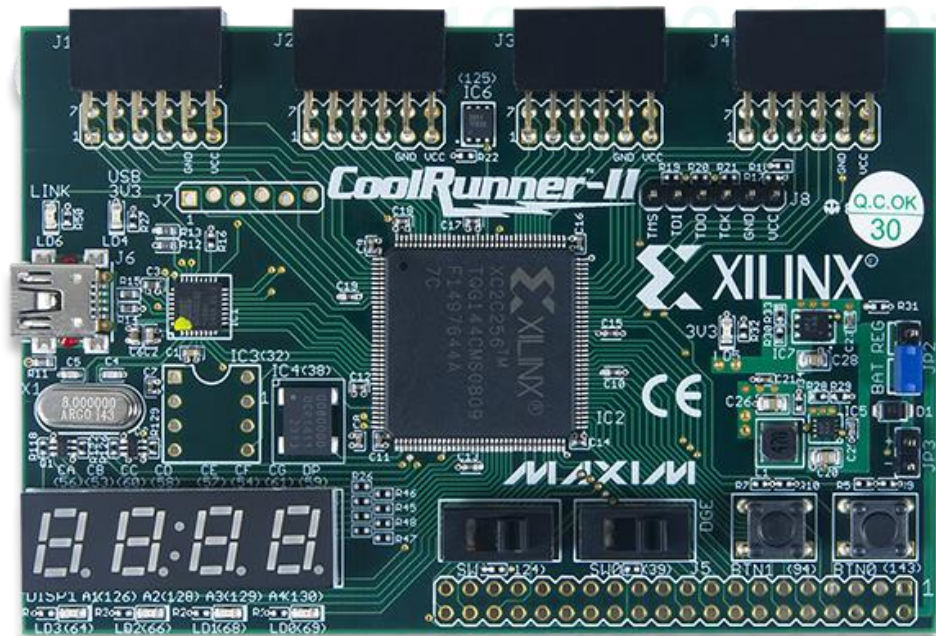# VHDL - stopky

Petr Kaštánek
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Coolrunner 2

1 tlačítko – start

1 tlačítko – reset

Časové signály

```vhdl
clk_sfi_o <=  '0' after 500 ms when clk_sfi_o = '1' else -- for seconds
        '1' after 500 ms when clk_sfi_o = '0';


clk_ssi_o <=  '0' after 5000 ms when clk_ssi_o = '1' else -- for tens of seconds
        '1' after 5000 ms when clk_ssi_o = '0';


clk_mfi_o <=  '0' after 50000 ms when clk_mfi_o = '1' else -- for minutes
        '1' after 50000 ms when clk_mfi_o = '0';


clk_msi_o <=  '0' after 500000 ms when clk_msi_o = '1' else -- for tens of minutes
        '1' after 500000 ms when clk_msi_o = '0';
```

Čítání času

```vhdl
if rising_edge(clk_sfi_o) then

    if sec_fi_o = "1001" then   -- countig seconds
        sec_fi_o <= "0000";

    else
        sec_fi_o <= sec_fin_o;
    end if;
end if;
```
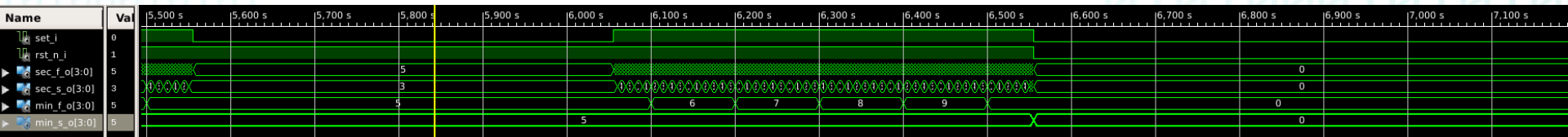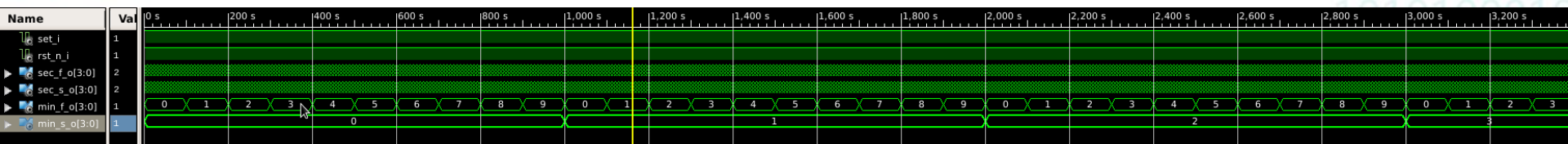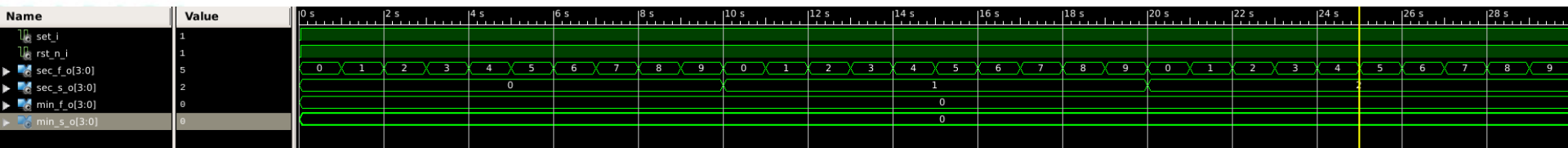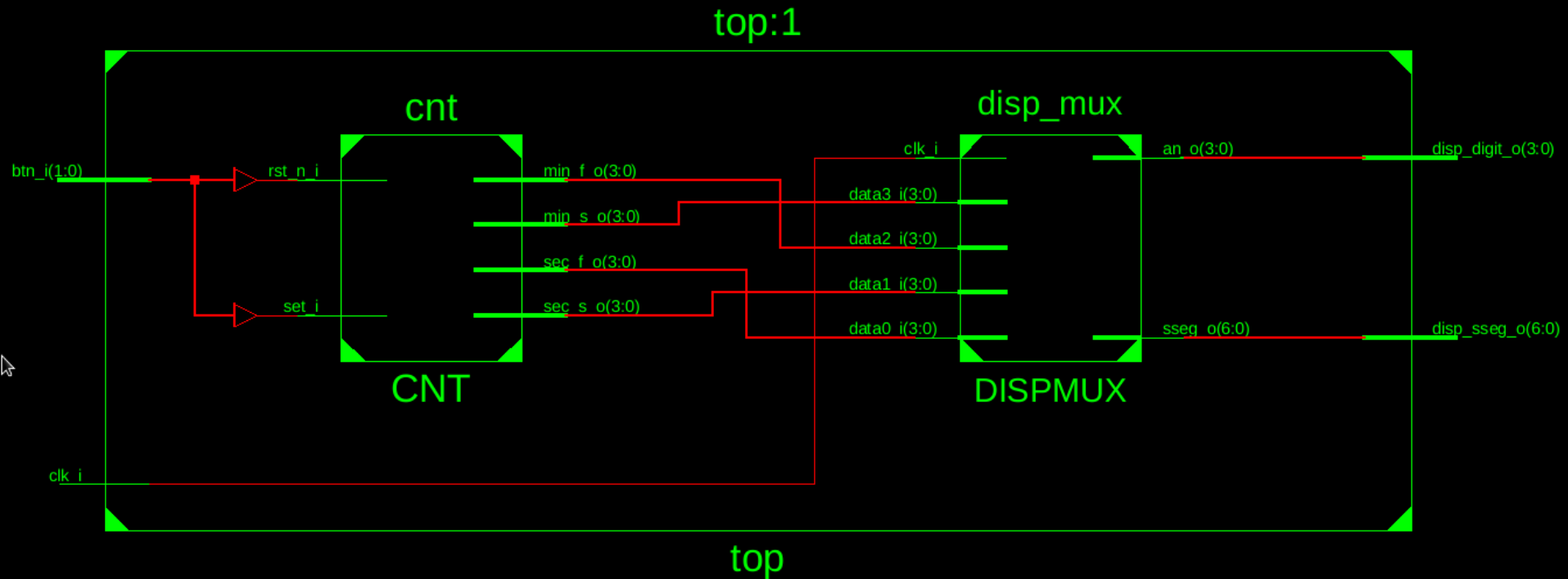
Schematické zapojení programu

Děkujeme za pozornost