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Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements

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Abstract

A novel approach for the readout of a TPC at the future linear collider is to use a CMOS pixel detector combined with some kind of gas gain grid. A first test using the photon counting chip Medipix2 with GEM or Micromegas demonstrated the feasibility of such an approach. Although this experiment demonstrated that single primary electrons could be detected the chip did not provide information on the arrival time of the electron in the sensitive gas volume nor did it give any indication of the quantity of charge detected. The Timepix chip uses an external clock with a frequency of up to 100 MHz as a time reference. Each pixel contains a preamplifier, a discriminator with hysteresis and 4-bit DAC for threshold adjustment, synchronization logic and a 14-bit counter with overflow control. Moreover, each pixel can be independently configured in one of four different modes: masked mode: pixel is off, counting mode: 1-count for each signal over threshold, TOT mode: the counter is incremented continuously as long as the signal is above threshold, and arrival time mode: the counter is incremented continuously from the time the first hit arrives until the end of the shutter. The chip resembles very much the Medipix2 chip physically and can be readout using slightly modified versions of the various existing systems. This paper presents the main features of the new design, electrical measurements and some first images.
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1. Introduction

The Medipix2 chip [1] has shown great potential in different applications requiring single photon counting approach. Successful tests using the chip for the readout of a TPC prototype for the ILC showed very promising results when coupled to GEM [2] or Micromegas [3] gain grids. Although these experiments demonstrated that single primary electrons could be detected, the chip did not provide information on the arrival time of the electron in the sensitive gas volume nor on the quantity of charge deposited. The Timepix chip is an evolution from the Medipix2 chip which allows for measurement in arrival time,"time-over-threshold" (TOT) and/or event counting independently in each pixel. An external reference clock (*Ref_Clk*) is used to generate the clock in each pixel that increments the counter depending in the selected operation mode. The chip has the same size, readout architecture and floorplan as the Medipix2 chip allowing almost a full backward compatibility with all the existing Medipix2 readout systems [4,5]. The architecture and functional behaviour of the Timepix chip are described in this paper together with first electrical measurements and first images.

2. The pixel cell

Fig. 1 shows the schematic of the Timepix pixel cell. Although the cell clearly resembles to the Medipix2 pixel it has three main differences: there is a single threshold with 4-bits threshold adjustment, each pixel can be configured in three different operation modes, and the counting clock is synchronized with the external clock reference (*Ref_Clk*).

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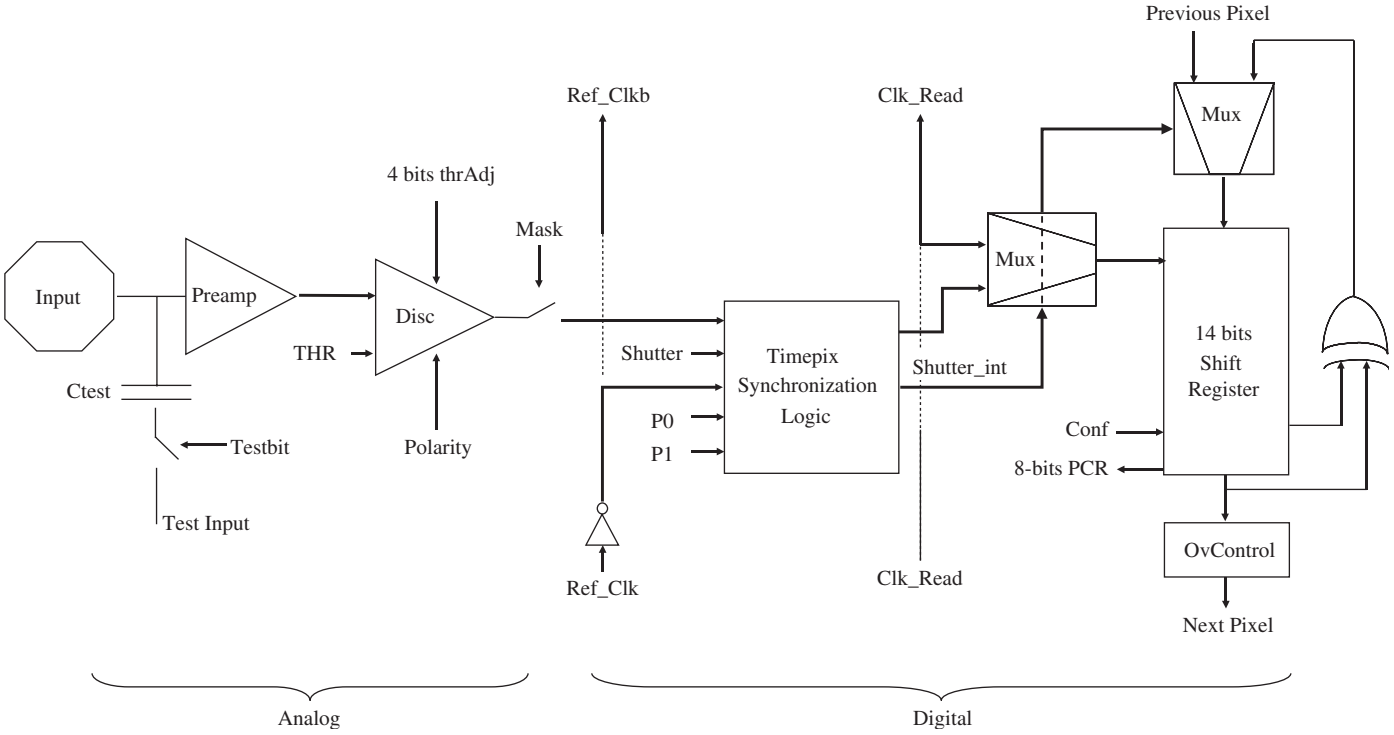

Fig. 1. Timepix pixel cell schematic.

The pixel is divided into two large blocks: the analog side formed by the preamplifier, the discriminator (with polarity control pin) and 4-bit threshold adjustment, and the digital side formed by the Timepix Synchronization Logic (*TSL*), the 14-bit shift register, the overflow control logic, the *Ref_Clk* pixel buffer and an 8-bit Pixel Configuration Register (*PCR*). The *PCR* contains 4 bits for the pixel threshold equalization, 1 bit for Masking (*MaskBit*), 1 bit for enabling the test pulse input (*TestBit*) and 2 bits for selecting the pixel operation mode (*P*0 and *P*1). The pixel cell contains ~550 transistors, its dimensions are $55 \times 55\,\mu m^2$ and the static power consumption is ~13.5 μW (in acquisition state and *Ref_Clk* = 80 MHz). Fig. 2 shows the Timepix pixel cell layout.

The pixel has two working states, depending on the *Shutter* signal. This signal is applied to all the pixels of the matrix simultaneously with a precision of ~5 ns. If the *Shutter* signal is high, an external clock is used to shift the data from pixel to pixel. Either the 8-bit configuration register (*PCR*) is programmed or the 14-bit shift register is readout. When the *Shutter* is low the 14-bit shift register behaves as a linear feedback shift register counter with a single XOR tap with a dynamic range of 11810 counts. In this state, the pixel counter is incremented by the *Ref_Clk* depending on the settings of the pixel operation mode bits (*P*0 and *P*1):

(i) *Event counting mode* (*P*0 = 0 *and* *P*1 = 0): Each event above threshold increments the counter by 1.
(ii) *TOT mode* (*P*0 = 1 *and* *P*1 = 0): The counter is incremented continuously while the input charge is over threshold.
(iii) *Arrival time mode* (*P*0 = 1 *and* *P*1 = 1): The counter is incremented from the moment the discriminator is activated until the global *Shutter* signal is set high.

2.1. Pixel analog section

Any charge collected by the octagonal 20 μm width pixel anode is integrated and compared to a global threshold. If the preamplifier output voltage crosses the threshold the output of the discriminator generates a pulse whose width corresponds to the length of time the preamplifier output voltage remains over threshold. The preamplifier follows the scheme proposed by Krummenacher [6] based on a cascoded differential CMOS amplifier. Some global DACs control the front end. The peaking time can be set from 90 to 180 ns by the *Preamp* DAC. The return to zero of a ~10 ke^- input charge can be adjusted from 500 to 2500 ns depending on *Ikrum* DAC settings. The DC output level of the preamplifier is controlled by the *Vfbk* voltage DAC and it is used to maximize the output voltage dynamic range depending on input charge polarity. The configuration permits the amplification of positive or negative charges and the compensation for detector leakage currents in both polarities, of up to *Ikrum*/2 per pixel. The amplifier gain in the default DAC settings is ~16.5 mV/ke^- with a linear voltage dynamic range up to ~50 ke^-. The preamplifier output is DC coupled to the discriminator. The discriminator contains an input multiplexer (controlled by the *Polarity* CMOS input to ensure that the discriminator output has the right polarity when a hit crosses the threshold for both input polarities), a differential

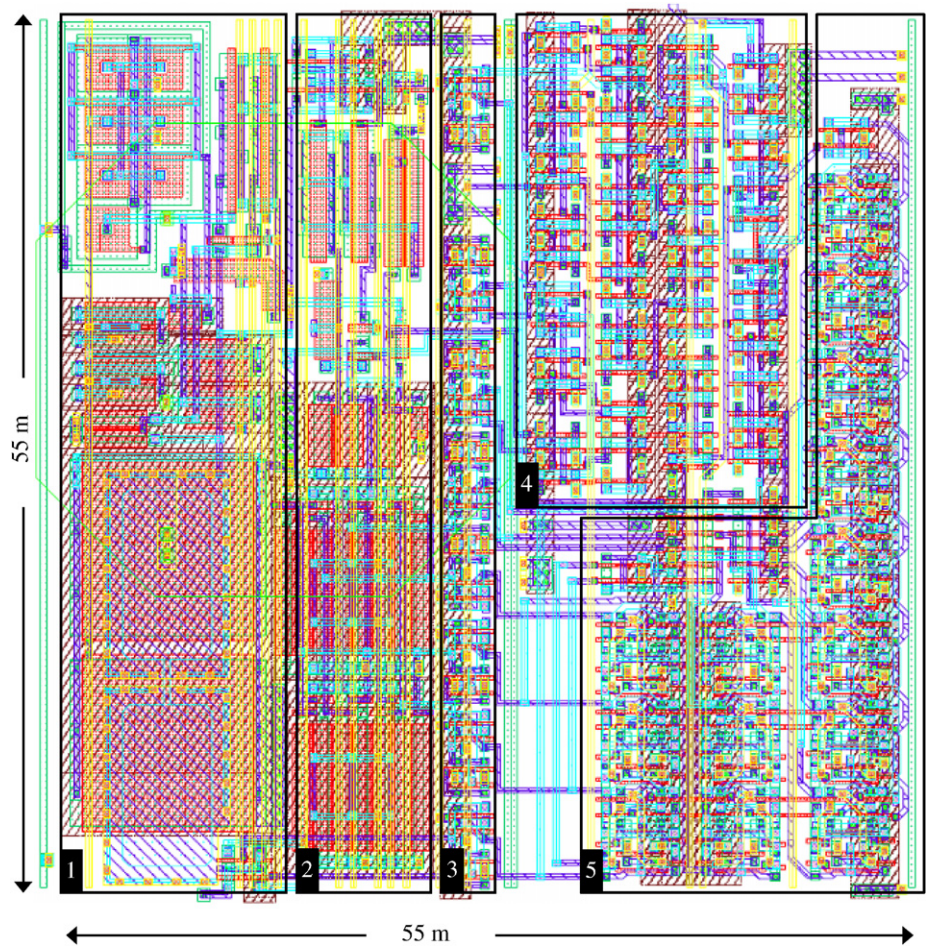

Fig. 2. Timepix pixel cell layout: (1) preamplifier; (2) discriminator with 4-bit threshold equalization; (3) 8-bit PCR; (4) *Ref_Clk* buffer and TSL and (5) 14-bit shift register and overflow control.

amplifier (configured to work as an OTA[1]), four independent selectable current sources (used for threshold equalisation); and a current discriminator with hysteresis. The total analog power consumption in nominal conditions is ~6.5 μW and its layout area is $55 \times 25\,\mu m^2$.

2.2. Pixel digital section

The analog output from the discriminator (*Hit*) is buffered and gated with the *Maskbit* at the entrance of the *TSL*. The pixel operation mode bits (*P*0 and *P*1) configure each pixel *TSL* in three different modes. In the acquisition state (i.e. *Shutter* is low) the *TSL* synchronizes the *Hit* and the *Shutter* with the *Ref_Clk* to generate a glitch free counting clock signal depending on the operation mode. The counter is stopped if the number of counts reaches the overflow limit of 11 810 counts. The *TSL* core uses an asynchronous network of SR flip-flops with race-free state assignment designed with controlled initialization. To minimize the digital power consumption the *TSL* core is only active when a *Hit* is present. The pixel digital part contains ~500 minimum-sized transistors and occupies an area of $55 \times 30\,\mu m^2$.

[1]OTA = Operational Transimpedance Amplifier.

3. The reference counting clock

The Timepix chip uses an externally generated tunable clock reference (*Ref_Clk*) as its counting clock which is distributed throughout the pixel matrix. To minimize the capacitive coupling and to maximize the digital power balance of the *Ref_Clk* distribution into the full matrix, each pixel includes a minimum-sized inverter to buffer the *Ref_Clk* to the next pixel up in the column. Furthermore, to minimize the digital coupling and to uniformly distribute the digital power, the *Ref_Clk* phase is alternated between columns. Assuming a simulated typical propagation delay of ~195 ps per pixel inverter/buffer the *Ref_Clk* is distributed to all the pixels in less than 50 ns. With a *Ref_Clk* of 80 MHz the measured digital power consumption due to clock distribution into the pixel matrix is ~450 mW. The Timepix chip shows no detectable increment of the minimum threshold when compared to the Medipix2 chip, which has no distributed clock and each pixel generates its own asynchronous counting clock.

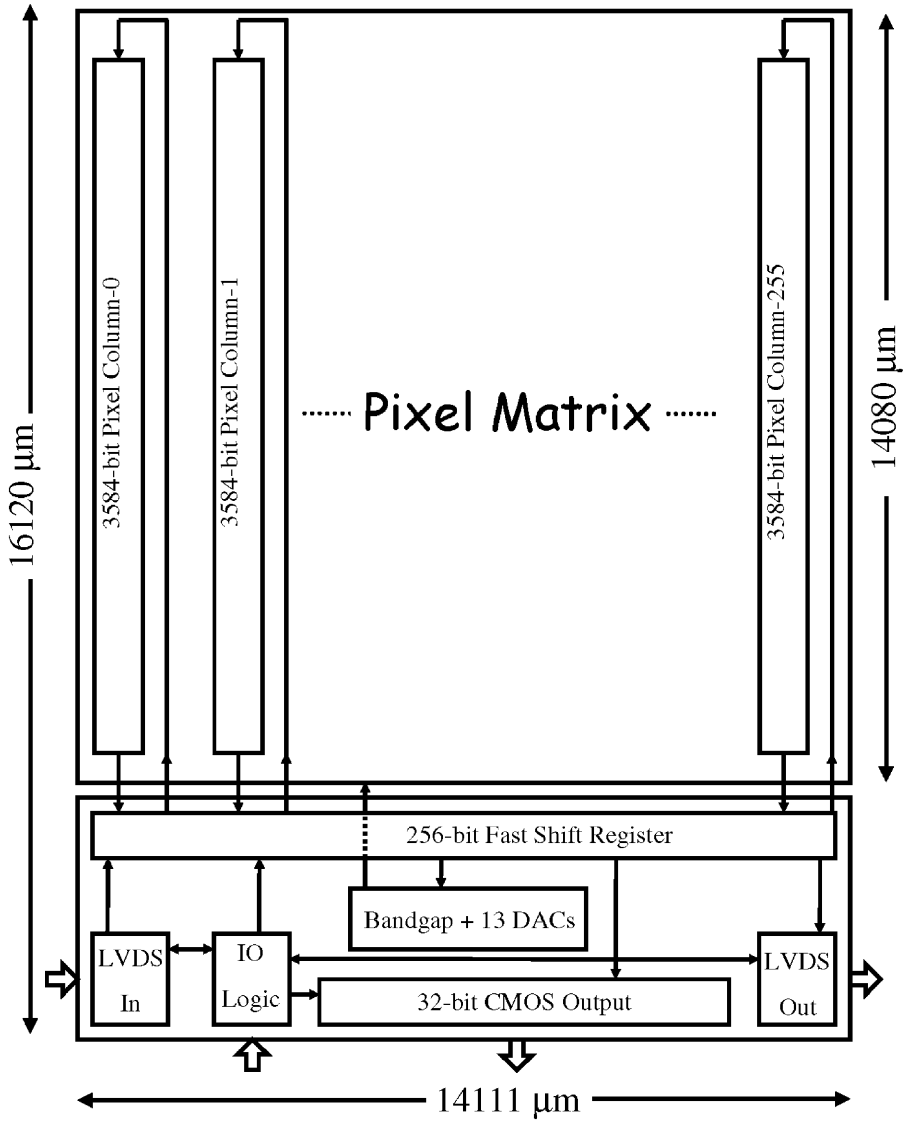

Fig. 3. Timepix floorplan: on the top square there is the 256 × 256 pixel matrix, on the bottom square there is the Timepix IO periphery and DACs.

4. Chip description

Fig. 3 shows the floorplan of the Timepix chip. To minimize non-sensitive area when butting together several chips, the periphery is placed at the bottom of the chip and the sensitive area is placed at the top, with less than 50 µm of non-sensitive area between the last pixel and the chip edge. The sensitive area (top box) is arranged as a matrix of 256 × 256 pixels of $55 \times 55\,\mu m^2$ resulting in a detection area of $1.98\,cm^2$ (87% of the entire chip area). The analog part of the periphery contains one band-gap circuit [7] which internally generates a stable reference voltage which is used by the 13 on-chip global DACs. This reference voltage has a temperature sensitivity of $0.22\,mV/^{\circ}C$ and a power supply sensitivity of less than 1 mV/V. There are eight 8-bit current DACs, four 8-bit voltage DACs and a single 14-bit voltage DAC which is used for the precise setting of the global threshold. At default settings, the threshold DAC LSB[2] corresponds to $\sim 25\,e^-$ with a INL[3] of less than 1.5 LSB in 10-bits. The digital part of the periphery contains all the input/output control logic, the IO wire-bonding pads and a 24-bit fused blown registry for unique chip identification. Using a 100 MHz readout clock the chip can be readout serially through the on-chip LVDS drivers in less than 10 ms, or in parallel through the 32-bit CMOS port in less than 300 µs. Both the analog and digital circuitry have been designed to operate with independent 2.2 V power supplies with a total analog power consumption of ~440 mW and a digital power consumption of ~450 mW (in acquisition state and $Ref\_Clk = 80$ MHz). The chip contains approximately 36 million transistors and is fabricated in a commercial six metal CMOS 0.25 µm technology.

[2]LSB = Least Significant Bit.
[3]INL = Integral Non-linearity.

5. Pixel electrical characterization

Initial electrical measurements were done with a Timepix chip mounted on a standard Medipix2 PCB, using the Medipix2 serial readout system with an updated Mur-osv2.1 readout board [4] and a modified version of the Pixelman software [5]. The electrical characterization was carried out using an external test pulse with a gain of 46.875 e^-/mV. The test pulse linear range extends to ~40 ke^-. Since the test pulse gain was extracted from simulations, it should be understood that all the following measurements are preliminary. In all measurements the *Ref_Clk* has been set to 60 MHz unless otherwise indicated.

5.1. Measurements in counting mode

The electronic noise and effective threshold can be measured using the s-curve method [8] when the pixel is set in counting mode. This method gives information on the noise of the front-end chain. Using a fixed threshold, an input charge is swept from a level where there are no counter counts (i.e. under threshold) to a level where the 100% of the test pulses are counted, creating an s-shaped curve. The effective threshold is at 50% of this s-curve. The charge difference between the 97.75% and 2.25% of the s-curve is four times the RMS noise of the front end assuming a gaussian distributed noise. Fig. 4 shows an example of four s-curves in electron collection mode. The gain can be calculated as the distance from the measured effective threshold to the noise floor for a given input charge. Fig. 5 shows the linearity (up to 20 ke^-) of a single pixel at the centre of the matrix for both polarities. The measured electronic noise is $99.4 \pm 3.8\,e^-$rms for hole collection and $104.8 \pm 6\,e^-$rms for electron collection. The measured DAC step gain is $24.7 \pm 0.7\,e^-$/step for hole collection and $25.4 \pm 1.2\,e^-$/step for electron collection.

5.2. Measurements in TOT mode

In TOT mode the counter is incremented continuously with *Ref_Clk* while the preamplifier output is above the threshold. Although the preamplifier output voltage pulse is only linear up to 50 ke^- (due to the limited power supply range [0–2.2 V]), and the relative high gain [~16.5 mV/ke^-], the discriminator output pulse width is linear up to much larger input charges because of the constant current return to zero, which is controlled by the *Ikrum* DAC. Simulations have shown that the linear TOT dynamic range extends up to ~200 ke^-. However, this could not be electrically confirmed due to the limited test pulse linear range (up to ~40 ke^-). The left hand plot of Fig. 6 shows the relationship between the input charge and the measured time at three different thresholds. The measured response is linear if the input charge is 3−4 ke^- above threshold. On the right-hand side of Fig. 6 the resolution measured as ΔTOT/TOT (%) is shown. The resolution is better than 5% when the input charge is ~1 ke^- above threshold. As the input charge increases the ΔTOT/TOT tends to 0 because the ΔTOT is kept constant independently of the increase of the detected charge.

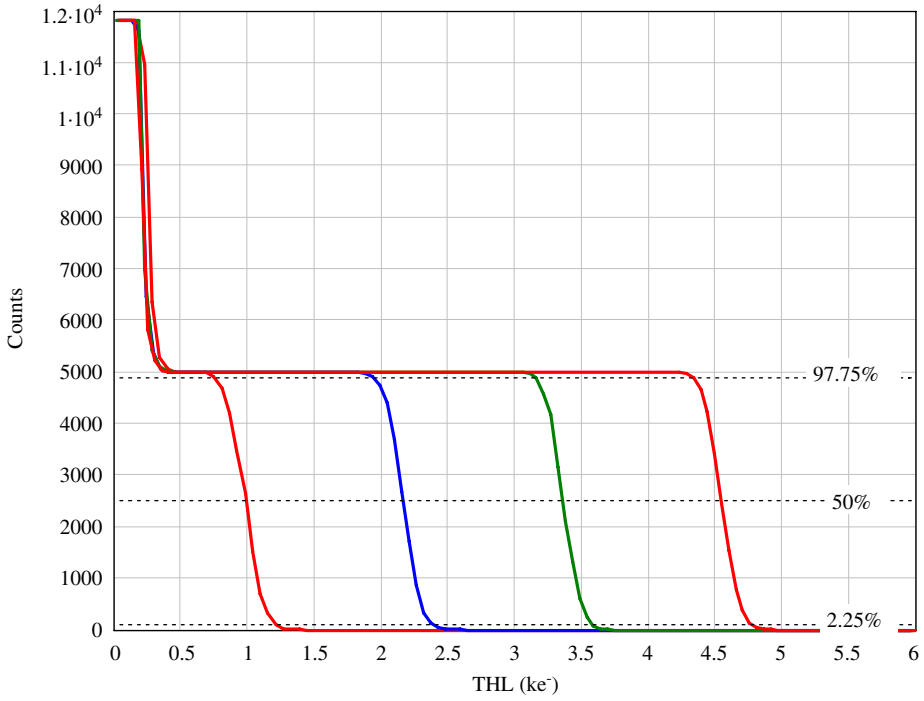

Fig. 4. An example of measured s-curves at four different thresholds. There are a total of 5000 test pulses sent in counting mode.

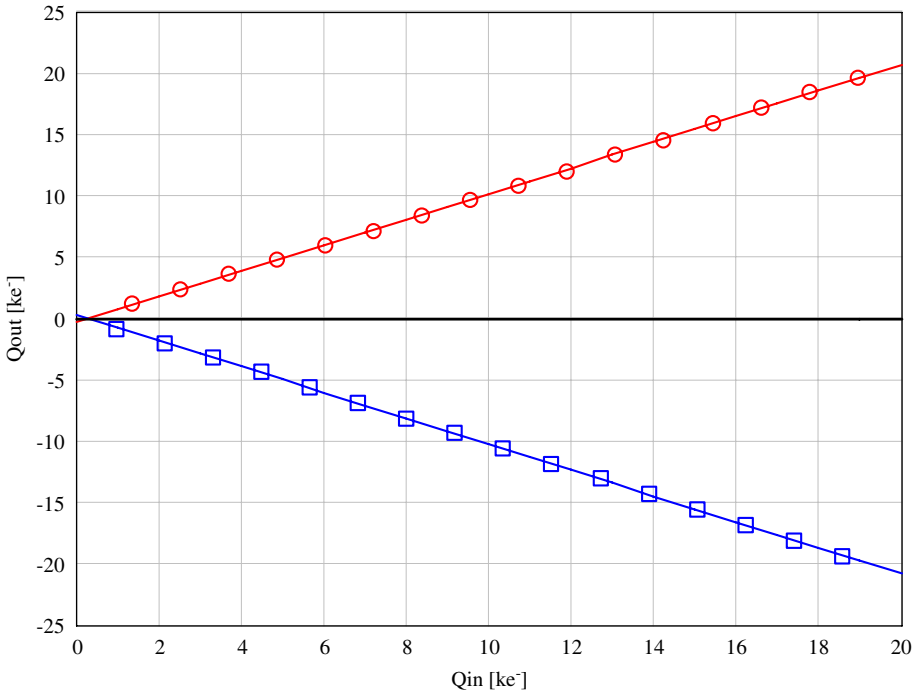

Fig. 5. Linearity plot up to ~20 ke^- for both polarities (holes on top and electrons on the bottom).

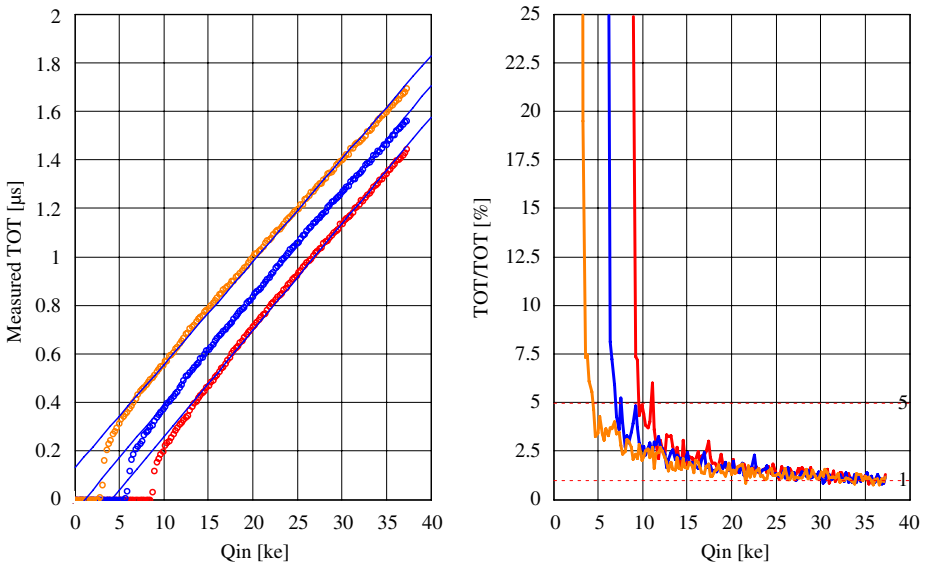

Fig. 6. Linearity of TOT measurements for three different thresholds. On the left is shown the measured energy resolution (ΔTOT/TOT (%)) with 1% and 5% markers.

5.3. Measurements in arrival time mode

When programmed in arrival time mode, the pixel behaves as a TDC.[4] During acquisition, the counter is incremented from the first time the discriminator output goes high to the closing of the *Shutter*. The quantization error can be up to two *Ref_Clk* periods since the start and end of the counting clock is synchronized to *Ref_Clk*. In the MUROSv2.1 readout system the test pulse timing is synchronized to *Ref_Clk*, therefore it is not possible to measure the quantization error at the pixel level. The time-walk is defined as the difference between the time measured from an input charge that is 1 ke^- over threshold and an infinite input charge. The faster the preamplifier peaking time, the better the time-walk value, since there is less time difference from a small charge to a big one crossing the

[4]TDC = Time to Digital Converter.

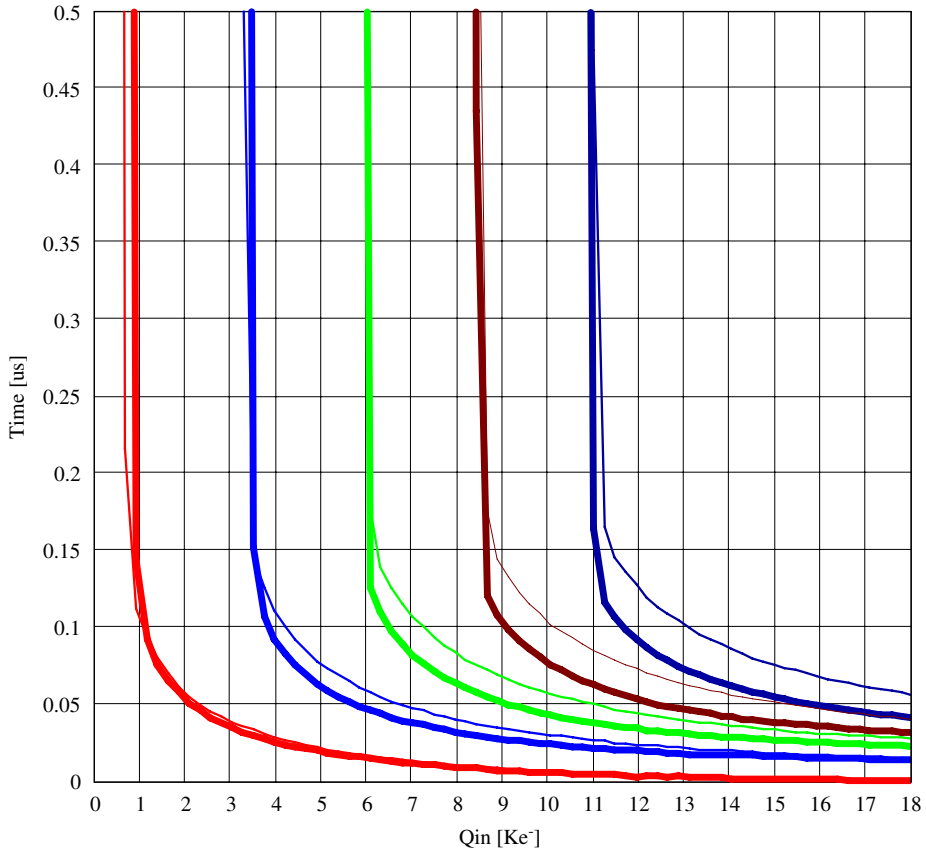

Fig. 7. Time-walk of 1 pixel of the centre of the matrix. The thick line curves are for *Preamp* = 255 (Preamp = 1.8 μA) and the thin line curves are with *Preamp* = 127 (Preamp = 900 nA).

same threshold level. The preamplifier peaking time is controlled by the *Preamp* current DAC. Fig. 7 shows the time-walk measured in a single pixel at the centre of the matrix for five different thresholds and two *Preamp* DAC settings. The measured time-walk is $\leqslant 50$ ns for the high *Preamp* current DAC setting. In systems where the charge deposition of a single event spreads over multiple pixels (i.e. GEMs), the matrix could be arranged in a kind of chess pattern, whereby some pixels could be configured in TOT mode and others in arrival time mode, in order to compensate off-line the time-walk through knowledge of the input charge deposited in the neighboring pixels.

6. Threshold equalization

Threshold equalization is used to compensate the pixel to pixel threshold variations due to local transistor threshold voltages and current mismatches [9] or more global effects like on-chip power drops. This compensation is done by means of a 4-bit current DAC placed in the discriminator chain of each pixel. The current range of this DAC is controlled by the *Ths* global DAC with a LSB range of 0–40 nA. The measured INL of this 4-bit DAC in the full pixel matrix is less than 0.8 LSB. To calculate the equalization mask the threshold distribution for each of the 16 threshold adjustment codes is found. Then the adjustment code is selected for each pixel to make its threshold as near as possible to the average of the threshold distribution mean values. Fig. 8 shows an example of a threshold equalization of a Timepix chip in both collection modes. The threshold variation before equalization is $\sim 240\,e^-$rms and after equalization the achieved noise free threshold variation is $\sim 35\,e^-$rms for both polarities. The minimum detectable charge is defined as the smallest input charge which all pixels are able to resolve when the global threshold is set just over the noise. The minimum detectable charge can be calculated by quadratically adding the measured electronic noise and the threshold variation because both measurements are uncorrelated. Before equalization the minimum detectable charge for the full matrix is $\sim 1600\,e^-$ and after equalization is $\sim 650\,e^-$ for both polarities.

7. Fixed pattern correction in TOT mode

The preamplifier output of all pixels can be reconstructed by scanning the threshold over 1 test pulse per *Shutter* period in arrival time and TOT mode consecutively. In arrival mode the peaking time of the preamplifier is reconstructed as a fixed test pulse is scanned by the global threshold. The preamplifier fall time is calculated by

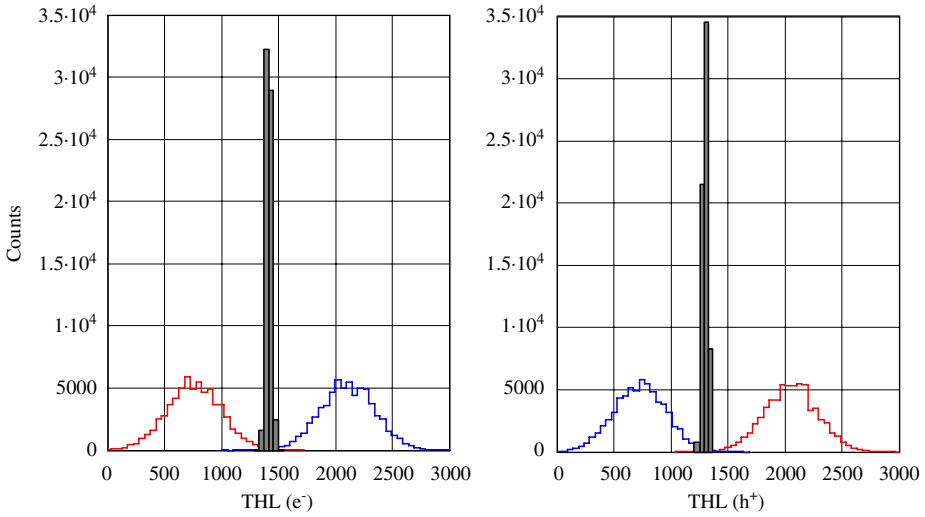

Fig. 8. Threshold equalization result for both polarities. On the left for electron collection and on the right for hole collection.

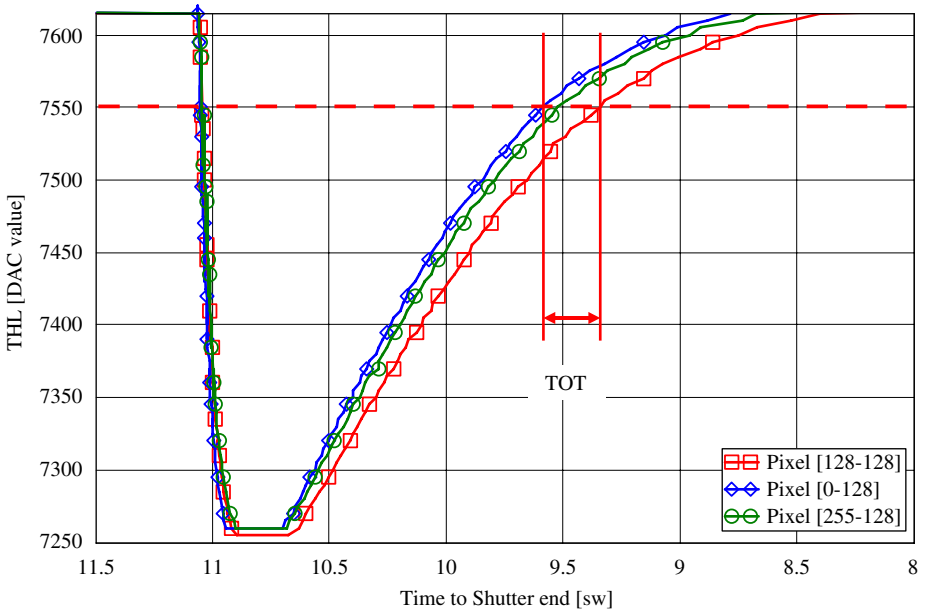

Fig. 9. Reconstructed preamplifier output pulse of three pixels along the central column of the matrix. Injected test pulse charge was ~9.3 ke$^-$.

subtracting the previously measured arrival time to the TOT measurement for each threshold. Fig. 9 shows an example of the preamplifier output pulse reconstruction of three pixels along the central column. It can be seen that the peaking time and the peak value is unchanged, but the return to zero shows a certain dispersion for the three tested pixels. The return to zero variation from pixel to pixel generates in TOT mode a pixel to pixel variation for the same global threshold, while in the other two modes the effect is undetectable. In each pixel the constant current discharge feedback loop is controlled by the global *Ikrum* DAC which has a nominal range of few nA. Given the small pixel area and the small current value the transistor size of the *Ikrum* current source is not big enough to compensate the pixel to pixel *Ikrum* current mismatch. Extrapolating to the full matrix pixel to pixel current mismatch generates a fix pattern noise in TOT mode. A correction mask for this effect can be found by calculating the transfer function of each pixel by scanning the test pulse over a fix global threshold. Once the correction mask is found it can be applied to any raw image to compensate for the *Ikrum* current mismatch. Fig. 10 shows an example of the full matrix being in TOT mode after sending in each pixel 1 test pulse of 18.75 ke$^-$; on the top left is the raw image, at the top right is the corrected image and at the bottom is shown the histogram of both 2D images. The FWHM of the full corrected matrix is ~1300 e$^-$.

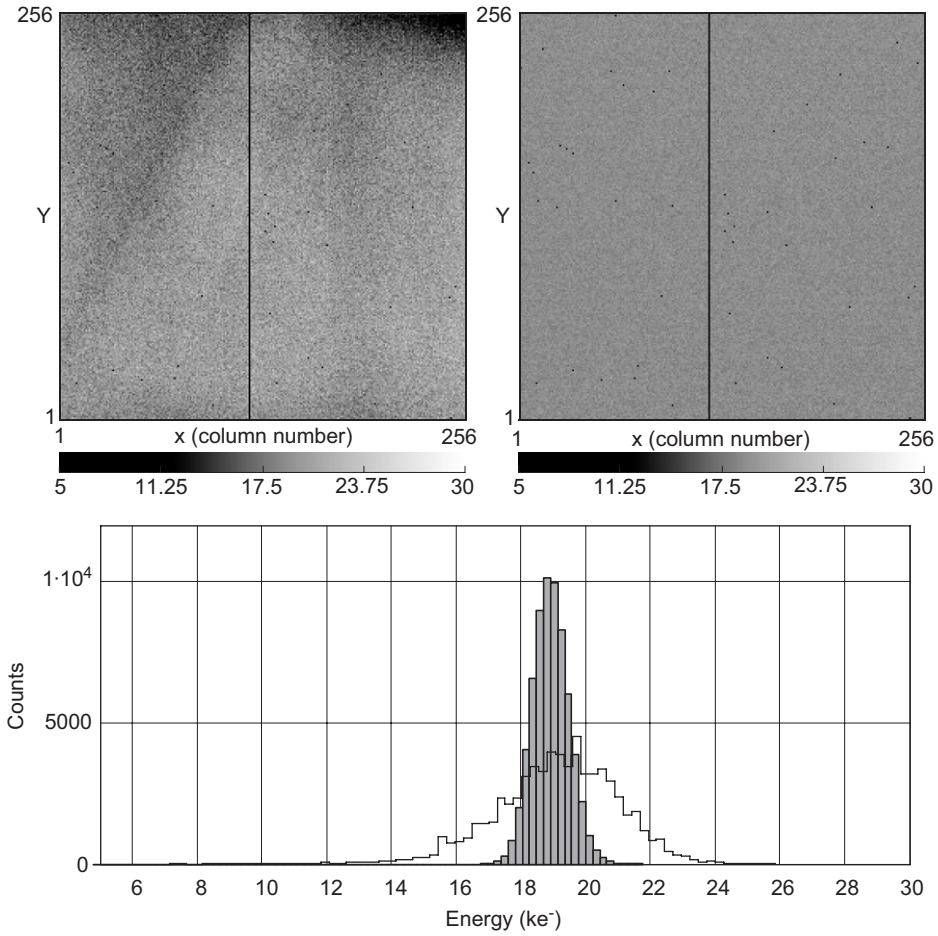

Fig. 10. An example of the full matrix programmed in TOT mode after sending in each pixel 1 test pulse of 18.75 ke^-. On the top left is the raw image, on the top right is the corrected image and at the bottom is shown the histogram of both 2D images. The FWHM of the full corrected matrix is ~1300 e^-.

8. First images

Fig. 11 shows a 2D image of an equalized chip after sending 10 test pulses of ~2.3 ke^-. This images shows the possibility of having simultaneously each pixel working in any of the three operation modes. In counting mode all the pixels count 10 and the masked pixels are at 0 counts. In TOT mode there is a certain spread due to the pixel to pixel TOT variation. In arrival time mode all the counts are between 8827 and 8829. Fig. 12 shows two images obtained with the two gas grain grid systems (GEM and Micromegas) which use a single naked Timepix as collection anode. On the left is shown a measurement in TOT mode of a single cosmic background particle interacting on a gas volume of a triple GEM detector. The maximum number pixel value of 1929 counts corresponds after calibration to ~120 ke^-. This image was taken during an EUDET testbeam in DESY with the collaboration of A. Bamberger and U. Renz, Freiburg (Germany). The right of Fig. 12 shows a measurement in arrival time of a cosmic background particle obtained with a Micromegas gas gain grid coupled to the Timepix chip. The measured counts difference is 56 which indicates an arrival time difference of 1.4 μs (with $Ref\_Clk = 40$ MHz). A triple scintillator is used as coincidence system to generate the *Shutter* trigger. This image was taken in Nikhef (The Netherlands) by J. Timmermans, H. van der Graaf and M. Chefdeville.

9. Conclusions

The Timepix chip has been designed using a commercial 0.25 μm technology, with a pixel cell of 55 × 55 μm^2. Each pixel can be programmed independently in counting, energy or arrival time modes. The chip has been characterized using an external test pulse. Initial measurements show an electronic pixel noise of ~100 e^-rms and a full matrix threshold variation ~35 e^-rms after equalization. The minimum detectable charge is ~650 e^-. In TOT mode the energy resolution ($\Delta TOT/TOT$) is better than 5% if the input charge is $\geqslant 1$ ke^- above threshold. The measured time-walk per pixel is $\leqslant 50$ ns. The first Timepix bump-bonded to a 300 μm Si semiconductor detector will be available shortly. At this point it will be possible to make an absolute calibration using a radiation source in order to confirm the figures presented here.

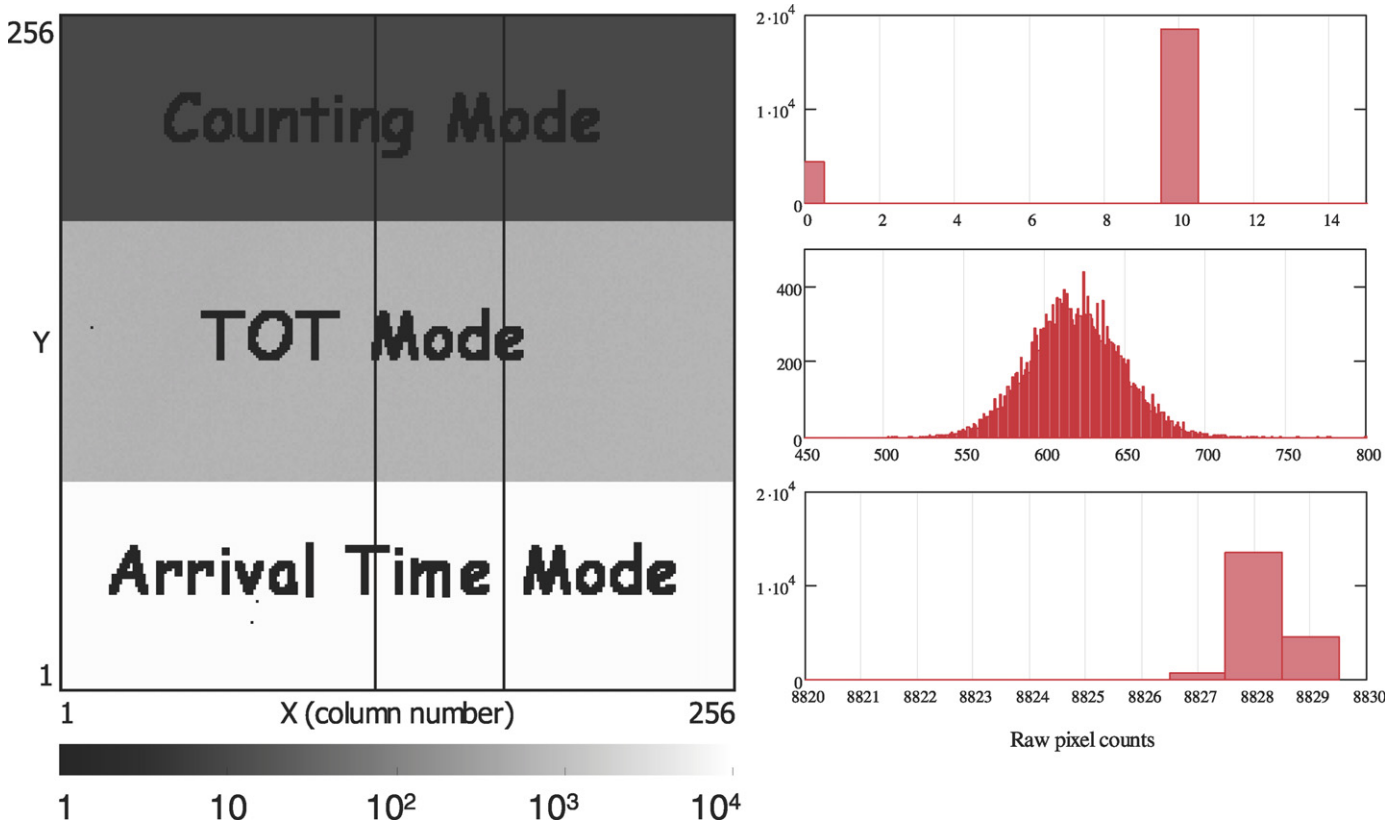

Fig. 11. On the left is a full matrix 2D image response of an equalized chip after sending 10 test pulses of ~2.3 ke$^-$. The matrix is split into three different working modes and the pixels that form the names are masked. On the right the histogram for each area (operation mode) is shown. The *Ref_Clk* is set to ~50 MHz.

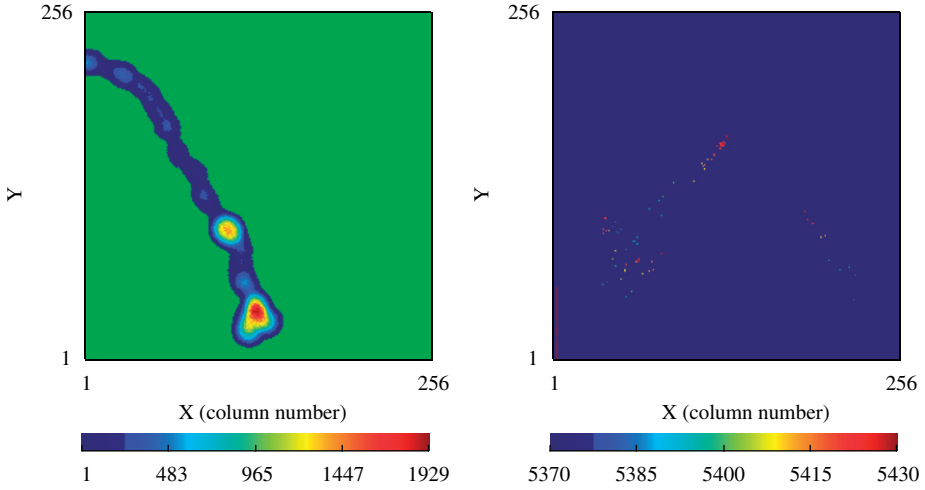

Fig. 12. On the left: TOT mode measurement of a single cosmic background particle interacting on a gas volume of a triple GEM detector. The maximum number pixel value of 1929 counts corresponds after calibration to ~120 ke$^-$. On the right: Arrival time measurement of a cosmic background particle obtained with a Micromegas gas gain grid coupled to the Timepix chip.

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