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FITPix — fast interface for Timepix pixel detectors

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ABSTRACT: The semiconductor pixel detector Timepix contains an array of 256×256 square pixels with pitch $55 \mu\text{m}$. In addition to high spatial granularity the single quantum counting detector Timepix can provide also energy or time information in each pixel. This device is a powerful tool for radiation and particle detection, imaging and tracking. A new readout interface for silicon pixel detectors of the Medipix family has been developed in our group in order to provide a higher frame rate and enhanced flexibility of operation. The interface consists of a field programmable gate array, a USB 2.0 interface chip, DAC, ADC and a circuit which generates bias voltage for the sensor. The main control system is placed in the FPGA circuit which fully controls the Timepix device. This approach offers an easy way how to include new functionality and extended operation. The interface for Timepix supports all operation modes of the detector (counting, TOT, timing). The FITPix is a successor of the USB 1.22 Interface and the electronic readout is built with the latest available components, which allows achieving up to 90 frames per second with a single detector. The frame rate is about 20 times faster compared to the previous system while it maintains all same capabilities supported. In addition FITPix newly enables an adjustable clock frequency and hardware triggering which is a useful tool when there is the need for synchronized operation of multiple devices. Three modes of hardware trigger have been implemented: hardware trigger which starts the measurement, hardware trigger which terminates the measurement and hardware trigger which controls measurement fully. The entire system is fully powered through the USB bus. FITPix supports also readout from several detectors in chain in which case just an external power source is required. FITPix is a fully flexible device and the user needs no other equipment. FITPix combines high performance and mobility and it opens new fields of applications. The current version of the FITPix interface has dimension $45 \text{ mm} \times 60 \text{ mm}$.

KEYWORDS: Trigger concepts and systems (hardware and software); Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Data acquisition concepts; Digital electronic circuits

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1 Introduction

The Timepix [1] is the next generation of pixel particle detector from the Medipix family [2]. The semiconductor pixel detector Timepix is the single quantum counting detector. Each pixel can provide independently one of three kinds of information from measurement. The first mode provides information about the count of detected particles. The second mode is the Time over Threshold (TOT) which provides information about energy of particles in each pixel and the last mode provides information about arrival time of particles in each pixel. The Timepix ASIC (figure 1) chip can be combined by the bump-bonding technology with different semiconductor sensors (i.e. different materials – e.g. Si, GaAs, CdTe, and thickness – e.g. 300, 700, 1000 μm) which convert the ionizing radiation into electric signals. The sensitive area of the sensor contains an array of 256×256 square pixels with 55 μm pitch.

The Timepix chip provides for each pixel of the sensor an independent electronic circuit in the chain. The electronic circuit is divided into an analogue and a digital part. Each pixel contains preamplifier, discriminator, 14-bit counter and shift register. Measured values are stored in counters and can be readout through shift registers. The Timepix chip provides two possibilities how to read data from the chip. The first approach is the serial readout through LVDS lines and the second approach is the parallel readout through 32-bit CMOS gate. Several Timepix detectors can be connected easily into the chain through LVDS serial interface. We obtain larger sensitive area by this approach. Thanks to the separated analogue and digital parts of the electronics, the Timepix detector has unique properties compared to the other detection technologies such as linearity and “infinite” dynamic range.

2 FITPix interface

2.1 Requirements

FITPix is a successor of the USB 1.22 Interface [3] both developed in the IEAP CTU Prague and are alternative readout interfaces to the MUROS Interface [4] developed of NIKHEF. FITPix was

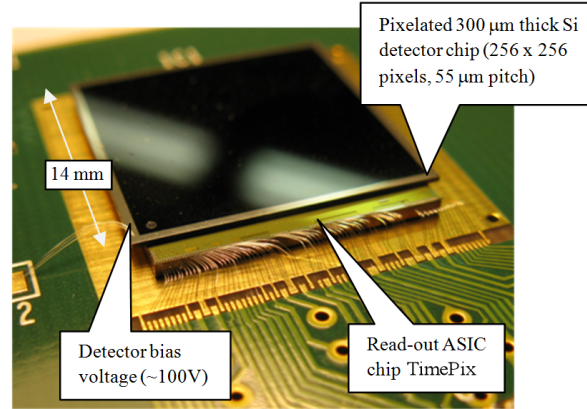


Figure 1. The Timepix ASIC chip. The sensor chip is bump-bonded to the readout chip. Wire bonds are visible.

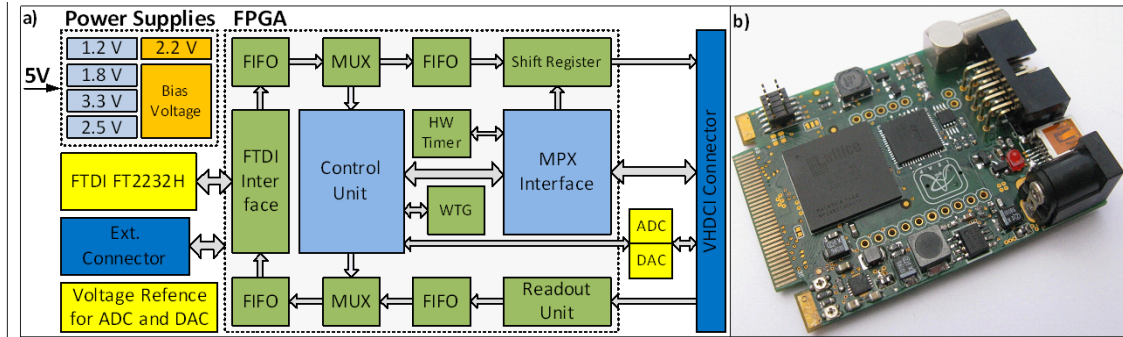


Figure 2. a) Architecture of FITPix interface, b) the final device with dimensions 45 mm × 60 mm.

created to fulfill the need for a faster, smaller, flexible and better interface for the Timepix. The USB 1.22 Interface is flexible device with many advanced features. However, the data acquisition speed is slow (up to 5 fps). The MUROS interface is faster compared to the USB 1.22 Interface (up to 50 fps), but the clock is generated by a RC oscillator and also the entire assembly has several parts with large dimensions. The main disadvantage is the clock from the RC oscillator. Timepix needs for proper measurements a stable clock. The aim of the FITPix interface is to offer a fast, flexible and portable interface for detectors from the Medipix family which does not need additional equipment for operation and use. Another demand is that the interface must be fully powered from the USB port. In this case the power consumption cannot be higher than 2.5 W. Another important demand is support for the HW triggering, support for the Medipix 2 MXR chips [5] as well as the Medipix 3 chips [6].

2.2 Hardware design

Figure 2 shows the block diagram of the FITPix and the final device.

The interface is based on the FPGA circuit which enables to achieve a high data frame-rate. The all digital system is placed in the FPGA clocked by a 50 MHz (main system clock). The readout frequency is two times higher than the main system clock. The Timepix chip uses CMOS

technology for control and LVDS technology for data transfer. All signals from the chipboard of Timepix are connected through a VHDCI connector. Thanks to the FPGA, a level converter is not necessary, because IO gates of FPGA circuit can handle many voltage standards. The connection between the PC and FITPix is USB 2.0, because data-rate is 480 Mbit/s. This bus is available in each computer today. The FT2232H [7] (manufactured by FTDI) was selected because this chip provides a synchronous FIFO mode at 60 MHz which enables a high data-rate. The interface contains also the ADC and DAC. The AD converter measures analogue values from the detector which is necessary for diagnostic of the detector and the FITPix interface. The DA converter provides an accurate analogue voltage levels for the detector when diagnostics is needed. The interface needs several power supplies for the Timepix (2.2 V for the analogue and digital part separately), FPGA (1.2 V, 2.2 V, 2.5 V and 3.3 V), FTDI (3.3 V) and an integrated circuit which generates bias for the sensor (5 V). The bias voltage for sensor has a range from 5 V to 100 V. All of these components are placed on a six layer PCB. The VHDCI connector is placed on one side of the PCB and on the opposite side are placed connectors for the USB, bias voltage, external power supply and external signals.

2.3 Firmware for FPGA

The whole digital system in the FPGA is divided into two main parts. The first main part is the Control Unit which is responsible for communication with the PC through the USB 2.0. This unit decodes commands and transfers information to the others units with parameters (each command contains three bytes parameter). The second main part is the MPX Interface which fully controls the different detectors from the Medipix family according with commands from the PC. The first operation after power up is the detection of the number detectors in the chain. The maximum readout speed is 90 frames per second with a single chip (the serial readout frequency for the Timepix chip is 100 MHz). The FITPix can currently control up to 12 detectors in the daisy chain. If the detection is finished then FITPix sends systems information to the PC such as the number of detectors in the chain, system clock, readout clock and version of the firmware. Figure 3a shows in a flowchart how FITPix works. The interface supports all functions of the Timepix and brings in hardware triggering system.

Three modes of hardware trigger have been implemented (Figure 3b shows the principles of operation with HW Trigger):

1. *Started immediately and stopped by HW trigger*: measurement starts immediately and FITPix registers the measuring time in this mode. An external event terminates the measurement and the measuring time is transmitted to the PC.
2. *Started by HW Trigger, stopped by timer*: the device is waiting for an external event and the measuring time is determined by the HW timer in this mode.
3. *Started by HW Trigger, stopped by HW trigger*: if the signal External Trigger is logic low, the detector measures. The measuring time is also recorded in this mode.

The response for the external trigger event is very fast, the time delay between the signal Shutter and the External Trigger is 70 ns. The maximum frame-rate with the HW Trigger is 40

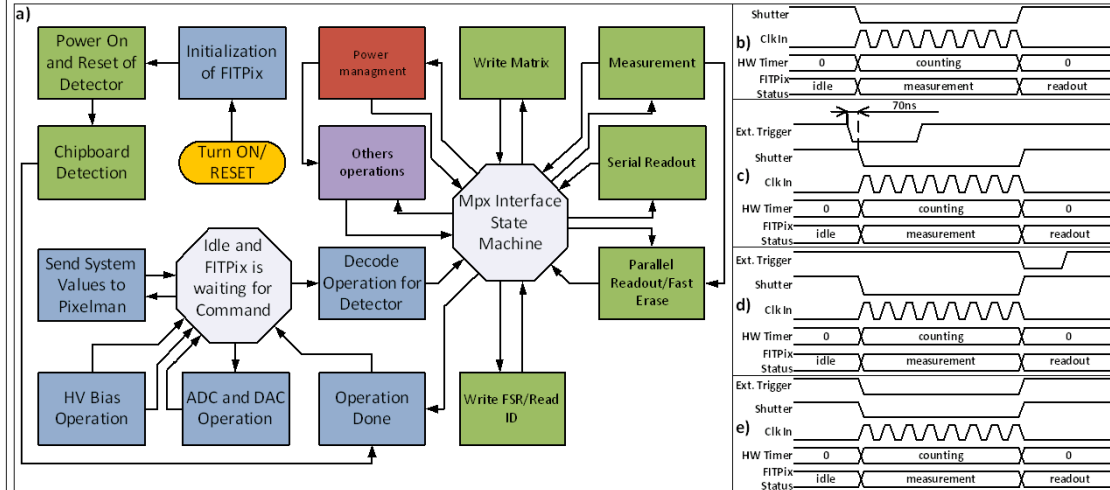


Figure 3. a) Flowchart of the FITPix interface, b) timing diagram of a typical measurement with the HW timer, c) timing diagram of first mode HW trigger Started immediately and stopped by HW trigger, d) timing diagram of first mode HW trigger Started by HW Trigger, stopped by timer, e) timing diagram of first mode HW trigger Started by HW Trigger, stopped by HW trigger.

frames per second. This frame rate determines the dead time which is the readout time and the transition into the measurement. The signal Busy (6th pin in the external connector) signalizes the dead time. If the signal Busy is active then the FITPix interface is not capable to process an external event.

2.4 Support of devices by the FITPix interface

The FITPix interface has been developed especially for the detector Timepix. However, FITPix is fully compatible with the detector Medipix 2 MXR because there is the exactly same digital interface for communication as those in Timepix. Another detector is the Medipix 3 which is the latest device for which a special version of firmware is required. There is a different approach for control and data acquisition because the internal control register controls Medipix 3. The Timepix detector uses input CMOS pins for control and the Medipix 3 uses LVDS standard. The frame rate is up to 50 frames per second for Medipix 3.

2.5 Results from first measurements

The main aim of new interface is high frame-rate which has been accomplished. Figure 4 shows the result from the first radiography measurement of ants with the FITPix and the Timepix detector. Figure 5 shows results from the previous USB 1.22 Interface. Since FITPix the dead time is only 11 ms and the transition to another picture is smooth. The motion is very coarse for pictures taken by USB 1.22 Interface whose dead time is 200 ms.

3 Conclusion

We have designed a new control and data acquisition interface for the Timepix detector based on the FPGA integrated circuit. We have achieved all targeted requirements. The readout speed is

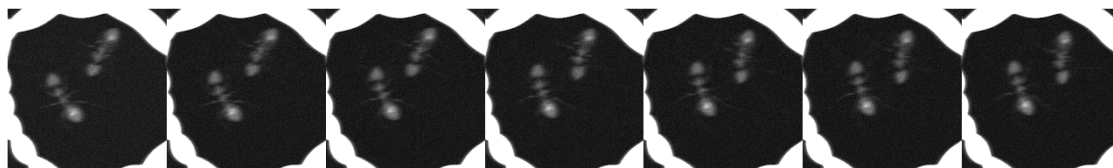


Figure 4. Sequence of radiograph pictures of ants. These pictures were taken with the FITPix interface. Thanks to the high frame-rate the motion is really smooth. Acquisition time is 10 milliseconds.

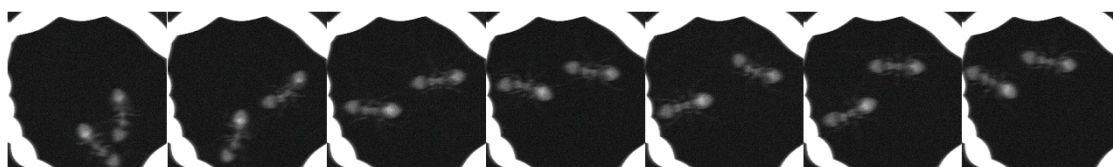


Figure 5. Similar sequence of radiograms of ants taken with the USB 1.0 Interface. Acquisition time is also 10 milliseconds.

up to 90 Mbit/s (≈ 90 fps) which opens new fields of applications. FITPix is about 20 times faster than the USB 1.1 Interface and it is almost two times faster than MUROS. It is fully powered from the USB bus. The interface must be powered from external power supply when several chips are connected. We have tested six detectors in a tile array chain with the interface fully operational. The firmware supports currently up to 12 chips in the chain. Another improvement is the HW triggering which has just a 70 ns delay, an adjustable internal measurement clock and an external measurement clock. The FITPix interface supports the older detector Medipix 2 MXR as well. Newly, the FITPix interface supports the latest detector Medipix 3. It is necessary to use special firmware for the Medipix 3 and an adapter board between FITPix and the detector chipboard. The power consumption is 775 mW for the FITPix interface. The low power consumption allows operation in vacuum without a particular cooling system.

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References

- [1] X. Llopart, R. Ballabriga, M. Campbell, L. Tlustos and W. Wong, Timepix, *A 65 k programmable pixel readout chip for arrival time, energy and/or photon counting measurements*, *Nucl. Instrum. Meth. A* **581** (2007) 485.
- [2] Web presentation of the MEDIPIX collaboration <http://medipix.web.cern.ch/MEDIPIX/>.
- [3] Z. Vykydal, J. Jakubek, M. Platkevic and S. Pospisil, *USB Interface for Medipix2 pixel device Enabling Energy and Position Detection of Heavy Charged Particles*, *Nucl. Instrum. Meth. A* **563** (2006) 112.

- [4] G. Bardelloni et al., *A new read-out system for an imaging pixel detector*, *IEEE Nucl. Sci. Symp. Conf. Rec.* **2** (2000) 57.
- [5] X. Llopert, M. Campbell, R. Dinapoli, D. San Segundo Bello and E. Pernigotti, *Medipix2, a 64 k pixel readout chip with 55 mm square elements working in single photon counting mode*, in *Proceedings of IEEE Nuclear Science Symposium and Medical Imaging Conference*, San Diego U.S.A., 4–10 November 2001.
- [6] R. Ballabriga et al., *Medipix3: A 64 k pixel detector readout chip working in single photon counting mode with improved spectrometric performance*, to be published in *Nucl. Instrum. Meth. A*.
- [7] Web presentation of the FTDI products at <http://www.ftdichip.com/Products/ICs/FT2232H.htm>.