

# Peter Hizalev

---

## CONTACT INFORMATION

Address: 6277 Valroy Drive, San Jose, CA 95123  
Phone: (510) 205-5386  
Email: [peter@hizalev.com](mailto:peter@hizalev.com)  
GitHub: [github.com/petrohi](https://github.com/petrohi)  
Blog: [k155la3.blog](https://k155la3.blog)

## SUMMARY

Experienced systems architect with a passionate interest in novel hardware and software-hardware interface.

## EXPERIENCE

**Co-founder and ML compiler lead, Tensil.AI, 2020-2022**

[Tensil.AI](#) was started in 2019 to find a novel approach to machine learning (ML) inference acceleration in hardware. The company went through the [YC](#) program in the summer of 2019. The initial approach was to unroll deep neural networks (DNN) onto hardware design with dedicated computation resources for each layer. This approach had two significant downsides. First, the resulting hardware was tied to the DNN architecture and would not allow easy modification if implemented in ASIC. Second, the approach required extreme quantization levels to maintain reasonable resource usage.

In 2020 the company pivoted to a more traditional processing unit architecture. The Tensil compute unit (TCU) is a processor with a systolic array at the core and a compact instruction set. The TCU is built with Chisel HDL in a way that enables deep architectural customization. This customization ability is the crucial differentiator allowing it to scale from low-cost and low-power embedded edge to the data center.

At Tensil, I mainly focused on DNN model compiler, emulation, and performance analysis. We established a hardware-software co-design cycle with many significant hardware advances made based on proof of concepts in the compiler and the emulator.

In 2021, we launched the Tensil.AI accelerator intellectual property (IP) and the toolchain optimized for Xilinx FPGAs. In early 2022 we open-sourced both IP and the toolchain at [github.com/tensil-ai/tensil](https://github.com/tensil-ai/tensil). I took on writing several [tutorials](#) to showcase Tensil and introduce machine learning and embedded audiences to FPGAs.

### **Director of engineering, 8x8 2017-2020**

I came to 8x8 with their acquisition of [Sameroom.io](#), where I was a co-founder and the CTO. While at 8x8, we took on re-implementing 8x8's team chat product. I was responsible for its architecture as well as the management of the team. In 2019 we launched a new 8x8 platform that unified team chat capabilities to be used by the entire portfolio of 8x8 products, seamlessly migrating existing customers.

### **Co-founder and CTO, Sameroom.io 2013-2017**

We started [Sameroom.io](#) as a team chat product. In 2015 we pivoted the company to become a bridging solution between various chat products. For example, users can connect their Skype group to a channel in Slack and have messages and files seamlessly replicated. As CTO, I led the product architecture and managed the team. In 2017 we sold Sameroom.io to 8x8, which remains one of the essential products in the portfolio.

### **Software architect, Xerox PARC 2009-2012**

I joined the Xerox PARC incubation project to productize research in natural language processing (NLP). I architected an intelligent email assistant product with a custom graph database at the core. The database allowed querying the semantic graph produced by indexing user email messages with PARC NLP algorithms. We launched it as a Microsoft Outlook plugin in 2011. Several patents have been filed as a result of my work.

### **Software architect, Mindjet 2000-2009**

I worked on many various projects during my tenure at [Mindjet](#). Most notably, I led the architecture for Mindjet's team collaboration product based on multi-user co-editing of mind map documents.

## **EDUCATION**

### **Lviv Polytechnic National University, Lviv, Ukraine**

- M.S. Computer Science, 2000
- B.S. Computer Science, 1998