tlv_pc_ifc Project Status			
Project File:	test_project.xise	**Parser Errors:**	No Errors
Module Name:	tlv_pc_ifc	**Implementation State:**	Placed and Routed
Target Device:	xc3s50-4pq208	• **Errors:**	No Errors
Product Version:	ISE 13.1	• **Warnings:**	102 Warnings (102 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary [-]				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	250	1,536	16%	
Number of 4 input LUTs	596	1,536	38%	
Number of occupied Slices	445	768	57%	
Number of Slices containing only related logic	445	445	100%	
Number of Slices containing unrelated logic	0	445	0%	
Total Number of 4 input LUTs	635	1,536	41%	
Number used as logic	595			
Number used as a route-thru	39			
Number used as Shift registers	1			
Number of bonded IOBs	26	124	20%	
Number of RAMB16s	3	4	75%	
Number of MULT18X18s	1	4	25%	
Number of BUFGMUXs	1	8	12%	
Average Fanout of Non-Clock Nets	3.22			

Performance Summary [-]			
Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports [-]					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	po 1. VI 18:19:42 2015	0	102 Warnings (102 new)	9 Infos (9 new)
Translation Report	Current	po 1. VI 18:19:48 2015	0	0	0
Map Report	Current	po 1. VI 18:19:56 2015	0	0	4 Infos (4 new)
Place and Route Report	Current	po 1. VI 18:20:33 2015	0	0	3 Infos (3 new)
Power Report					
Post-PAR Static Timing Report	Current	po 1. VI 18:20:36 2015	0	0	5 Infos (5 new)
Bitgen Report					

Secondary Reports [-]		
Report Name	**Status**	**Generated**

Date Generated: 06/01/2015 - 18:33:24