CZECH TECHNICAL UNIVERSITY IN PRAGUE

Faculty of Electrical Engineering

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Technical report

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Table 2 - 1 Control signal encoding table for instructions to be processed by the Division Module.

State	RTL Code	14 ld0	13 ld1	12 ld2	11 ld3	10 ld4	9 SelR1	8 SelR2[1]	7 SelR2[0]	6 SelR3	5 SelR4	4 SelSh1	3 SelM1[1]	2 SelM1[0]	1 SelM2	0 SelS1	CV
S0	R1 ← D;	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	2000h
S1	R1 ← R1 « 32; (Sh1)	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0	2210h
S2	R2 ← 1.882 x R1; (M1) R3 ← N;	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	1804h
S3	R2 ← 2.82 - R2; (Sub1) R3 ← R3 « 32; (Sh1)	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	18C0h
S4	R4 ← R2 x R1; (M1)	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	420h
S5	R4 ← R2 x R4; (M1) R2 ← 2 x R2; (M2)	0	0	1	0	1	0	1	0	0	1	0	1	0	0	0	1528h
S6	R2 ← R2 - R4; (S1)	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	1081h
S7	R4 ← R2 x R3; (M2)	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	402h
S8	R0 ← R4;	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	4000h

Conclusion

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Appendix A: List of symbols and abbreviations

A.1 List of abbreviations

SoC System on a chip

A.2 List of symbols

P_n (W) jmenovitý výkon stroje