ECE4514 Spring 2019
Homework 10: Final Project - Deliverables

Final Project Deliverable Due on 4 May 11:59PM

This note describes the deliverables for your final project.

- By Saturday 4 May, you have to deliver a repository with Verilog source code, and a fully functioning project according to the specification you have prepared for Homework 9. Follow the homework 10 link to create a private repository on github where you can upload your work.
- For the last lecture, on 7 May, you may be asked to briefly talk about your design in class (5-min). Participation is voluntary, and does not affect your grade either way. You will be notified beforehand (by Monday 5/6 evening) if you will be asked to speak in front of the class.

Project Deliverable

The project you upload on your repository contains two components: the Verilog code you created (the entire Quartus project, cleaned from intermediate files and code), and a short report in PDF format.

The Quartus project needs to include all Verilog Source Code for your project, as well as a compiled bitstream (sof file). Do not deliver buggy/incomplete code; everything you turn in as your final project needs to work.

The report needs to conclude a block diagram of the system that you have implemented, with sufficient detail to express individual Verilog Modules. If you have used third-party modules, clearly list the source references. The report does need to be extensive: the most important element of the project deliverable is the actual Quartus project. The report is only meant as a guide for the instructor and TA to understand your project design.