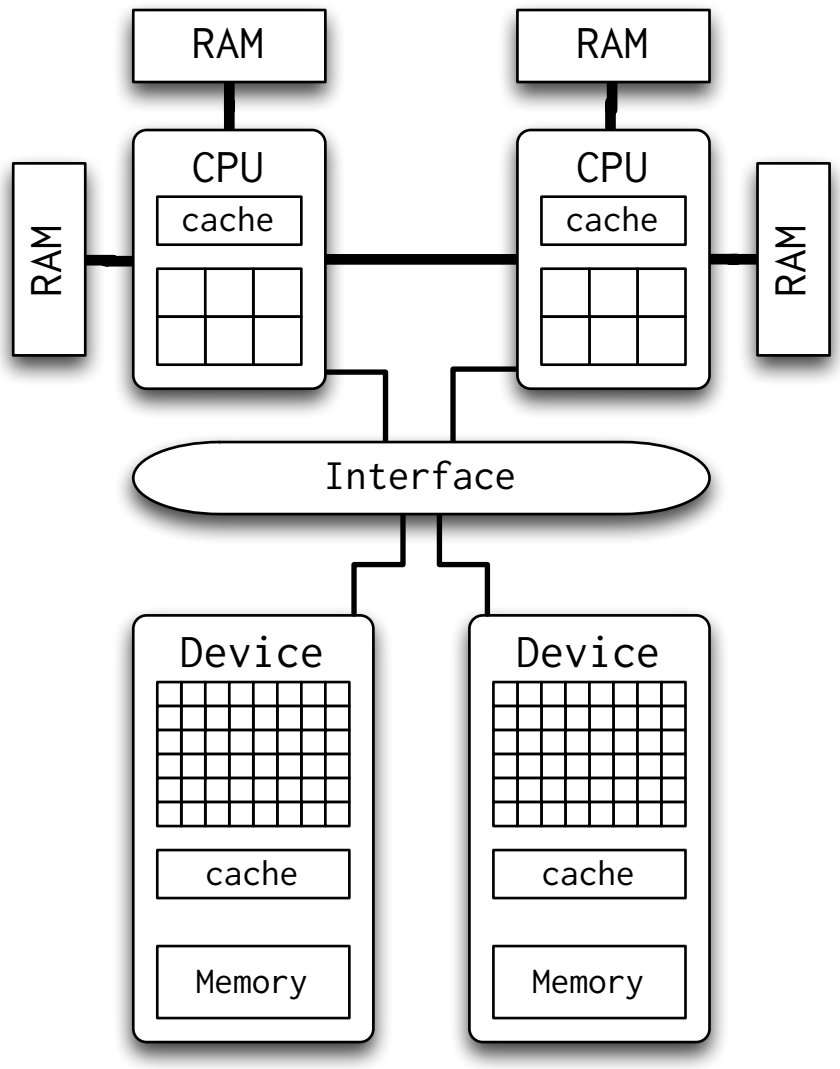
Heterogeneous Platforms

One or more computational nodes interconnected, allowing different CPU chips to work together;

Accelerator devices inside the computational nodes, working side by side with the CPU;

Distributed Memory architectures: data has to be explicitly transferred between distinct memory spaces.



	2005	2006	2007	2008	2009	2010	2011	2012
Intel	*Paxville*		*Kentsfield*	*Dunnington*		*Beckton*	*Westmere*	*Knights Corner*
	2 cores		4 cores	6 cores		8 cores	10 cores	60 cores
NVidia		*G80*		*GT200*	*Fermi*			*Kepler GK110*
		128 cores		240 cores	512 cores			2,688 cores

Environmental Setup

- 2× Intel Xeon E5-2650 @ 2.00 GHz
  - ⇒8 cores;
  - ⇒HyperThreading technology (2 threads / core);
  - ⇒Sandy Bridge micro-architecture;
- 64GB of RAM @ 1333 MHz (NUMA)
- Intel C++ Compiler 12.0.0
- Intel Math Kernel Library 11.0
- Armadillo C++ linear algebra library 3.800.2

Methodology

- Best result of 3 measurements, which differ no more than 5%;
- Minimum: 10 measurements;
- Maximum: 20 measurements;