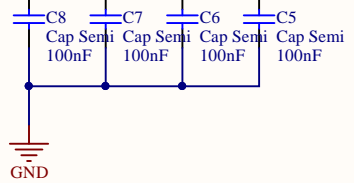
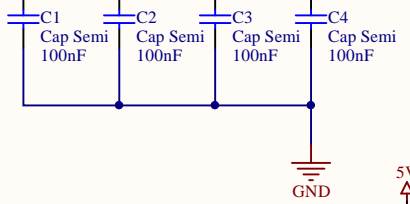
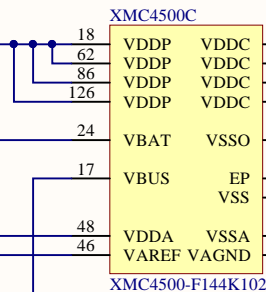


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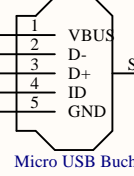
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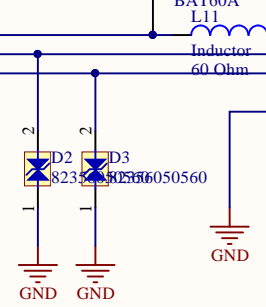
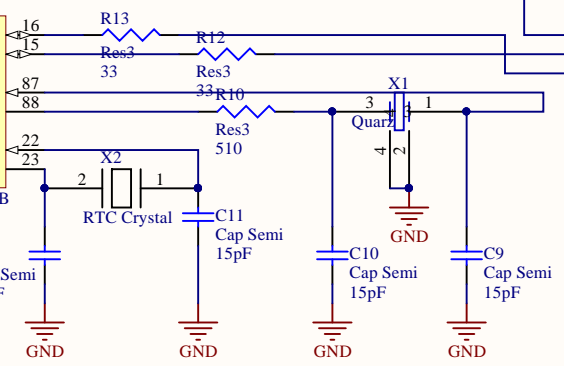
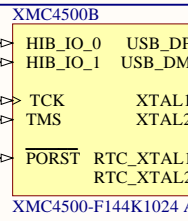
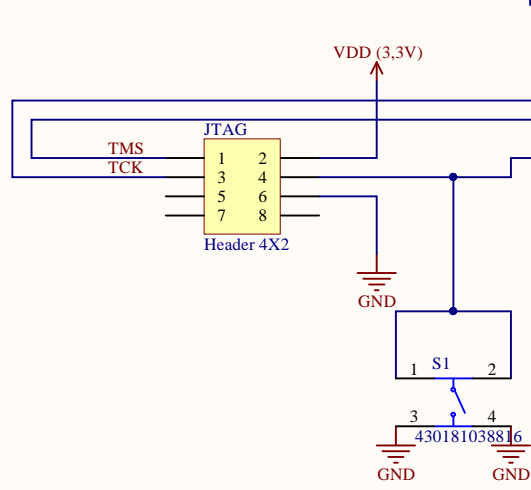
5V



J1



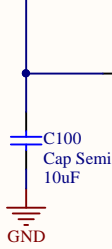
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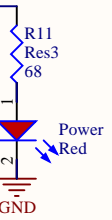
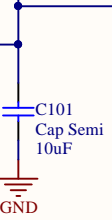
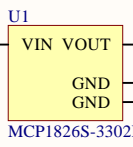
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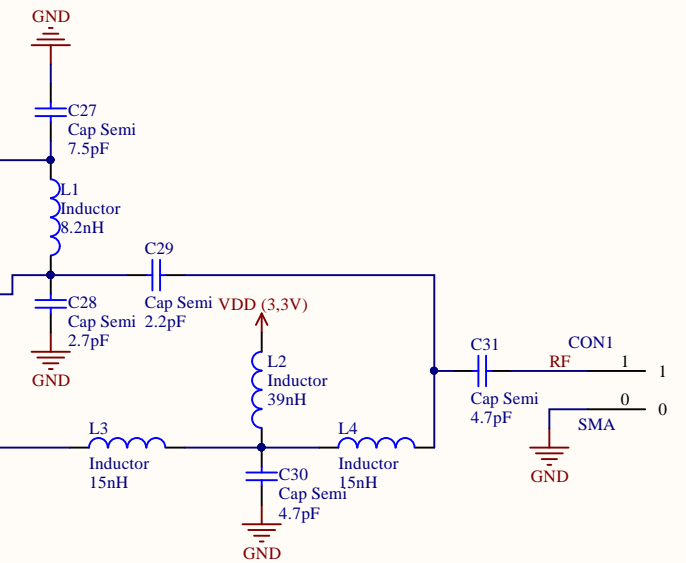
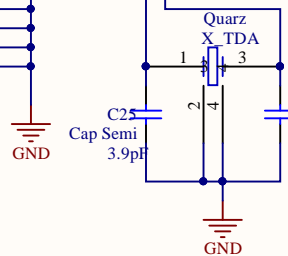
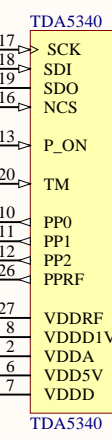
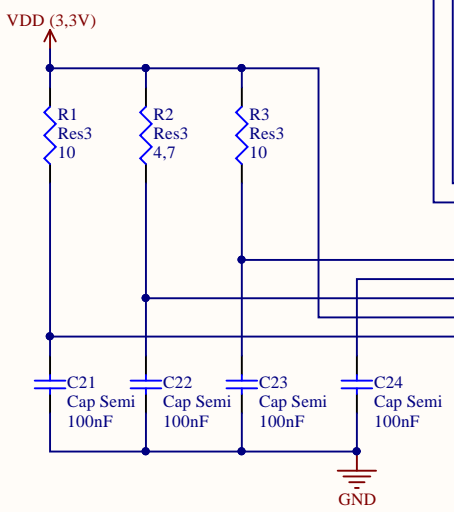
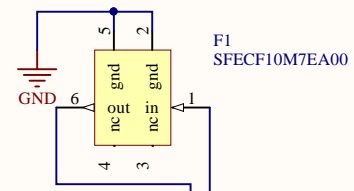
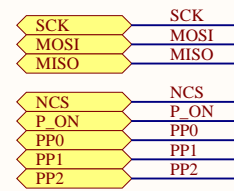
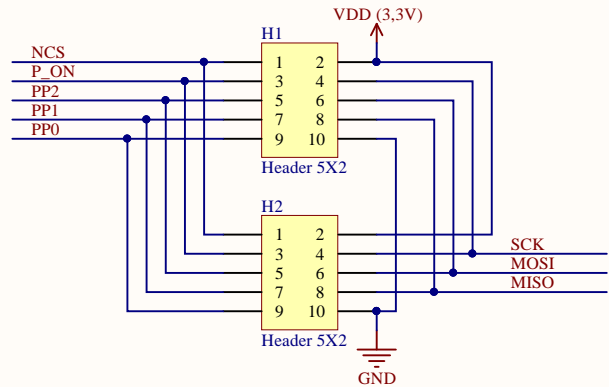
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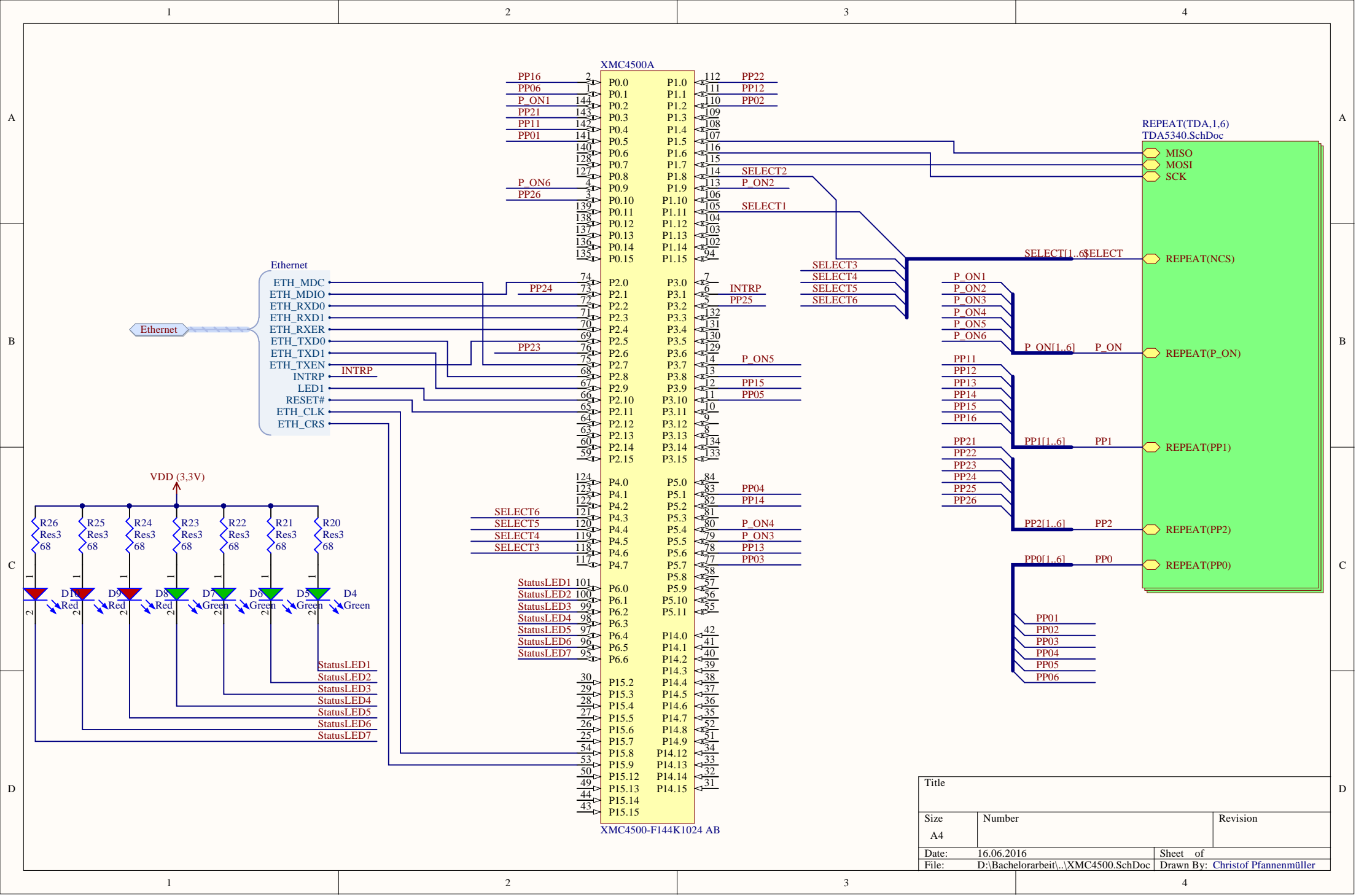
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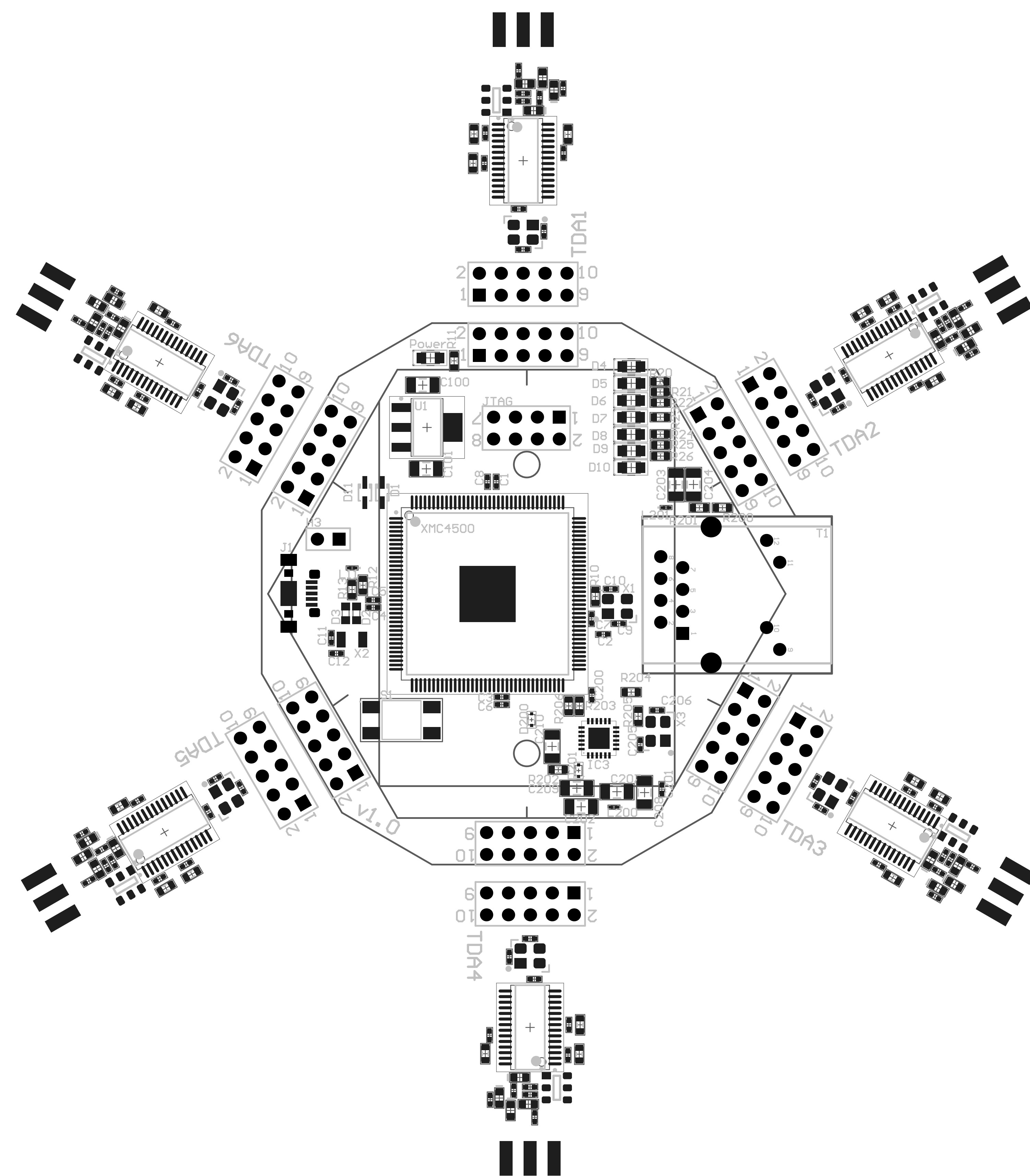


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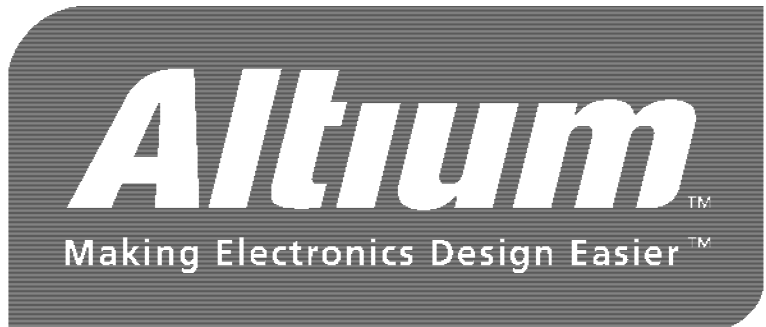
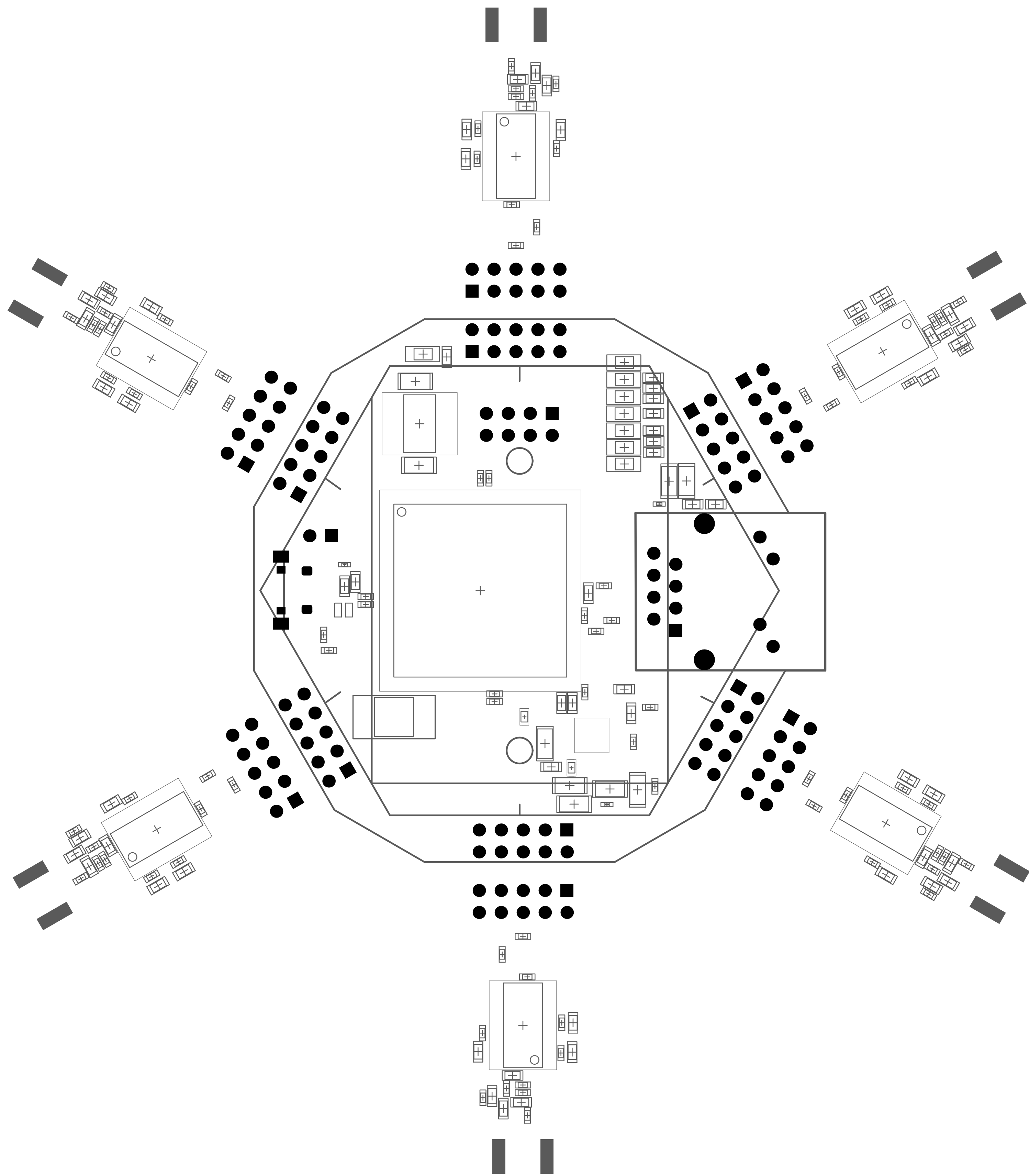
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ENGINEER: <b>Christof Pfannenmueller</b>	TITLE:	
PCB DESIGNER:		
DATE: 16.06.2016	PART NO.:	REV:
FILE NAME: PCB_Testplatine.PcbDoc	DWG NO:	SCALE:



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ENGINEER: Christof Pfannenmueller	TITLE:		
PCB DESIGNER:			
DATE: 16.06.2016	PART NO.:	REV:	
FILE NAME: PCB_Testplatine.PcbDoc	DWG NO:	SCALE:	