USIC

Universal Serial Interface Channel

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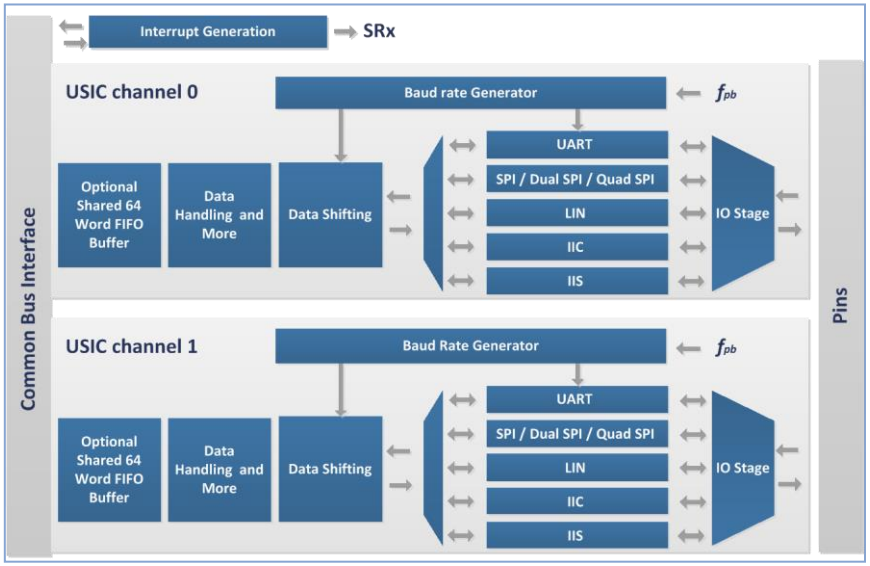


Highlights

Each USIC module provides two universal serial communication channels to interface with external devices. It is tailored for various serial protocols like UART, SPI, IIC and IIS. A shared 64 words FIFO buffer is available in each USIC module.

Key Feature

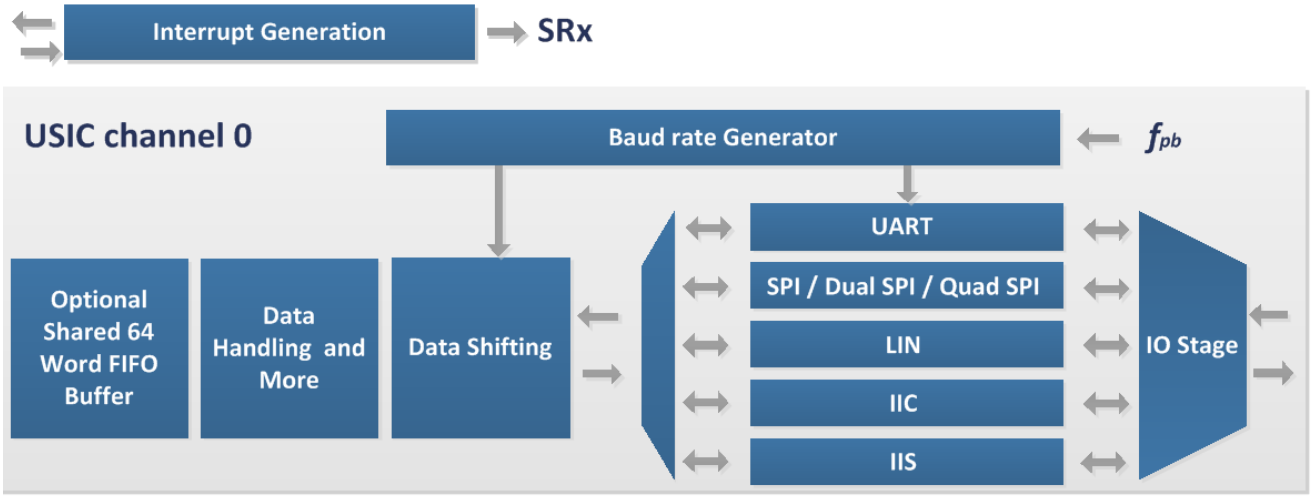
- Flexible serial interface that supports UART, SPI, IIC and IIS protocol
- Support for Standard, Dual and Quad SPI mode
- Shared FIFO buffer available in every USIC channel

Customer Benefits

- Common serial communication protocol are supported by one peripheral
- Direct hardware control of all signals needed for external memory device
- Offload CPU and CPU can perform other critical task

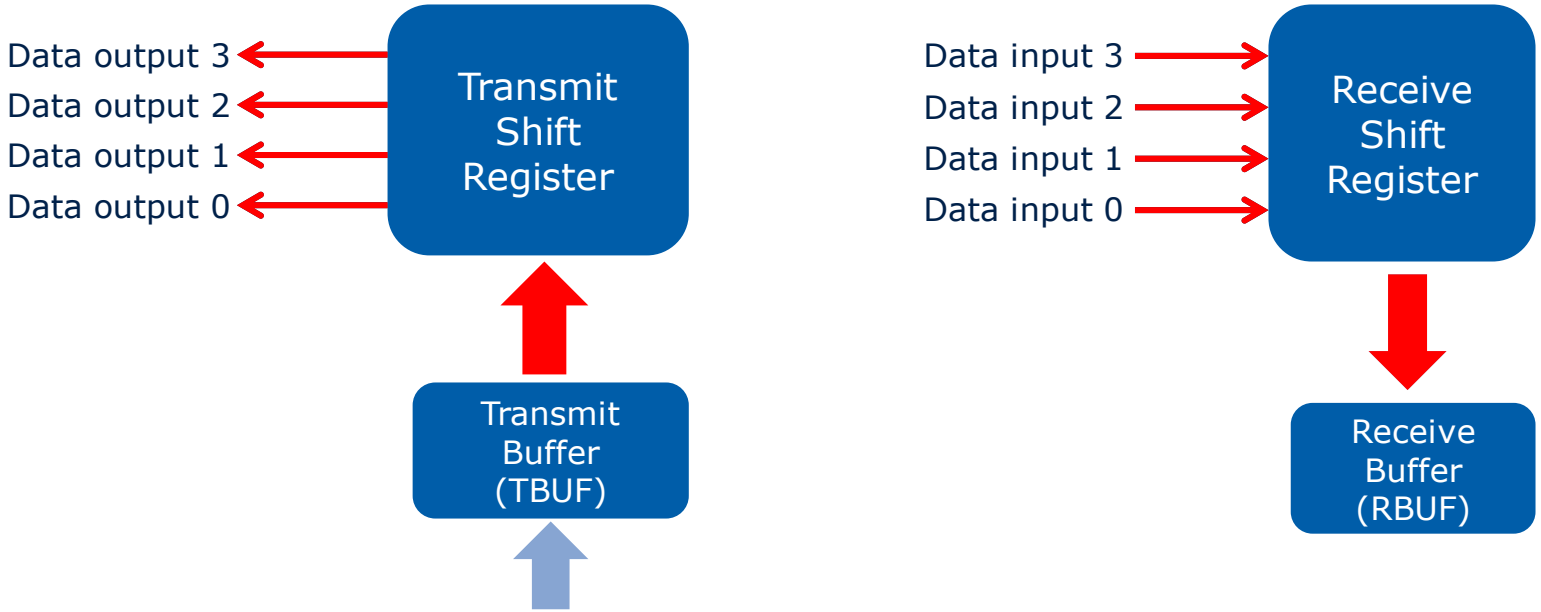
USIC
Flexible Serial Interface Protocol

- USIC support different serial communication protocols on every channel
  - UART, SSC/SPI, IIC, IIS
- This gives user the flexibility to select the desired serial interface on each USIC channel
- This flexibility allows user to have the same or different protocol on the each USIC channel



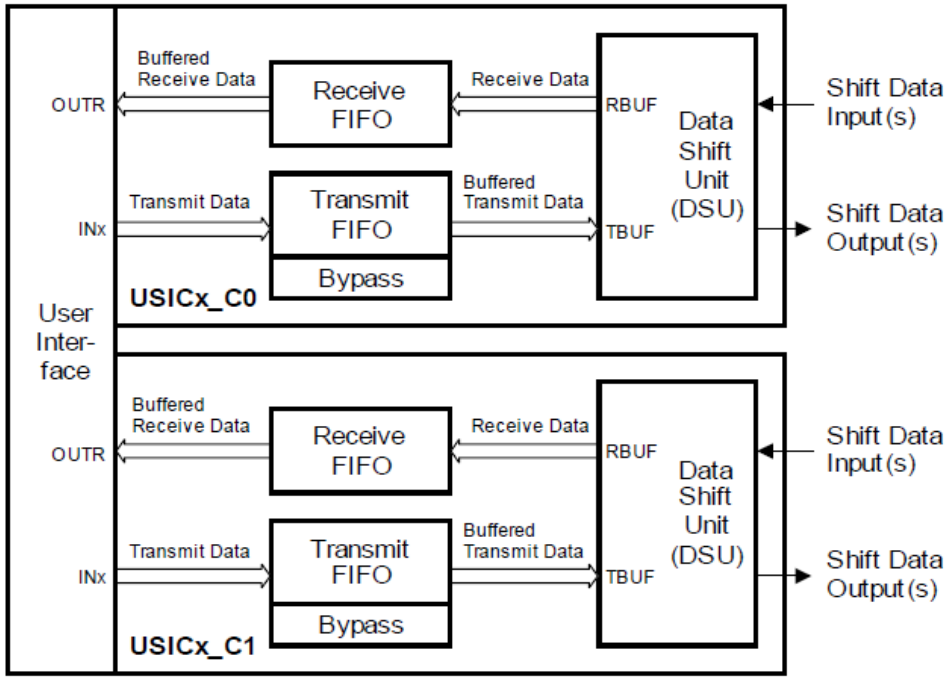
USIC
Support Dual and Quad-SPI

- The transmit data can be shifted out one, two or four bits each time depending on the selected mode
- Receive data also can be shifted in one, two or four bits each time depending on the selected mode
- The data throughput on Quad-SPI four times higher than the standard SPI

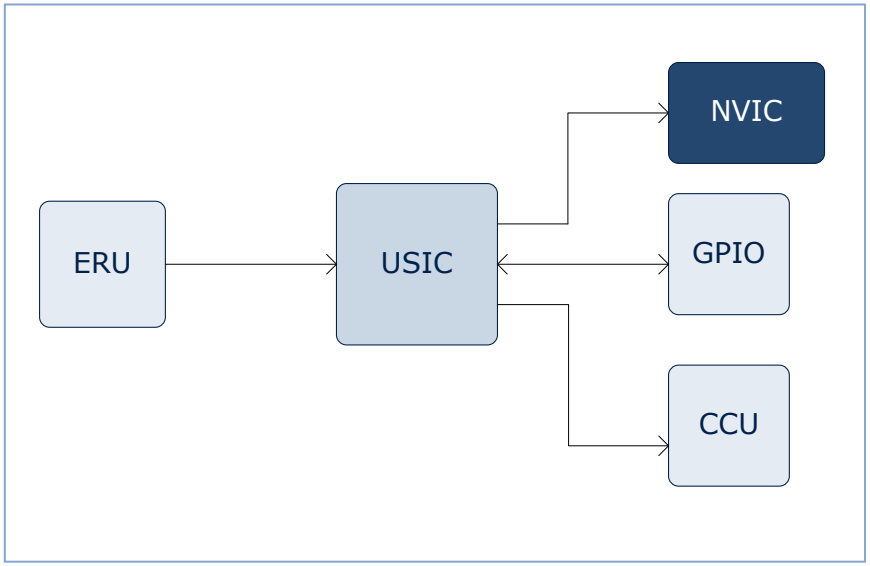


USIC
FIFO Buffer Capability

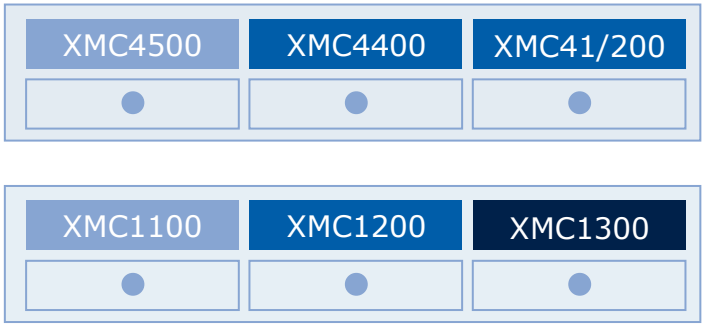
- Total of 64 data words buffer entries shared between two channel for transmit and receive.
- User configurable FIFO buffer size.
- Offload CPU to perform other tasks while the USIC is transmitting.



USIC
System Integration



- Target applications
  - Connectivity/Communication



USIC is interconnected with several modules in the MCU system.

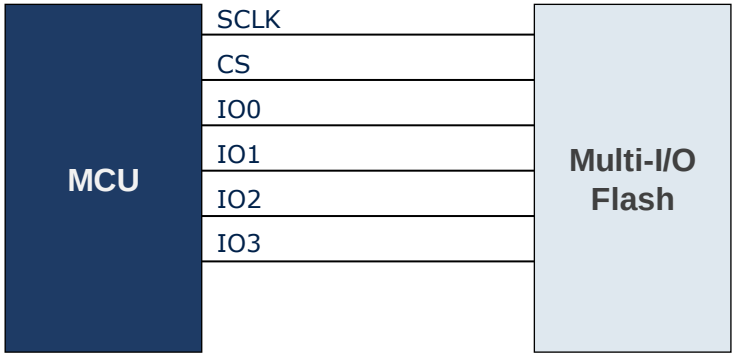
NVIC – To generate interrupt

GPIO – Signal connection to the Input and Output pins

ERU – If the input to USIC does not have direct connection to USIC, the signal can be mapped to ERU module and connected to USIC

CCU4 – Input signal to CCU4 module

Application Example
Interface with external flash via Quad SPI



In Brief

USIC able to interface with external flash that support multi I/O via quad SPI communication where data throughput can be dramatically increase compare to the standard SPI communication.

Overview

In today's market, there are SPI flash memory that support multiple I/O SPI capability. This means the transferring of data is done with multiple data lines using SPI protocols.

To support this feature, Dual and Quad SPI has been implemented into USIC module. Using quad SPI to interface with external flash, the data throughput is increase by four times over standard SPI.

This allows application that requires higher data transfer rate to external memory can be implemented using USIC. As the protocol is taken care by the USIC module, software implementation to transfer and receive data becomes simple and easy.

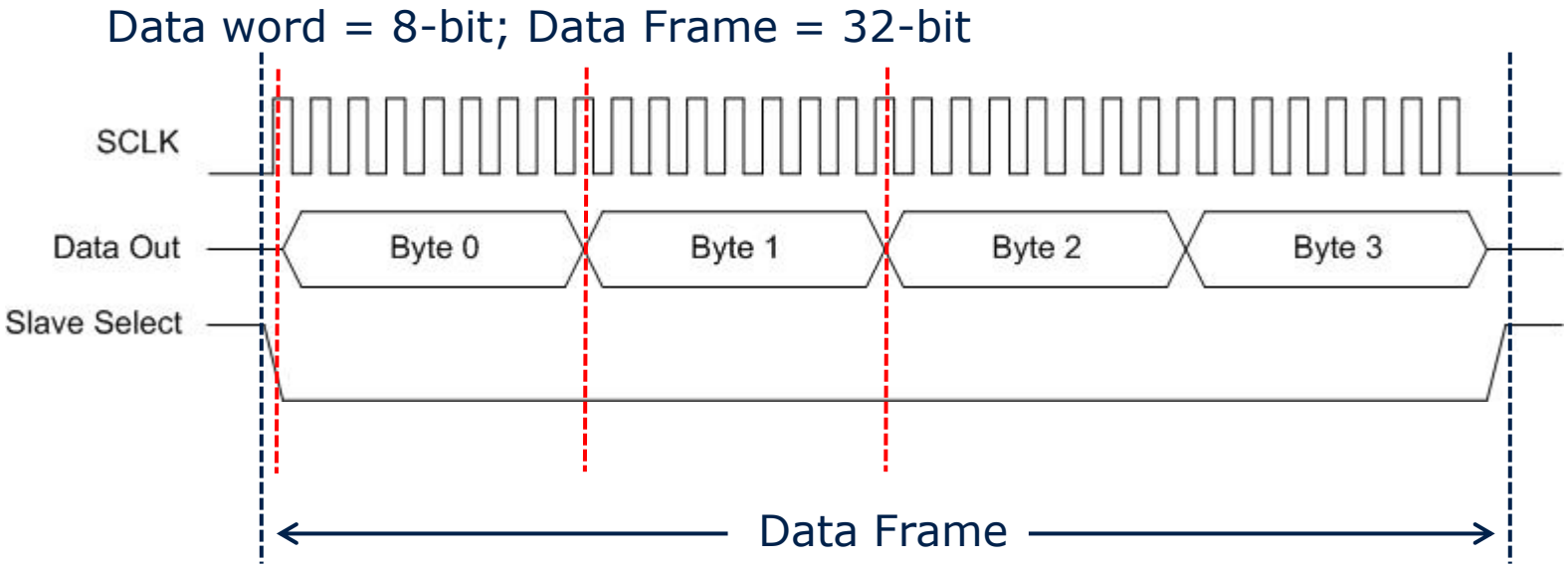
USIC - Highlight features
Table of Content

- Flexible Data Word and Data Frame Length Control
- Transmit Control Information
- Flexible Routing
- Transfer Trigger Capability
- Interrupt Events
- Baud Rate Generation
- Debugger Support

USIC - Highlight features
Flexible Data Word and Data Frame Length Control

- There are two options to handle data frame size
- Option 1: Known frame length
  - Set to a fixed length
  - Support up to 63-bit

Example: SPI in Master Mode

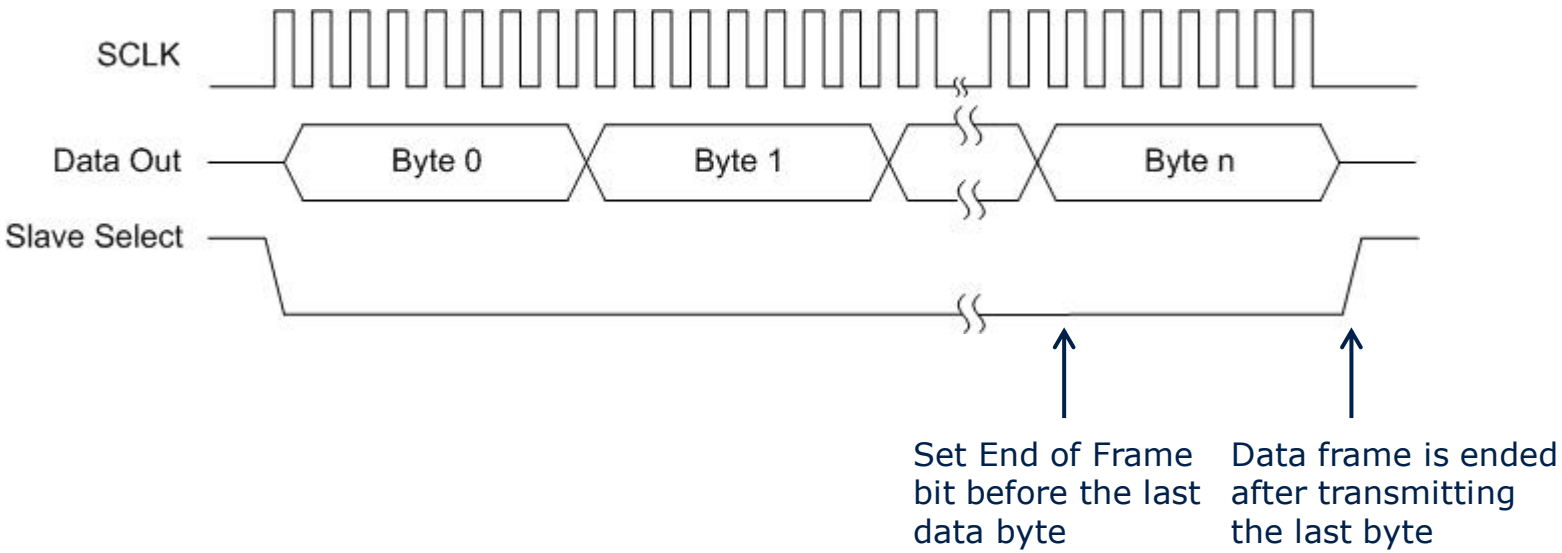


USIC - Highlight features
Flexible Data Word and Data Frame Length Control

- Option 2:Flexible frame length
  - Provide infinite frame length
  - The frame length can be dynamically controlled by End of frame bit

Example: SPI in Master Mode

Data word = 8-bit; Data Frame = 64 (infinite)



USIC - Highlight features
Transmit Control Information (1/3)

- Transmit control information (TCI) is a 5-bit data generated automatically when the data to be transmit is written to the transmit buffer input location TBUFx or FIFO transmit buffer - INx (x = 00 – 31).

TCI = 00000	TBUF00 / IN00
TCI = 00001	TBUF01 / IN01
…	…
TCI = 11111	TBUF31 / IN31

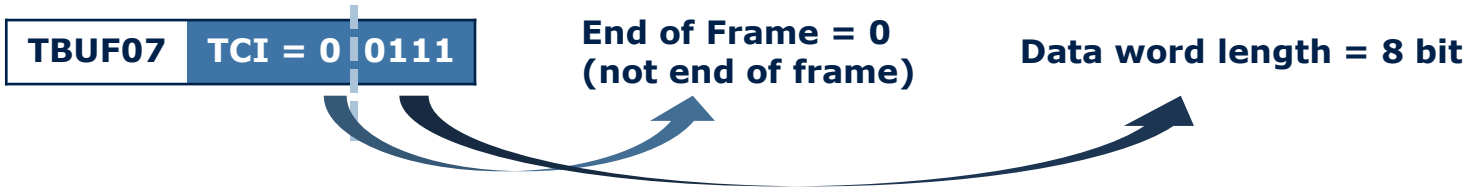
- TCI can be used as an additional control parameter for various function such as:
  - Dynamic change of data word length or data frame length
  - Automatic slave select for SPI
  - Channel select control for IIS

USIC - Highlight features
Transmit Control Information (2/3)

- Dynamic change of data word length
  - With correct configuration, TCI can be use to adjust data word length and to end the data frame.
  - Bit 3 – 0 of TCI configures the data word length and bit 4 of TCI indicates this is last data of the frame (End of Frame).

Example:

1) Writing data to TBUF07



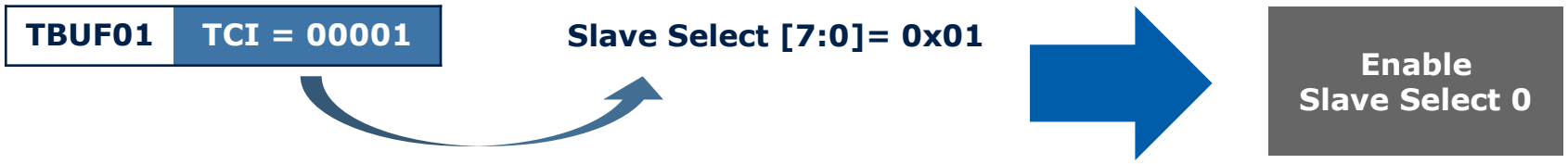
2) Writing data to TBUF23

USIC - Highlight features
Transmit Control Information (3/3)

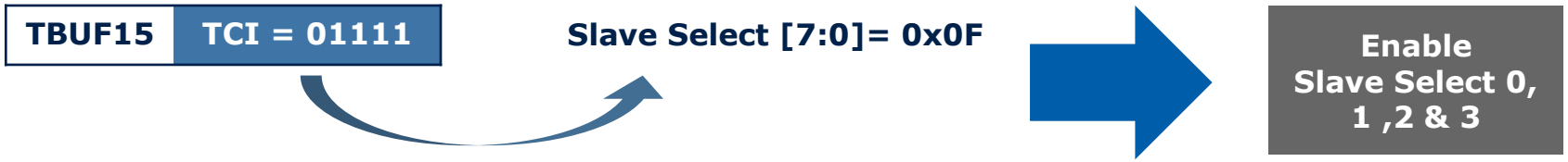
- Automatic Slave select
  - TCI also can be used to trigger slave select signal automatically when USIC is operated in SPI Master mode.
  - Total of 8 slave select signal available in each USIC channel and the generated 5-bit TCI value can control only Slave select signal 0 – 4.

Example:

1) Writing data to TBUF01

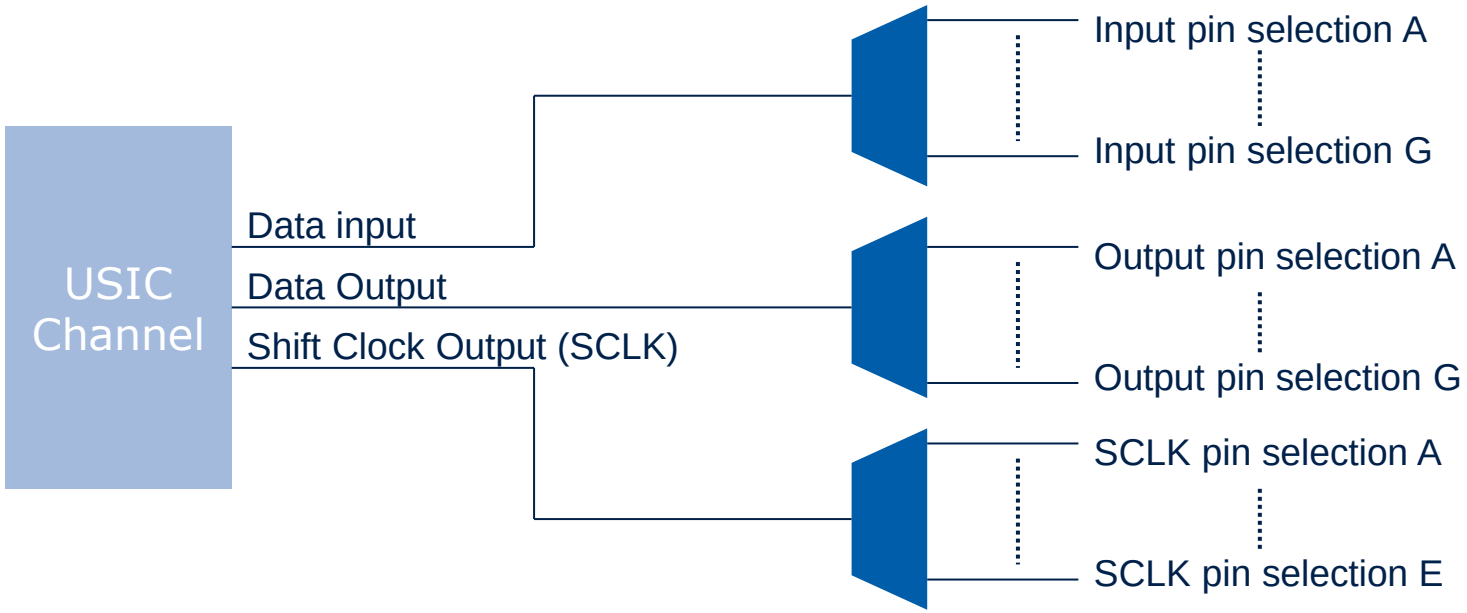


2) Writing data to TBUF15



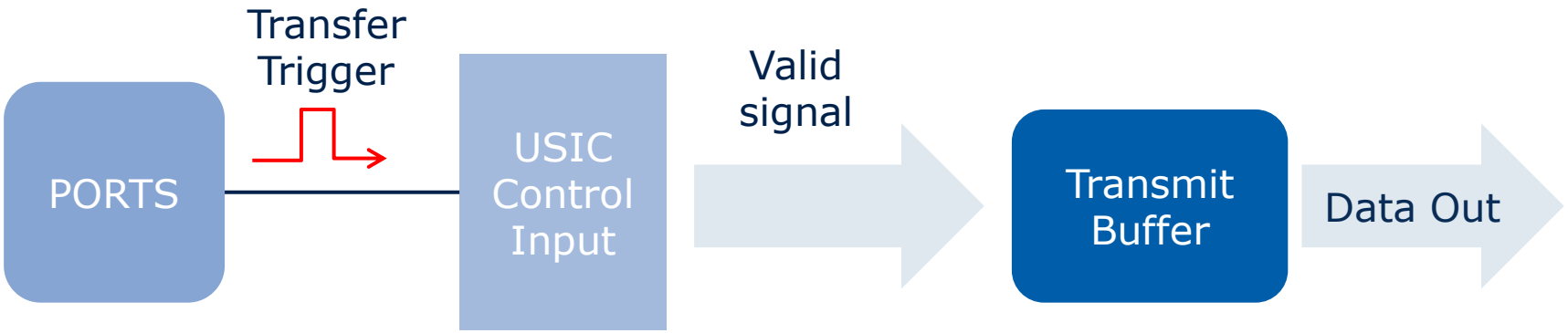
USIC - Highlight features
Flexible Routing

- Each channel offers several possible input and output pins
- Pin reconfiguration without resetting the device
- Refer to USIC-Interconnect chapter in device Reference Manual on the available pins for USIC transmit and receive pin



USIC - Highlight features
Transfer Trigger capability

- Data transfer can be gated and only transfer when trigger signal is triggered.
- Events outside USIC module (i.e. CCU4 timer or input pin) can trigger a data transfer.

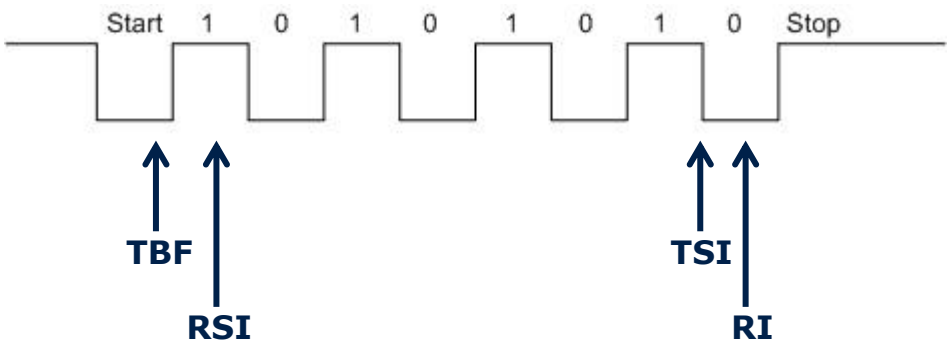


- Refer USIC-Interconnect chapter in device Reference Manual for the available pins for USIC Control Input.

USIC - Highlight features
Interrupt Events (1/2)

- Support various interrupt for every protocol
  - Transmit Shift interrupt (TSI)
  - Transmit Buffer interrupt (TBF)
  - Standard Receive interrupt (RI)
  - Received Start interrupt (RSI)
  - Alternative Receive interrupt
  - Data Lost interrupt

(e.g. UART data word)

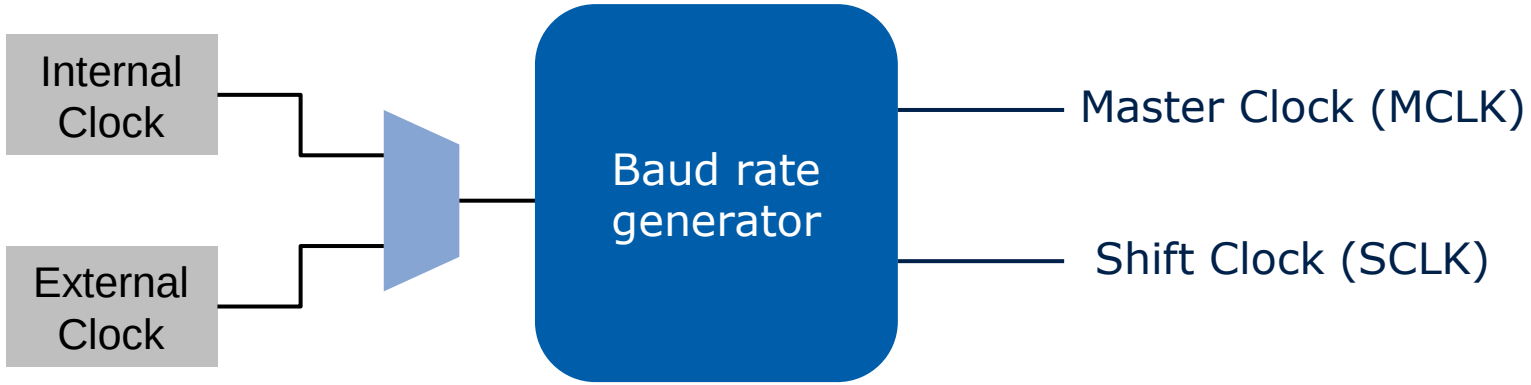


USIC - Highlight features
Interrupt Events (2/2)

- Alternative Receive Interrupt
  - UART – Parity error occurs
  - SPI – Reception of first data word in a data frame
  - IIC – First data word of new data frame
  - IIS – Data for the right channel
- Support also protocol related interrupt
  - Some examples:
    - UART – Noise detection, Collision detection, Sync break detection..etc
    - SPI – MSLS event, Slave Select input event, Parity Error Interrupt
    - IIC – Start Condition, Stop Condition, ACK received, NACK received..etc
    - IIS – WA rising/ falling edge, WA end event, Trigger signal activation

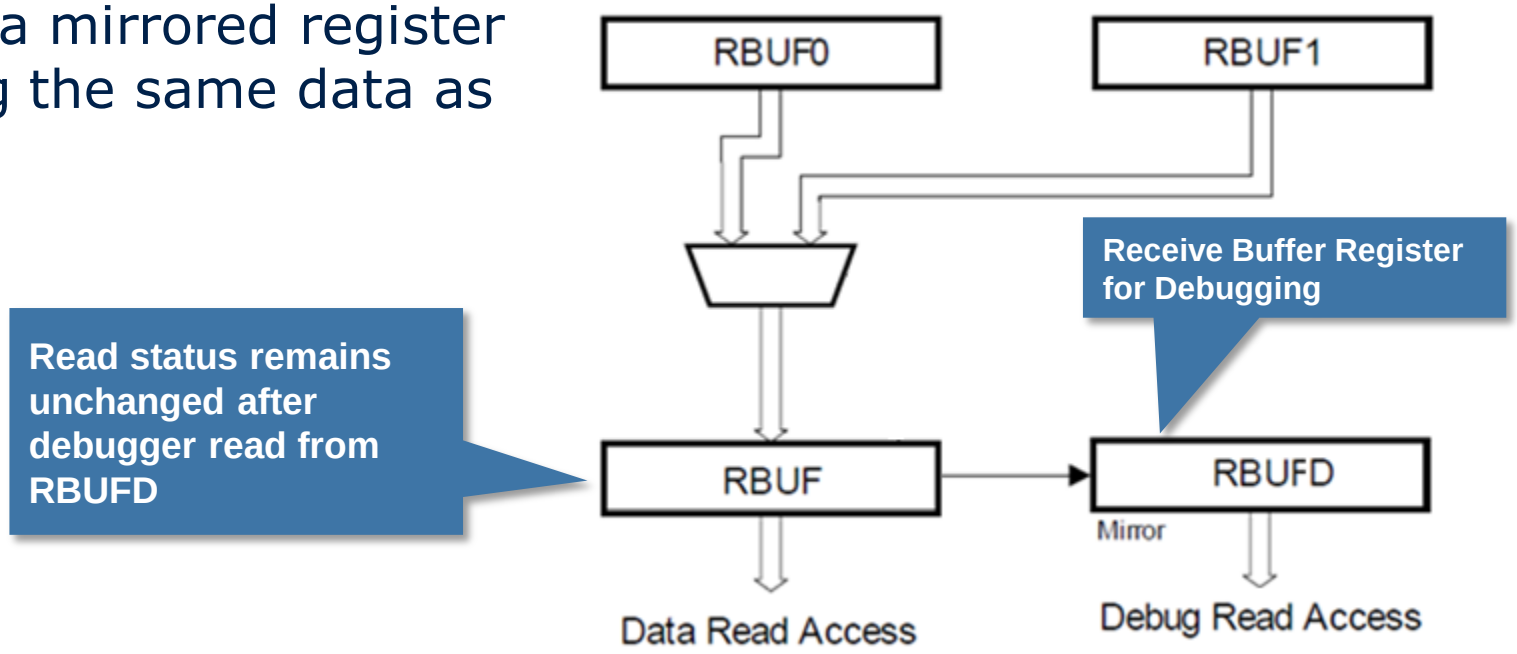
USIC - Highlight features
Baud Rate Generation

- Dedicated baud rate generator available on each USIC channel to provide independent baud rate generation
- USIC baud rate can be selected from internal system frequency or external clock source
- Baud rate generator provides protocol specific signal generation



USIC - Highlight features
Debugger Support

- When received data read from received buffer (RBUF), the read status will changed and new incoming data will be transferred to RBUF
- To prevent read status changed during debugging, USIC offer receive buffer register for debugging (RBUFD)
- RBUFD is a mirrored register containing the same data as RBUF



General Information

- For latest updates, please refer to:

  http://www.infineon.com/xmc1000

- For support:

  http://www.infineonforums.com/forums/8-XMC-Forum

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