EPSON TOYOCOM

Application Manual

Real Time Clock Module

RTC-62421/3

Model	Product Number
62421	Q42624211xxxx00
62423	Q42624231xxxx00

EPSON TOYOCOM CORPORATION

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CONTENTS

4-Bit Parallel Interface Real Time Clock Module

RTC-62421 /RTC-62423

- Built-in quartz crystal removes need for adjustment and reduces installation costs
- Microprocessor bus compatible(Tww, tRD = 120 ns)
- Use of C-MOS IC enables low current consumption (1.8 μA Max. at VDD = 2.0 V)
- Compatibility with Intel CPU bus
- Address latch enable (ALE) pin compatible with multiplex bus CPUs
- Time (hours, minutes, seconds) and calendar (year, month, day) counter
- 24-hour/12-hour switch over and automatic leap-year correction functions
- Fixed-period interrupt function
- 30-seconds correction (adjustment) function
- Stop, start, and reset functions
- Battery back-up function
- Same mounting conditions as general-purpose SMD ICs possible (RTC-62423)

* Pins and functions compatible with the MSM6242B series

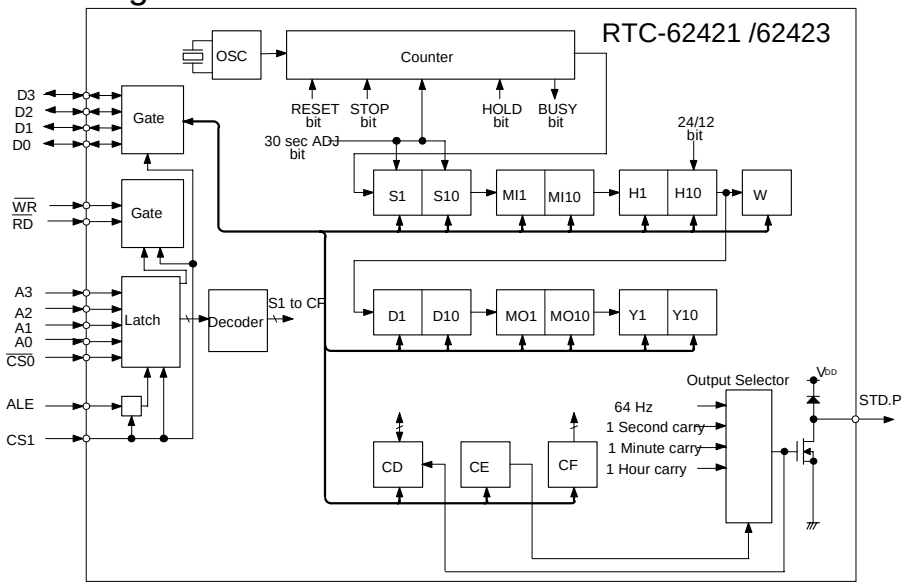
■ Overview

The RTC-62421 /RTC-62423 module is a real time clock that can be connected directly to a microprocessor's bus. Its built-in quartz crystal enables highly accurate timekeeping with no physical access required for adjustment and, since there is no need to connect external components, mounting and other costs can be reduced.

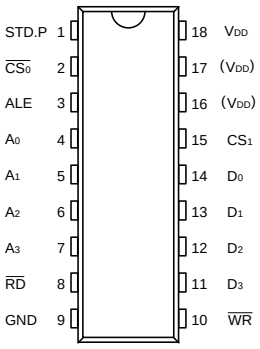
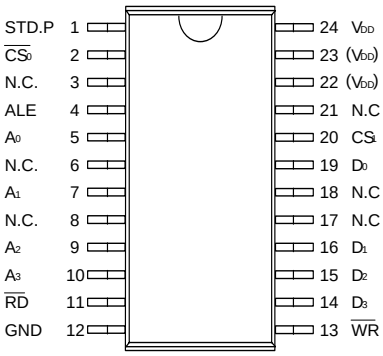
In addition to its time and calendar functions, the RTC-62421 /RTC-62423 enables the use of 30-seconds correction and fixed-period interrupt functions.

The RTC-62421 /RTC-62423 module is ideally suited for applications requiring timing management, such as personal computers, dedicated word processors, fax machines, multi-function telephones, and sequencers.

■ Block diagram

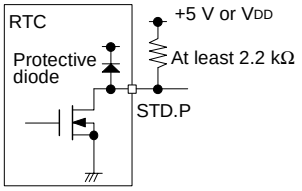


■ Pin connections

RTC-62421	RTC-62423
	

The (VDD) pins are at the same electrical level as VDD. Do not connect these pins externally.
The N.C. pins are not connected internally. Ground them in order to prevent noise.

■ Pin functions

<table>
<tr><th rowspan="2">Signal</th><th colspan="2">Pin No</th><th rowspan="2">Input/ Output</th><th rowspan="2">Function</th></tr>
<tr><th>RTC-62421</th><th>RTC-62423</th></tr>
<tr><td>D0 -D3
(Data bus)</td><td>14,13,12,11</td><td>19,16,15,14</td><td>Bi-direction</td><td>Connect these pins to a bi-directional data bus or CPU data bus. Use this bus to read to and write from the internal counter and registers.
<table>
<tr><th>CS1</th><th>$\overline{CS0}$</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>Mode of D0 to D3</th></tr>
<tr><td>H</td><td>L</td><td>L</td><td>H</td><td>Output mode (read mode)</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>L</td><td>Input mode (write mode)</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>L</td><td>Do not use</td></tr>
<tr><td>L</td><td colspan="3">H or L</td><td>High impedance (back-up mode)</td></tr>
<tr><td>H</td><td>H</td><td colspan="2">H or L</td><td>High impedance (RTC not selected)</td></tr>
</table></td></tr>
<tr><td>A0 -A3
(Address bus)</td><td>4,5,6,7</td><td>5,7,9,10</td><td>Input</td><td>Address input pins used for connection to CPU addresses, etc. Used to select the RTC's internal counter and registers (address selection). When the RTC is connected to a multiplexed-bus type of CPU, these pins can also be used in combination with the ALE described below.</td></tr>
<tr><td>ALE
(Address Latch Enable)</td><td>3</td><td>4</td><td>Input</td><td>Reads in address data and $\overline{CS0}$ state for internal latching. When the ALE is high, the address data and $\overline{CS0}$ state is read into the RTC. When the (through-mode) ALE falls, the address data and $\overline{CS0}$ state at that point are held. The held address data and $\overline{CS0}$ status are maintained while the ALE is low.
<table>
<tr><th>ALE</th><th>Address data and $\overline{CS0}$ status</th></tr>
<tr><td>H</td><td>Read into the RTC to set address data</td></tr>
<tr><td>L</td><td>Held in the RTC (latched at the trailing edge of the ALE)</td></tr>
</table>
If the RTC is connected to a CPU that does not have an ALE pin and thus there is no need to use this ALE pin, fix it to V_{DD}.</td></tr>
<tr><td>$\overline{WR}$
(WRite)</td><td>10</td><td>13</td><td>Input</td><td>Writes the data on D0 to D3 into the register of the address specified by A0 to A3, at the leading edge of $\overline{WR}$.
Make sure that $\overline{RD}$ and $\overline{WR}$ are never low at the same time.</td></tr>
<tr><td>$\overline{RD}$
(ReaD)</td><td>8</td><td>11</td><td>Input</td><td>Outputs data to D0 to D3 from the register at the address specified by A0 to A3, while $\overline{RD}$ is low.
Make sure that $\overline{RD}$ and $\overline{WR}$ are never low at the same time.</td></tr>
<tr><td>CS1, $\overline{CS0}$
(Chip Select)</td><td>15, 2</td><td>20, 2</td><td>Input</td><td>When CS1 is high and $\overline{CS0}$ is low, the RTC's chip-select function is valid and read and write are enabled.
When the RTC is connected to a multiplexed-bus type of CPU, $\overline{CS0}$ requires the operation of the ALE (see the description of the ALE).
Use CS1 connected to a power voltage detection circuit. When CS1 is high, the RTC is enabled; when it is low, the RTC is on standby.
When CS1 goes low, the HOLD and RESET bits in the RTC registers are cleared to 0.</td></tr>
<tr><td>STD.P
(STanDard Pulse)</td><td>1</td><td>1</td><td>Output</td><td>This is an N-channel open drain output pin.
Depending on the setting of the C_E register, a fixed-period interrupt signal and a pulse signal are output.
The output from this pin cannot be inhibited by the CS1 and $\overline{CS0}$ signals.
Use a load voltage that is less than or equal to V_{DD}. If not using this pin, keep it open-circuit.
An example of STD.P connection is shown below.
 

If the STD.P output is not to be used during standby operation, connecting the pull-up resistor to +5 V provides a reduction in current consumption. If the STD.P output is to be used even during standby, connect the pull-up resistor to the RTC's V_{DD}. In this case, the current consumption will be increased by the amount of current flowing through the pull-up resistor.</td></tr>
<tr><td>V_{DD}</td><td>18</td><td>24</td><td></td><td>Connect this pin to the power source. Supply 5 V ±10 % to this pin during normal operation; at least 2 V during battery back-up operation.</td></tr>
<tr><td>GND</td><td>9</td><td>12</td><td></td><td>Connect this pin to ground.</td></tr>
<tr><td>(V_{DD})</td><td>16, 17</td><td>22, 23</td><td></td><td>These pins are connected internally to V_{DD}. Leave them open circuit.</td></tr>
<tr><td>N.C.</td><td>-</td><td>3, 6, 8, 17, 18, 21</td><td></td><td>These pins are not connected internally. Ground them.</td></tr>
</table>

■ Characteristics

1. Absolute maximum ratings

Item	Symbol	Condition	Specifications	Unit
Supply voltage	V_{DD}	Ta=+25 °C	-0.3 to 7.0	V
Input voltage	V_I	Ta=+25 °C	GND-0.3 to V_{DD}+0.3	
Output voltage	V_O	Ta=+25 °C	GND-0.3 to V_{DD}+0.3	
Storage temperature	T_{STG}	RTC-62421	-55 to +85	°C
		RTC-62423	-55 to +125	

2. Operating conditions

Item	Symbol	Condition	Specifications	Unit
Supply voltage	V_{DD}		4.5 to 5.5	V
Operating temperature	T_{OPR}	No condensation	-40 to +85	°C
Data hold voltage	V_{DH}		2.0 to 5.5	V
CS1 data hold time	T_{CDR}	See the section on data hold timing (page 17)	2.0 Min.	µs
Operation recovery time	tr			

3. Frequency characteristics and current consumption characteristics

Item	Symbol	Condition		Specifications		Unit
Frequency tolerance	Δf/f0	Ta=+25 °C V_{DD}=5.0 V	RTC-62421A	± 10		x 10^{-6}
			RTC-62421B	± 50		
			RTC-62423A	± 20		
			RTC-62423	± 50		
Frequency temperature characteristics		-10 °C to +70 °C (reference 25°C)		+10 / –120		
		-40 °C to +85 °C (reference 25°C)		+10 / –220		
Frequency voltage characteristics		Ta=+25 °C V_{DD}=4.5 V to 5.5 V		± 5 Max.		x 10^{-6} / V
Aging	fa	V_{DD}=5.0 V, Ta=+25 °C		± 5 Max.		x 10^{-6} / year
Shock resistance	S.R.	Drop test of 3 times on a hard board from 750 mm height, or 29400 m/s^2 x 0.3 ms x 1/2sine wave x 3 directions		± 10 Max.		x10^{-6}
Current consumption	I_{DD}1	Ta=+25 °C,CS1=0 V I/O currents excluded	V_{DD}=5.0 V	15 Typ.	30 Max.	µA
	I_{DD}2		V_{DD}=2.0 V	1 Typ.	1.8 Max.	

4. Electrical characteristics (DC characteristics)

Item	Signal	Condition	Applicable pins	Min.	Typ.	Max.	Unit
High input voltage 1	V_{IH}1		All input pins except for CS1	2.2			V
Low input voltage 1	V_{IL}1					0.8	
Input leakage current 1	I_{LK}1	V_I=V_{DD} /0 V	Input pins except for D0 to D3			1 /-1	µA
Input leakage current 2	I_{LK}2		D0 to D3			10 /-10	
Low output voltage 1	V_{OL}1	I_{OL}=2.5 mA				0.4	V
High output voltage	V_{OH}	I_{OH}=-400 µA		2.4			
Low output current 1	I_{OL}1	V_{OL}1=0.4 V		2.5			mA
High output current	I_{OH}	V_{OH}=2.4 V		-400			µA
Low output voltage 2	V_{OL}2	I_{OL}=2.5 mA	STD.P			0.4	V
Low output current 2	I_{OL}2	V_{OL}2=0.4 V		2.5			mA
Off-state leakage current	I_{OFFLK}	V_I=V_{DD} /0 V				10 /-10	µA
Input capacitance	C_I	Input frequency 1 MHz	Input pins		5		pF
High input voltage 2	V_{IH}2	V_{DD}=2.0 V to 5.5 V	CS1	4/5V_{DD}			V
Low input voltage 2	V_{IL}2					1/5V_{DD}	
Oscillation start time	tOSC	See note 1				1	s

Note 1: When Ta = +25 °C, measured from the time at which V_{DD} goes to 4.5 V; the STD.P pin output is 64 Hz.

■ Switching characteristics (AC characteristics)

1. When ALE is used

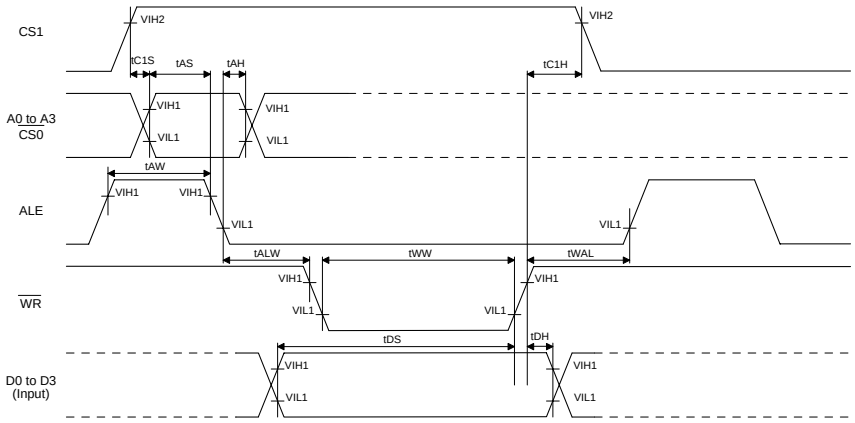
Write mode (V_{DD}=5 V±0.5 V, Ta=–40 °C to +85 °C)

Item	Symbol	Condition	Min.	Max.	Unit
CS1 set-up time	t_{C1S}		1000		ns
Address set-up time before ALE	t_{AS}		25		
Address hold time after ALE	t_{AH}		25		
ALE pulse width	t_{AW}		40		
ALE set-up time before write	t_{ALW}		10		
Write pulse width	t_{WW}		120		
ALE set-up time after write	t_{WAL}		20		
Data input set-up time before write	t_{DS}		100		
Data input hold time after write	t_{DH}		10		
CS1 hold time	t_{C1H}		1000		
Write recovery time	t_{RCV}		60		

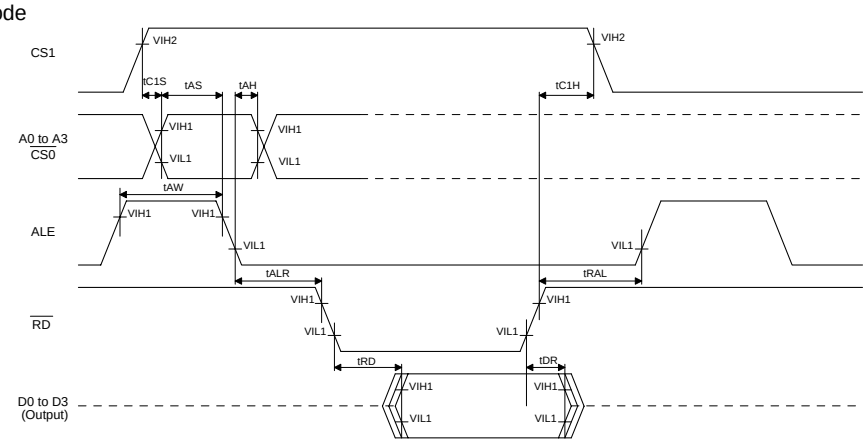
Read mode (V_{DD}=5 V±0.5 V, Ta=–40 °C to +85 °C)

Item	Symbol	Condition	Min.	Max.	Unit
CS1 set-up time	t_{C1S}		1000		ns
Address set-up time before ALE	t_{AS}		25		
Address hold time after ALE	t_{AH}		25		
ALE pulse width	t_{AW}		40		
ALE set-up time before read	t_{ALR}		10		
ALE set-up time after read	t_{RAL}		10		
Data output transfer time after read	t_{RD}	C_L=150 pF		120	
Data output floating transfer time after read	t_{DR}		0		
CS1 hold time	t_{C1H}		1000		
Read recovery time	t_{RCV}		60		

(1)Write mode



(2) Read mode



2. When ALE is fixed at V_{DD}

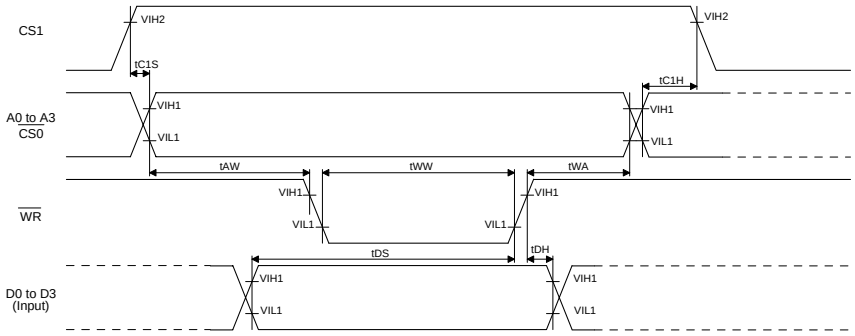
Write mode (V_{DD}=5 V±0.5 V, Ta=–40 °C to +85 °C)

Item	Symbol	Condition	Min.	Max.	Unit
CS1 set-up time	t_{C1S}		1000		ns
CS1 hold time	t_{C1H}		1000		
Address set-up time before write	t_{AW}		20		
Address hold time after write	t_{WA}		10		
Write pulse width	t_{WW}		120		
Data input set-up time before write	t_{DS}		100		
Data hold time after write	t_{DH}		10		
Write recovery time	t_{RCV}		60		

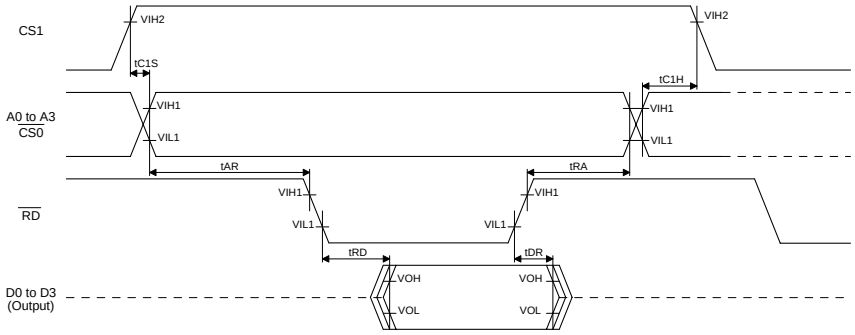
Read mode (V_{DD}=5 V±0.5 V, Ta=–40 °C to +85 °C)

Item	Symbol	Condition	Min.	Max.	Unit
CS1 set-up time	t_{C1S}		1000		ns
CS1 hold time	t_{C1H}		1000		
Address set-up time before read	t_{AR}		20		
Address hold time after read	t_{RA}		0		
Data output transfer time after read	t_{RD}	C_L=150 pF		120	
Data output floating transfer time after read	t_{DR}		0		
Read recovery time	t_{RCV}		60		

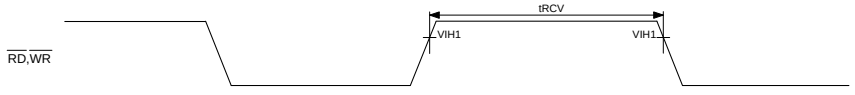
(1) Write mode



(2) Read mode



(3) Read/write recovery time



■ Registers

1. Register table

Address (Hex)	A3	A2	A1	A0	Register name	Data				Count (BCD)	Remarks
						D3	D2	D1	D0		
0	0	0	0	0	S1	s8	s4	s2	s1	0 to 9	1-second digit register
1	0	0	0	1	S10	*	s40	s20	s10	0 to 5	10-seconds digit register
2	0	0	1	0	MI1	mi8	mi4	mi2	mi1	0 to 9	1-minute digit register
3	0	0	1	1	MI10	*	mi40	mi20	mi10	0 to 5	10-minutes digit register
4	0	1	0	0	H1	h8	h4	h2	h1	0 to 9	1-hour digit register
5	0	1	0	1	H10	*	PM /AM	h20	h10	0 to 1 or 2	10-hours digit register
6	0	1	1	0	D1	d8	d4	d2	d1	0 to 9	1-day digit register
7	0	1	1	1	D10	*	*	d20	d10	0 to 3	10-days digit register
8	1	0	0	0	MO1	mo8	mo4	mo2	mo1	0 to 9	1-month digit register
9	1	0	0	1	MO10	*	*	*	mo10	0 to 1	10-months digit register
A	1	0	1	0	Y1	y8	y4	y2	y1	0 to 9	1-year digit register
B	1	0	1	1	Y10	y80	y40	y20	y10	0 to 9	10-years digit register
C	1	1	0	0	W	*	w4	w2	w1	0 to 6	Day-of-the-week register
D	1	1	0	1	CD	30-s ADJ	IRQ FLAG	BUSY	HOLD		Control register D
E	1	1	1	0	CE	t1	t0	ITRPT /STND	MASK		Control register E
F	1	1	1	1	CF	TEST	24 /12	STOP	RESET		Control register F

2. Notes

(1) The counts at addresses 0 to C are all positive logic. Therefore, a register bit that is 1 appears as a high-level signal on the data bus. Data representation is BCD.

(2) Do not set an impossible date or time in the RTC. If such a value is set, the effect is unpredictable.

(3) When the power is turned on (before the RTC is initialized), the state of all bits is undefined. Therefore, write to all registers after power-on, to set initial values. For details of the initialization procedure, see "Using the RTC-62421 /RTC-62423" on page 14.

(4) The TEST bit of control register F is used by EPSON for testing. Operation cannot be guaranteed if 1 is written to this bit, so make sure that it is set to 0 during power-on initialization.

3. Functions of register bits (overview)

Bit name	Function
* mark	Not used. Writing to this bit has no effect; reading it always returns 0.
Seconds-to-year digits	All written in BCD code.
Day-of-the-week digit	This is a septal (base 7) counter that increments each time the day digits are incremented. It counts from 0 to 6. Since the value in the counter bears no relationship to the day of the week, the user can choose the coding that relates the counter value to the day of the week. The following is just one example of this relationship: Count 0 1 2 3 4 5 6 Day Sunday Monday Tuesday Wednesday Thursday Friday Saturday
PM /AM	The PM/AM bit is 1 for p.m. times; 0 for a.m. times. This bit is valid only for 12-hour-clock mode (when the 24/12 bit is 0); in 24-hour-clock mode (when the 24 /12 bit is 1), this bit is always 0.
30-seconds ADJ	Writing 1 to this bit executes a 30-seconds correction.
IRQ FLAG	The IRQ FLAG bit is set to 1 when an interrupt request is generated in interrupt mode. Writing 0 to this bit clears it. Note that it is possible to write 1 to this bit, but this will have no effect. In fixed-period pulse output mode, this bit is at 1 while the pulse output is active (while the STD.P pin output is low), and is automatically cleared when pulse output ends. Writing 0 to this bit while pulse output is active forcibly cancels the pulse output.
BUSY	Use the BUSY bit when accessing data in the S1 to W registers. This bit is set to 1 during the incrementation cycle of the S1 to W registers, and is set to 0 otherwise. When the BUSY bit is 1, access to the S1 to W registers is inhibited. Note that the HOLD bit must also be used when accessing the S1 to W registers. The BUSY bit is always 1 when the HOLD bit is 0. There is no need to check the BUSY bit when accessing the control registers (C_D, C_E, and C_F).
HOLD	When 1 has been written to the HOLD bit, the status of the BUSY bit can be checked. While the HOLD bit is 1, any incrementation of the digits is held just once. (The incrementation is held only once, even if the HOLD bit remains at 1 for two or more seconds.) Clear the HOLD bit to 0 by forcing the CS1 pin low.
t1, t0	These bits set the timing for fixed-period pulse output and interrupts (1/64 seconds, 1 second, 1 minute, or 1 hour).
ITRPT /STND	The ITRPT /STND bit sets fixed-period pulse output mode and interrupt mode. Write 1 to this bit to set interrupt (ITRPT) mode; when write 0 to it to set pulse output (STND) mode.
MASK	The MASK bit disables fixed-period pulse output and interrupts. Write 1 to this bit to mask and inhibit these modes; write 0 to it to enable these modes.
TEST	The TEST bit is used by EPSON for test purposes. Operation cannot be guaranteed if 1 is written to this bit, so make sure that it is set to 0 during power-on initialization.
24 /12	The 24 /12 bit switches between 24-hour clock and 12-hour clock. Write 1 to this bit to set 24-hour mode; write 0 to it to set 12-hour mode. When the 24/12 bit is set, both the timer registers and the timer mode must be reset to match. Note that the h20 bit of the H10 register is never set to 1 by the timer but it can be written to. To avoid timer errors, always keep the h20 bit at 0 in 12-hour clock mode. In the setting of the timer mode, it is necessary to set the RESET bit to 1 then 0 after the 24/12 bit is set.
STOP	The STOP bit sets an inhibition on clock operation in 8192-Hz steps which are divider of the 1-second signal from the RTC's internal 32,768-Hz oscillation source. The clock is inhibited when the STOP bit is 1, and released again when it becomes 0. The internal oscillation circuit continues to operate even when the STOP bit is 1.
RESET	The RESET bit resets the part of the counter that is below a seconds. Write 1 to this bit to reset; 0 to release the reset. If the clock mode has been affected by the setting of the 24/12 bit, it is necessary to set the RESET bit to 1 then 0. RESET bit is cleared to 0, by a CS1 falling to low level.

4. Setting the fixed-period pulse output mode and interrupt mode

Mode	MASK	ITRPT/STND	ITRPT/STND	STD.P pin
Fixed-period pulse output mode	0	0	Set to 1 when active	Set low when active
Interrupt mode	0	1		
Fixed-period pulse output inhibited	1	0 or 1	"0"	Open-circuit

Setting of fixed-period output timing				
t1 bit	0	0	1	1
t0 bit	0	1	0	1
Output period	1/64 s	1 s	1 min	1 hour

5. Resetting the fixed-period pulse output mode and interrupt mode

Mode	IRQ FLAG	IRQ FLAG	STD.P pin
Fixed-period pulse output mode MASK=0 ITRPT /STND=0	Write 0	Reset immediately after the write (1"→"0")	Reset immediately after the write (low → open-circuit)
	No write	Automatically returned by the set period ("1"→"0")	Automatically returned by the set period (low → open-circuit)
Interrupt mode MASK=0 ITRPT /STND=1	Write 0	Reset immediately after the write ("1"→"0")	Reset immediately after the write (low → open-circuit)
	No write	The interrupt request continues, with no reset. The next interrupt is ignored.	

■ Register description

1. Timing registers

(1) S1 to Y10 registers

These registers are 4-bit, positive logic registers in which the digits of the year, month, day, hour, minute, and second are continuously written in BCD code.

For example, when (1, 0, 0, 1) has been written to the bits of the S1 register, the current value in the S1 register is 9. As described previously, data is handled by 4-bit BCD codes. Therefore, the S1 to Y10 registers consist of units registers and tens registers. When seconds are read, for example, the values in the S1 and S10 registers are both read out to give the total number of seconds.

(2) W register

The W register is a counter that increments each time the day digits are incremented. It counts from 0 to 6. Since the value in the counter bears no relationship to the day of the week, the user can choose the coding that relates the counter value to the day of the week. The following is just one example of this relationship:

Count	0	1	2	3	4	5	6
Day	Sunday	Monday	Tuesday	Wednesday	Thursday	Friday	Saturday

(3) H10 register (PM/AM, h20, h10)

The H10 register contains a combination of the 10-hours digit bits and the PM /AM bit. Therefore, the contents of this register will depend on whether the 12-hour clock or 24-hour clock is selected. If the 12-hour clock is selected, the user must bear in mind that this register will contain two types of data: 10-hour data in the h10 bit and a.m./p.m. data in the PM/AM bit. The PM/AM bit is 0 for a.m. and 1 for p.m.

For example, if a value of 48 is obtained from the H10 and H1 registers when the H10, H1, M10, and M1 registers are read, remember that the inclusion of a set PM /AM bit (PM/ AM = 1) will make the tens digit appear to be 4. Since this bit is 1, the time is p.m. If the value read from the M10 and M1 registers is 00, the actual time should be read as 8:00 p.m.

Similarly, if the value read from the H10 and H1 registers is 11, the PM /AM bit is 0, and so this time is therefore a.m. If the value read from the M10 and M1 registers is 30, this time should be read as 11:30 a.m.

When the 12-hour clock is used, the h20 bit should never be 1, but it is nonetheless physically possible to write a 1 in this bit. The user should be careful to write a 0, to avoid unpredictable consequences. Note that, if a mistake in the PM/AM value is made while in 12-hour-clock mode, the date digits will be half a day out. Correct setting is needed.

If the 24-hour clock is selected, the PM/AM bit will always be 0.

For details of how to set 12-hour or 24-hour clock, see the sections on the 24/12 bit on pages 13 and 17.

Setting	Possible times
12-hour clock	12:00 to 11:59, a.m. and p.m.
24-hour clock	00:00 to 23:59

(4) Y1 and Y10 registers

The Y1 and Y10 registers can handle the last two digits of the year in the Gregorian calendar. Leap years are automatically identified, and this affects the handling of the month and day digits for February 29.

[Leap years]

In general, a year contains 365 days. However, the Earth takes slightly longer than exactly 365 days to rotate around the sun, so we need to set leap years in compensation. A leap year occurs once every four years, in years in the Gregorian calendar that are divisible by four. However, a further small correction is necessary in that years that are divisible by 100 are ordinary years, but years that are further divisible by 400 are leap years.

The main leap and ordinary years since 1900 and into the future are listed on the right.

[Leap years in the RTC-62421 /RTC-62423]

To identify leap years, the RTC-62421 /RTC-62423 checks whether or not the year digits are divisible by four. As implied above, 2000 will be a leap year, and so no further correction will be necessary in that case.

This process identifies the following years as leap years:

(19)96, (20)00, (20)04, (20)08, (20)12,...

The turn-of-the-century years for which the RTC-62421 /RTC-62423 will require a correction are shown shaded in the table on the right.

If Japanese-era years are set, accurate leap-year identification will only be possible if the era years that are divisible by four are actually leap years. As it happens, years in the current era, Heisei, that are divisible by four are leap years, which means that Heisei years can be set in these registers.

Actual leap years and ordinary years

Year	Leap year	Ordinary year
1900		○
:		
1993		○
1994		○
1995		○
1996	○	
1997		○
1998		○
1999		○
2000	○	
2001		○
2002		○
2003		○
2004	○	
2005		○
:		
2100		○
2200		○
2300		○
2400	○	
:		

(5) Out-of-range data

If an impossible date or time is set, this may cause errors. If such a date is set, the behavior of the device is in general unpredictable, so make sure that impossible data is not set.

2. CD register (control register D)

(1) HOLD bit (D0)

Use the HOLD bit when accessing the S1 and W registers. For details, see "Read/write of S1 to W registers" on page 15.

HOLD bit	Function of HOLD bit
0	The BUSY bit is always 1 (the BUSY status cannot be checked).
1	The BUSY status can be checked. When the HOLD bit is 1 and the BUSY bit is 0, read and write are enabled.

When the HOLD bit is 1, any incrementation in the count is held within the RTC. The held incrementation is automatically compensated for when the HOLD bit becomes 0. (Second and subsequent incrementations are ignored.) Therefore, if the HOLD bit is at 1 for two or more seconds in succession, the time will be slightly slow (delay). Make sure that any access to the S1 to W registers is completed within one second, then clear the HOLD bit to 0.

The status of the BUSY bit remains as set while the HOLD bit is at 1. If the HOLD bit is not cleared temporarily to 0, the BUSY bit will not indicate any change within the RTC of the BUSY status. Therefore, when checking the status of the BUSY bit, write 0 to the HOLD bit each time the BUSY bit is read, to update the status of the BUSY bit.

If the CS1 pin goes low while the HOLD bit is 1, the HOLD bit is automatically cleared to 0.

There is no need to use the HOLD bit when accessing the control registers (CD, CE, and CF).

(2) BUSY bit (D1)

The BUSY bit indicates whether or not the digits from the seconds digit onward are being incremented, and is used when accessing the S1 to W registers. For details, see "Read/write of S1 to W registers" on page 15.

There is no need to check the BUSY bit when accessing the control registers (CD, CE, and CF).

BUSY bit	Significance of the BUSY bit	Condition	Remarks
0	Access enabled	HOLD=1	The RTC is not counting
1	Access disabled		The count has been incremented in the RTC (190 μs, Max.)
1	BUSY is always 1	HOLD=0	The count cannot be checked

The status of the BUSY bit remains as set while the HOLD bit is at 1. If the HOLD bit is not cleared temporarily to 0, the BUSY bit will not indicate any change within the RTC of the BUSY status. Therefore, when checking the status of the BUSY bit, write 0 to the HOLD bit each time the BUSY bit is read, to update the status of the BUSY bit.

The BUSY bit is a read-only bit, so any attempt to write 1 or 0 to it is ignored.

(3) IRQ FLAG bit (D2)

The IRQ FLAG bit is an internal status bit that corresponds to the status of the STD.P pin output, to indicate whether or not an interrupt request has been issued to the CPU. When the STD.P pin output is low, the IRQ FLAG bit is 1; when the STD.P pin output is open-circuit, the IRQ FLAG bit is 0.

When writing data to the CD register, keep the IRQ FLAG bit at 1, except when deliberately writing 0 to it. Writing 0 to the IRQ FLAG bit cancels its status if it had become 1 at that instant or just before.

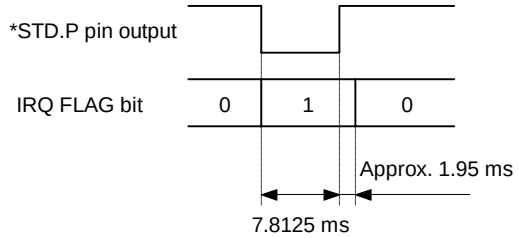
i. Interrupt processing (interrupt status monitor function)

Since the IRQ FLAG bit indicates that an interrupt request has been generated to the CPU, it is in synchronizations with the status of the STD.P pin output. In other words, the status of the STD.P pin output can be monitored by monitoring the IRQ FLAG bit.

In fixed-period pulse output mode, the relationship between the IRQ FLAG bit and the STD.P pin output is as follows:

STD.P pin output	IRQ FLAG bit
Low	1
Open (for open-drain output)	0

The timing of the IRQ FLAG bit and the STD.P pin output in fixed-period pulse output mode is as follows:

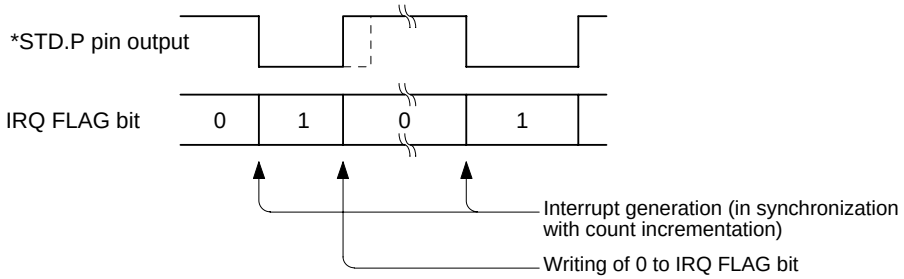


The output levels of the STD.P pin are low (down) and open circuit (up).

ii. STD.P pin output reset function

The STD.P pin output can be reset after an interrupt is generated by writing 0 to the IRQ FLAG bit. The relationships of this operation are shown below. Note that writing 1 to this bit is possible, but it has no effect.

IRQ FLAG bit	STD.P pin output
1	Low
0	Open (for open-drain output)



The output levels of the STD.P pin are low (down) and open circuit (up).

Note: If the STD.P pin output remains low as set, subsequently generated interrupts are ignored. In order to prevent interrupts from being overlooked, write 0 to the IRQ FLAG bit before the next interrupt is generated, to return the STD.P pin to high.

iii. Initial setting of IRQ FLAG bit

If the interrupt mode is not used, set the IRQ FLAG bit to 1. If the interrupt mode is used, set the IRQ FLAG bit to 0.

(4) 30-second ADJ bit (D3)

The 30-seconds ADJ bit provides a 30-seconds correction (by which term is meant a rounding to the nearest whole minute) when 1 is written to it. The 30-seconds correction takes a maximum of 125 μs to perform, and after the correction the 30-seconds ADJ bit is automatically returned to 0. This operation also clears the sub-second bits of the internal counter down to the 1/8192-seconds counter. During the 30-seconds correction, access to the counter registers at addresses 0 to C is inhibited, so monitor the 30-seconds ADJ bit to check that this bit has returned to 0, before starting subsequent processing. If no access is made to the RTC for 125 μs or more after 1 is written to the 30-seconds ADJ bit, there is no need to check the 30-seconds ADJ bit again.

i. Operation of 30-seconds ADJ bit

Writing 1 to the 30-seconds ADJ bit performs a 30-second correction. This 30-seconds correction changes the seconds and minutes digits as shown below. If the minutes digits have been incremented, an upward carry is propagated.

Status of seconds digits before correction	Status of seconds digits after correction
Up to 29 seconds	00 seconds. No carry to the minutes digits.
30 to 59 seconds	00 seconds. Carry to the minutes digits.

Example: The correction caused by the 30-seconds ADJ bit sets the time within the RTC to 00:00:00 if it was within the range of 00:00:00 to 00:00:29, or to 00:01:00 if it was within the range of 00:00:30 to 00:00:59.

ii. Access inhibited after 30-seconds correction

For 125 μs after 1 is written to the 30-seconds ADJ bit, the RTC is engaged in internal processing, so read to and write from the S1 to W registers is inhibited. The 30-seconds ADJ bit is automatically cleared to 0 at the end of the 125 μs.

3. CE register (control register E)

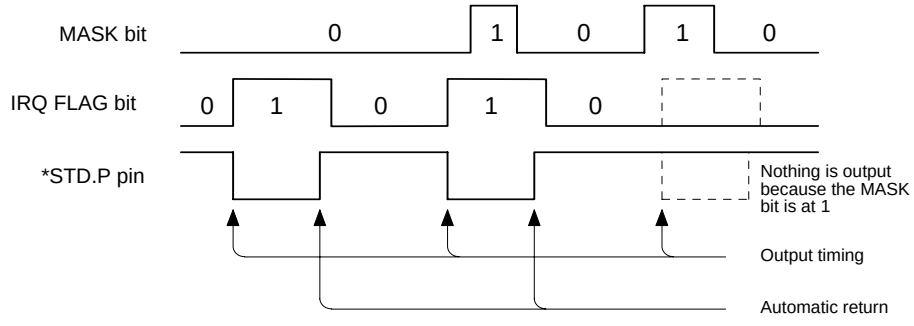
(1) MASK bit (D0)

The MASK bit controls the STD.P pin output. The relationships between the MASK bit, ITRPT/STND bit, and STD.P pin output are as follows:

MASK	ITRPT/STND	Status of STD.P pin output
0	0	Fixed-period pulse output mode
0	1	Interrupt mode
1	0 or 1	Open circuit (while the MASK bit remains at 1)

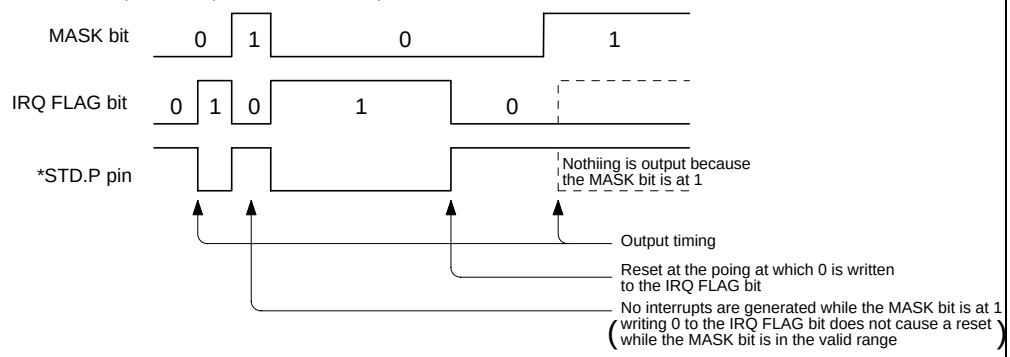
The timings of the MASK bit, ITRPT/STND bit, and STD.P pin output are as follows:

1. Fixed-period pulse output mode (ITRPT/STND = 0)



The output levels of the STD.P pin are low (down) and open circuit (up).

2. Interrupt mode (ITRPT/STND = 1)



The output levels of the STD.P pin are low (down) and open circuit (up).

(2) ITRPT/STND bit (D1)

The ITRPT/STND bit specifies fixed-period pulse output mode or interrupt mode for the fixed-period operating mode. The mode selected by each setting of this bit is as follows:

ITRPT/STND	Operating mode
0	Fixed-period pulse output mode
1	Interrupt mode

For details of the timing of fixed-period operation, see the section on the t0 and t1 bits below.

(3) t0 (D2) and t1 (D3) bits

These bits select the timing of fixed-period operation in fixed-period pulse output mode or interrupt mode. There is no special counter within the RTC for fixed-period operation; the fixed-period operation is performed at the incrementation of the time (period) specified by the t0 and t1 bits.

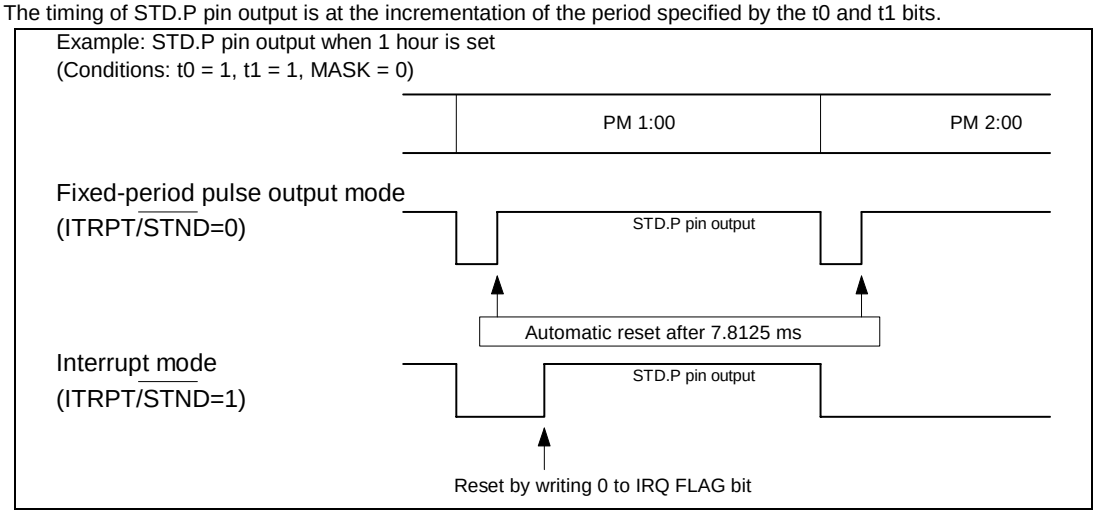
i. Setting t0 and t1

Setting these bits specifies the generation timing for fixed-period pulse output or fixed-period interrupts.

t0	t1	Period (frequency)	Remarks
0	0	1/64 second (64 Hz)	In fixed-period pulse output mode, the STD.P pin output is low for 7.8125 ms (note that half the 1/64-second period is 7.8125 ms)
0	1	1 second (1 Hz)	
1	0	1 minute (1/60 Hz)	
1	1	1 hour (1/3600 Hz)	

ii. STD.P pin output control

The timing of STD.P pin output is at the incrementation of the period specified by the t0 and t1 bits.



iii. Frequency of STD.P pin output in fixed-period pulse output mode

In fixed-period pulse output mode, the timing of output is determined by the frequency of the internal quartz crystal. This means that the output can be used to measure any error in the frequency of the quartz crystal.

Note: The 30-seconds correction could generate a carry. If such a carry occurs when the t0 and t1 bits are set to (0, 1) or (1, 1), the STD.P pin output could end up low. If the ITRPT/STND bit is 0, this low-level STD.P pin output will be held from the time that the part of the counter that is below one second is cleared by the 30-seconds correction until the incrementation of the 1/64-second digit of the internal counter restarts. Note that this may be different from the normal case in which the STD.P pin output is low for 7.8125 ms.

The time of the low-level output of the first STD.P pin output after a RESET or STOP operation, or after 1 has been written to the IRQ FLAG bit, may not be 7.8125 ms.

If any one of the t0, t1, or ITRPT/STND bits is overwritten, the IRQ FLAG bit may become 1. Therefore, after writing to any of these bits, it is necessary to first write 0 to the IRQ FLAG bit then wait until the IRQ FLAG bit changes back to 1.

4. CF register (control register F)

(1) RESET bit (D0)

Writing 1 to the RESET bit clears the sub-second bits of the internal counter down to the 1/8192-seconds counter. The reset continues for as long as the RESET bit is 1. End the reset by writing 0 to the RESET bit. If the level of the CS1 pin goes low, the RESET bit is automatically cleared to 0.

When switching the timer mode from 24-hour clock to 12-hour clock, or vice versa, write 1 to the RESET bit then 0.

Because RESET bit function is invalid on STOP bit in case of "1", please don't use it together with STOP bit.

(2) STOP bit (D1)

Writing 1 to the STOP bit stops the clock of the internal counter from the 1/8192 second bit onward. Writing 0 to the STOP bit restarts the clock.

This function can be used to create a cumulative timer.

(3) 24/12 bit (D2)

Set the 24/12 bit to select either 12-hour clock or 24-hour clock as the timer mode. In 12-hour clock mode, the PM/AM bit is used.

i Switching between 12-hour clock and 24-hour clock

Writing 1 to the 24/12 bit, then setting the RESET bit first to 1 then to 0, selects 24-hour clock mode.

Writing 0 to the 24/12 bit selects 24-hour clock mode. In 24-hour clock mode, the PM/AM bit is inoperative and is always 0.

Writing 0 to the 24/12 bit selects 12-hour clock mode. In 12-hour clock mode, the PM/AM bit becomes valid. It is 0 for a.m. times and 1 for p.m. times.

ii. Overwriting the 24/12 bit

Overwriting the contents of the 24/12 bit could destroy the contents of the registers from the H1 register upward (from the 1-hour digit upward). Therefore, before overwriting the 24/12 bit, it is necessary to save the contents of the hour (H1, H10), day (D1, D10), month (MO1, MO10), year (Y1, Y10), and day-of-the-week (W) registers, then re-write the data back into the registers to suit the new timer mode, after overwriting the 24/12 bit.

iii. Handling of RESET bit

Simply writing to the 24/12 bit does not trigger the switch over between 24-hour and 12-hour clock modes, and it is also necessary to set the RESET bit first to 1 then to 0. Therefore, if the system proceeds to another operation without changing the RESET bit after a write to the 24/12 bit, operation will continue without changing the timer mode. If the RESET bit is changed later for some reason, the timer mode will change at that point. This careless change in status is not advisable from the software point of view, and it may be difficult to determine the cause of such an error if it occurs infrequently, so make sure that the RESET bit is changed immediately after the 24/12 bit is written to. Alternatively, design software in such a manner that it is aware of the 24/12 bit when the RESET bit is written to.

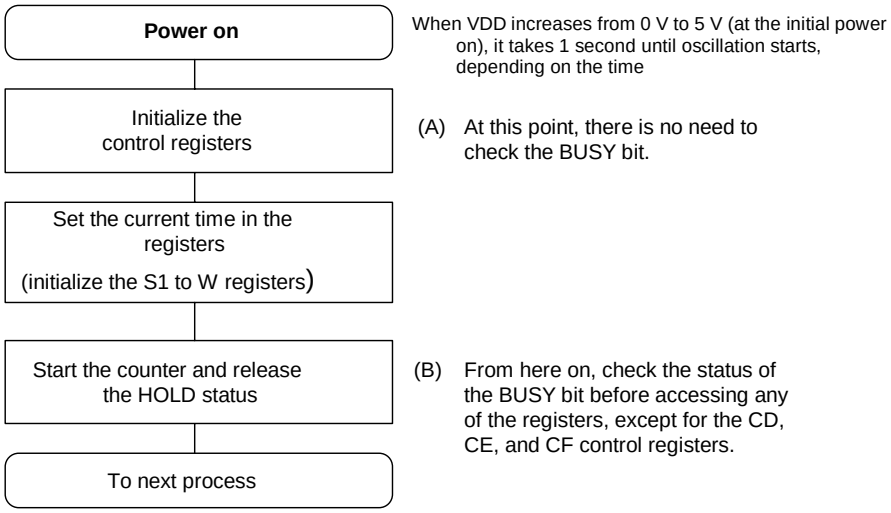
(4) TEST bit (D3)

The TEST bit is used by EPSON for test purposes. Operation cannot be guaranteed if 1 is written to this bit, so make sure that it is set to 0 during power-on initialization.

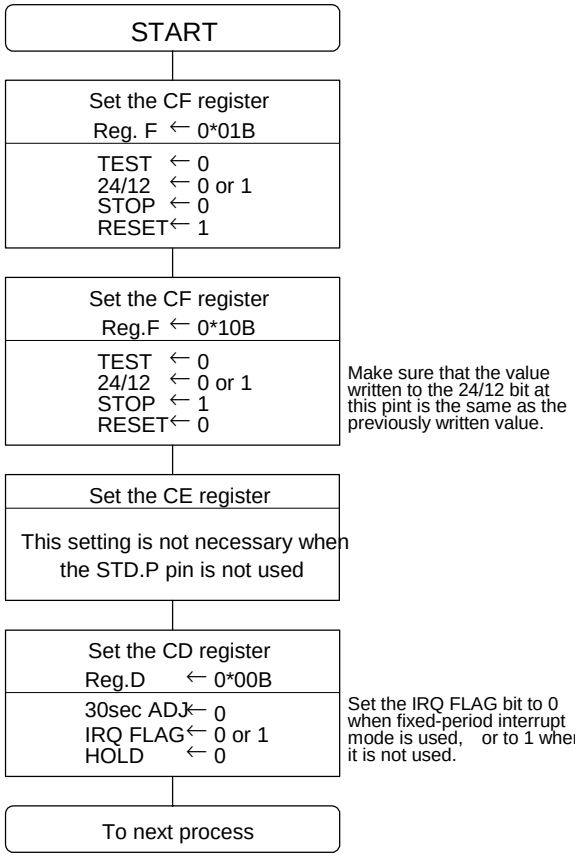
■ Using the RTC-62421 /RTC-62423

1. Power-on procedure (initialization)

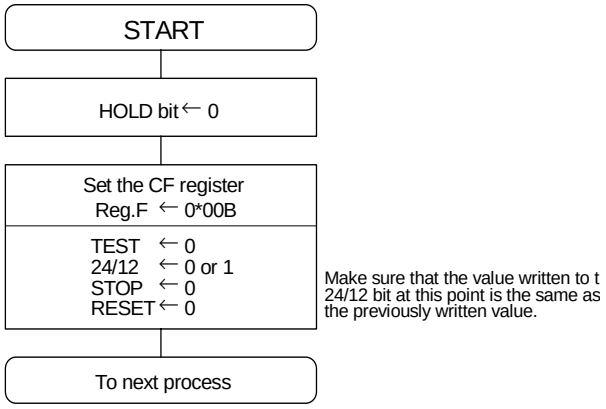
When power is turned on, the contents of all registers and the output from the STD.P pin are undefined. Therefore, all the registers must be initialized after power on. Follow the procedure given below for initialization.



(A) Initializing the control registers



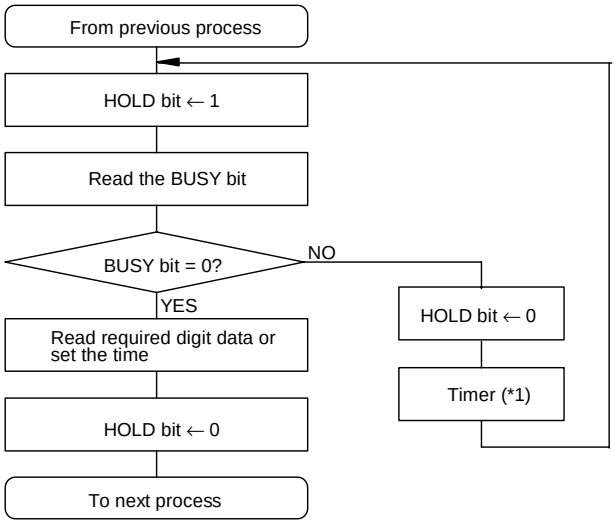
(B) Starting the count and releasing the HOLD status



2. Read /write of S1 to W registers

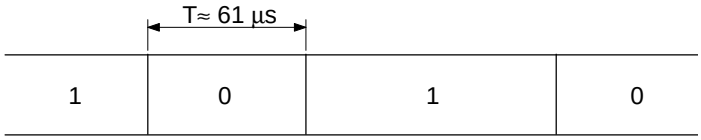
Use one of the procedures shown below to access registers other than the control registers (C_D, C_E, and C_F) while the RTC is operating. Note that the control registers can be accessed regardless of the status of the BUSY bit.

Read or write when the HOLD bit is used

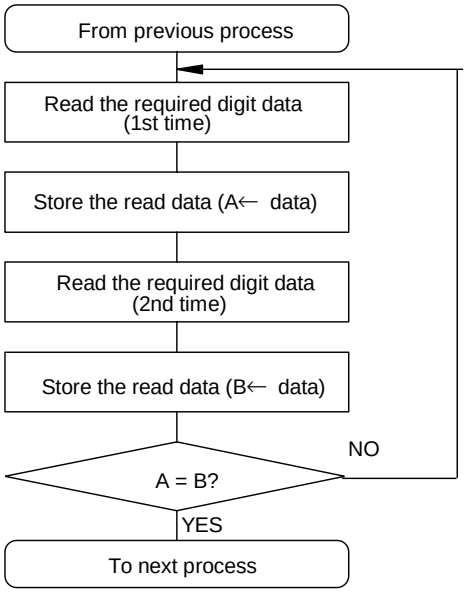


(*1) Within the RTC, the BUSY bit returns to 0 when the HOLD bit becomes 0. However, the status of the HOLD bit is sampled at a frequency of approximately 16 kHz to determine whether the BUSY bit should be cleared, so if the period during which the HOLD bit is 0 is extremely short, the clearing of the BUSY bit could be delayed. To prevent this, make sure that the period during which the HOLD bit is 0 is maintained for about 61 μs, as shown on the right.

Status of HOLD bit

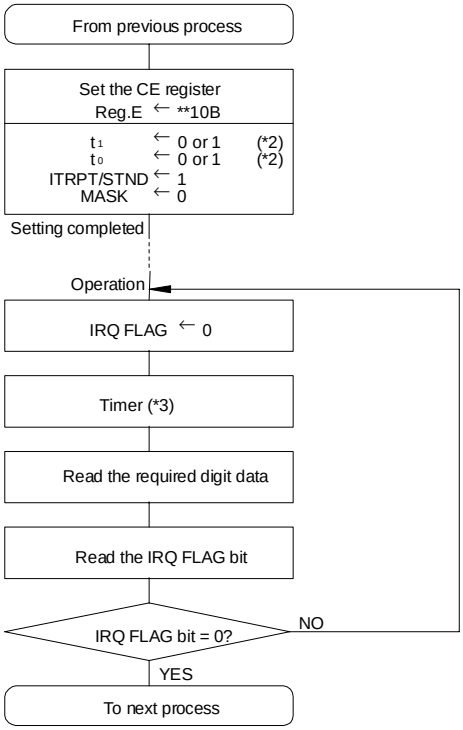


Read when the HOLD bit is not used (1)

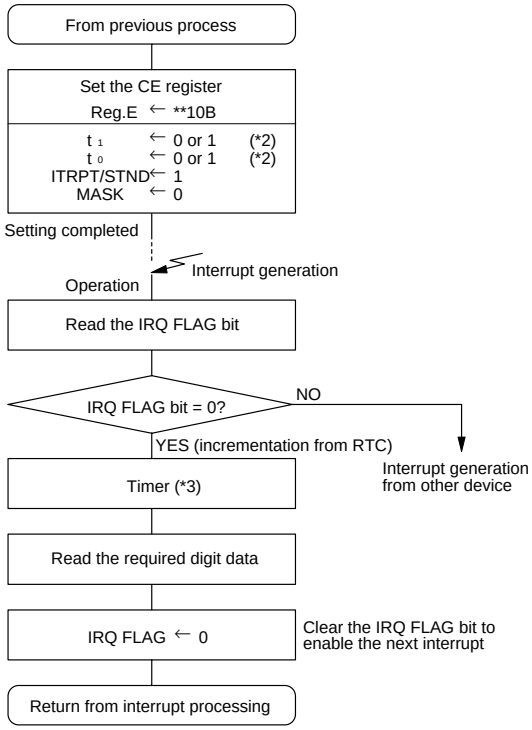


This operation involves reading the same digit twice and comparing the read values. This is to avoid the problem of reading unstable data that would occur if the data was read while the RTC was incrementing the count.

Read when the HOLD bit is not used (2)



Read using an interrupt



(*2) Setting of interrupt generation frequency by the t1 and t0 bits

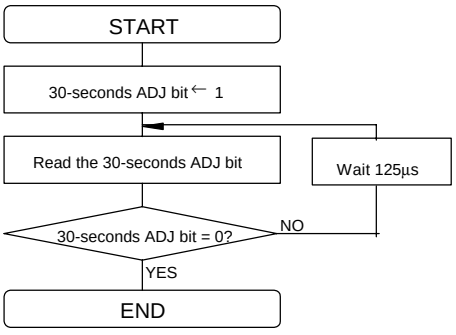
Interrupt frequency	t1 setting	t0 setting
Every second	0	1
Every minute	1	0
Every hour	1	1

(*3) Timer wait times

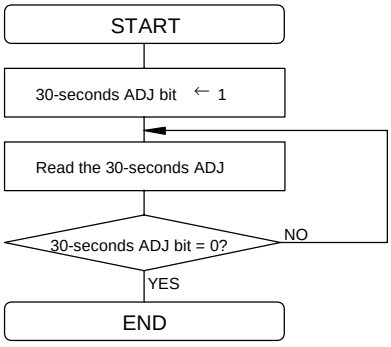
Timer mode	Timer wait time
12-hour clock	35 μs
24-hour clock	3 μs

3. Write to 30-second ADJ bit

The 30-seconds ADJ function is enabled by writing 1 to the 30-seconds ADJ bit. Note that the counter registers (S1 to W) cannot be accessed for 125 μs after this write. Therefore, follow one of the procedures shown below to use this function.



or

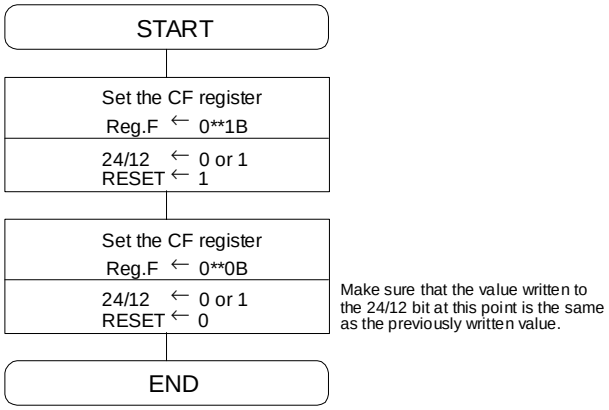


Note

The quartz crystal could be damaged if subjected to excessive shock. If the quartz crystal should stop operating for such a reason, the timer within the RTC will stop. While the quartz crystal is operating, the BUSY bit is automatically reset every 190 μs and the 30-seconds ADJ bit, every 125 μs, but this automatic reset cannot be done if the oscillation stops. Therefore, in such a status, it is no longer possible to escape from the BUSY bit status check loop shown in subsection 2 above or the 30-seconds ADJ bit status check loop shown in subsection 3 above, and you should consider backing up the system. To design a fail-safe system, provide an escape from the loop to a procedure that can process such an error if the loop is repeated for more than 0.5 to 1.0 ms.

4. Switch over between 24- and 12-hour clock modes

Switching between the 24- and 12-hour clock modes is done by writing 1 or 0 to the 24/12 bit and simultaneously performing a RESET within the RTC. Since the 24/12 bit and the RESET bit are in the same control register F, follow the procedure below to set them.



5. Using the CS1 pin

The RTC-62421/RTC-62423 has 2 chip-select signal systems: $\overline{CS0}$ and CS1. Use $\overline{CS0}$ as chip-select for ordinary bus access.

CS1 is not only used for CPU bus control, it also has the main function of switching between standby mode and operating mode.

(1) Functions

Providing the CS1 pin with the rated voltage levels enables CS1 to have the following functions:

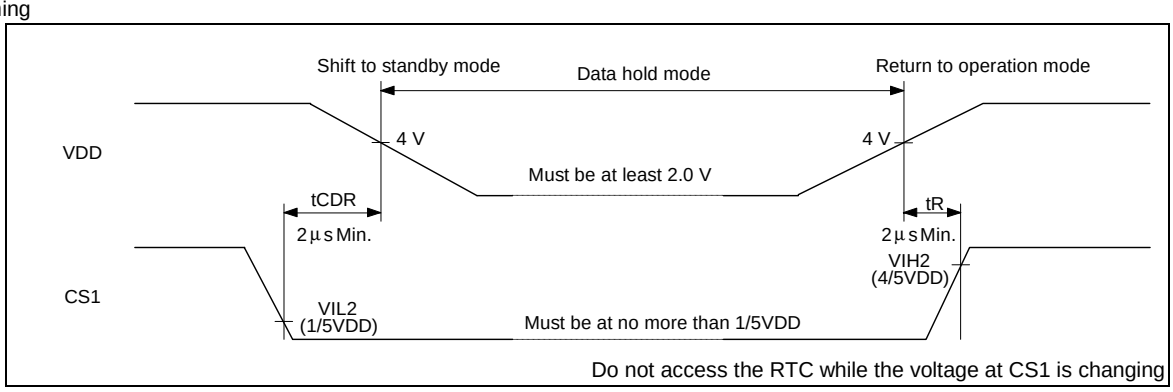
- Enabling interface with microprocessor during operation within the operating voltage range (5.0 V ±0.5 V)
- Reducing current consumption during standby (to prevent through currents caused by unstable inputs, which is inherent to C-MOS devices)
- Protecting internal data during standby

To ensure these functions, make sure that operation of the CS1 pins observes that following conditions:

- Make sure that the voltage input to the CS1 pin during operation is at least 4/5 V_{DD}.
- Make sure that the voltage input to the CS1 pin during standby is as close as possible to 0 V, to prevent through currents.
- Make sure that the operation conforms to the timing chart below during a shift to standby mode or a return to operating mode.

* Standby mode is a state in which a voltage lower than the RTC's rated range of operating supply voltage is applied (4.5 V to 2.0 V). Under this condition, the timer continues to operate under battery back-up power, but the interface between the interior and exterior of the RTC cannot be guaranteed.

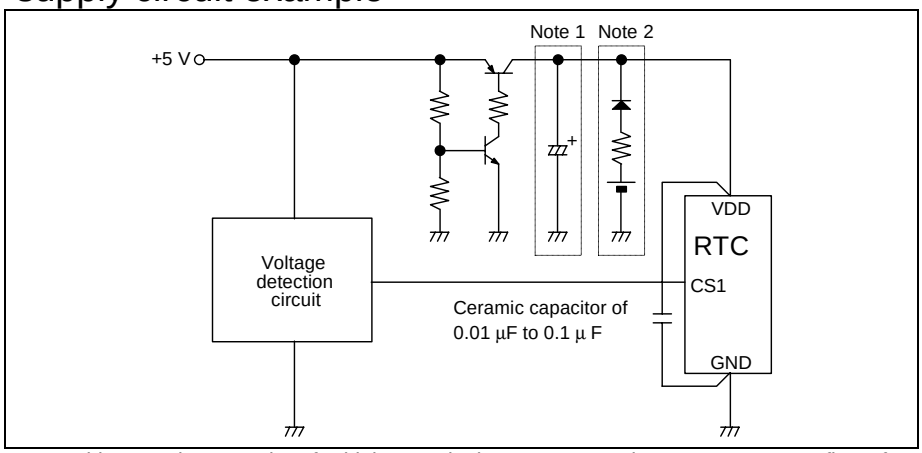
(2) Timing



(3) Note

If the RTC is operated with timing conditions different from those shown above, data within the RTC could be overwritten during a shift to standby mode or a return to operating mode. For example, if a write signal ($\overline{WR}$) is generated during either of the timing conditions (t_{CDR}, t_R) shown in the timing chart above, the data will be input before the RTC has stabilized. To ensure that data is held throughout the entire standby process, make sure that the timing conditions shown in the chart are followed.

■ Power supply circuit example



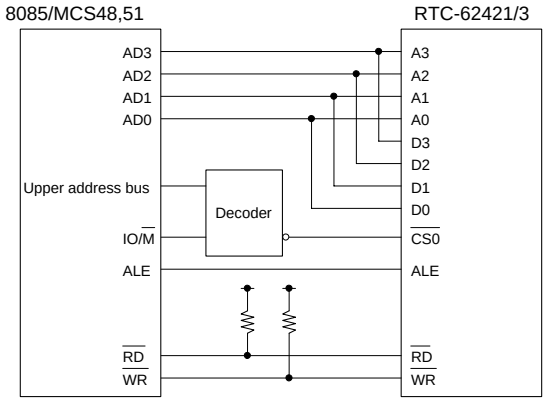
Note 1: This capacitor must be of a high capacity because a transient reverse current flows from the collector to the emitter of the transistor when the power is turned off.

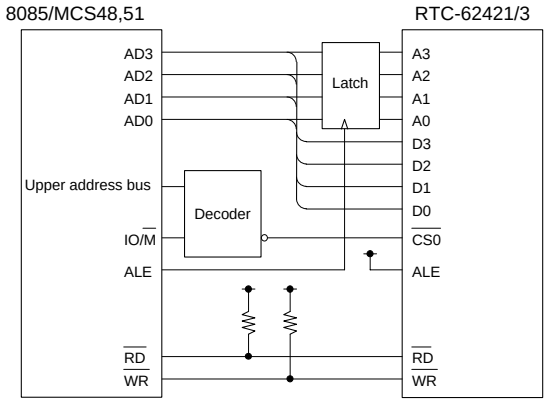
Note 2: Use a chargeable or lithium battery. If a chargeable battery is used, there is no need for the diode. If a lithium battery is used, the diode is necessary. For specific details of the resistance of the resistor, contact the manufacturer of the battery that is used.

■ Examples of connection to general-purpose microprocessor

When connecting the RTC-62421/RTC-62423 to a microprocessor, carefully check the AC timings of both the RTC and the microprocessor.

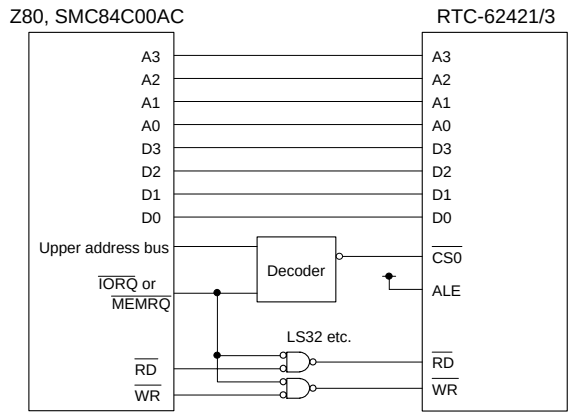
1. Connection to multiplexed bus type





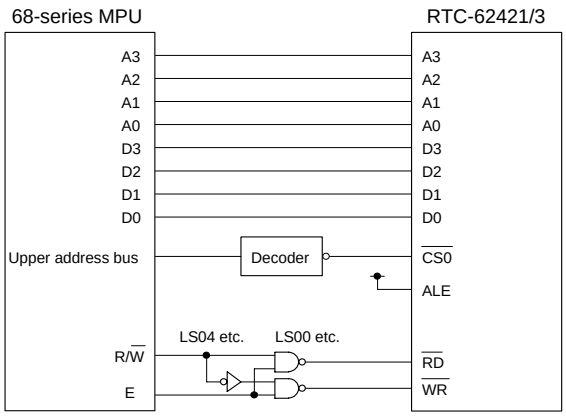
The resistors on the $\overline{RD}$ and $\overline{WR}$ lines are not necessary if the CPU does not have a HALT or HOLD state.

2. Connection to Z80 or compatible CPU



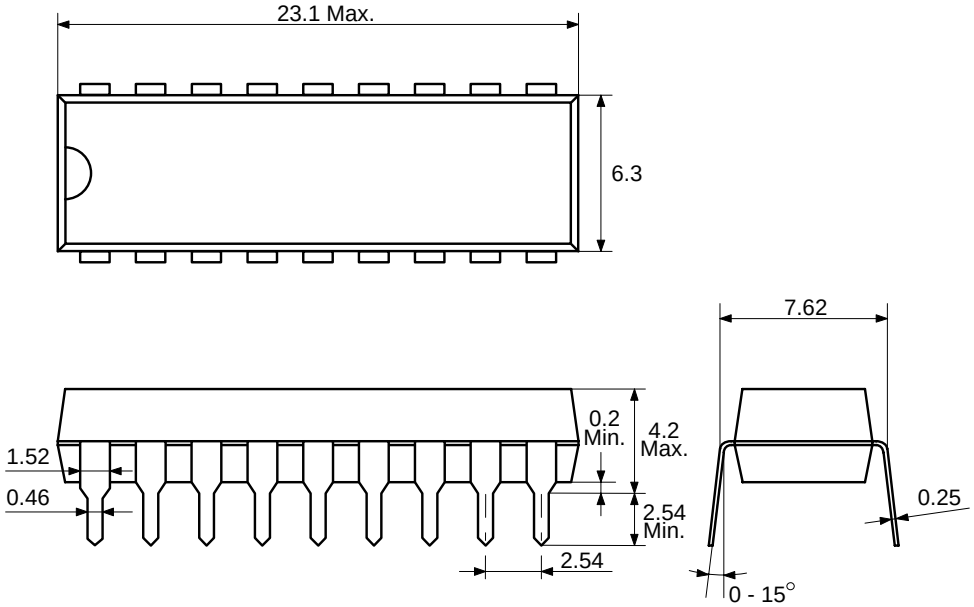
*Select $\overline{IORQ}$ or $\overline{MEMRQ}$ depending on whether the RTC maps I/O or memory of the CPU.

3. Connection to 68-series MPU

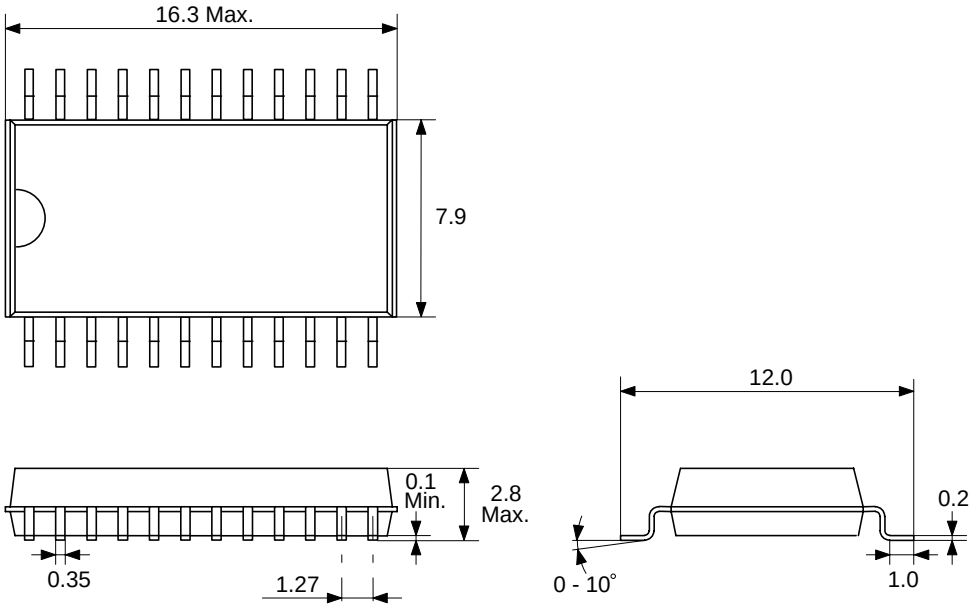


■ External dimensions

1. RTC-62421

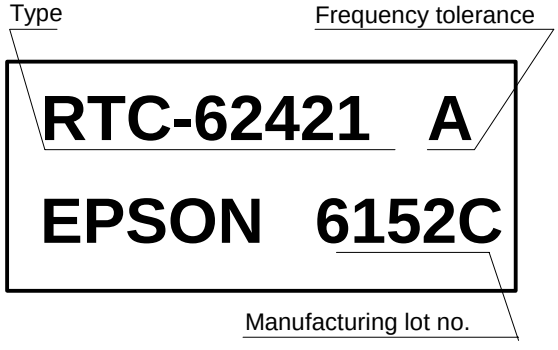


2. RTC-62423



Unless otherwise stated, all units are [mm]

■ Marking layout



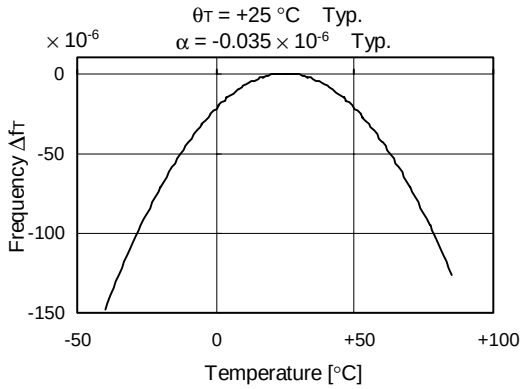
IIndications of frequency tolerance

Type	Symbol	Tolerance
RTC-62421	A	$\pm 10 \times 10^{-6}$
	B	$\pm 50 \times 10^{-6}$
RTC-62423	A	$\pm 20 \times 10^{-6}$
	Blank	$\pm 10 \times 10^{-6}$

Note: The illustration is a general representation of the content and location of information on the label, and is not a detailed specification of the typeface, size, or positioning of printing used on the label.

■ Reference data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$\Delta fT = \alpha (\theta T - \theta X)^2$

ΔfT		: Frequency deviation in any temperature
α	($1 / °C^2$)	: Coefficient of secondary temperature (-0.035 ± 0.005) $\times 10^{-6} / °C^2$
θT	(°C)	: Ultimate temperature (+25±5 °C)
θX	(°C)	: Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$\Delta f/f = \Delta f/fo + \Delta fT + \Delta fV$

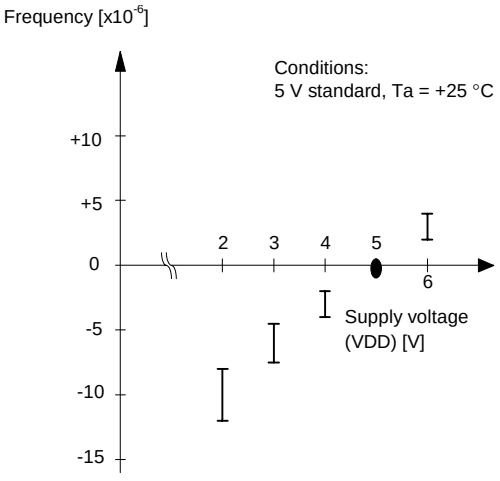
$\Delta f/f$	: Clock accuracy (stable frequency) in any temperature and voltage.
$\Delta f/fo$	: Frequency precision
ΔfT	: Frequency deviation in any temperature.
ΔfV	: Frequency deviation in any voltage.

3. How to find the date difference

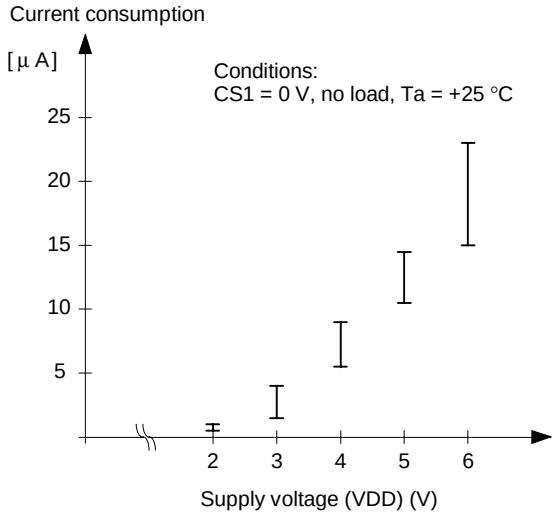
Date Difference = $\Delta f/f \times 86400$(s)

* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second/day.

(2) Frequency voltage characteristics (typical)



(3) Current consumption voltage characteristics (typical)



Note: This data shows average values for a sample lot.
For rated values, see the specifications on page 4.

■ Application notes

1. Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other such devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up." In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater that 0.1 μF as close as possible to the power supply pins (between V_{DD} and GND). Also, avoid placing any device that generates high level of electronic noise near this module.

∗ Do not connect signal lines to the shaded area in the figure shown in Fig.1 and, if possible, embed this area in a GND land.

(3) Voltage levels of input pins

Apply signal levels that are as close as possible to V_{DD} and ground, to all pins except the CS1 pin. Mid-level potentials will cause increased current consumption and a reduced noise margin, and can impair the functioning of the device.

Since it is likely that power consumption will increase excessively and operation cannot be guaranteed, the setting of the voltage range of V_{IH2} and V_{IL2} at the CS1 pin should be such that the system is designed so that it is not affected by ripple or other noise.

Note that the CS1 pin cannot handle a TTL interface.

(4) Handling of unused pins

Since the input impedance of the signal pins is extremely high, operating the device with these pins open circuit can lead to malfunctions due to noise. Pull-up or pull-down resistors should be provided for all unused signal pins. The N.C. pins should be connected to either V_{DD} or GND, to prevent noise. If not using the ALE pin, connect it directly to V_{DD}.

2. Notes on packaging

(1) Soldering temperature conditions

If the temperature within the package exceeds +260 °C, the characteristics of the crystal oscillator will be degraded and it may be damaged. Therefore, always check the mounting temperature before mounting this device. Also, check again if the mounting conditions are later changed.

∗ See Fig.2 for the soldering conditions of SMD products.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the mounting conditions are later changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, state of the inside of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

Leakage between pins may occur if the power is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

Fig. 1 : Example GND Pattern

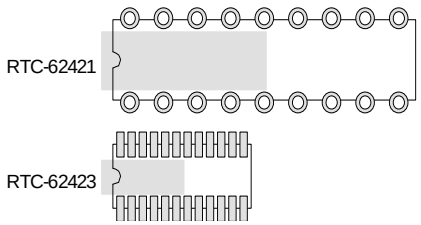
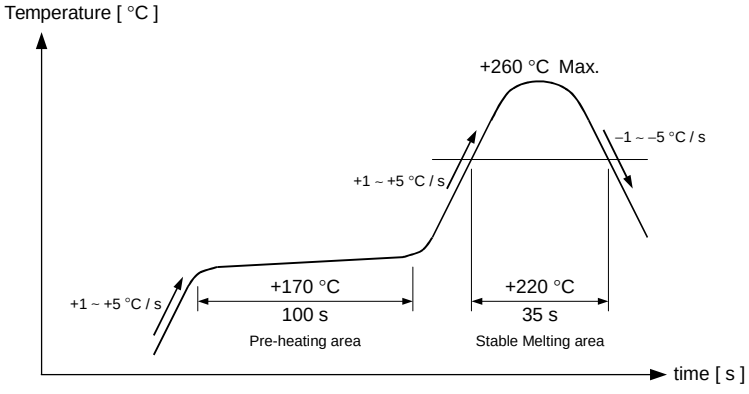


Fig. 2 : Reference profile for our evaluation of Soldering heat resistance.
(SMD Products)



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Application Manual

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