1 `display_surface` - An HDMI Framebuffer Peripheral

1.1 Abstract

`display_surface` is a video display peripheral comprising an HDMI transmitter and a custom AXI master, automatically accessing a framebuffer located in host memory and displaying it over a TMDS channel. This project was developed using the Digilent Zybo, and is capable of rendering a frame or sequence of frames with next to no load on the CPU.

1.2 Architecture

1.2.1 Clocking

The clocks for the AXI master and the TMDS encoder may differ. This clock crossing is resolved by alternating banks of a dual-port block RAM functioning as a FIFO.

The timing of the switch-over of these banks is constrained such that the stream of output pixels to the transmitter never underruns.

1.2.2 The TMDS Encoder

The TMDS encoder (see `tmds_channel.v`) is a 4-stage pipelined module implementing the algorithm outlined in the Digital Video Interface specification.

1.2.3 The AXI Master - Framebuffer DMA

The AXI Master feeds the HDMI transmitter FIFO with data from host memory (DRAM). It issues AXI burst transactions whenever space is available in the FIFO, and when the end of the screen is reached, it either starts on the next framebuffer or loops back to the current framebuffer. It may also send an interrupt to the CPU, if enabled.

1.2.4 The AXI Slave - Configuration Registers

The AXI config registers are the means by which the CPU provides a 4k-aligned address to read the framebuffer(s) from, as well as select double-buffering and enable interrupts.