1 An In-order RISC-V Subset Core

1.1 Abstract

This article documents the architecture and operation of an in-order, 5-stage pipelined CPU core implementing a subset of the 32-bit RISC-V rv32ui instruction set.

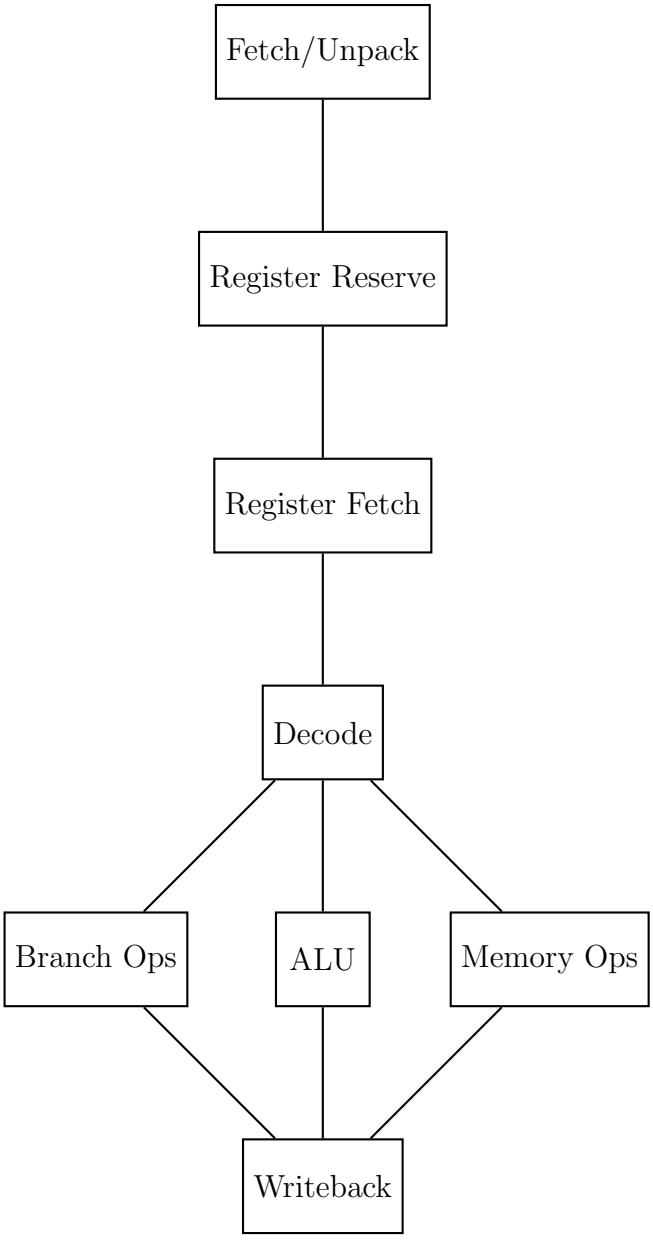

Figure 1.1: Pipeline