Presentation Deck of a Talk given by Dr. Pete Frankwicz

220th Meeting of the Electrochemical Society, Boston MA USA

October 2012.

Reduction of Greenhouse Gas Emissions by Metal Interconnect Etch Process Optimization

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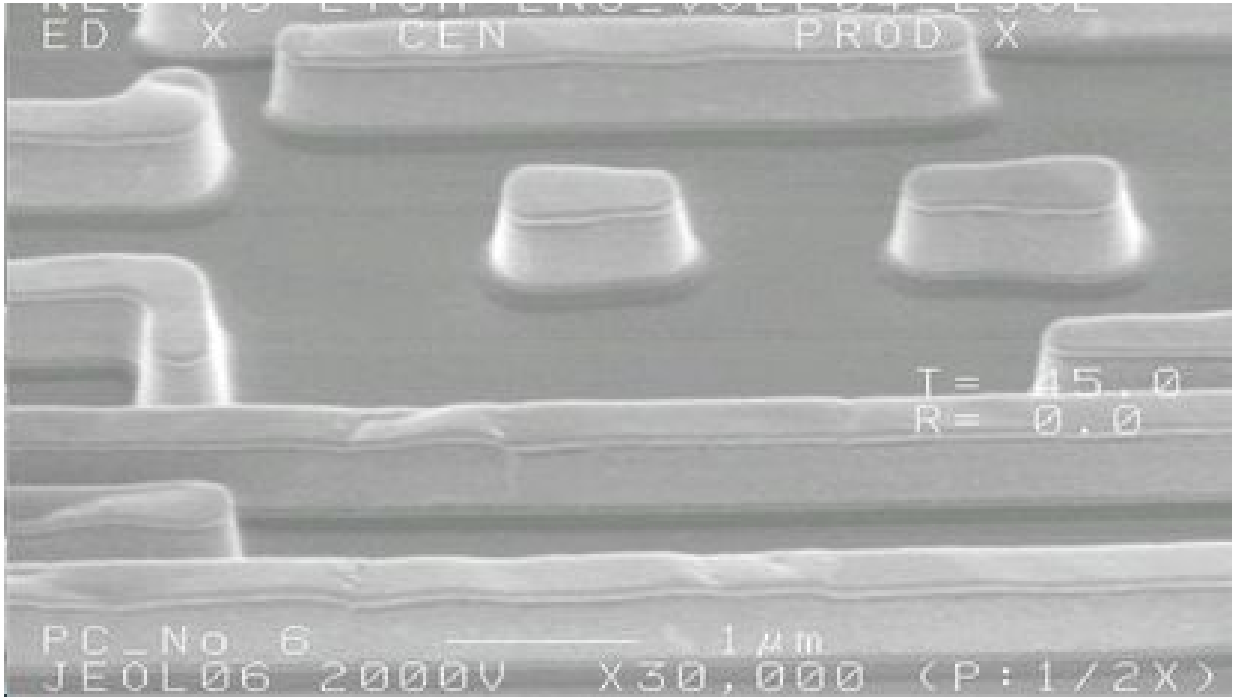
TEXAS INSTRUMENTS

Outline

- Greenhouse gas usage (GHG) in semiconductor manufacturing.
- Opportunities for GHG reduction and substitution.
- Unit Process Development and optimization of GHG-free processing in 200 mm wafer manufacturing.
- Summary.



Inline SEM image of interconnect lines

Semiconductor Manufacturing and GHG

- Best known methods to fabricate metal interconnect arrays patterned by oxide hard masks are generally based on dry etch processes that contain fluorine in an energetic plasma .
- The vast majority of perfluorocarbon (PFC) etchant gas species have been identified and categorized as “greenhouse gases” (GHG) for their theorized negative impact on the climate of the earth.
- Although carbon dioxide emissions are the vast majority of total world GHG inventory, the PFC species have substantially higher global warming potentials factors and lifetime in the atmosphere of the earth:
  - CO_2 365 ppm, Lifetime 5 to 200 years
  - CF_4 80 ppt, Lifetime > 50,000 years.

Global Warming Potential

- Commonly used process gases in semiconductor manufacturing.

TABLE 3. Global Warming Potential (GWP) relative to carbon dioxide*.

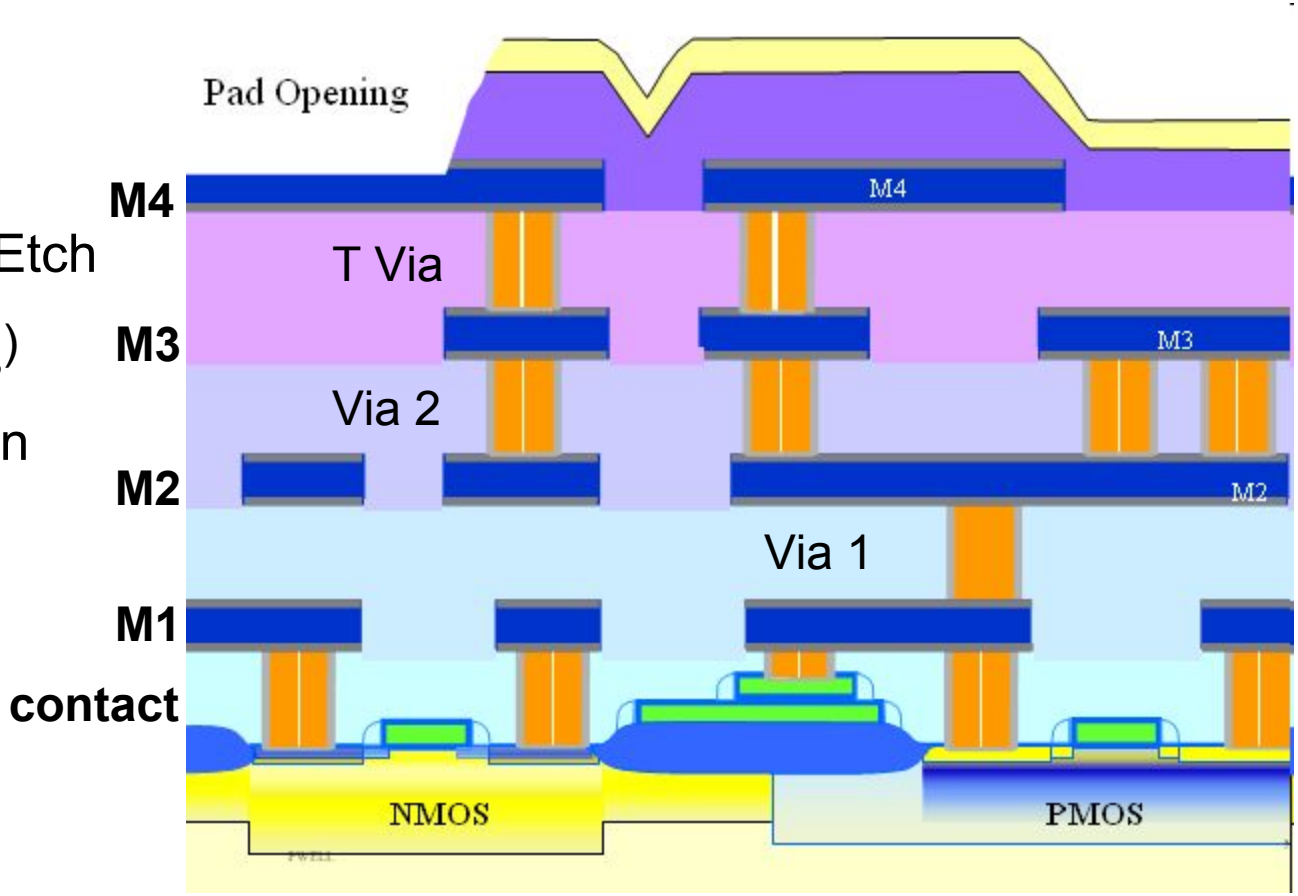
Gas Species	Global Warming Potential	Lifetime (years)
CO_2	1	-
CH_4	62	12
CH_3F	330	2.6
CH_2F_2	1800	5
CF_4	3900	50000
C_2F_6	8000	10000
CHF_3	9400	260
SF_6	15100	3200

*GWP for 20 year time horizon – IPCC 2001 *Technical Summary of the Working Group I Report*

The Face of Climate Change

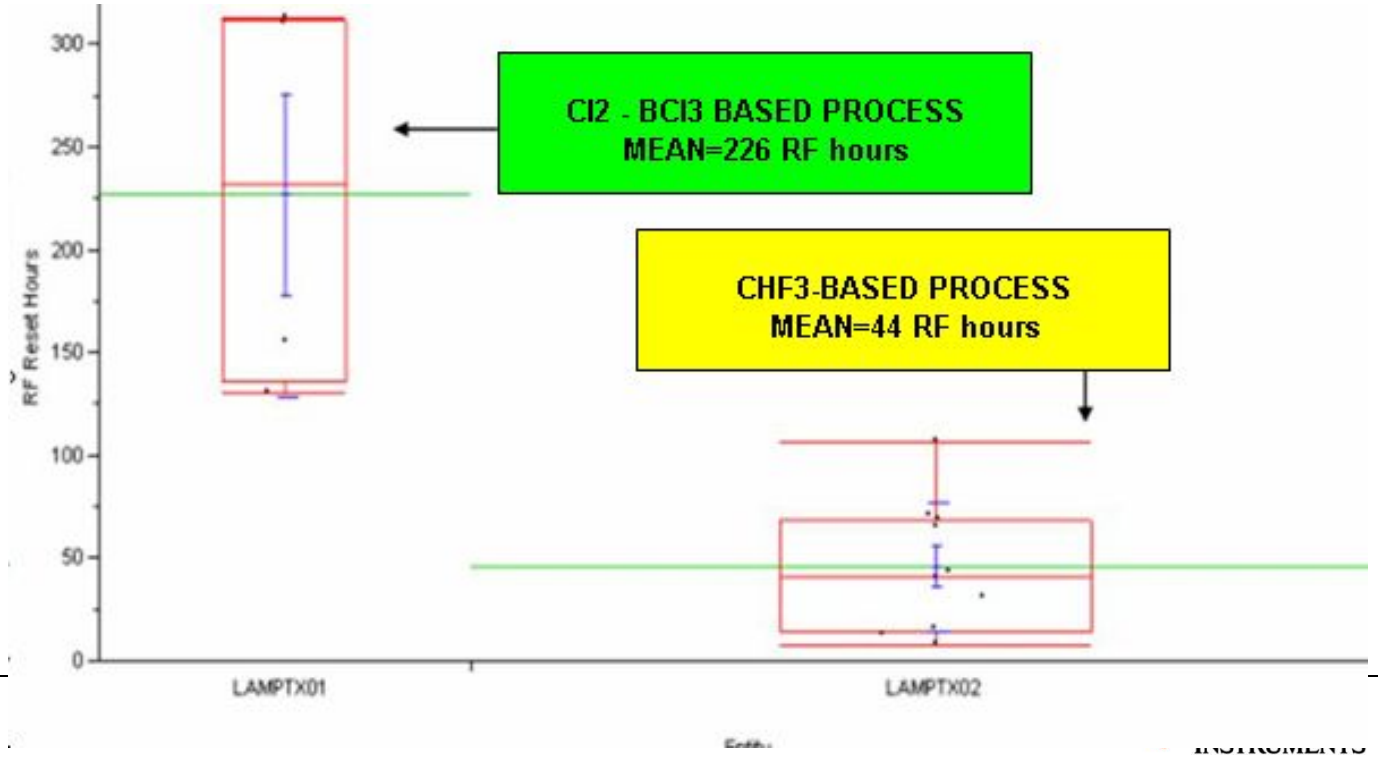
Opportunities for GHG – PFC Reduction and Substitution

- Back-end-of-line (BEOL) construction analysis: Contact to Top Metal
- Contact and Via Oxide Etch
  - CHF_3
  - C_4F_8
- Metal Interconnect Etch
  - CHF_3 (Cl_2 & BCl_3)
- Process optimization can be deployed at multiple process layers.



Manufacturing Cost and Availability

- CHF_3 processes had poor mean time between failure (MTBF) performance.
- Process chamber dedication because of limited compatibility with etch byproducts of non-fluorine containing metal etch processes (*i.e.* Cl_2 - BCl_3 processes).
- **Bottom line: Higher cost of ownership and lower tool availability**



Interconnect Etch Workcell at MFAB1

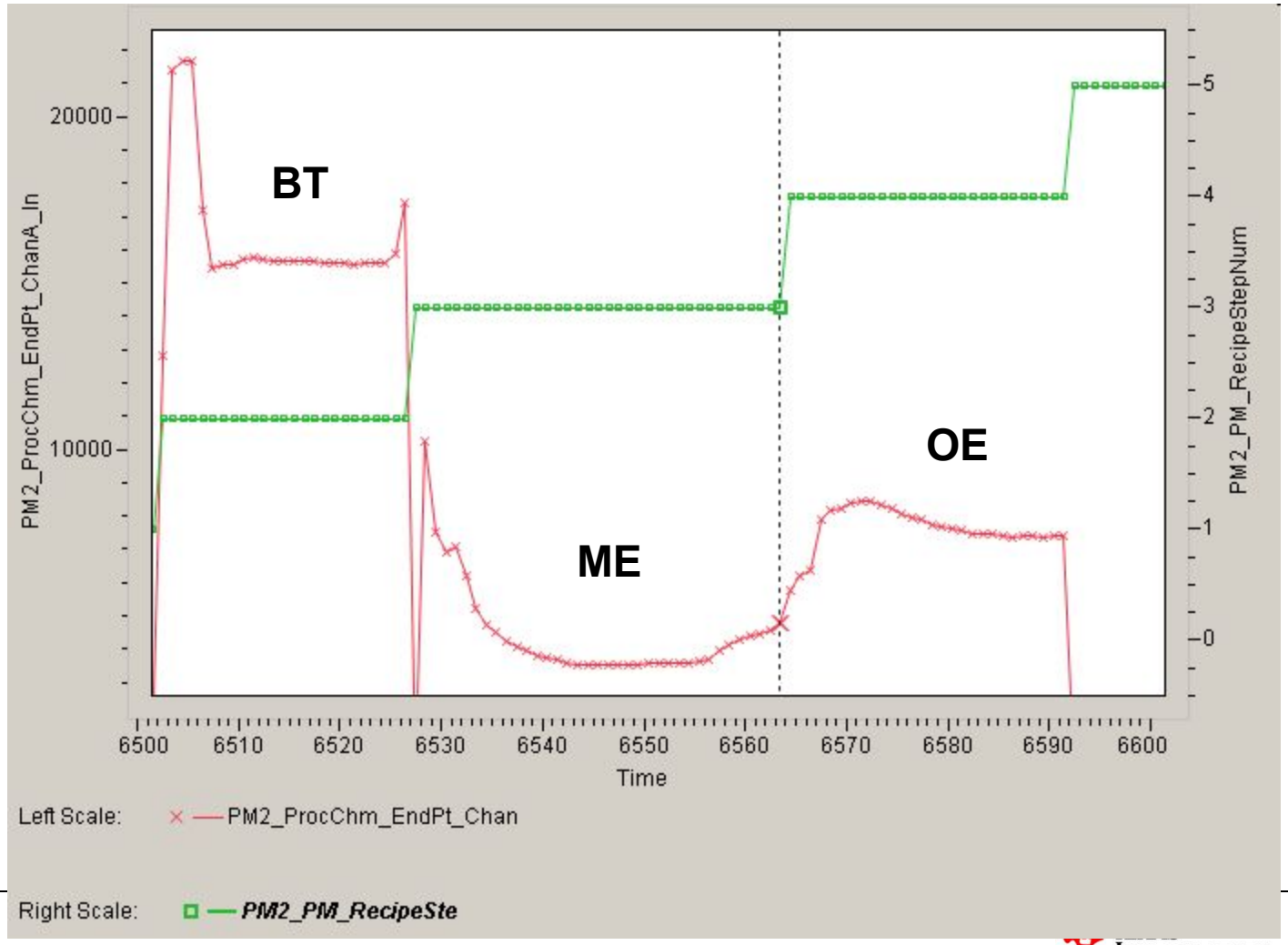
- Analog fabrication center in qualified 350nm to 130nm technology node production.
- Interconnect etch tool sets (200mm wafer tool base):
  - 8 LAMPTX 9600 metal etch chambers
  - 5 LAMTCP 9600 metal etch chambers
- Mean weekly metal layers in production (k thousand layers):
  - 17k metal layers 250nm & 350nm technology nodes
  - 7k metal layers 180nm and lower technology nodes
- Process Flows:
  - Mixed node production across multiple process flows.
- Products: Core CMOS to high speed BiCMOS.

Unit Process Development

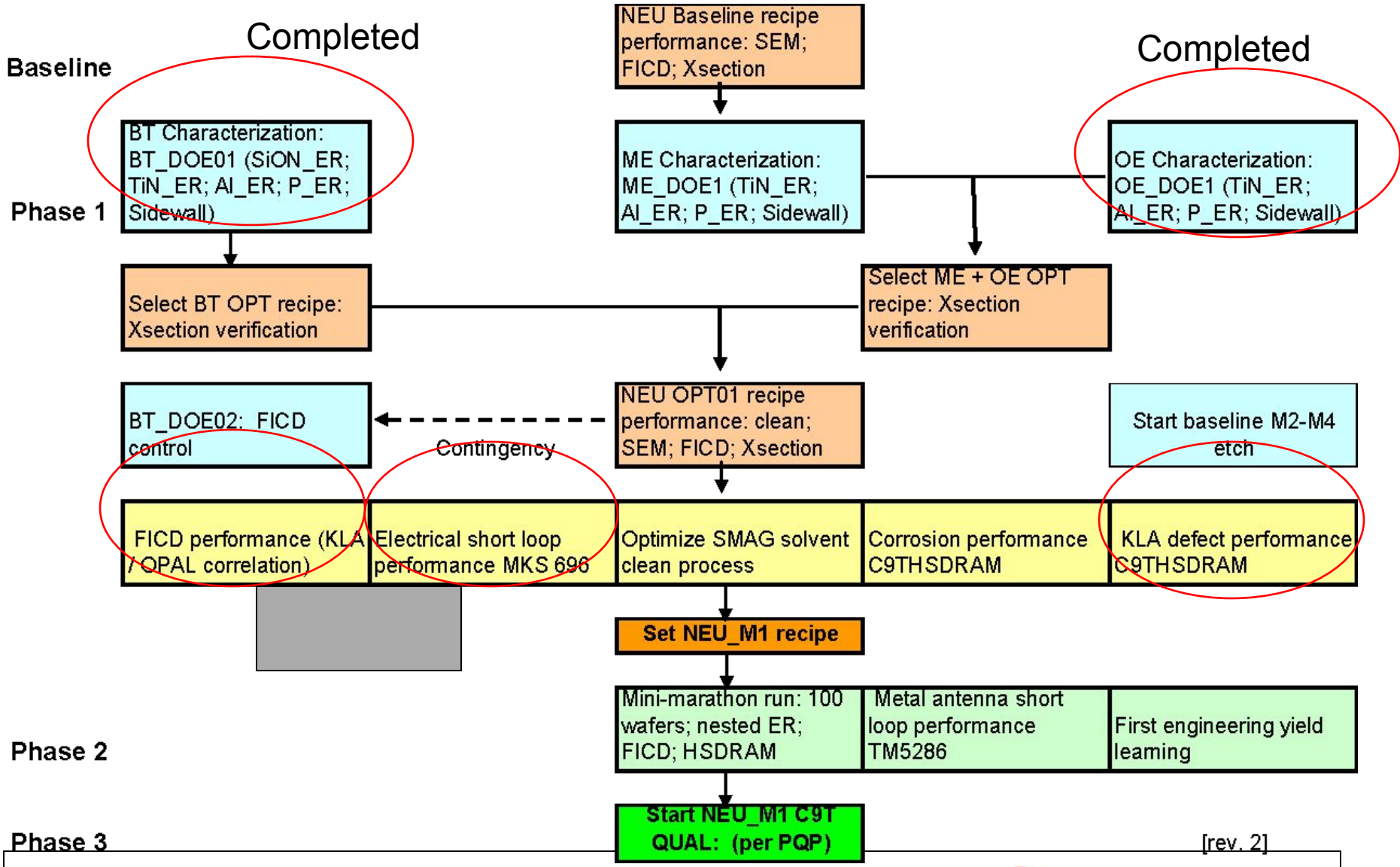
- Process: CMOS 180nm technology with conventional aluminum – 0.5% copper interconnect architecture with 240nm interconnect line – space metal layer M1 design rules and five layers of metal interconnects.
- Unit process development was conducted on the LAM Research LAMPTX9600 metal etch platform in standard production configuration.
- M1 “Short loop” methodology for simulation of production process:
  - 180nm node high density SRAM M1 metal reticle.
  - MDR reticle layout featured M1 design rule and sub-design rule interconnects structures (combs, snakes, etc).
  - Automated defect inspections for process induced defect detection
  - Electrically testable design rule (DR) and sub-DR metal bridging, combs, snakes and conductivity structures
- The original CHF_3-based metal etch chemistry qualified as process of record (POR) utilized a vendor best known method with flow rates for CHF_3 in the SiON break-through, main and overetch steps of 5 sccm.

Metal Etch Optical Spectrum

- Optical line 740nm *versus* time of etch processing
  - BT Break through, ME main etch and OE overetch steps



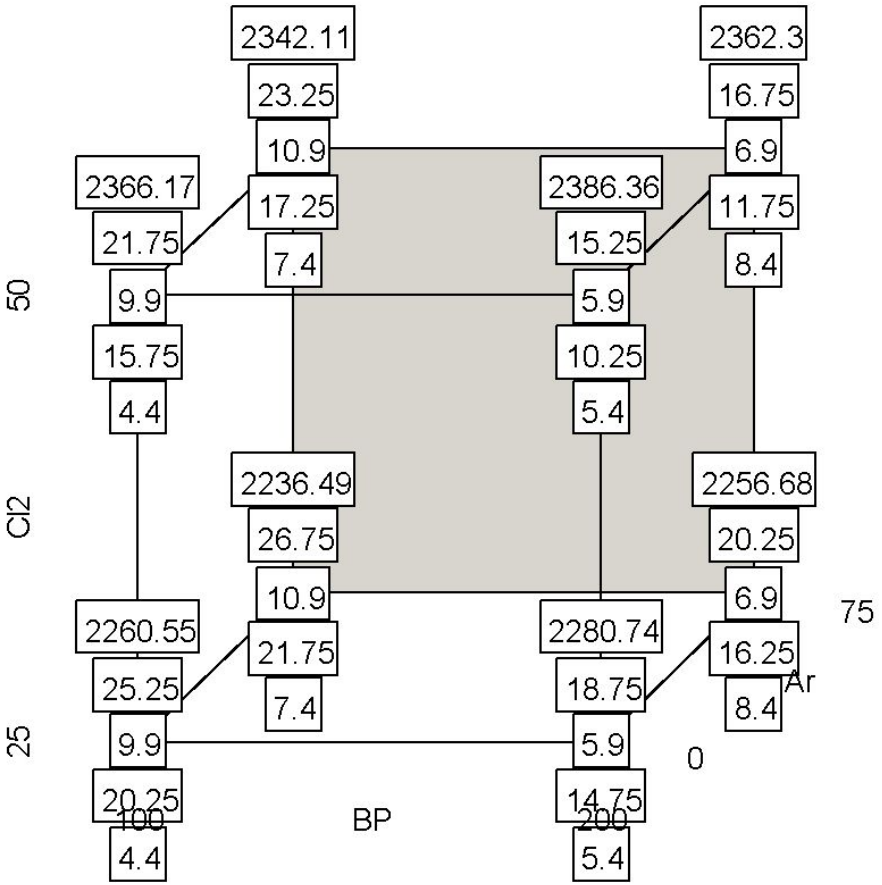
Unit Process Development Flow Chart



[rev. 2]

Building in Process Robustness

- Example of design of experiment (DOE) to identify robust process space for the break through chemistries.

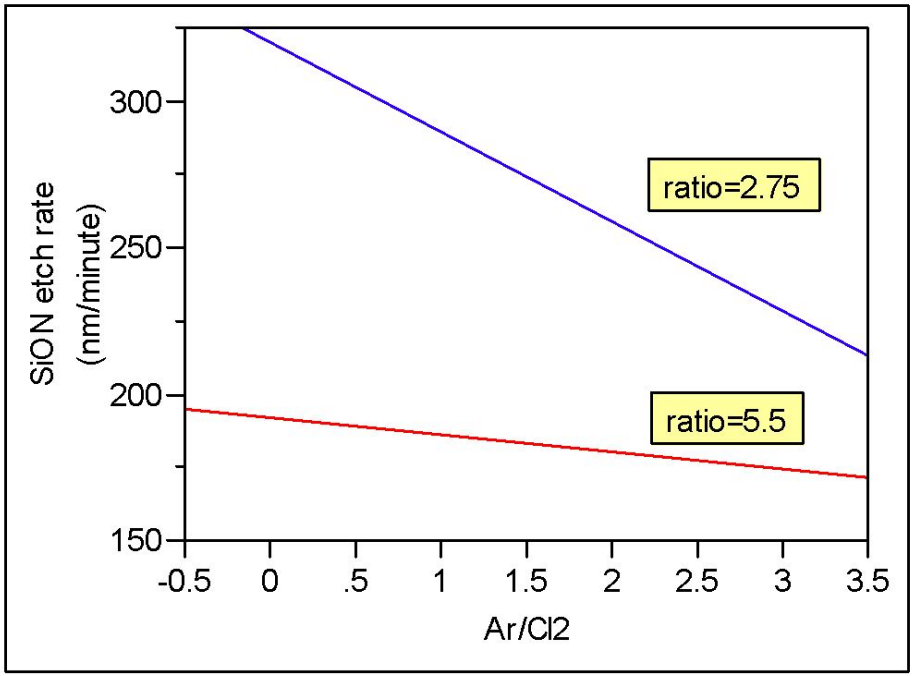


BT_DOE05
PROCESS
SPACE

Response
PRE-POST DELTA
BT TIME
CHA ONSET
CHA PEAK
SIDEWALL GRADE

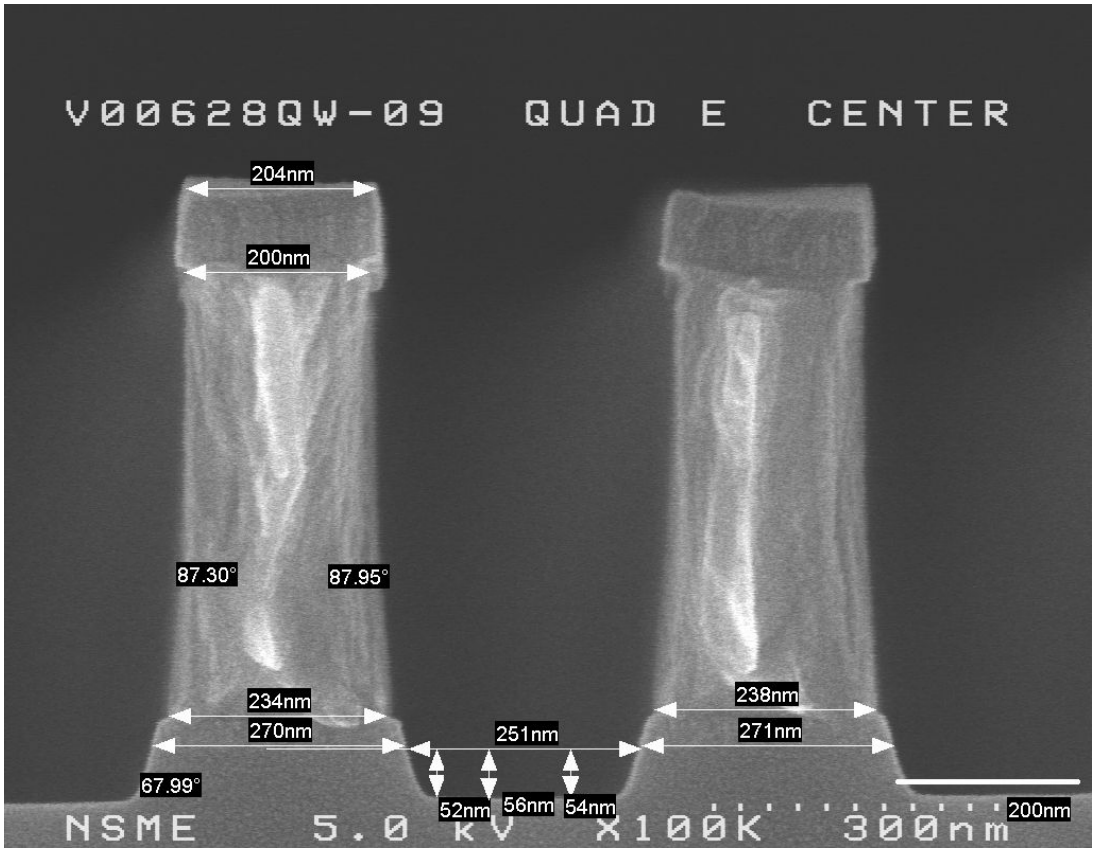
Break Through Step Optimization

- Key requirement of break through step (BT) is to etch the oxide hard mask and break through to the underlying aluminum.
- The SiON break though step process-of-record Cl2 / 5 sccm CHF_3 was replaced with Cl_2 / 100 sccm Ar.
- BT Process optimization for:
  - SiON hard mask etch rate
  - Photoresist selectivity
  - Critical Image performance



Combined Optimized Etch

- Optimization of the overetch step chemistry without CHF_3 through design of experiments resulted in increasing the Cl_2/BCl_3 ratio from 0.91 to 1.8 and total process gas flow by 27%. A low flow of nitrogen was added to the main and overetch steps to maximize sidewall passivation.



Summary

1. This investigation has qualified a greenhouse gas free aluminum – copper interconnect etch process for analog 180 nm technology node in 200 mm wafer production. The new process was successfully released for mixed production with conventional (Cl_2- BCl_3) etch processes at the 250 nm and greater technology nodes.
2. Reduction and substitute of high Global Warming Potential gas species in etch process chemistries are effective strategies to reduce perfluorocarbon (PFC) gas usage in 200 mm wafer semiconductor manufacturing.
3. Manufacturing process requalification can require significant engineering time and resources and must be planned accordingly to meet World Semiconductor Council voluntary greenhouse gas reduction goals and timetables.

Acknowledgements

- Co-authors Les Gardner and Tom Moutinho, MFAB1 Operations Engineering.
- Thanas Budri and the Texas Instruments South Portland Failure Analysis Group (MFAB1) for cross sections of scores of design of experiment wafers.

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