ECS Transactions, 41 (34) 1-7 (2012)
10.1149/1.3697456 ©The Electrochemical Society

Reduction of Greenhouse Gas Emissions by Metal Interconnect Etch Process Optimization

P. S. Frankwicz[a], L. Gardner [b] and T. Moutinho[b]

[a] Analog Technology Development
[b] Operations Engineering
MFAB1
Texas Instruments Incorporated
5 Foden Rd., South Portland, Maine 04106 USA
Email: peter.frankwicz@ti.com

Fluorine containing dry etch processes have been a cornerstone of semiconductor manufacturing since inception of the industry. Greenhouse gases (GHG) commonly used in device fabrication are CF_4, C_2F_6, SF_6, CHF_3 and NF_3. Texas Instruments Incorporated has been voluntarily pursuing GHG priorities aligned with ISO14001:2004, World Semiconductor Council and United States Environmental Protection Agency (1,2). This paper details manufacturing and unit process optimization to eliminate CHF_3 in metal interconnect dry etch of an aluminum – copper analog 180nm technology node process flow in 200mm wafer volume production.

Introduction

Best known methods to fabricate electrically conductive interconnect arrays patterned by silicon - oxide compounds are generally based on dry etch processes that contain fluorine containing gas in the energetic plasma (3). Common perfluorocarbons (PFC) etchant gas species used in semiconductor production are nitrogen trifluoride (NF_3), sulfur hexafluoride (SF_6), tetrafluoromethane (CF_4), hexafluoroethane (C_2F_6), octofluoropropane (C_3F_8), octofluorocyclobutane (c-C_4F_8), and hydrofluorcarbons (HFCs) such as trifluoromethane (CHF_3). A plasma containing free radicals of fluorine greatly improves etching of oxide-based dielectrics and hard mask anti-reflective coatings by the formation of volatile silicon – fluorine species. The vast majority of PFC etchant gas species have been identified and categorized as “greenhouse gases” for their theorized negative impact on the climate of the earth. Table I summarizes Global Warming Potential relative to carbon dioxide and resident lifetimes in the atmosphere of technological important PFC process gases in semiconductor production (4). Although carbon dioxide emissions are the vast majority of total GHG inventory, the PFC species have substantially higher global warming potentials factors and lifetime in the atmosphere of the earth. Two effective strategies to reduce PFC in semiconductor production are substitution and reduction of high GWP gas species in etch manufacturing processes. For example, many best-know-methods (BKM) for thick silicon nitride layers utilize a timed bulk etch step with high flow rates of SF_6. Unit Process Development methodologies can be used to characterize low GWP-based processes to substitute for SF_6-based chemistries. Unsaturated flurocarbons (UFC) such as C_3F_6 and C_5F_8 have been investigated to replace high GWP etchant species used in high aspect ratio contact

and via etch processes (5). The next generation of 300mm wafer production tools are successfully deploying reduced PFC etch processes. Original equipment manufacturers are reporting 50% to 90% reductions in PFC usage in dielectric oxide etch recipes and complete substitution in applications such as dual damascene via etch (6).

TABLE I. Global Warming Potential (GWP) relative to carbon dioxide (4).

Gas Species	Global Warming Potential*	Lifetime (years)
CO_2	1	-
CH_4	62	12
CH_3F	330	2.6
CH_2F_2	1800	5
CF_4	3900	50000
C_2F_6	8000	10000
CHF_3	9400	260
SF_6	15100	3200

*GWP for 20 year time horizon

From a purely manufacturing standpoint, process chemistries that have plasmas containing free radicals of fluorine have disadvantages that negatively impact manufacturing tool availability and process capability. These fluorine containing chemistries have low selectivity to photoresist formulations that contribute to significant degradation of isolated line sidewall passivation and final image critical dimension (FICD) sensitivity to percent of open area on the wafer. Degraded interconnect lines can result in increase line resistance and shifts in product electrical performance. Secondly, polymer residues of fluorinated hydrocarbons (C-F-H compounds) that are generated on the manufacturing chamber walls have limited compatibility with etch byproducts of non-fluorine containing metal etch processes (i.e. Cl_2 - BCl_3 processes). This byproduct incompatibility can result in undesirable manufacturing chamber dedication to fluorine or chlorine containing gas processing chemistries, exclusively. Production chambers that were dedicated to CHF_3 processes exhibited significantly lower chamber lifetimes in comparison to conventional (Cl_2 - BCl_3) process chambers (Figure 1). This equates to higher cost of ownership because of frequent process chamber cleans and kit replacements. Unfortunately, attempts to use both fluorine and chlorine based process chemistries in the same manufacturing chamber can result in process induced defects caused by polymer flaking or shedding from the interior of the chamber walls to the surface of the wafer substrate. High levels of process induced defects (PID) on interconnect arrays can result in significant electrical shorting of minimum geometric features and lower product yield. Texas Instruments Incorporated has implemented aggressive plasma etch production tool qualifications and process induced defect monitoring to insure product quality (7,8).

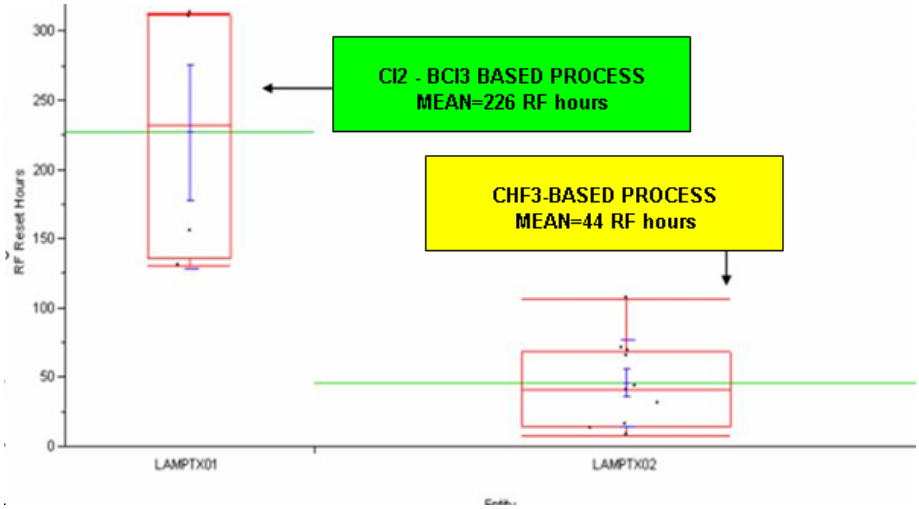


Figure 1. Mean time between cleans (MTBC) in production hours for LAMPTX9600 metal etch chambers in conventional (Cl_2 - BCl_3) process production (mean 225 hours) *versus* production chambers dedicated to CHF_3 process (mean 48 hours).

The principle mission of this investigation was to develop a metal interconnect etch recipe for 180nm technology node without GHG species that could be phased into mixed node production with 250nm and 350nm technology process recipes containing no CHF_3. From a Unit Process Development perspective, process requalification of a technology in daily production is a rather complex undertaking. The development process chamber was also in concurrent production with 250nm and 350nm technology node high volume production. The new etch process must achieve online process monitor (OLPM) specifications such as final image critical dimension, process bias (final image - developed image critical dimension), and electrical parametics (i.e. contact chain and line resistance). The dimensional aspect is especially important because replacement of hundreds of photolithographic reticles would be prohibitive for both cost and disruption of production. A summary of major failure mode and effects analysis (FMEA) is presented in Table II. Failure modes with risk priority numbers (RPN) above 50 need additional characterization and built in safe guards for process robustness in manufacturing. In the present investigation, the paramount success metrics are demonstration that metal interconnects etched with the GHG-free etch process possess equivalent end-of-line electrical test and product sort yield as the process of record (POR).

TABLE II. Failure Mode and Effects Analysis for Metal Interconnect Etch Processing.

Failure Mode	Effects of Failure	Risk Priority Number (RPN)
Process Induced Defects	Interconnect shorts and masking	140
Under etch	Interconnect electrical shorts	105
Over etch	Interconnect degradation and loss	84
Plasma damage	Damaged transistor gate oxide	40
FICD out of specification	Interconnect bridging and shorts	21

Experimental Details

Unit process development was conducted on the LAM Research LAMPTX9600 metal etch platform in standard production configuration. The original CHF_3-based metal etch chemistry qualified as process of record (POR) utilized a vendor best known method with flow rates for CHF_3 in the SiON break-through, main and overetch steps of 5 sccm (9). The analog CMOS 180nm technology process-of-record (POR) features a conventional aluminum – 0.5% copper interconnect architecture with 240nm interconnect line – space metal layer M1 design rules and five layers of metal interconnects. Test wafers of 200mm size were fabricated on production short process flows from contact liner to first metal layer define (M1). Applied Materials 5500 Endura metal deposition toolsets were used for interconnect deposition of conventional aluminum – 0.5% copper interconnect alloy. The wafers patterned with the multiple design rule (MDR) metal bridging reticle to evaluate interconnect electrical performance and construction. The MDR reticle layout featured design rule, sub-design rule metal snakes, combs and programmed defects for in-fab defect inspections. Electrical test measures of metric were bridging monitor yield and Weibul analysis of leakage current. Failure analysis cross sections of design rule and sub-design rule dense and isolated lines were evaluated for interconnect cross section construction, sidewall angle and overetch depth into the underlying dielectric oxide layer.

Results and Discussion

Unit process optimization to eliminate CHF_3 in metal interconnect dry etch required partitioning the etch process recipe and re-optimizing the hard mask break through and overetch process steps. The hard mask break through step is required to etch an oxide containing thin film and is important in defining the final image critical dimension that is generated by the subsequent main aluminum etch step. Conventional (Cl_2 - BCl_3) etch break through chemistries used to etch TiN anti-reflective coatings exhibit poor performance against oxide containing thin films. The SiON break though step process-of-record Cl_2 / 5sccm CHF_3 was replaced with Cl_2 / 100sccm Ar. This resulted in a beneficial -20nm reduction in the final image critical dimension (FICD) process bias. Optimization of the overetch step chemistry without CHF_3 through design of experiments resulted in increasing the Cl_2/BCl_3 ratio from 0.91 to 1.8 and total process gas flow by 27%. A low flow of nitrogen was added to the main and overetch steps to maximize sidewall passivation. The resultant metal lines produced by the new optimized metal etch recipe featured normal sidewall construction and sufficient overetch into the underlying dielectric oxide layer as shown in figure 2.

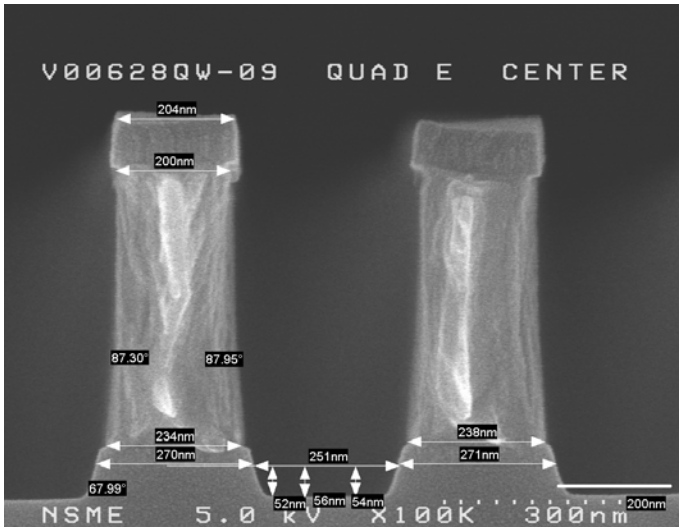
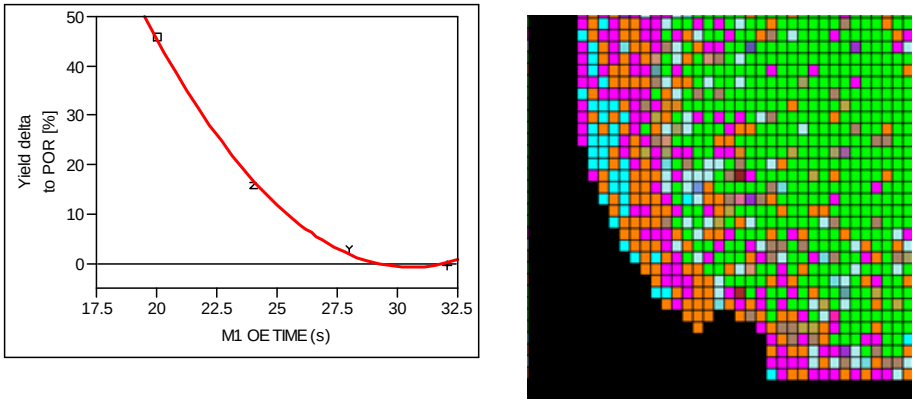


Figure 2. Scanning electron micrograph of metal interconnect cross section that was etched with optimized non-CHF_3 etch recipe and metal solvent clean.

Process verification lots were fabricated with new optimized metal etch recipe and overetch time for evaluation of electrical test, sort yield and wafer level reliability. Product yield versus overetch time of the optimized metal etch recipe are shown in figure 3; equivalent yield to POR was achieved at greater than 27 seconds overetch step time. Yield degradation at shorter overetch times displayed high wafer edge yield fallout that is characteristic of the LAMPTX9600 etch platform. In subsequent process verification trials, the optimized metal etch at all metal layers demonstrated statistically equivalent sort yield in comparison to POR CHF_3-based metal etch recipe. The optimized metal etch recipe without CHF_3 was released under limited pilot production in parallel with the existing 250nm and 350nm production recipes. The LAMPTX9600 pilot tool achieved a factor of 4.5 increase in mean time between cleans in comparison to production chambers dedicated solely to CHF_3–based production recipes. The mean defective die percentage associated with process induced defects decreased by over 50% on 180nm monitor SRAM wafers etched with the new optimized metal etch without CHF_3. The overall Unit Process Development project was qualified GHG free and released to full production in approximately eight months.



A B.

Figure 3. A. Relative sort yield failure (POR yield – trial yield) *versus* overetch step time at first metal layer (M1) for analog 180nm product Alpha. B. Partial section of a wafer yield map displaying failing product die due to metal shorts on the edge of the wafer overetch time of 20 seconds (color green denotes yielding product die).

Conclusions

This investigation has qualified a greenhouse gas free aluminum – copper interconnect etch process for analog 180nm technology node in 200mm wafer production. The new process was successfully released for mixed production with conventional (Cl_2- BCl_3) etch processes at the 250nm and 350nm technology nodes. Reduction and substitute of high Global Warming Potential gas species in etch process chemistries are effective strategies to reduce perfluorocarbon gas usage in 200mm wafer semiconductor manufacturing. Manufacturing process requalification can require significant engineering time and resources and must be planned accordingly to meet World Semiconductor Council voluntary greenhouse gas reduction goals and timetables.

Acknowledgments

PSF acknowledges Thanas Budri and the Texas Instruments South Portland Failure Analysis Group (MFAB1) for cross sections of scores of design of experiment wafers. Lacie Kennedy (Operations Process Engineering) and Don Scipione (Operations Equipment Engineering) are gratefully acknowledged for assisting in the Operations Review Board process qualification.

References

1. “Mandatory Reporting of Greenhouse Gases: Additional Sources of Fluorinated GHGs 40 CFR Part 98”; Environmental Protection Agency, Federal Register Vol. 75, No. 230 (2010).
2. Joint Statement of the 15th Meeting of the World Semiconductor Council, pgs. 6-7; World Semiconductor Council, Fukuoka Japan, May 26, 2011
3. Yunju Ra, S.G. Bradley and Ching-Hwa Chen, *J. Vac. Sci. Technol.* **A12,** 1328 (1994).

4. *Technical Summary of the Working Group I Report*, Intergovernmental Panel on Climate Change (IPCC); F. Joos, A. Ramirez-Rojas, J.M.R. Stone and J. Zillman, Editors, pgs. 36-44, Cambridge University Press, Cambridge (2001).
5. Hyun-Kyu Ryua, Yil-Wook Kimb, Kangtaek Leec, CheeBurm Shind and Chang-Koo Kimd, *Microelectronic Journal*, **36**, 125 (2007).
6. "Greenhouse Gas Reduction and Energy Efficiency–Opportunities for Equipment Suppliers"; S. Hughes, Proceedings of the Plasma Applications Group, American Vacuum Society Northern California User Group, pg.17, May 15, 2008.
7. "Comprehensive interconnect etch tool qualification methodology for high volume mixed technology node production"; P. S. Frankwicz, R. Clark, K. Hayes, M. Johnson, L. Kennedy, D. Scipione, C. Viera and T. Moutinho, Proceedings of the International Symposium on Semiconductor Manufacturing (ISSM), Santa Clara, CA; Institute of Electrical and Electronics Engineers (IEEE Catalog 07CH37896), pgs. 350-353 (2007).
8. "Process Excursion Detection using Statistical Analysis Methodologies in High Volume Semiconductor Production"; P.S. Frankwicz, S. E. Romano and T. Moutinho, Proceedings of the Northeast SAS Users Group (NESUG), Burlington VT (2009); (online at http://www.nesug.org/proceedings/).
9. "TCP9600PTX 0.18 Micron Metal Etch Process Release"; G. Goldspring, E. Bosch, R. O'Donnell, and C. Ordonie, Report #27003 Revision A, pg. 7, Lam Research Corporation, Freemont, CA (2000).