In this paper Kim et al. (2014) did an experimental study on an issue of scaling down of DRAM process technology impacting on memory reliability called as Disturbance Errors. They described the problem as if repeatedly reading from the same address, it is possible to corrupt data in nearby addresses also known as row hammer and figured out root cause of the problem and also proposed a solution to prevent errors.

They discussed that repeatedly opening and closing a row induces disturbance errors in adjacent rows due to mainly three reasons – (1) Electromagnetic coupling – Toggling the word line voltage briefly increases the voltage of adjacent word lines; (2) Conductive bridges and; (3) Hot-carrier injection.

To develop an understanding of disturbance errors, they designed 129 DRAM modules on an FPGA-based testing platform 129 modules from 3 largest DRAM manufacturers 110 of 129 modules are vulnerable

They examined and proposed seven solutions to tolerate, prevent, or mitigate disturbance errors such as make better DRAM chips, refresh frequently, sophisticated ECC and access counters to retire cells (manufacturers and users). All these solutions were very complex and not effective in terms of cost and power. However, they believed that PARA (probabilistic adjacent row activation) is an effective and low-overhead solution to prevent disturbance errors because the key idea is after closing a row, refresh one of its neighbors with a low probability that guaranteed the reliability because when probability is low chances of errors are very less. They stated that PARA refreshes rows infrequently and PARA is stateless meaning that PARA is low cost and low complexity solution. Average slowdown was 0.20% (for 29 benchmarks) Maximum slowdown was 0.75%.