Pranav Gangwar

Summary

Pursuing unanswerable questions at the intersection of computer engineering and biology, while judiciously leveraging today's computational power to push the boundaries of knowledge.

Education

2021 - Present PhD in Computer Engineering at **UC San Diego** (GPA: 4.0/4.0)
2014 - 2018 BTech in ECE at **Delhi Technological University** (Aggregate: 83.33%)

Publications

Minxuan Zhou, Yujin Nam, **Pranav Gangwar**, et al. (2023). *FHEmem: A Processing In-Memory Accelerator for Fully Homomorphic Encryption*. arXiv: 2311.16293 [cs.AR]. URL: https://arxiv.org/abs/2311.16293.

Uday Mallappa, **Pranav Gangwar**, Behnam Khaleghi, et al. (2022). "TermiNETor: Early Convolution Termination for Efficient Deep Neural Networks". In: *2022 IEEE 40th International Conference on Computer Design (ICCD)*, pp. 635–643. DOI: 10.1109/ICCD56317.2022.00098.

Pranav Gangwar, Satvik Maurya, Shubham Garg, et al. (2019). "Hardware/Software Co-Design of a High-Speed Othello Solver". In: *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1223–1226. DOI: 10.1109/MWSCAS.2019.8885136.

Pranav Gangwar, Neeta Pandey, and Rajeshwari Pandey (2019). "Novel Control Unit Design for a High-Speed SHA-3 Architecture". In: *2019 IEEE 62nd International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 904–907. DOI: 10.1109/MWSCAS.2019.8885323.

Research Projects

Wastewater based Epidemiology Turakhia Lab

- Developed phylogenetic based algorithm to detect SARS-CoV-2 from wastewater
- Detects the entire genome of SARS-CoV-2 strains in wastewater (16 million SARS-CoV-2 strains), which is a mixture containing heavily fragmented genomes from multiple strains
- Much higher resolution and accuracy over state-of-the-art softwares, which can only detect pathogens' family of related strains
- Incorporating large language models to detect novel strains from the wastewater
- Working with the Centers for Disease Control and Prevention (CDC) to analyze wastewater data across the United States with this algorithm and its potential integration to the National Wastewater Surveillance System (NWSS). Also working towards extending this algorithm to other infectious diseases

Diffusion generative modelling Turakhia Lab

- Working on algorithmic modifications to improve sampling speed of diffusion models
- Applying diffusion models to interesting bioinformatics problems

TermiNETor SEE LAB

– Designed bit-serial hardware architecture to efficiently accelerate convolution operations in deep neural networks. Co-designed the architecture with novel early convolution termination algorithm that conserved energy by predicting redundant computations

– Evaluated performance on analytical simulator and estimated area and power from RTL. Results showed 120x energy-efficiency over GPU and 2x over sparsity-aware accelerators

Processing in memory based hardware accelerators SEE LAB

– Designed NeRF rendering low-power accelerator using In-DRAM computing and near data processing

– Worked on DRAM based accelerator for fully homomorphic encryption based CKKS algorithm

Work Experience

GPU Architecture Intern - Intel Jun-Sept 2023, Jun-Sept 2022

– Modelled next generation Tensor cores on analytical simulator and explored different architectures

– Implemented dense matrix multiplication decomposition algorithm inspired from Stream-K, which picked best tile size based on Tensor core's utilization and memory bandwidth bottlenecks

– Compared Stream-K's performance results on Intel's next generation GPU with existing matrix decomposition algorithm

Digital Design Engineer - Texas Instruments July 2018 - July 2021

– Designed backend for wireless transceiver subsystems: floorplanning, module placement, clock tree synthesis, routing, and physical verification. Also helped with restructuring of pipeline in the modules to meet stringent input-output timing constraints

– Developed power recovery flow that reduced total design power by recommending standard cell resizing at sign-off stage. It took advantage of lower pessimism in timing constraints at sign-off as compared to place and route stage

Skills

Languages C++, Verilog, Python, Tcl, Shell
Softwares PyTorch, Innovus™, Tempus™, Voltus™, PVS, Assura®, Vivado®, MATLAB®, Virtuoso®

Teaching Assistant

Winter 2023	ECE-111: Advanced Digital Design Project	UC San Diego
Spring 2023	ECE-111: Advanced Digital Design Project	UC San Diego

Mentoring

Summer 2024 - Present	Abhishikta Panja, Graduate Student	UC San Diego
Spring 2024 - Present	Manu Bhat, Undergraduate Student	UC San Diego
Spring 2024	Reya Sadhu, Graduate Student	UC San Diego
Spring 2023 - Winter 2024	Girish Krishna, Undergraduate Student	UC San Diego
Spring 2023 - Winter 2024	Carolyn Zhang, Undergraduate Student	UC San Diego