

# Pranav Gangwar

 |  pgangwar@ucsd.edu |  San Diego, California

## SUMMARY

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PhD Candidate seeking a Summer 2026 internship with experience in GPU architecture, performance modeling, and custom architecture design for emerging applications.

## EDUCATION

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2021 – Present	PhD in Computer Engineering at <b>UC San Diego</b>	(GPA: 4.0)
2021 – 2024	MS in Computer Engineering at <b>UC San Diego</b>	(GPA: 4.0)

**Relevant Coursework:** Principles of Computer Architecture, Principles of Operating Systems, Low-power VLSI for Machine Learning, Introduction to Visual Learning, Parallel Computation, Parallel Computing in Bioinformatics

## WORK EXPERIENCE

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<b>GPU Performance Architecture Intern</b>	<b>Intel</b> (Jun-Sept 2023, Jun-Sept 2022)
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- Analyzed multiple next-generation Tensor Core architecture proposals on the architectural simulator to identify performance bottlenecks and guide design improvements.
- Designed and implemented a matrix tile-size selection algorithm tailored for Intel's GPU architecture, improving performance on machine learning workloads by increasing utilization and reducing stalls.
- Adapted and evaluated a state-of-the-art matrix decomposition algorithm, achieving further improvements in GPU utilization beyond the baseline tile-size selection approach.
- Characterized emerging neural graphics workloads by developing performance models, enabling the identification of key performance bottlenecks in the proposed architecture.

<b>Digital Design Engineer</b>	<b>Texas Instruments</b> (July 2018 - July 2021)
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- Designed and verified backend flows (floorplanning, placement, CTS, routing, and physical verification) and optimized digital pipelines to meet stringent I/O timing constraints.
- Developed a power recovery flow that reduced total design power by recommending standard cell resizing at the sign-off stage, leveraging lower timing pessimism.

## RESEARCH PROJECTS

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### Computer Architecture Research

<b>TermiNETor: An Energy-Efficient DNN Accelerator</b>	Sep 2021 - Jun 2022
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- Achieved  $120\times$  energy efficiency over GPUs by co-designing a novel bit-serial hardware architecture with an early-termination algorithm to prune redundant computations.
- Validated the architecture design and performance gains using an analytical simulator and RTL-based power and area estimation.

<b>PIM and NDP Hardware Accelerators</b>	Sep 2021 - Dec 2022
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- Designed a low-power accelerator for NeRF rendering using Processing-in-Memory (PIM) and Near-Data Processing (NDP) techniques.
- Contributed to the development of a DRAM-based NDP accelerator for Fully Homomorphic Encryption (FHE).

## Applied Computational Research

### Wastewater-Based Epidemiology

Jan 2023 - Jun 2025

- Developed a scalable, multi-threaded, and memory-efficient algorithm that processes millions of noisy genome fragments against a 16-million SARS-CoV-2 genome database in hours, accurately identifying complete genomes—solving a previously considered intractable problem.
- Enabled early detection of new variants to drive timely public health interventions; collaborating with the Centers for Disease Control and Prevention (CDC) for nationwide integration.
- Generalized this idea to identify complete genomes of multiple pathogens circulating in wastewater samples, as well as clinical DNA samples of patients from hospitals.

### SARS-CoV-2 Vaccines Strain Selector

Sep 2024 - Present

- Extracting new insights from 16 million SARS-CoV-2 genomes to develop a low-complexity model, achieving performance at par with complex protein language models.
- Developed a lightweight Machine Learning model for vaccine strain selection, deployable even on edge devices, and outperforming the Food and Drug Administration (FDA) recommendations.

## PUBLICATIONS

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1. “TermiNETor: Early convolution termination for efficient deep neural networks”, U Mallappa, **P Gangwar**, B Khaleghi, H Yang, T Rosing. *IEEE Int. Conference on Computer Design (ICCD)*, 2022.
2. “FHEmem: A processing in-memory accelerator for fully homomorphic encryption”, M Zhou, Y Nam, **P Gangwar**, W Xu, A Dutta, et al. *IEEE Transactions on Emerging Topics in Computing*, 2025.
3. “WEPP: Phylogenetic Placement Achieves Near-Haplotype Resolution in Wastewater-Based Epidemiology”, **P Gangwar**, P Katte, M Bhat, Y Turakhia. *medRxiv*, 2025.

## SKILLS

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**Languages** C, C++, CUDA, Verilog, Python, Tcl, Shell

**Software & Tools** PyTorch, Innovus<sup>TM</sup>, Tempus<sup>TM</sup>, Voltus<sup>TM</sup>, PVS, Assura<sup>®</sup>, Vivado<sup>®</sup>, MATLAB<sup>®</sup>