Pranav Gangwar

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Summary

PhD Candidate seeking a Summer 2026 internship with experience in GPU architecture, performance modeling, and custom architecture design for emerging applications.

Education

2021 – Present PhD in Computer Engineering at **UC San Diego** (GPA: 4.0)
2021 – 2024 MS in Computer Engineering at **UC San Diego** (GPA: 4.0)

Relevant Coursework: Parallel Computation, Principles of Computer Architecture, Principles of Operating Systems, Low-power VLSI for Machine Learning, Introduction to Visual Learning

Work Experience

GPU Performance Architecture Intern **Intel** (Jun-Sept 2023, Jun-Sept 2022)

- Analyzed multiple next-generation Tensor Core architecture proposals on the architectural simulator to identify performance bottlenecks and guide design improvements.
- Designed and implemented a matrix tile-size selection algorithm tailored for Intel's GPU architecture, improving performance on machine learning workloads by increasing utilization and reducing stalls.
- Adapted and evaluated a state-of-the-art matrix decomposition algorithm, achieving further improvements in GPU utilization beyond the baseline tile-size selection approach.
- Characterized emerging neural graphics workloads by developing performance models, enabling the identification of key performance bottlenecks in the proposed architecture.

Digital Design Engineer **Texas Instruments** (July 2018 - July 2021)

- Designed and verified backend flows (floorplanning, placement, CTS, routing, and physical verification) and optimized digital pipelines to meet stringent I/O timing constraints.
- Developed a power recovery flow that reduced total design power by recommending standard cell resizing at the sign-off stage, leveraging lower timing pessimism.

Research Projects

Computer Architecture Research

TermiNETor: An Energy-Efficient DNN Accelerator Sep 2021 - Jun 2022

- Achieved 120× energy efficiency over GPUs by co-designing a novel bit-serial hardware architecture with an early-termination algorithm to prune redundant computations.
- Validated the architecture design and performance gains using an analytical simulator and RTL-based power and area estimation.

PIM and NDP Hardware Accelerators Sep 2021 - Dec 2022

- Designed a low-power accelerator for NeRF rendering using Processing-in-Memory (PIM) and Near-Data Processing (NDP) techniques.
- Contributed to the development of a DRAM-based NDP accelerator for Fully Homomorphic Encryption (FHE).

Applied Computational Research

Wastewater-Based Epidemiology Jan 2023 - Jun 2025

- Developed a multi-threaded, scalable algorithm to analyze millions of fragmented wastewater sequences on a 16-million-genome SARS-CoV-2 database in hours, accurately identifying complete genomes—a task previously considered infeasible.
- Enabled early detection of new variants to drive timely public health interventions; collaborating with the Centers for Disease Control and Prevention (CDC) for nationwide integration.

Effective SARS-CoV-2 Strain Selection for Vaccines Sep 2024 - Present

- Analyzed 16-million SARS-CoV-2 genomes to develop a simple model achieving comparable performance to complex protein language models and multinomial logistic likelihood models.
- Reformulated the SARS-CoV-2 evolution prediction problem by incorporating small stochastic variations, improving predictions over existing models.

Publications

1. "TermiNETor: Early convolution termination for efficient deep neural networks", U Mallappa, **P Gangwar**, B Khaleghi, H Yang, T Rosing. *IEEE Int. Conference on Computer Design (ICCD)*, 2022.
2. "FHEmem: A processing in-memory accelerator for fully homomorphic encryption", M Zhou, Y Nam, **P Gangwar**, W Xu, A Dutta, et al. *IEEE Transactions on Emerging Topics in Computing*, 2025.
3. "WEPP: Phylogenetic Placement Achieves Near-Haplotype Resolution in Wastewater-Based Epidemiology", **P Gangwar**, P Katte, M Bhat, Y Turakhia. *medRxiv*, 2025.

Skills

Languages	C++, Verilog, Python, Tcl, Shell
Software & Tools	PyTorch, Innovus™, Tempus™, Voltus™, PVS, Assura®, Vivado®, MATLAB®