

Laser Frame in Acquisition Mode							
Word #	Word	Name	Origin	Meaning or comment		Lasco Init	
0	B0 F0 00 00	Start of Frame	VME	Control Word		0xB0F00000	
1	EE 12 34 EE	Start of Header Marker	VME			0xEE1234EE	
2	00 00 00 09	Header Size	VME			9	
3	03 01 01 00	Format Version Number	VME	Major = 3.01	Minor = 1.00	0x03010100	
4	00 50 00 00	Source Identifier	VME	0x50 = LASCAR		0x00500000	
5	rr rr rr rr	Run Number	VME			0	
6	ee ll ll ll	Extended Event Identifier	FPGA	ee = ECRIId	lllll= LIAId	0	
7	00 00 0b bb	Bunch Identifier	FPGA	BCID		0	
8	00 00 00 tt	L1A Tigger Type	FPGA			0	
9	00 00 00 tt	Detector Event Type	VME			0	
10	FF 12 34 FF	Start of Fragment Marker	VME			0xFF1234FF	
11	00 00 00 nn	Fragment Size	VME			131	
12	00 20 00 17	Sub-Fragment Id	VME			0x00200017	
13	00 00 00 tt	Daq Type	FPGA	Laser=20		0	
14	nn nn nn nn	Count	FPGA	Laser Count		0	
15	rr rr mm mm	Laser Intensity	FPGA	rrrr= Requested Intensity	mmmm = measured intensity	0	
16	00 0f dd dd	Filter -Delay Laser	FPGA	f = filter	dddd = Delay Slama	0	
17	00 00 ll ll	Linearity DAC Value	FPGA			0	
18	ll ll hh hh	ADC Channel	0 & 1	FPGA	PhotoDiode K7 No 1	High & Low Gain	0
19	ll ll hh hh	ADC Channel	2 & 3	FPGA	PhotoDiode K7 No 2	High & Low Gain	0
20	ll ll hh hh	ADC Channel	4 & 5	FPGA	PhotoDiode K7 No 3	High & Low Gain	0
21	ll ll hh hh	ADC Channel	6 & 7	FPGA	PhotoDiode K7 No 4	High & Low Gain	0
22	ll ll hh hh	ADC Channel	8 & 9	FPGA	PhotoDiode K7 No 5	High & Low Gain	0
23	ll ll hh hh	ADC Channel	10 & 11	FPGA	PhotoDiode K7 No 6	High & Low Gain	0
24	ll ll hh hh	ADC Channel	12 & 13	FPGA	PhotoDiode K7 No 7	High & Low Gain	0
25	ll ll hh hh	ADC Channel	14 & 15	FPGA	PhotoDiode K7 No 8	High & Low Gain	0
26	ll ll hh hh	ADC Channel	16 & 17	FPGA	PhotoDiode K7 No 9	High & Low Gain	0
27	ll ll hh hh	ADC Channel	18 & 19	FPGA	PhotoDiode K7 No 10	High & Low Gain	0
28	ll ll hh hh	ADC Channel	20 & 21	FPGA	PhotoMultiplier N° 0	High & Low Gain	0
29	ll ll hh hh	ADC Channel	22 & 23	FPGA	External CIS N° 0	High & Low Gain	0
30	ll ll hh hh	ADC Channel	24& 25	FPGA	Internal CIS	High & Low Gain	0
31	ll ll hh hh	ADC Channel	26 & 27	FPGA	PhotoDiode Phocal	High & Low Gain	0