Laser Frame in Acquistion Mode					
Word #	Word	Name	Origin	Meaning or comment	
0	B0 F0 00 00	Start of Frame	VME	Control Word	
1	EE 12 34 EE	Start of Header Marker	VME		
2	00 00 00 09	Header Size	VME		
3	03 01 01 00	Format Version Number	VME	Major = 3.01	Minor = 1.00
4	00 50 00 00	Source Identifier	VME	0x50 = LASCAR	
5	rr rr rr rr	Run Number	VME		
6	ee ll ll ll	Extended Event Identifier	FPGA	ee = ECRId	llllll= LIAId
7	00 00 0b bb	Bunch Identifier	FPGA	BCID	
8	00 00 00 tt	L1A Tigger Type	FPGA		
9	00 00 00 tt	Detector Event Type	VME		
10	FF 12 34 FF	Start of Fragment Marker	VME		
11	00 00 00 nn	Fragment Size	VME		
12	00 20 00 17	Sub-Fragment Id	VME		
13	00 00 00 tt	Daq Type	FPGA	Laser=20	
14	nn nn nn nn	Count	FPGA	Laser Count	
15	rr rr mm mm	Laser Intensity	FPGA	rrrr= Requested Intensity	mmmm = measured intensity
16	00 0f dd dd	Filter -Delay Laser	FPGA	f = filter	dddd = Delay Slama
17	00 00 ll ll	Linearity DAC Value	FPGA		
18	ll ll hh hh	ADC Channel 0 & 1	FPGA	PhotoDiode K7 No 1	High & Low Gain
19	ll ll hh hh	ADC Channel 2 & 3	FPGA	PhotoDiode K7 No 2	High & Low Gain
20	ll ll hh hh	ADC Channel 4 & 5	FPGA	PhotoDiode K7 No 3	High & Low Gain
21	ll ll hh hh	ADC Channel 6 & 7	FPGA	PhotoDiode K7 No 4	High & Low Gain
22	ll ll hh hh	ADC Channel 8 & 9	FPGA	PhotoDiode K7 No 5	High & Low Gain
23	ll ll hh hh	ADC Channel 10 & 11	FPGA	PhotoDiode K7 No 6	High & Low Gain
24	ll ll hh hh	ADC Channel 12 & 13	FPGA	PhotoDiode K7 No 7	High & Low Gain
25	ll ll hh hh	ADC Channel 14 & 15	FPGA	PhotoDiode K7 No 8	High & Low Gain
26	ll ll hh hh	ADC Channel 16 & 17	FPGA	PhotoDiode K7 No 9	High & Low Gain
27	ll ll hh hh	ADC Channel 18 & 19	FPGA	PhotoDiode K7 No 10	High & Low Gain
28	ll ll hh hh	ADC Channel 20 & 21	FPGA	PhotoMultiplier N° 0	High & Low Gain
29	ll ll hh hh	ADC Channel 22 & 23	FPGA	External CIS N° 0	High & Low Gain
30	ll ll hh hh	ADC Channel 24& 25	FPGA	Internal CIS	High & Low Gain
31	ll ll hh hh	ADC Channel 26 & 27	FPGA	PhotoDiode Phocal	High & Low Gain
32	ll ll hh hh	ADC Channel 28 & 29	FPGA	PhotoMultiplier N° 1	High & Low Gain
33	ll ll hh hh	ADC Channel 30 & 31	FPGA	External CIS N° 1	High & Low Gain
34	aa aa bb bb	TDC 1 & 0	FPGA	aaaa = TDC N°1	bbbb = TDC N°0
35	xx xx xx xx	Global Satus	FPGA	FPGA Global Status	
36	xx xx xx xx	DCS Time Stamp	FPGA		
37	00 00 0p pp	PhotoDiode Polarity	FPGA		
38	00 00 00 00	Free	VME		
39	xx xx xx xx	Free	VME		
40	xx xx xx xx	Free	VME		
41		Calibration Run Number	VME		
42		Calibration Type	FPGA	0 et 1=Pied, 2=Led, 3=Alpha	
43		Sum X_i channel 0	FPGA	PhotoDiode K7 No 1	
44		Sum X_i channel 1	FPGA		
45		Sum X_i^2 LSB channel 0	FPGA		
46		Sum X_i^2 MSB channel 0	FPGA		
47		Sum X_i^2 LSB channel 1	FPGA		
48		Sum X_i^2 MSB channel 1	FPGA		
49		Sum X_i channel 2	FPGA	PhotoDiode K7 No 2	
50		Sum X_i channel 3	FPGA		
51		Sum X_i^2 LSB channel 2	FPGA		
52		Sum X_i^2 MSB channel 2	FPGA		
53		Sum X_i^2 LSB channel 3	FPGA		
54		Sum X_i^2 MSB channel 3	FPGA		
55		Sum X_i channel 4	FPGA	PhotoDiode K7 No 3	
56		Sum X_i channel 5	FPGA		
57		Sum X_i^2 LSB channel 4	FPGA		
58		Sum X_i^2 MSB channel 4	FPGA		
59		Sum X_i^2 LSB channel 5	FPGA		
60		Sum X_i^2 MSB channel 5	FPGA		
61		Sum X_i channel 6	FPGA	PhotoDiode K7 No 4	
62		Sum X_i channel 7	FPGA		