32	ll ll hh hh	ADC Channel	28 & 29	FPGA	PhotoMultiplier N° 1	High & Low Gain	0
33	ll ll hh hh	ADC Channel	30 & 31	FPGA	External CIS N° 1	High & Low Gain	0
34	aa aa bb bb	TDC	1 & 0	FPGA	aaaa = TDC N°1	bbbb = TDC N°0	0
35	xx xx xx xx	Global Satus		FPGA	FPGA Global Status		0
36	xx xx xx xx	DCS Time Stamp		FPGA			0
37	00 00 0p pp	PhotoDiode Polarity		FPGA			0
38	00 00 00 00	Free		VME			0
39	xx xx xx xx	Free		VME			0
40	xx xx xx xx	Free		VME			0
41		Calibration Run Number		VME			0
42		Calibration Type		FPGA	0 et 1=Pied, 2=Led, 3=Alpha		0
43		Sum X_i channel	0	FPGA	PhotoDiode K7 No 1		0
44		Sum X_i channel	1	FPGA			0
45		Sum X_i^2 LSB channel	0	FPGA			0
46		Sum X_i^2 MSB channel	0	FPGA			0
47		Sum X_i^2 LSB channel	1	FPGA			0
48		Sum X_i^2 MSB channel	1	FPGA			0
49		Sum X_i channel	2	FPGA	PhotoDiode K7 No 2		0
50		Sum X_i channel	3	FPGA			0
51		Sum X_i^2 LSB channel	2	FPGA			0
52		Sum X_i^2 MSB channel	2	FPGA			0
53		Sum X_i^2 LSB channel	3	FPGA			0
54		Sum X_i^2 MSB channel	3	FPGA			0
55		Sum X_i channel	4	FPGA	PhotoDiode K7 No 3		0
56		Sum X_i channel	5	FPGA			0
57		Sum X_i^2 LSB channel	4	FPGA			0
58		Sum X_i^2 MSB channel	4	FPGA			0
59		Sum X_i^2 LSB channel	5	FPGA			0
60		Sum X_i^2 MSB channel	5	FPGA			0
61		Sum X_i channel	6	FPGA	PhotoDiode K7 No 4		0
62		Sum X_i channel	7	FPGA			0
63		Sum X_i^2 LSB channel	6	FPGA			0