124		Sum X <sub>i</sub> <sup>2</sup> MSB channel 26	FPGA		0
125		Sum X <sub>i</sub> <sup>2</sup> LSB channel 27	FPGA		0
126		Sum X <sub>i</sub> <sup>2</sup> MSB channel 27	FPGA		0
127		Sum X <sub>i</sub> channel 28	FPGA	PhotoMultiplier N° 1	0
128		Sum X <sub>i</sub> channel 29	FPGA		0
129		Sum X <sub>i</sub> <sup>2</sup> LSB channel 28	FPGA		0
130		Sum X <sub>i</sub> <sup>2</sup> MSB channel 28	FPGA		0
131		Sum X <sub>i</sub> <sup>2</sup> LSB channel 29	FPGA		0
132		Sum X <sub>i</sub> <sup>2</sup> MSB channel 29	FPGA		0
133		Sum X <sub>i</sub> channel 30	FPGA	External CIS N° 1	0
134		Sum X <sub>i</sub> channel 31	FPGA		0
135		Sum X <sub>i</sub> <sup>2</sup> LSB channel 30	FPGA		0
136		Sum X <sub>i</sub> <sup>2</sup> MSB channel 30	FPGA		0
137		Sum X <sub>i</sub> <sup>2</sup> LSB channel 31	FPGA		0
138		Sum X <sub>i</sub> <sup>2</sup> MSB channel 31	FPGA		0
139		Nb event	FPGA		0
140		TimeStamp	FPGA		0
141	00 00 00 00	Status Element	VME	0 = Ok	0
142	00 00 00 01	Number of status Element	VME		1
143	00 00 00 nn	Number of data Element	VME		131
144	00 00 00 01	Status Block Position	VME		1
145	E0 F0 00 00	End of Frame	VME	Control Word	0xE0F00000