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AI-generated content may be incorrect.

**ECE 274A – Digital Logic** **Spring 2025**

## **Lab Project Report**

**Project 4: Building RAM and Program Counter**

Please list below all sources consulted regarding this project

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Lab Partner Name** | **Other People** | **Printed material** | **URL (web)** | **Other** |
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Please consult the Syllabus for Collaboration Policy in the lab and UA Code of Academic Integrity for additional information regarding academic misconduct – it is your responsibility to understand what constitutes academic misconduct and to ensure that you do not commit it.

**I certify that I have listed above all the sources that I consulted regarding this project, and that I have not received nor given any assistance that is contrary to the letter or the spirit of the lab collaboration guidelines.**

**Last, First Name: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Lab Section (Mon/Tu/Thu): \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Date:** **\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**OBJECTIVE**

*Identify the main function of the RAM and PC chips used in in this project.*

**METHODOLOGY**

*(A) Logic Circuit Diagram for following Chips. Briefly explain each of the logic diagram in few sentences. Without this, no HDL or Verilog Coding will be accepted!*

1. *RAM8 - using Register(s)*
2. *RAM64 - using RAM8 chip(s)*
3. *RAM512 - using RAM64 chip(s)*
4. *PC*

*(B) Screenshot of Nand2Tetris HDL Code*

1. *RAM8*
2. *RAM64*
3. *RAM512*
4. *PC*

***[BONUS Section]***

*(C) Screenshot of Verilog Code for Program Counter (PC)*

*(D) Screenshot of Verilog Testbench for Program Counter*

*(E) Screenshot of Waveforms: both behavioral simulation and Post-Synthesis Functional Simulation*

*(F) Screenshot of RTL Schematic*

**CONCLUSIONS***You should summarize what you have learned in this project.*