# Lab 4: Area-optimized Multiplier and Handshake Protocol Design on Datapath

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## 1. Diagram

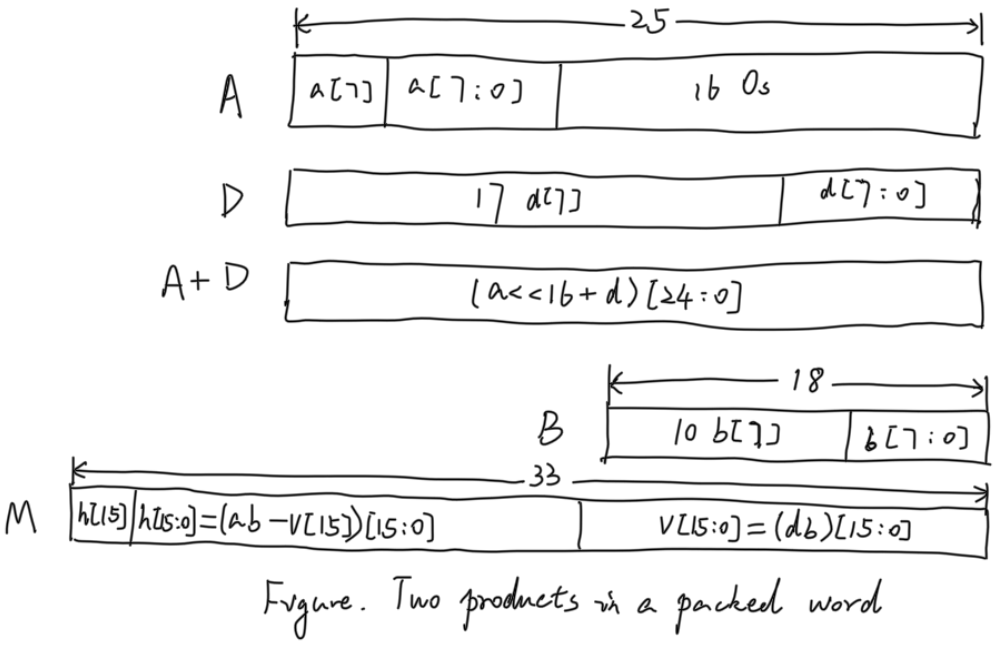



Figure. Two products in a packed word

## 2. Tables

### a) Resources

i. Slice Logic

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Slice LUTs | 5 | 0 | 20800 | 0.02 |
| LUT as Logic | 5 | 0 | 20800 | 0.02 |
| LUT as Memory | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 35 | 0 | 41600 | 0.08 |
| Register as Flip Flop | 35 | 0 | 41600 | 0.08 |
| Register as Latch | 0 | 0 | 41600 | 0.00 |
| F7 Muxes | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 8150 | 0.00 |

ii. DSP

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| DSPs | 1 | 0 | 90 | 1.11 |
| DSP48E1 only | 1 | | | |

iii. IO and GT Specific

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Bonded IOB | 62 | 0 | 106 | 58.49 |
| IOB Master Pads | 30 | | | |
| IOB Slave Pads | 31 | | | |
| Bonded IPADs | 0 | 0 | 10 | 0.00 |
| Bonded OPADs | 0 | 0 | 4 | 0.00 |
| PHY_CONTROL | 0 | 0 | 5 | 0.00 |
| PHASER_REF | 0 | 0 | 5 | 0.00 |
| OUT_FIFO | 0 | 0 | 20 | 0.00 |
| IN_FIFO | 0 | 0 | 20 | 0.00 |
| IDELAYCTRL | 0 | 0 | 5 | 0.00 |
| IBUFDS | 0 | 0 | 104 | 0.00 |
| GTPE2_CHANNEL | 0 | 0 | 2 | 0.00 |
| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 20 | 0.00 |
| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 20 | 0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 250 | 0.00 |
| IBUFDS_GTE2 | 0 | 0 | 2 | 0.00 |
| ILOGIC | 0 | 0 | 106 | 0.00 |
| OLOGIC | 0 | 0 | 106 | 0.00 |

iv. Primitives

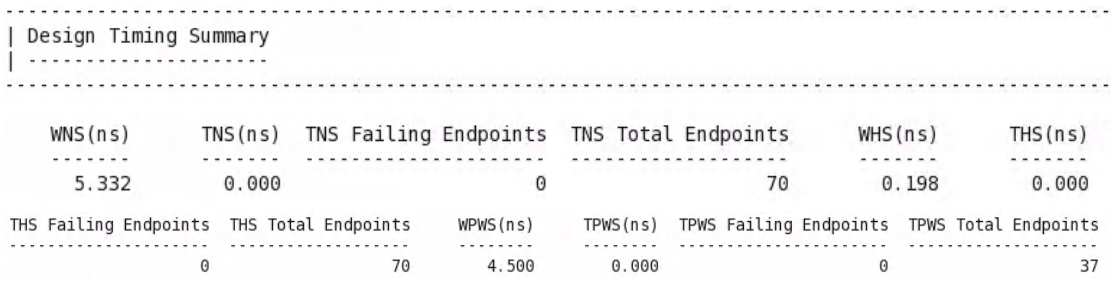
| Ref Name | Used | Functional Category |
|---|---|---|
| FDRE | 35 | Flop & Latch |
| OBUF | 34 | IO |
| IBUF | 28 | IO |
| CARRY4 | 4 | CarryLogic |
| LUT4 | 2 | LUT |
| LUT2 | 2 | LUT |
| LUT5 | 1 | LUT |
| LUT3 | 1 | LUT |
| DSP48E1 | 1 | Block Arithmetic |
| BUFG | 1 | Clock |

**b) Power**

| | |
|---|---|
| Total On-Chip Power (W) | 0.091 |
| Dynamic (W) | 0.021 |
| Device Static (W) | 0.070 |
| Effective TJA (C/W) | 5.0 |
| Max Ambient (C) | 84.5 |
| Junction Temperature (C) | 25.5 |
| Confidence Level | Low |
| Setting File | --- |
| Simulation Activity File | --- |
| Design Nets Matched | NA |

Dynamic: 0.021W Static: 0.070W

**c) Worst Negative Slack**



Design Timing Summary

| WNS(ns) | TNS(ns) | TNS Failing Endpoints | TNS Total Endpoints | WHS(ns) | THS(ns) |
|---|---|---|---|---|---|
| 5.332 | 0.000 | 0 | 70 | 0.198 | 0.000 |

| THS Failing Endpoints | THS Total Endpoints | WPWS(ns) | TPWS(ns) | TPWS Failing Endpoints | TPWS Total Endpoints |
|---|---|---|---|---|---|
| 0 | 70 | 4.500 | 0.000 | 0 | 37 |

## 3. Answer the question

Why don't we immediately stall the current stage if the next stage is stalled but instead take into consideration of the valid signal? Use scenarios to explain your thought. (Answer should not exceed 6 sentences)

We assume the scenario of counter-example as following. If the valid signal from current stage is 0, the data in current stage that is not useful and valid should be thrown away. Thus, if we do not take the valid signal into consideration, then there may be some junk data held in the producer, which results in a wasteful use of resources. If we take the valid signal into consideration, then there is only valid data kept by the producer, which is a more reasonable design.