# Lab 6: Distributed Arithmetic

Name: Peng Guo
GTID: 903424176

## 1. Tables

### a) Resources

*i. Slice Logic*

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Slice LUTs | 39 | 0 | 20800 | 0.19 |
| LUT as Logic | 39 | 0 | 20800 | 0.19 |
| LUT as Memory | 0 | 0 | 9600 | 0.00 |
| Slice Registers | 18 | 0 | 41600 | 0.04 |
| Register as Flip Flop | 18 | 0 | 41600 | 0.04 |
| Register as Latch | 0 | 0 | 41600 | 0.00 |
| F7 Muxes | 0 | 0 | 16300 | 0.00 |
| F8 Muxes | 0 | 0 | 8150 | 0.00 |

*ii. IO and GT Specific*

| Site Type | Used | Fixed | Available | Util% |
|---|---|---|---|---|
| Bonded IOB | 31 | 0 | 106 | 29.25 |
| IOB Master Pads | 15 | | | |
| IOB Slave Pads | 15 | | | |
| Bonded IPADs | 0 | 0 | 10 | 0.00 |
| Bonded OPADs | 0 | 0 | 4 | 0.00 |
| PHY_CONTROL | 0 | 0 | 5 | 0.00 |
| PHASER_REF | 0 | 0 | 5 | 0.00 |
| OUT_FIFO | 0 | 0 | 20 | 0.00 |
| IN_FIFO | 0 | 0 | 20 | 0.00 |
| IDELAYCTRL | 0 | 0 | 5 | 0.00 |
| IBUFDS | 0 | 0 | 104 | 0.00 |
| GTPE2_CHANNEL | 0 | 0 | 2 | 0.00 |
| PHASER_OUT/PHASER_OUT_PHY | 0 | 0 | 20 | 0.00 |
| PHASER_IN/PHASER_IN_PHY | 0 | 0 | 20 | 0.00 |
| IDELAYE2/IDELAYE2_FINEDELAY | 0 | 0 | 250 | 0.00 |
| IBUFDS_GTE2 | 0 | 0 | 2 | 0.00 |
| ILOGIC | 0 | 0 | 106 | 0.00 |
| OLOGIC | 0 | 0 | 106 | 0.00 |

*iii.* *Primitives*

| Ref Name | Used | Functional Category |
|---|---|---|
| IBUF | 19 | IO |
| FDRE | 18 | Flop & Latch |
| LUT5 | 16 | LUT |
| OBUF | 12 | IO |
| LUT4 | 10 | LUT |
| LUT6 | 8 | LUT |
| LUT3 | 8 | LUT |
| CARRY4 | 4 | CarryLogic |
| LUT2 | 2 | LUT |
| LUT1 | 2 | LUT |
| BUFG | 1 | Clock |

**b) Power**

| | |
|---|---|
| Total On-Chip Power (W) | 0.080 |
| Dynamic (W) | 0.010 |
| Device Static (W) | 0.070 |
| Effective TJA (C/W) | 5.0 |
| Max Ambient (C) | 84.6 |
| Junction Temperature (C) | 25.4 |
| Confidence Level | Low |
| Setting File | --- |
| Simulation Activity File | --- |
| Design Nets Matched | NA |

Dynamic: 0.010W Static: 0.070W

**c) Worst Negative Slack**

| Design Timing Summary

| WNS(ns) | TNS(ns) | TNS Failing Endpoints | TNS Total Endpoints | WHS(ns) | THS(ns) |
|---|---|---|---|---|---|
| 5.844 | 0.000 | 0 | 20 | 0.157 | 0.000 |

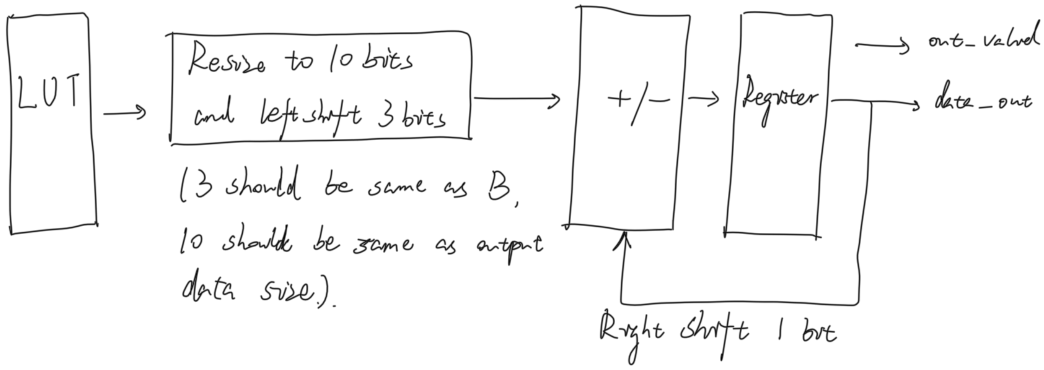
| THS Failing Endpoints | THS Total Endpoints | WPWS(ns) | TPWS(ns) | TPWS Failing Endpoints | TPWS Total Endpoints |
|---|---|---|---|---|---|
| 0 | 20 | 4.500 | 0.000 | 0 | 19 |

## 2. Questions and Answers

Is there an area-efficient way to do the left-shift which is after the output of LUT?

Yes.

**a) If yes, draw the updated block diagram starting from the LUT on the left to the output data_out on the right.**




**b) Write down the mathematical recurrence relation induced from Eq. 3 that proves your thought above.**

$$y = -2^B \left( \sum_{n=0}^{N-1} c[n] \times x_B[n] \right) + \sum_{b=0}^{B-1} 2^b \left( \sum_{n=0}^{N-1} c[n] \times x_b[n] \right)$$

$$= -2^B \left( \sum_{n=0}^{N-1} c[n] \times x_B[n] \right) + \sum_{b=0}^{B-1} 2^{b-B} \left( \left( \sum_{n=0}^{N-1} c[n] \times x_b[n] \right) \times 2^B \right)$$

If we denote $\sum_{n=0}^{N-1} c[n] \times x_b[n] = r_b$, we set $B=3$ as an example.

$$y = -2^B \cdot r_3 + \sum_{b=0}^{2} 2^{b-3} r_b \times 2^3$$

$$= -2^B \times r_3 + 2^{-3} \times r_0 \times 2^3 + 2^{-2} \times r_1 \times 2^3 + 2^{-1} \times r_2 \times 2^3$$

$$= \left( \left( r_0 \times 2^3 \times 2^{-1} + r_1 \times 2^3 \right) \times 2^{-1} + r_2 \times 2^3 \right) \times 2^{-1} + r_3 \times 2^3$$

And that's how my code accomplish the calculation.

**c) Why the original left-shift is not a good idea and why the updated one is area-efficient? (Answer should not exceed 4 sentences)**

Because the original left-shift requires different shift bits, which requires different shift registers with more area to do it. As for the updated one, it uses the same bits shift, so it is area-efficient.