GEORGIA INSTITUTE OF TECHNOLOGY

School of Electrical and Computer Engineering

ECE-6276-A DSP Hardware System Design (Fall 2018)

Lab 1: Introduction to ModelSim and Vivado with the Design of Barrel Shifter

Assigned Date: Wednesday, August 29, 2018

Due Date : 23:55, Thursday, September 6, 2018

1 Introduction

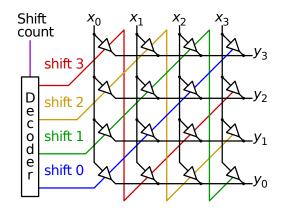


Figure 1 Schematic of a 4-bit crossbar barrel shifter. (Source: https://en.wikipedia.org/wiki/File:Crossbar_barrel_shifter.svg)

The purpose of this lab is to get acquainted with the Mentor Graphics ModeSim and Xilinx Vivado toolchain through a Simple Design. A *barrel shifter* is a digital circuit that can shift a data word by a specified number of bits. For more information, refer https://en.wikipedia.org/wiki/Barrel_shifter. In this lab, we will be designing a 16-bit left-shift barrel shifter with a control word of bit-width 4.

2 Instructions

1. Simulate the design in ModelSim (instructions are given in the document *ece6276_lab1_instructions.pdf*). You will find that the first two test cases are correct and the rest are incorrect because the design is not complete.

- 2. Complete the design barrel shifter.vhd.
- 3. Simulate the design in ModelSim again.
- 4. Also, write three test cases in the testbench corresponding to your gtID. If your gtID is 123456789, the 3 test cases are:
 - (a) input => 16'h0102 (16'b0000_0001_0000_0010), ctrl => 4'h3 (4'b0011)
 - (b) input => 16'h0405 (16'b0000 0100 0000 0101), ctrl => 4'h6 (4'b0110)
 - (c) input => 16'h0708 (16'b0000 0111 0000 1000), ctrl => 4'h9 (4'b1001)

These 3 test-cases should be added after any of the already defined test cases (Instructions are given as comments in the testbench).

- 5. Take a screenshot of your waveform (including the pre-defined test cases and your own). While taking the screenshot of the ECE Linux screen, make sure that your name is visible in the top right corner of the screen.
- 6. Compare the obtained results (only for the 3 gtID test cases) with your manual answer.
- 7. Synthesize this barrel shifter in Vivado (instructions are given in the document *ece6276_lab1_instructions.pdf*) and study the implemented area (utilization) and power reports, namely,

```
barrel_shifter_utilization_placed.rpt
barrel_shifter_power_routed.rpt
```

3 Deliverables

- 1. Create a PDF report containing:
 - Screenshot of the simulated waveform.
 - Manual verification of the 3 gtID test cases (Just simple reasoning is enough).
 - Tables of
 - (a) Resources (Only "Slice Logic", "IO and GT Specific", "Primitives") from barrel_shifter_utilization_placed.rpt
 - (b) Power (Dynamic and Static) from barrel_shifter_power_routed.rpt
 - Answer the question: Is the verification strategy used in the current testbench the best strategy? If not, what are the other strategies that could be used and what are their pros and cons? Answer should not exceed 3-4 sentences.
 - (extra points) Answer the question: When we do synthesis and implementation, we will usually add a constraint file in the Vivado specifying the clock period, e.g.

```
create_clock -period 25.000 -name clk_pin_p -waveform {0.000 12.500} [get_ports clk]
```

Why don't we need to specify this in this lab? In what condition will this specification be meaningful? Answer should not exceed 3-4 sentences.

The name of the PDF should be of the form lab1_firstname_lastname.pdf, e.g. lab1_george_burdell.pdf.

- 2. The completed design file barrel shifter.vhd.
- 3. The simulated output file output .txt in the "run" folder.
- 4. The implemented area (utilization) and power reports, namely, barrel_shifter_utilization_placed.rpt barrel_shifter_power_routed.rpt

Move all of these files into a folder called lab1_firstname_lastname_gtID. Zip the folder and upload the archive lab1_firstname_lastname_gtID.zip on T-Square (eg. lab1_george_burdell_123456789.zip). Please strictly follow this naming convention. Otherwise my script will not work and you might get points deduction.

Note: Late submissions are not accepted. In case of extraordinary circumstances, written permission must be obtained from Dr. Madisetti.