Lab 3: Multiplier Design

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1. Tables

a) Resources

i. Slice Logic

✓ From multiplier_utilization_placed.rpt

Site Type	Used	Fixed	Available	Util%
Slice LUTs	122	0	20800	0.59
LUT as Logic	122	0	20800	0.59
LUT as Memory	0	0	9600	0.00
Slice Registers	58	0	41600	0.14
Register as Flip Flop	58	0	41600	0.14
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

✓ From multiplier_updated_utilization_placed.rpt

Site Type	Used	Fixed	Available	Util%
Slice LUTs	54	0	20800	0.26
LUT as Logic	54	0	20800	0.26
LUT as Memory	0	0	9600	0.00
Slice Registers	56	0	41600	0.13
Register as Flip Flop	56	0	41600	0.13
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

ii. DSP

✓ From multiplier_utilization_placed.rpt

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	90	0.00

✓ From multiplier_updated_utilization_placed.rpt

Site Type	Used	Fixed	Available	Util%
DSPs	1	0	90	1.11
DSP48E1 only	1			

iii. IO and GT Specific

✓ From multiplier_utilization_placed.rpt

Site Type	Used	Fixed	Available	Util%
Bonded IOB	60	0	106	56.60
IOB Master Pads	29			
IOB Slave Pads	30			
Bonded IPADs	0	0	10	0.00
Bonded OPADs	0	0	4	0.00
PHY_CONTROL	0	0	5	0.00
PHASER_REF	0	0	5	0.00
OUT_FIFO	0	0	20	0.00
IN_FIFO	0	0	20	0.00
IDELAYCTRL	0	0	5	0.00
IBUFDS	0	0	104	0.00
GTPE2_CHANNEL	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	250	0.00
IBUFDS_GTE2	0	0	2	0.00
ILOGIC	0	0	106	0.00
OLOGIC	0	0	106	0.00

✓ From multiplier_updated_utilization_placed.rpt

Site Type	Used	Fixed	Available	Util%
Bonded IOB	60	0	106	56.60
IOB Master Pads	29			
IOB Slave Pads	29			
Bonded IPADs	0	0	10	0.00
Bonded OPADs	0	0	4	0.00
PHY_CONTROL	0	0	5	0.00
PHASER_REF	0	0	5	0.00
OUT_FIFO	0	0	20	0.00
IN_FIFO	0	0	20	0.00
IDELAYCTRL	0	0	5	0.00
IBUFDS	0	0	104	0.00
GTPE2_CHANNEL	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	250	0.00
IBUFDS_GTE2	0	0	2	0.00
ILOGIC	0	0	106	0.00
OLOGIC	0	0	106	0.00

iv. Primitives

✓ From multiplier_utilization_placed.rpt

Ref Name	Used	Functional Category
FDRE	58	Flop & Latch
LUT6	52	LUT
LUT4	50	LUT
LUT2	48	LUT
OBUF	33	IO
IBUF	27	IO
CARRY4	26	CarryLogic
LUT5	12	LUT
LUT3	12	LUT
BUFG	1	Clock

✓ From multiplier_updated_utilization_placed.rpt

Ref Name	Used	Functional Category
FDRE	56	Flop & Latch
OBUF	33	IO
IBUF	27	IO
LUT1	23	LUT
LUT2	18	LUT
CARRY4	13	CarryLogic
LUT6	11	LUT
LUT4	3	LUT
LUT5	2	LUT
DSP48E1	1	Block Arithmetic
BUFG	1	Clock

b) Power

✓ From multiplier_power_placed.rpt
Dynamic: 0.03W
Static: 0.1 – 0.03 = 0.07W

Total On-Chip Power (W)	0.100
Dynamic (W)	0.030
Device Static (W)	0.070
Effective TJA (C/W)	5.0
Max Ambient (C)	84.5
Junction Temperature (C)	25.5
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

✓ From multiplier_updated_power_placed.rpt
Dynamic: 0.033W
Static: 0.07W

Total On-Chip Power (W)	0.103
Dynamic (W)	0.033
Device Static (W)	0.070
Effective TJA (C/W)	5.0
Max Ambient (C)	84.5
Junction Temperature (C)	25.5
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

c) Worst Negative Slack

✓ From multiplier_timing_summary.rpt

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)
2.998	0.000	0	33	0.245	0.000

✓ From multiplier_updated_timing_summary.rpt

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)
4.350	0.000	0	44	0.181	0.000

2. Answers

a) Compare the tables above and briefly explain the difference between two designs. (Answer should not exceed 4 sentences)
Compared with the original design, the updated one uses DSP and fewer LUTs, consumes a little bit more power, and has larger worst negative slack.

b) What is the advantage of using DSP instead of LUTs on FPGA? (Answer should not exceed 4 sentences)
The DSP has multiplication operation unit, also called mac unit, it can finish a multiplication and addition in a cycle. Also, the operation speed is quicker and the wasted resources is less.