Lab2: Sequence Detector

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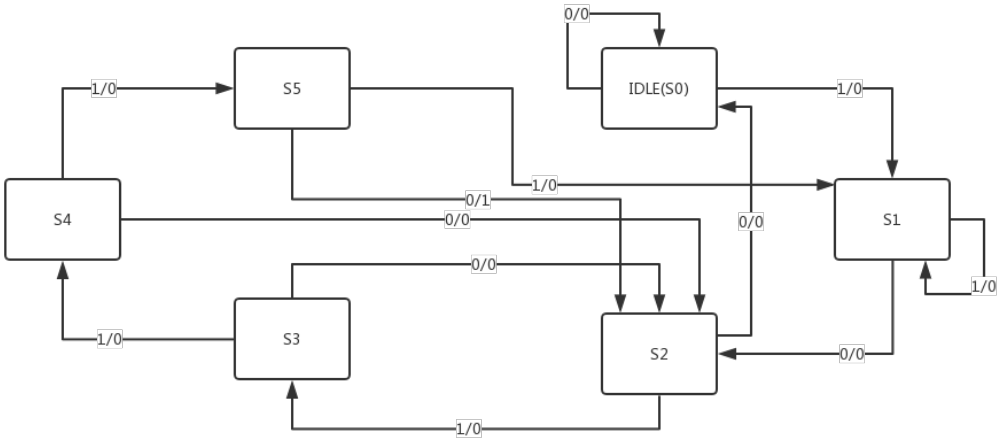
1. State machine diagram of the design for detecting “101110”



2. Tables

a) Resources

- Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	5	0	20800	0.02
LUT as Logic	5	0	20800	0.02
LUT as Memory	0	0	9600	0.00
Slice Registers	6	0	41600	0.01
Register as Flip Flop	3	0	41600	<0.01
Register as Latch	3	0	41600	<0.01
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

- IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	4	0	106	3.77
IOB Master Pads	2			
IOB Slave Pads	1			
Bonded IPADs	0	0	10	0.00
Bonded OPADs	0	0	4	0.00
PHY_CONTROL	0	0	5	0.00
PHASER_REF	0	0	5	0.00
OUT_FIFO	0	0	20	0.00
IN_FIFO	0	0	20	0.00
IDELAYCTRL	0	0	5	0.00
IBUFDS	0	0	104	0.00
GTPE2_CHANNEL	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	250	0.00
IBUFDS_GTE2	0	0	2	0.00
ILOGIC	0	0	106	0.00
OLOGIC	0	0	106	0.00

- Primitives

Ref Name	Used	Functional Category
LUT4	3	LUT
LDCE	3	Flop & Latch
IBUF	3	IO
FDCE	3	Flop & Latch
OBUF	1	IO
LUT3	1	LUT
LUT2	1	LUT
BUFG	1	Clock

b) Power

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	<0.001	3	---	---
Slice Logic	<0.001	14	---	---
LUT as Logic	<0.001	5	20800	0.02
Register	0.000	6	41600	0.01
Others	0.000	3	---	---
Signals	<0.001	13	---	---
I/O	<0.001	4	106	3.77
Static Power	0.068			
Total	0.069			

Total On-Chip Power (W)	0.069
Dynamic (W)	0.000
Device Static (W)	0.068
Effective TJA (C/W)	5.0
Max Ambient (C)	84.7
Junction Temperature (C)	25.3
Confidence Level	Low
Setting File	---
Simulation Activity File	---
Design Nets Matched	NA

Dynamic: 0.000W
Static: 0.068W

c) Worst Negative Slack

Design Timing Summary

WNS(ns)	TNS(ns)	TNS Failing Endpoints	TNS Total Endpoints	WHS(ns)	THS(ns)
NA	NA	NA	NA	NA	NA

THS Failing Endpoints	THS Total Endpoints	WPWS(ns)	TPWS(ns)	TPWS Failing Endpoints	TPWS Total Endpoints
NA	NA	12.000	0.000	0	4

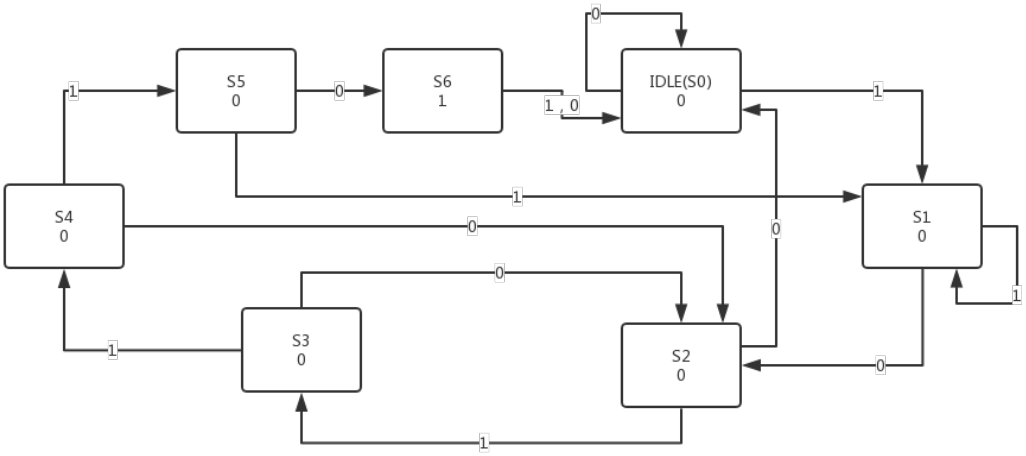
All user specified timing constraints are met.

3. Questions & Answers

a) What kind of state machine is your design? What's the name of the other type of state machine?
I use Mealy FSM in my design. The other type of state machine is Moore FSM.

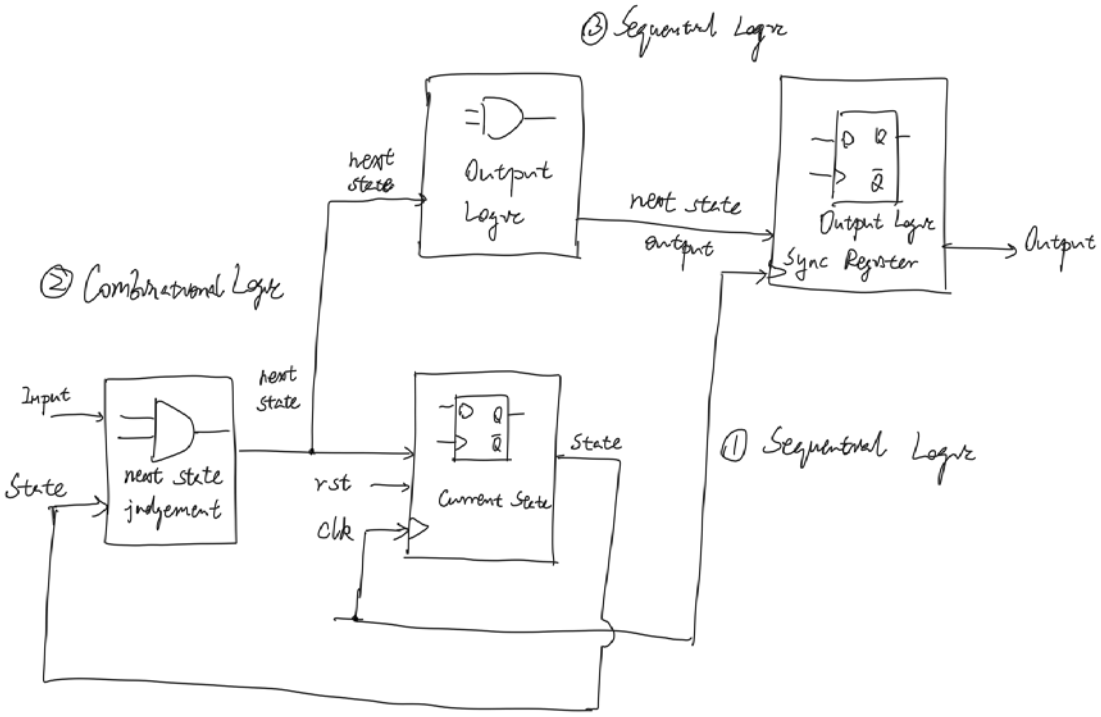
b) What are the pros and cons of these two types of state machines considering the timing and flexibility?
For Moore FSM, the effect of the input on the output will not be reflected until the next clock cycle. For Mealy FSM, since the output is directly affected by the input, and the input can be changed at any time during the clock cycle. Thus, the changed output of the Mealy FSM arrives one cycle ahead of the changed output of the Moore FSM. Compared with Mealy FSM, the Moore FSM has better timing with clock synchronization. However, with Mealy FSM, the output responds quickly to the input and the circuit structure is simpler.

c) Draw the other type of state machine for overlapped "101110" sequence detector.



d) <u>Is there any other simpler way to detect the overlapped “101110” sequence? If yes, draw the corresponding block diagram. Briefly explain the disadvantage of this method.</u>

Yes.



With this method, the circuit design is more complicated. And the output responds slower by one clock cycle to the input compared with the design in this lab.