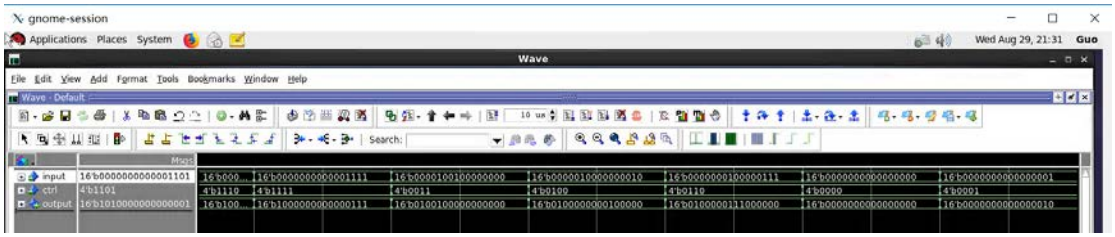
Lab Report 1

Name: Peng Guo
GTID#903424176

1. Screenshot of the simulated waveform



2. Manual verification of the 3 gtID test cases

Answer:

The barrel shifter is a multi-input, single output circuit. For input signal *input[15:0]*, the shifter determines how many bits to shift to the left based on the signal *ctrl[3:0]*, and then output the result *output[15:0]*.

For test cases with GTID 903424176, three group input and control signals are as follows.

(a) input1 => 16'h0900 (16'b0000_1001_0000_0000), ctrl1 => 4'h3 (4'b0011)

(b) input2 => 16'h0402 (16'b0000_0100_0000_0010), ctrl2 => 4'h4 (4'b0100)

(c) input3 => 16'h0107 (16'b0000_0001_0000_0111), ctrl3 => 4'hb (4'b0110)

As mentioned above, three bits of input1 should be shifted to the left. Four bits of input2 should be shifted to the left. Six bits of input3 should be shifted to the left.

Thus, the output should be as following.

(a) output1 => 16'h4800 (16'b0100_1000_0000_0000)

(b) output2 => 16'h4020 (16'b0100_0000_0010_0000)

(c) output3 => 16'h41C0 (16'b0100_0001_1100_0000)

Therefore, the outputs calculated correspond with the result obtained from the simulation.

3. Tables of Resources and Power

- Resources
  - Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice	9	0	8150	0.11
SLICEL	9	0		
SLICEM	0	0		
LUT as Logic	32	0	20800	0.15
using O5 output only	0			
using O6 output only	32			
using O5 and O6	0			
LUT as Memory	0	0	9600	0.00
LUT as Distributed RAM	0	0		
LUT as Shift Register	0	0		
LUT Flip Flop Pairs	0	0	20800	0.00
Unique Control Sets	0			

  - IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	36	0	106	33.96
IOB Master Pads	17			
IOB Slave Pads	18			
Bonded IPADs	0	0	10	0.00
Bonded OPADs	0	0	4	0.00
PHY_CONTROL	0	0	5	0.00
PHASER_REF	0	0	5	0.00
OUT_FIFO	0	0	20	0.00
IN_FIFO	0	0	20	0.00
IDELAYCTRL	0	0	5	0.00
IBUFDS	0	0	104	0.00
GTPE2_CHANNEL	0	0	2	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	20	0.00
PHASER_IN/PHASER_IN_PHY	0	0	20	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	250	0.00
IBUFDS_GTE2	0	0	2	0.00
ILOGIC	0	0	106	0.00
OLOGIC	0	0	106	0.00

  - Primitives

Ref Name	Used	Functional Category
LUT6	32	LUT
IBUF	20	IO
OBUF	16	IO

- Power

Dynamic (W)	9.142
Static (W)	0.128

4. Question & Answer

Is the verification strategy used in the current testbench the best strategy? If not, what are the other strategies that could be used and what are their pros and cons?

Answer:

The verification strategy used in the current testbench is not the best strategy. The core of designing test cases is to use less cases to cover more conditions, thus to save the resources and perfect the design. In fact, we can test all the cases, but it is not worth to do so because of an increasing investment with a decreasing profit. We can improve the testbench with boundary test, anomaly test, and random test.

5. Extra Questions

When we do synthesis and implementation, we will usually add a constraint file in the Vivado specifying the clock period.

Why don't we need to specify this in this lab? In what condition will this specification be meaningful?

Answer:

We need constraints for porting the Logic onto the FPGA for hardware level application, but we are not doing that in this Lab. Also, for this lab we do not have a clock (combinational design), so constraints will not be needed.