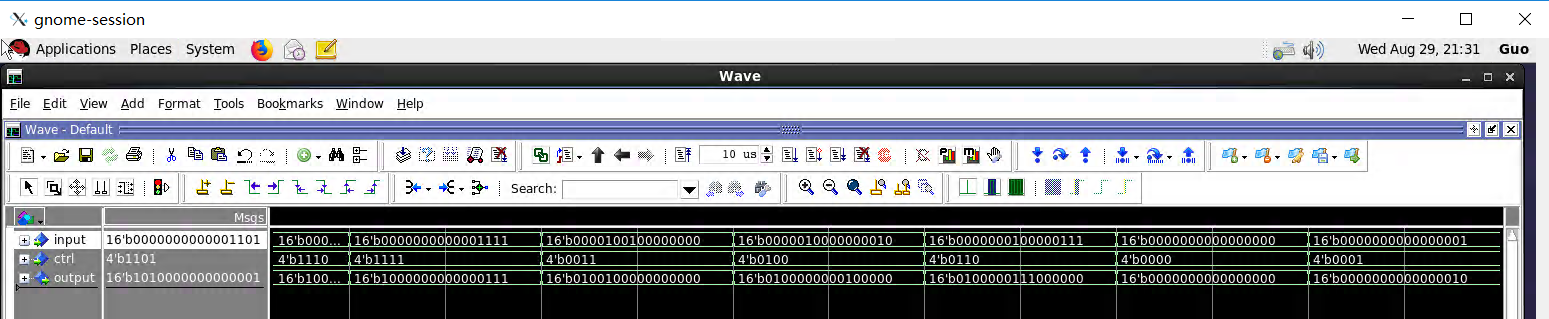
**Lab Report 1**

Name: Peng Guo

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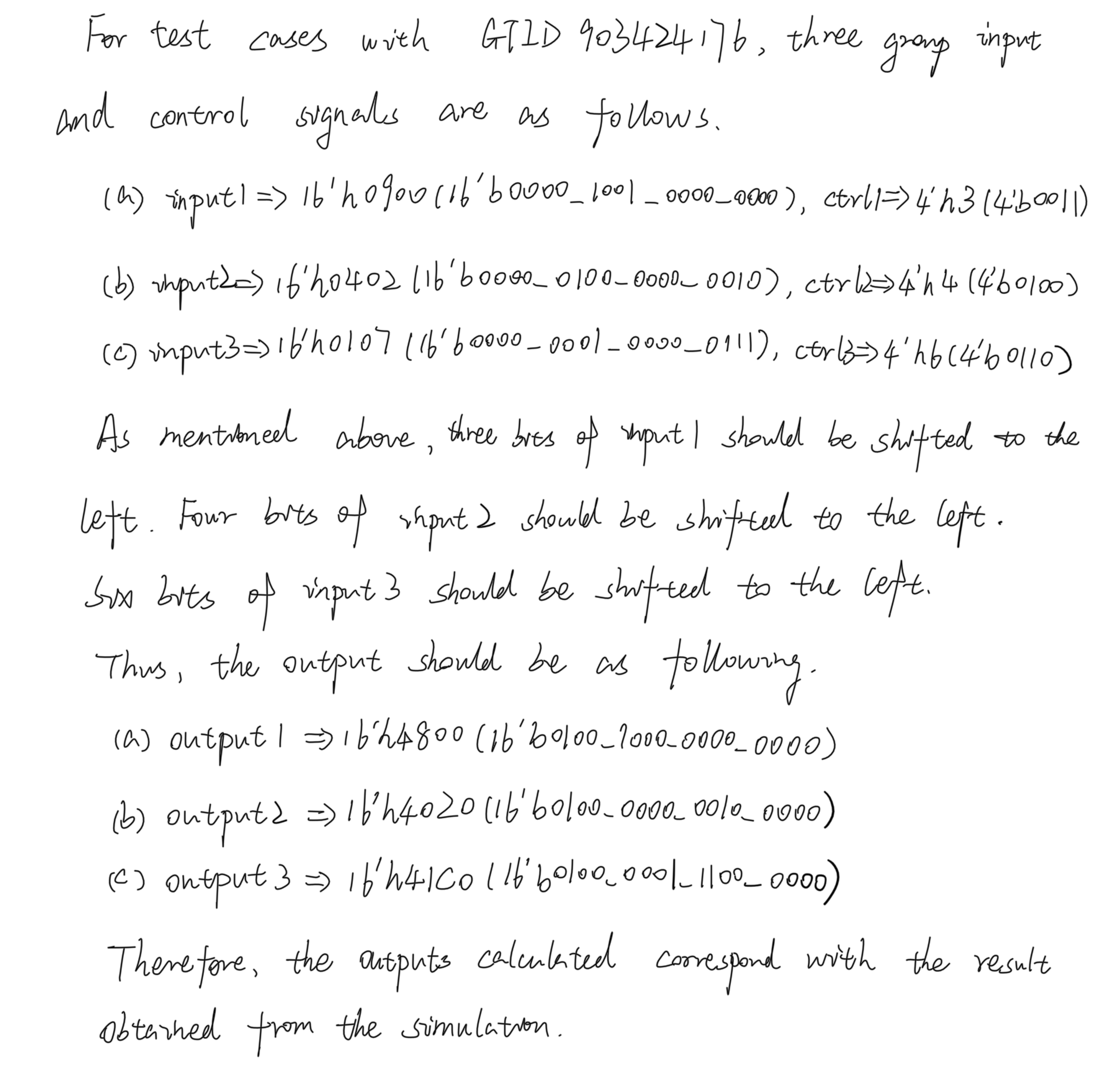
1. **Screenshot of the simulated waveform**



1. **Manual verification of the 3 gtID test cases**

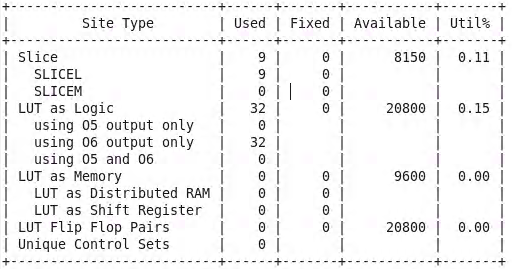
Answer:

The barrel shifter is a multi-input, single output circuit. For input signal *input[15:0]*, the shifter determines how many bits to shift to the left based on the signal *ctrl[3:0]*, and then output the result *output[15:0]*.

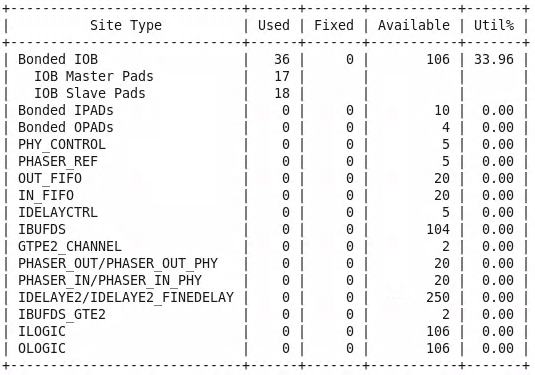


1. **Tables of Resources and Power**

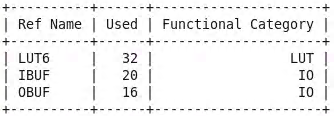
* Resources
  + Slice Logic



* + IO and GT Specific



* + Primitives



* Power

|  |  |
| --- | --- |
| Dynamic (W) | 9.142 |
| Static (W) | 0.128 |

1. **Question & Answer**

Is the veriﬁcation strategy used in the current testbench the best strategy? If not, what are the other strategies that could be used and what are their pros and cons?

Answer:

The veriﬁcation strategy used in the current testbench is not the best strategy. The core of designing test cases is to use less cases to cover more conditions, thus to save the resources and perfect the design. In fact, we can test all the cases, but it is not worth to do so because of an increasing investment with a decreasing profit. We can improve the testbench with boundary test, anomaly test, and random test.

1. **Extra Questions**

When we do synthesis and implementation, we will usually add a constraint ﬁle in the Vivado specifying the clock period.

Why don’t we need to specify this in this lab? In what condition will this speciﬁcation be meaningful?

Answer:

We need constraints for porting the Logic onto the FPGA for hardware level application, but we are not doing that in this Lab. Also, for this lab we do not have a clock (combinational design), so constraints will not be needed.