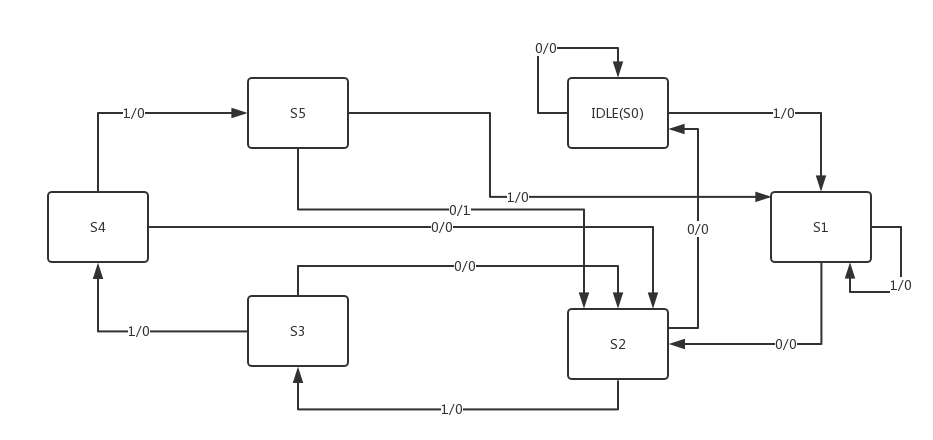
**Lab2: Sequence Detector**

Name: Peng Guo

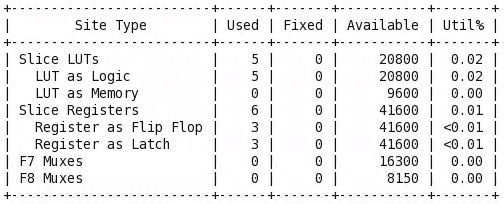
GTID: 903424176

1. **State machine diagram of the design for detecting “101110”**

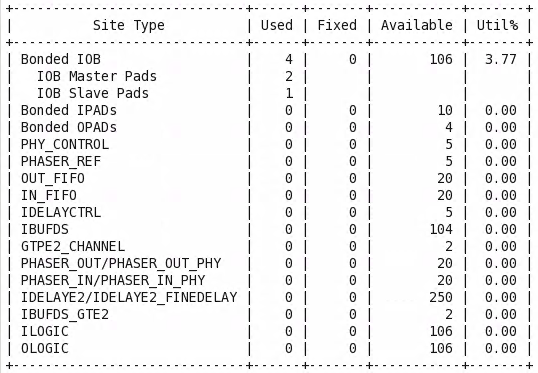


1. **Tables**
   1. **Resources**

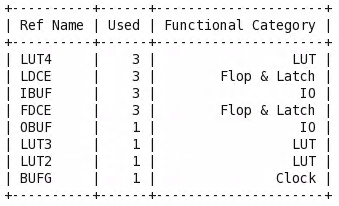
* Slice Logic



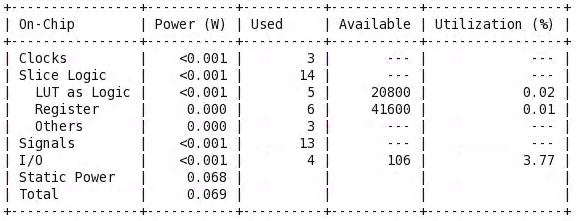
* IO and GT Specific

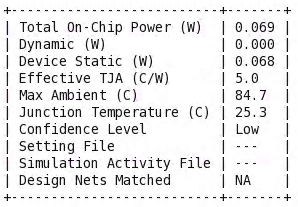


* Primitives



* 1. **Power**

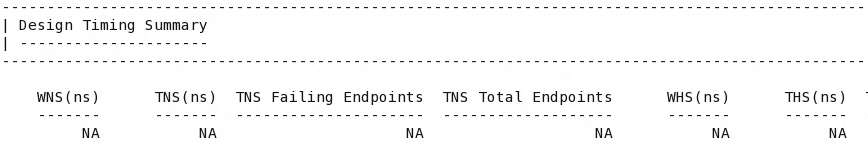


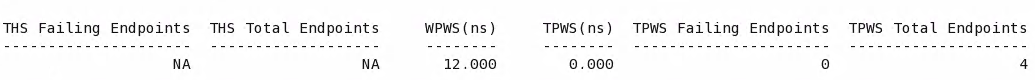


Dynamic: 0.000W

Static: 0.068W

* 1. **Worst Negative Slack**





All user specified timing constraints are met.

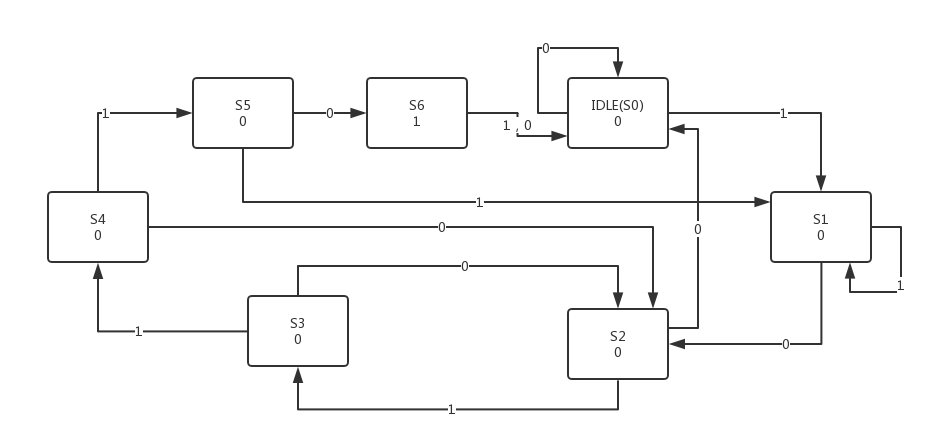
1. **Questions & Answers**
   1. What kind of state machine is your design? What’s the name of the other type of state machine?

I use Mealy FSM in my design. The other type of state machine is Moore FSM.

* 1. What are the pros and cons of these two types of state machines considering the timing and flexibility?

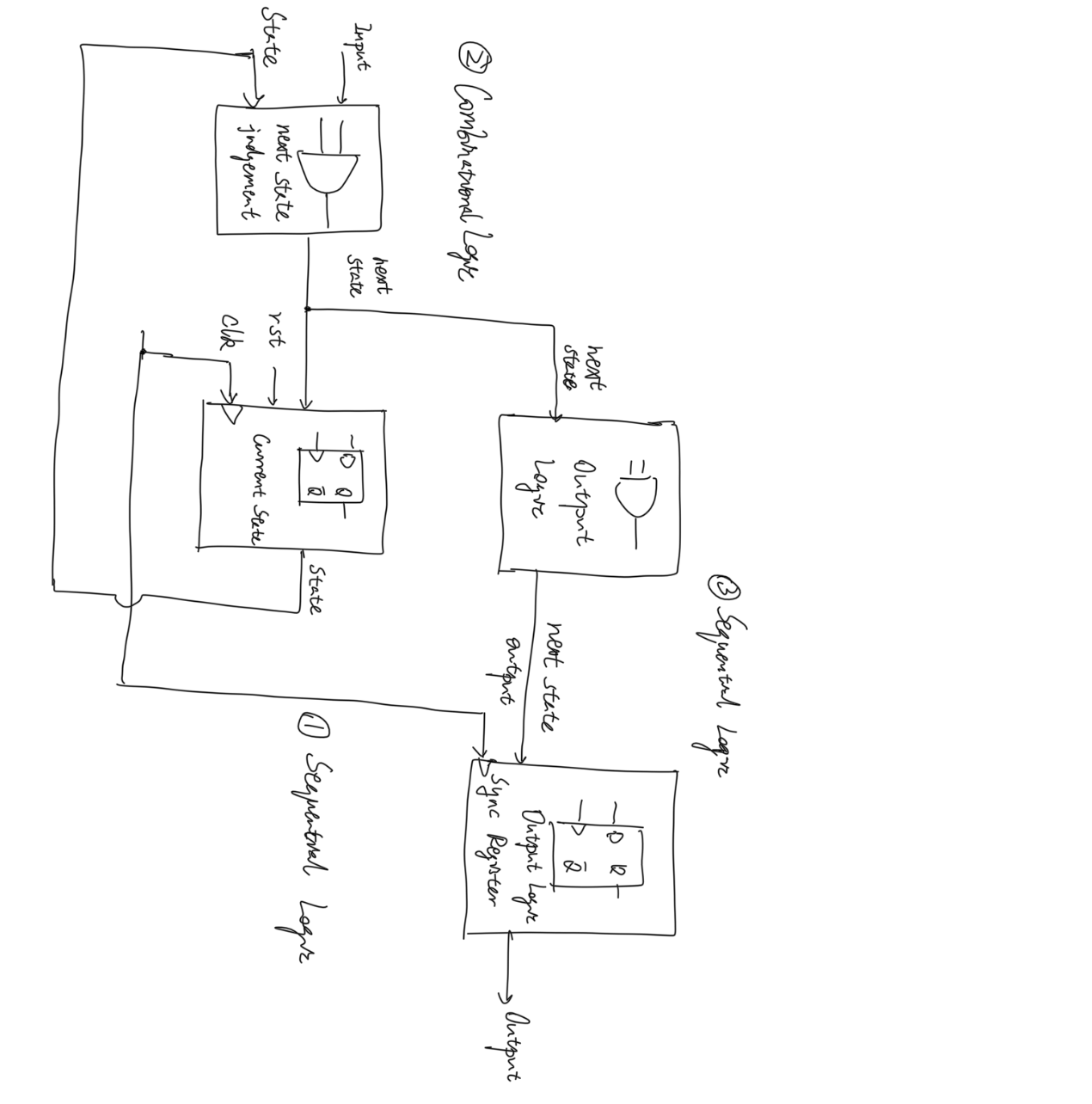
For Moore FSM, the effect of the input on the output will not be reflected until the next clock cycle. For Mealy FSM, since the output is directly affected by the input, and the input can be changed at any time during the clock cycle. Thus, the changed output of the Mealy FSM arrives one cycle ahead of the changed output of the Moore FSM. Compared with Mealy FSM, the Moore FSM has better timing with clock synchronization. However, with Mealy FSM, the output responds quickly to the input and the circuit structure is simpler.

* 1. Draw the other type of state machine for overlapped “101110” sequence detector.



* 1. Is there any other simpler way to detect the overlapped “101110” sequence? If yes, draw the corresponding block diagram. Briefly explain the disadvantage of this method.

Yes.



With this method, the circuit design is more complicated. And the output responds slower by one clock cycle to the input compared with the design in this lab.