



Senior 3D-DRAM

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☰ Class	DRAM Controller

Table 2: Addressing

Parameter	512 Meg x 4	256 Meg x 8	128 Meg x 16
Configuration	64 Meg x 4 x 8 banks	32 Meg x 8 x 8 banks	16 Meg x 16 x 8 banks
Refresh count	8K	8K	8K
Row addressing	32K (A[14:0])	32K (A[14:0])	16K (A[13:0])
Bank addressing	8 (BA[2:0])	8 (BA[2:0])	8 (BA[2:0])
Column addressing	2K (A[11, 9:0])	1K (A[9:0])	1K (A[9:0])
Page size	1KB	1KB	2KB

Basic spec and modification to DDR3

- This is modified from 256Meg x 8

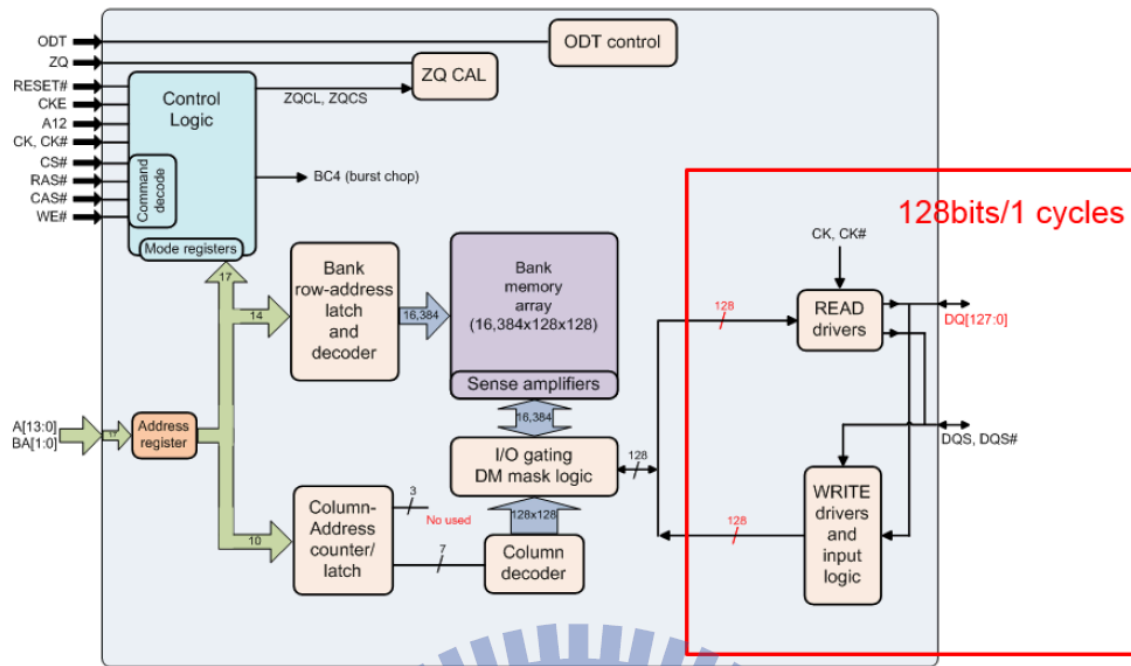


Figure 3.8 Rearrangement of I/O pin

- Manufacture process: 40nm
- DQ 128 bits, A[13:0], BA[1:0] for 4 banks due to stacking of 4 layers
- Internal memory bits modified to 128 bits
- Page size should be 128, with no row buffer locality at all

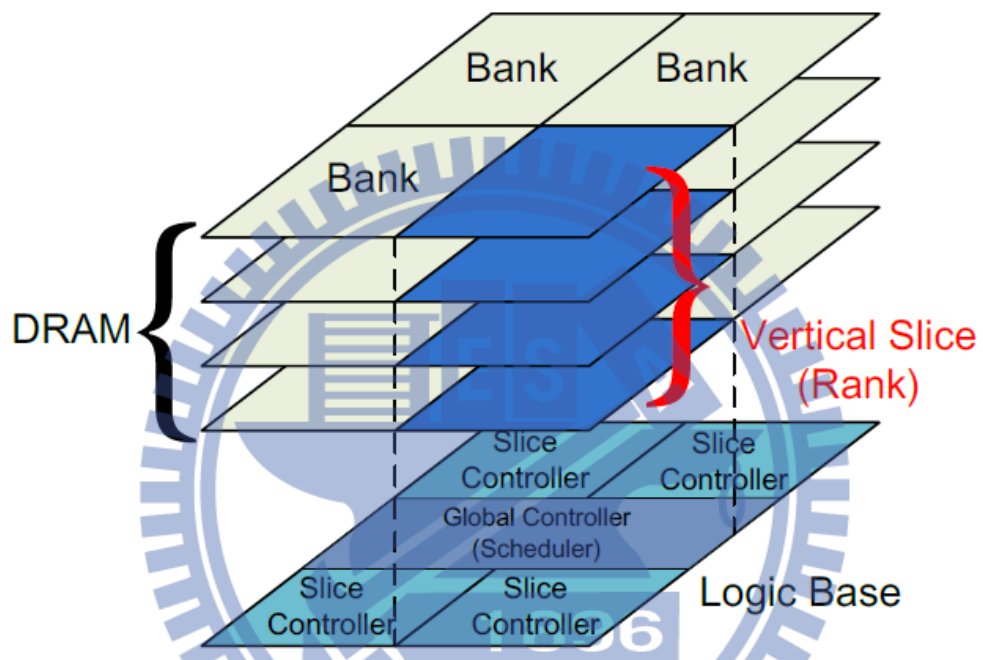


Figure 3.12 Proposed 3D-stacked DRAM

Proposed Wide-I/O 3D-stacked DRAM Specification	
VDD [V]	1.5
Density	4Gb
Organization	4-bank per vertical slice (Rank)
I/O pin	x512 (128pin per rank)
Data Rate [MHz]	333
Data Bandwidth [GB/s]	21.3

Table 3.3 Proposed Wide-I/O 3D-stacked DRAM specification

Test Pattern configuration	
Data access bits per cycle	128
Number of random R/W command	10000
System configuration	
Clock rate	333MHz
Command FIFO depth	128
Data FIFO depth	128
DRAM configuration	
Channel/Rank/Bank	1/1/4 (One Vertical Slice)
Model	Proposed 3D-stacked DRAM

Table 4.2 Local slice controller simulation configuration

- Since the voltage is 1.5

DDR3 timing constraints used by seniors

```

275 `elsif sg125E ..... // sg125E is equivalent to the JEDEC DDR3-1600 (10-10-10) speed bin
276   parameter TCK_MIN ..... = 1250; // tCK ..... ps ..... Minimum Clock Cycle Time
277   parameter TJIT_PER ..... = 70; // tJIT(per) ..... ps ..... Period Jitter
278   parameter TJIT_CC ..... = 140; // tJIT(cc) ..... ps ..... Cycle to Cycle jitter
279   parameter TERR_2PER ..... = 103; // tERR(2per) ..... ps ..... Accumulated Error (2-cycle)
280   parameter TERR_3PER ..... = 122; // tERR(3per) ..... ps ..... Accumulated Error (3-cycle)
281   parameter TERR_4PER ..... = 136; // tERR(4per) ..... ps ..... Accumulated Error (4-cycle)
282   parameter TERR_5PER ..... = 147; // tERR(5per) ..... ps ..... Accumulated Error (5-cycle)
283   parameter TERR_6PER ..... = 155; // tERR(6per) ..... ps ..... Accumulated Error (6-cycle)
284   parameter TERR_7PER ..... = 163; // tERR(7per) ..... ps ..... Accumulated Error (7-cycle)
285   parameter TERR_8PER ..... = 169; // tERR(8per) ..... ps ..... Accumulated Error (8-cycle)
286   parameter TERR_9PER ..... = 175; // tERR(9per) ..... ps ..... Accumulated Error (9-cycle)
287   parameter TERR_10PER ..... = 180; // tERR(10per) ..... ps ..... Accumulated Error (10-cycle)
288   parameter TERR_11PER ..... = 184; // tERR(11per) ..... ps ..... Accumulated Error (11-cycle)
289   parameter TERR_12PER ..... = 188; // tERR(12per) ..... ps ..... Accumulated Error (12-cycle)
290   parameter TDS ..... = 10; // tDS ..... ps ..... DQ and DM input setup time relative to DQS
291   parameter TDH ..... = 45; // tDH ..... ps ..... DQ and DM input hold time relative to DQS
292   parameter TDQSQ ..... = 100; // tDQSQ ..... ps ..... DQS-DQ skew, DQS to last DQ valid, per group, per access
293   parameter TDQSS ..... = 0.27; // tDQSS ..... tCK ..... Rising clock edge to DQS/DQS# latching transition
294   parameter TDSS ..... = 0.18; // tDSS ..... tCK ..... DQS falling edge to CLK rising (setup time)
295   parameter TDSH ..... = 0.18; // tDSH ..... tCK ..... DQS falling edge from CLK rising (hold time)
296   parameter TDQCK ..... = 225; // tDQCK ..... ps ..... DQS output access time from CK/CK#
297   parameter TQSH ..... = 0.40; // tQSH ..... tCK ..... DQS Output High Pulse Width
298   parameter TQSL ..... = 0.40; // tQSL ..... tCK ..... DQS Output Low Pulse Width
299   parameter TDIPW ..... = 360; // tDIPW ..... ps ..... DQ and DM input Pulse Width
300   parameter TIPW ..... = 560; // tIPW ..... ps ..... Control and Address input Pulse Width
301   parameter TIS ..... = 170; // tIS ..... ps ..... Input Setup Time
302   parameter TIH ..... = 120; // tIH ..... ps ..... Input Hold Time
303   parameter TRAS_MIN ..... = 35000; // tRAS ..... ps ..... Minimum Active to Precharge command time
304   parameter TRC ..... = 47500; // tRC ..... ps ..... Active to Active/Auto Refresh command time
305   parameter TRCD ..... = 12500; // tRCD ..... ps ..... Active to Read/Write command time
306   parameter TRP ..... = 12500; // tRP ..... ps ..... Precharge command period
307   parameter TXP ..... = 6000; // tXP ..... ps ..... Exit power down to a valid command
308   parameter TCKE ..... = 5000; // tCKE ..... ps ..... CKE minimum high or low pulse width
309   parameter TAON ..... = 250; // tAON ..... ps ..... RTT turn-on from ODTI on reference
310   parameter TWLS ..... = 165; // tWLS ..... ps ..... Setup time for tDQS flop
311   parameter TWLH ..... = 165; // tWLH ..... ps ..... Hold time of tDQS flop
312   parameter TWLO ..... = 7500; // tWLO ..... ps ..... Write levelization output delay
313   parameter TAA_MIN ..... = 12500; // TAA ..... ps ..... Internal READ command to first data
314   parameter CL_TIME ..... = 12500; // CL ..... ps ..... Minimum CAS Latency
315

```

```

622 `elsif sg125E
623   parameter TRRD ..... = 7500; // tRRD ..... ps ..... (2KB page size) Active bank a to Active bank b command time
624   parameter TFAW ..... = 40000; // tFAW ..... ps ..... (2KB page size) Four Bank Activate window

```

CACTI-3DD Modeling Results

```

51 ----- CACTI (version 7.0.3DD Prerelease of Aug, 2012) 3D DRAM Main Memory -----
52
53 Memory Parameters:
54   Total memory size (Gb): 4
55   Stacked die count: 4
56   TSV projection: industrial conservative
57   Number of banks: 4
58   Technology size (nm): 40
59   Page size (bits): 16384
60   Burst depth: 1
61   Chip IO width: 128
62   Best Ndw1: 128
63   Best Ndbl: 128
64   # rows in subarray: 128
65   # columns in subarray: 128
66
67 Results:
68 Timing Components:
69   ...t_RCD (Row to column command delay): 7.79592 ns
70   ...t_RAS (Row access strobe latency): 10.993 ns
71   ...t_RC (Row cycle): 13.1979 ns
72   ...t_CAS (Column access strobe latency): 14.4662 ns
73   ...t_RP (Row precharge latency): 2.9324 ns
74   ...t_RRD (Row activation to row activation delay): 2.19039 ns
75 Power Components:
76   ...Activation energy: 0.52456 nJ
77   ...Read energy: 0.941145 nJ
78   ...Write energy: 0.941151 nJ
79   ...Precharge energy: 0.45601 nJ
80 Area Components:
81   ...DRAM core area: 32.5495 mm2
82   ...Area efficiency: 32.4602%
83   ...DRAM die width: 4.90998 mm
84   ...DRAM die height: 6.52147 mm
85 TSV Components:
86   ...TSV area overhead: 0.5292 mm2
87   ...TSV latency overhead: 0.72752 ns
88   ...TSV energy overhead per access: 0.0859231 nJ

```

- Need for finding a sweet spot, shall perform design space exploration for practical needs
- This makes sense since now we are only accessing one single bank per layer, thus faster access.

Model on Ramulator2

```

// Senior's model
[5]={"DDR3_2Gb_x16", { .density=2 << 10, .dq=128, .count={ [0]=1, [1]=1, [2]=1, [3]=1 << 14, [4]...1 << 10 } } },
//

```

```

49 // Senior's timing paramters
50 // rate nBL nCL nRCD nRP nRAS nRC nWR nRTP nCWL nCCD nRRD nWTR nFAW nRFC nREFI nCS tCK_ps
51 {[0]=1600, [1]=4, [2]=10, [3]=10, [4]=10, [5]=28, [6]=38, [7]=12, [8]=6, [9]=9, [10]=4, -1, 6, -1, -1, -1, 2, 1250}},
52 //

277 // Load the organization specific timings
278 int dq_id = [](int dq) -> int {
279     switch (dq) {
280     case 4:
281         return 0;
282     case 8:
283         return 1;
284     case 16:
285         return 2;
286     case 128: // Senior's model
287         return 2;
288     default:
289         return -1;
290     }
}

```

- Uses the same timing as 16, since it is not modified in DDR3 dram model either.

Address mapping scheme

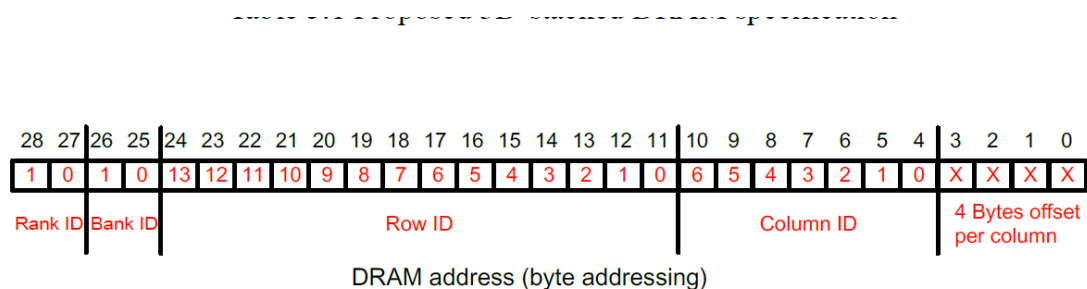


Figure 5.13 mapping scheme for the 3D-stacked DRAM

Scheduler